5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 8*.

Note: It is recommended to perform a calibration after each power-up.

Table 45. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	ADC power supply		2.4		3.6	V
V_{REF+}	Positive reference voltage		2.4		V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin			160(1)	220(1)	µA
f_{ADC}	ADC clock frequency		0.6		14	MHz
f_S(2)	Sampling rate		0.05		1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz			823	kHz
					17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)		0 (V_{SSA} or V_{REF-} tied to ground)		V_{REF+}	V
R_{AIN}(2)	External input impedance		See *Equation 1* and *Table 46*			kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor				5	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz			0.214	µs
					3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz			0.143	µs
					2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	µs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Data based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 3: Pin descriptions* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 45*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 46. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	1.2
7.5	0.54	10
13.5	0.96	19
28.5	2.04	41
41.5	2.96	60
55.5	3.96	80
71.5	5.11	104
239.5	17.1	350

1. Data guaranteed by design, not tested in production.

Table 47. ADC accuracy - limited test conditions(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error(3)	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after ADC calibration V_{REF+} = V_{DDA}	±1.3	±2	LSB
EO	Offset error(3)		±1	±1.5	
EG	Gain error(3)		±0.5	±1.5	
ED	Differential linearity error(3)		±0.7	±1	
EL	Integral linearity error(3)		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. Data based on characterization, not tested in production.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.

Table 48. ADC accuracy(1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error(4)	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error(3)		±1.5	±2.5	
EG	Gain error(3)		±1.5	±3	
ED	Differential linearity error(3)		±1	±2	
EL	Integral linearity error(3)		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. Data based on characterization, not tested in production.
4. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.

Figure 29. ADC accuracy characteristics

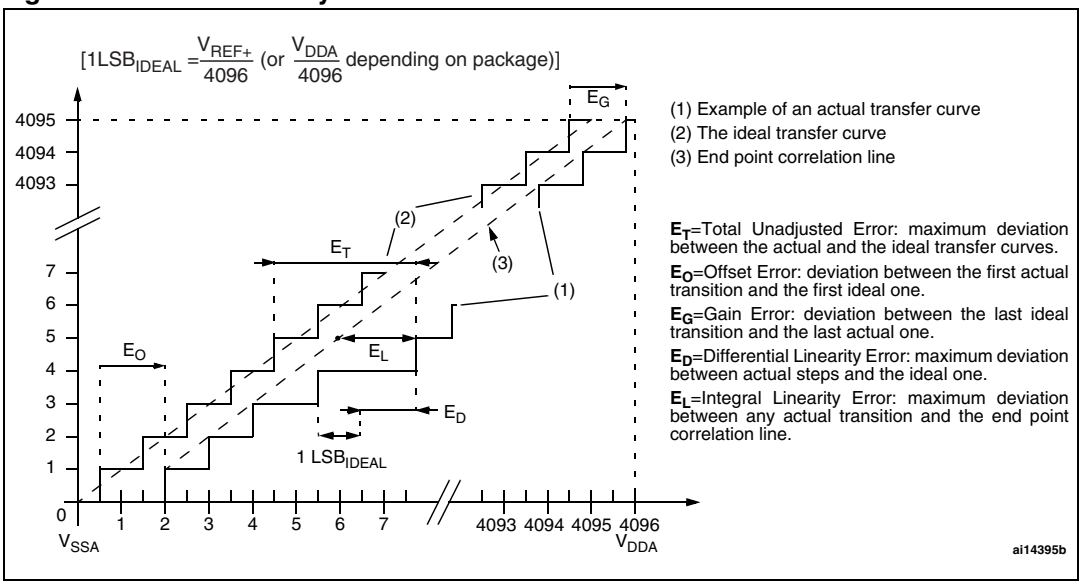
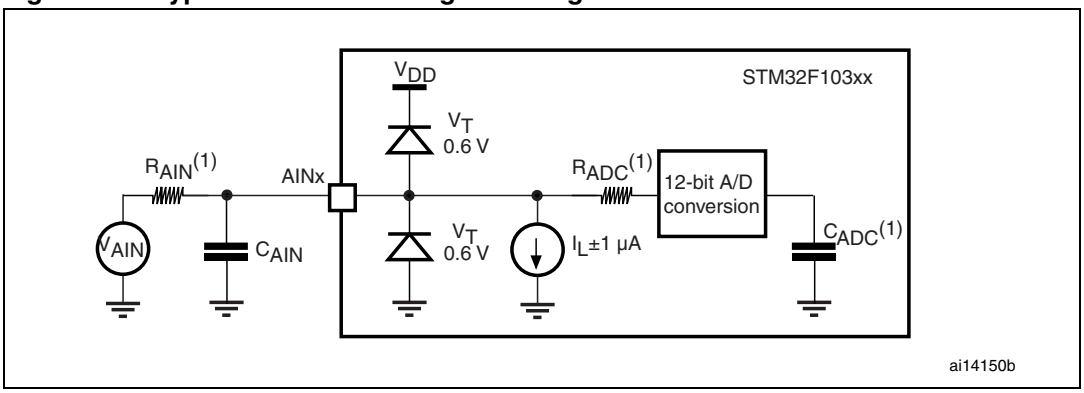


Figure 30. Typical connection diagram using the ADC

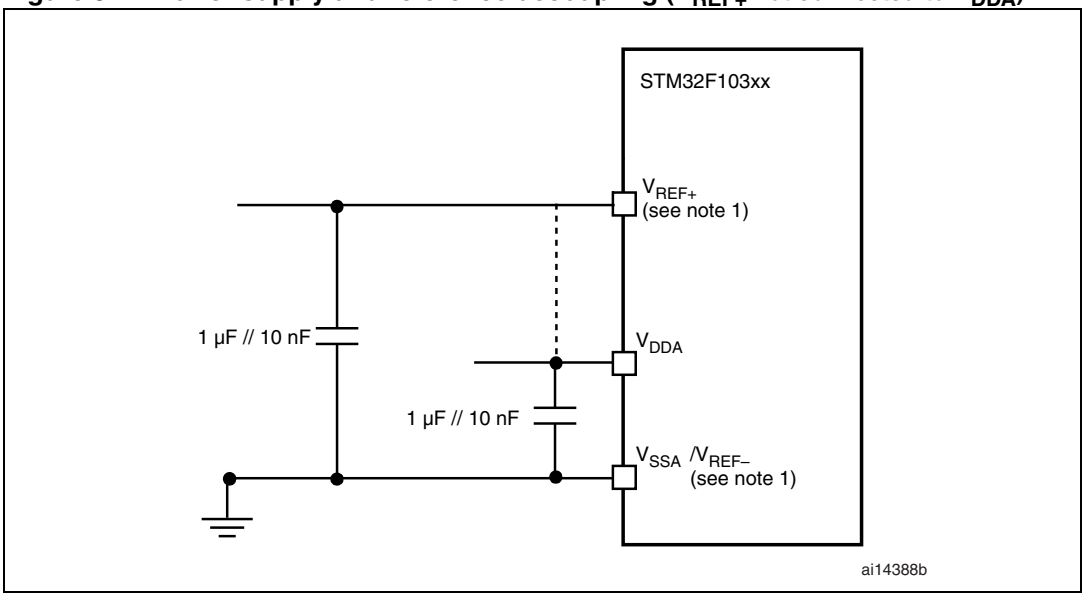


1. Refer to *Table 45* for the values of C_{AIN}, R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{PARASITIC}$ must be added to C_{AIN}. It represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

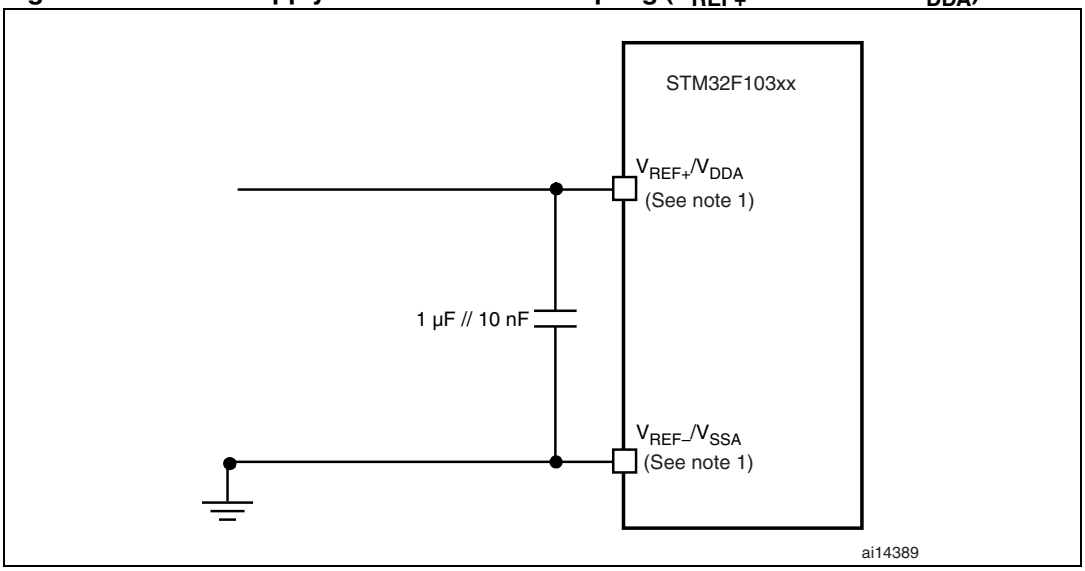
Power supply decoupling should be performed as shown in *Figure 31* or *Figure 32*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 31. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Figure 32. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.18 Temperature sensor characteristics

Table 49. TS characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature			±1	±2	°C
Avg_Slope(1)	Average slope		4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25 °C		1.34	1.43	1.52	V
t_{START}(2)	Startup time		4		10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature			2.2	17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Data guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers the STM32F103xx in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.
The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.