Virtex-II Pro™(P4/P7) Development Board User's Guide

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1   About this Kit

The Memec Design Virtex-II Pro™ Development Kit provides a complete development platform for designing and verifying applications based on the Xilinx Virtex-II Pro FPGA family. This kit enables designers to implement embedded processor based applications with extreme flexibility using IP cores and customized modules. The Virtex-II Pro FPGA with its integrated PowerPC™ processor and powerful Rocket I/O™ Multi-Gigabit Transceivers (MGT) makes it possible to develop highly flexible and high-speed serial transceiver applications.

The Memec Design Virtex-II Pro Development Kit includes the following:

- Virtex-II Pro development board (2VP4 or 2VP7 version)
- 5V/3amp DC power supply
- RS-232 serial cable
- Two coax loop back cables for MGT testing
- Documentation CD
- Xilinx Embedded Development Kit CDs (EDK)

Optional items that support development efforts:

- Xilinx ISE software
- JTAG cable
- SystemACE Module
- Additional coax loop back cables

Contact your local Memec distributor for assistance with any of these items.

2   The Virtex-II Pro Development Board

The Virtex-II Pro development board utilizes either the Xilinx XC2VP4-7FG456CES or XC2VP7-7FG456CES FPGA, depending on which version of the kit you have. Both the XC2VP4 and the XC2VP7 FPGAs contain a single PowerPC processor and four or eight Rocket I/O transceivers supporting serial data transfer rates of up to 2.5Gbps/port. The development board is designed to provide four Rocket I/O transceivers, hence, when the board is populated with the XC2VP7 FPGA, four out of the eight Rocket I/O transceivers on the XC2VP7 FPGA will not be available.

The Virtex-II Pro development board includes 8Mx32 SDRAM memory, three clock sources, an RS-232 port and additional user support circuitry to develop a complete system. The board also supports the Memec Design P160 expansion module standard, allowing application specific expansion modules to be easily added. A System ACE™ interface on the development board gives software designers the ability to run real-time operating systems (RTOS) from removable CompactFlash cards. Memec Design offers an optional System ACE programming module (DS-KIT-SYSTEMACE) that connects to this interface.

Figure 1 shows the Virtex-II Pro development board.
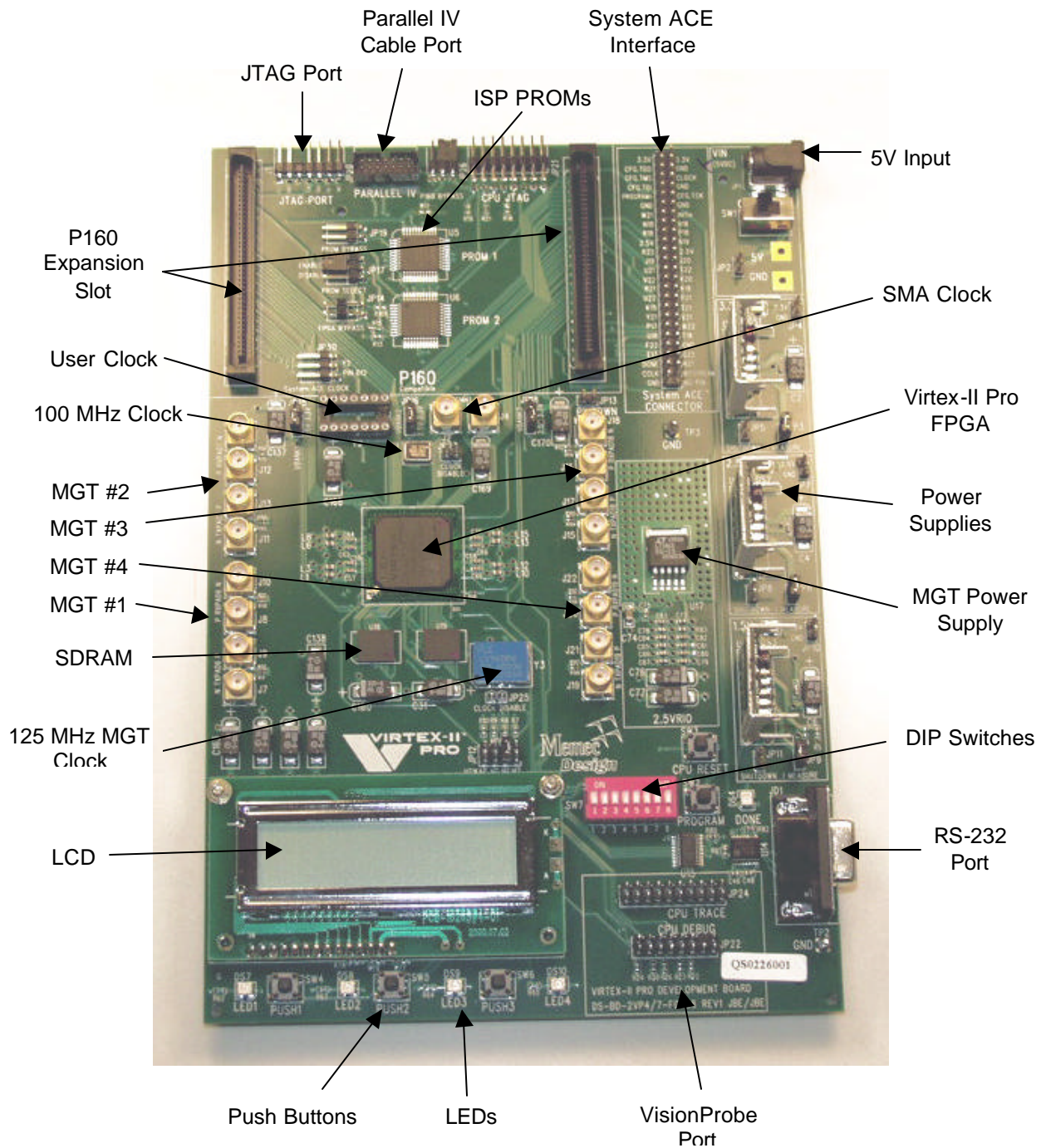
Figure 1 – Virtex-II Pro Development Board

A high-level block diagram of the Virtex-II Pro development board is shown in Figure 2, followed by a brief description of each board section.
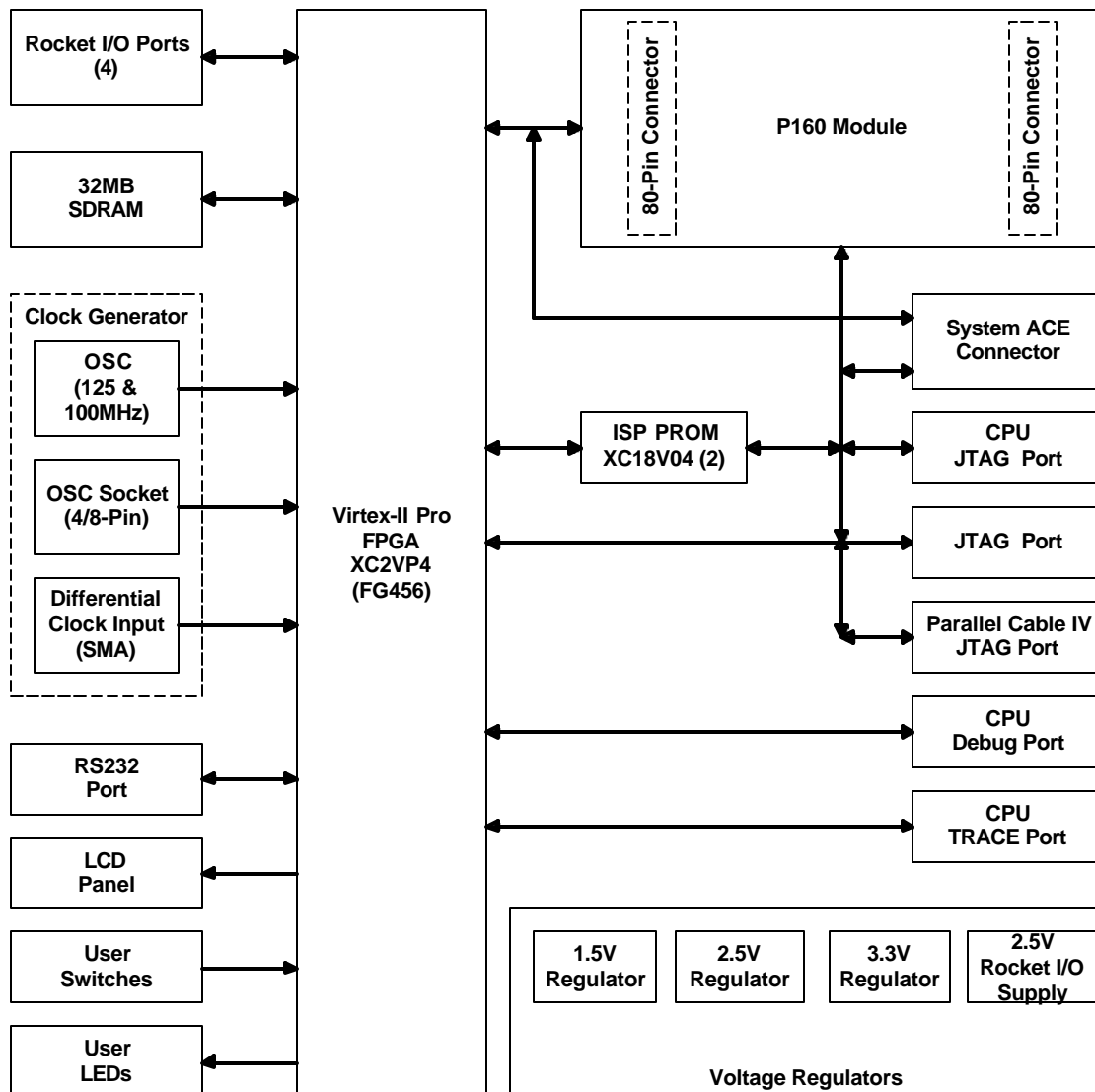
Figure 2 – Virtex-II Pro Development Board Block Diagram

2.1 Clock Generation

The Clock Generation section of the Virtex-II Pro development board provides all necessary clocks for the PowerPC processor and the Rocket I/O transceivers integrated into the Virtex-II Pro FPGA. Four clock sources are provided:

- 125 MHz LVDS oscillator (for the four MGTs)
- Differential SMA clock inputs (for the four MGTs)
- 100 MHz LVTTL oscillator (general clock input)
- User clock socket (2.5V LVTTL compatible)

The 125 MHz on-board LVDS oscillator and a pair of differential SMA connectors provide the reference clock input to the Rocket I/O transceivers. It should be noted that the 125 MHz clock and the differential SMA clock inputs are connected to the global clock inputs of the FPGA that are located on the top side of the FPGA and also the lower side of the device. This scheme provides direct clock access to the Rocket I/O transceivers that are located on the top side as well the ones located on the lower side of the FPGA.

An on-board 100 MHz oscillator provides the system clock input to the processor section. This 100 Mhz clock can used by the Virtex-II Pro Digital Clock Managers (DCMs) to generate various processor clocks. A socket is also provided for a single-ended 2.5 V LVTTL clock input to the FPGA via an 8 or 4-pin oscillator. The following table shows the clock sources on the Virtex-II Pro board.

Table 1 - Clock Generation

Signal Name	Virtex-II Pro Pin #	Direction	Description
CLK.CAN.LVDS.P	C11, W11	Input	Positive LVDS Clock Input - On-board 125 MHz LVDS Oscillator
CLK.CAN.LVDS.N	D11, Y11	Input	Negative LVDS Clock Input - On-board 125 MHz LVDS Oscillator
CLK.CAN.HS	V12	Input	On-board 100 MHz LVTTL Oscillator
CLK.SOCKET	U12	Input	On-board socket for LVTTL Oscillator
CLK.SMA.P	D12, Y12	Input	Positive Differential Clock Input – SMA connector
CLK.SMA.N	C12, W12	Input	Negative Differential Clock Input – SMA connector

2.2   Rocket I/O Ports

The Rocket I/O transceiver is based on Mindspeed's SkyRail™ technology. Up to 16 transceiver modules are available on a single Virtex-II Pro FPGA, depending on the part being used. The transceiver module is designed to operate at any serial bit rate in the range of 500 Mb/s to 3.125 Gb/s per channel, including the specific bit rates used by the communications standards listed in the following table. The serial bit rate need not be configured in the transceiver, as the received data, the applied reference clock, and the SERDES_10B attribute imply the operating frequency of the transceiver.

Table 2 - Communications Standards Supported by Rocket I/O Transceiver

Mode	Channels (# of transceivers)	I/O Bit Rate (Gb/s)	Internal Clock Rate (REF_CLK Mhz)
Fibre Channel	1	1.06	53
		2.12	106
Gbit Ethernet	1	1.25	62.5
XAUI (10-Gbit Ethernet)	4	3.125	62.5
Infiniband	1, 4, 12	2.5	62.5
Aurora (Xilinx protocol)	1, 2, 4	0.840 – 3.125	62.5
Custom Mode	1, 2, 4, 8, …	up to 3.125	62.5

The following figure shows the four Rocket I/O transceiver ports used on the Virtex-II Pro development board. These transceivers are physically located at the top and the lower side of the

XC2VP4/P7 device. The Virtex-II Pro development board is designed to provide low jitter reference clock inputs (CLK.CAN.LVDS, CLK.SMA) to the top and lower sections of the device in order to improve the performance of the transceivers. An on-board 125 MHz LVDS differential clock oscillator is used to drive the CLK.CAN.LVDS input, while the CLK.SMA is connected to a pair of SMA connectors to allow external clock input via an external signal generator.
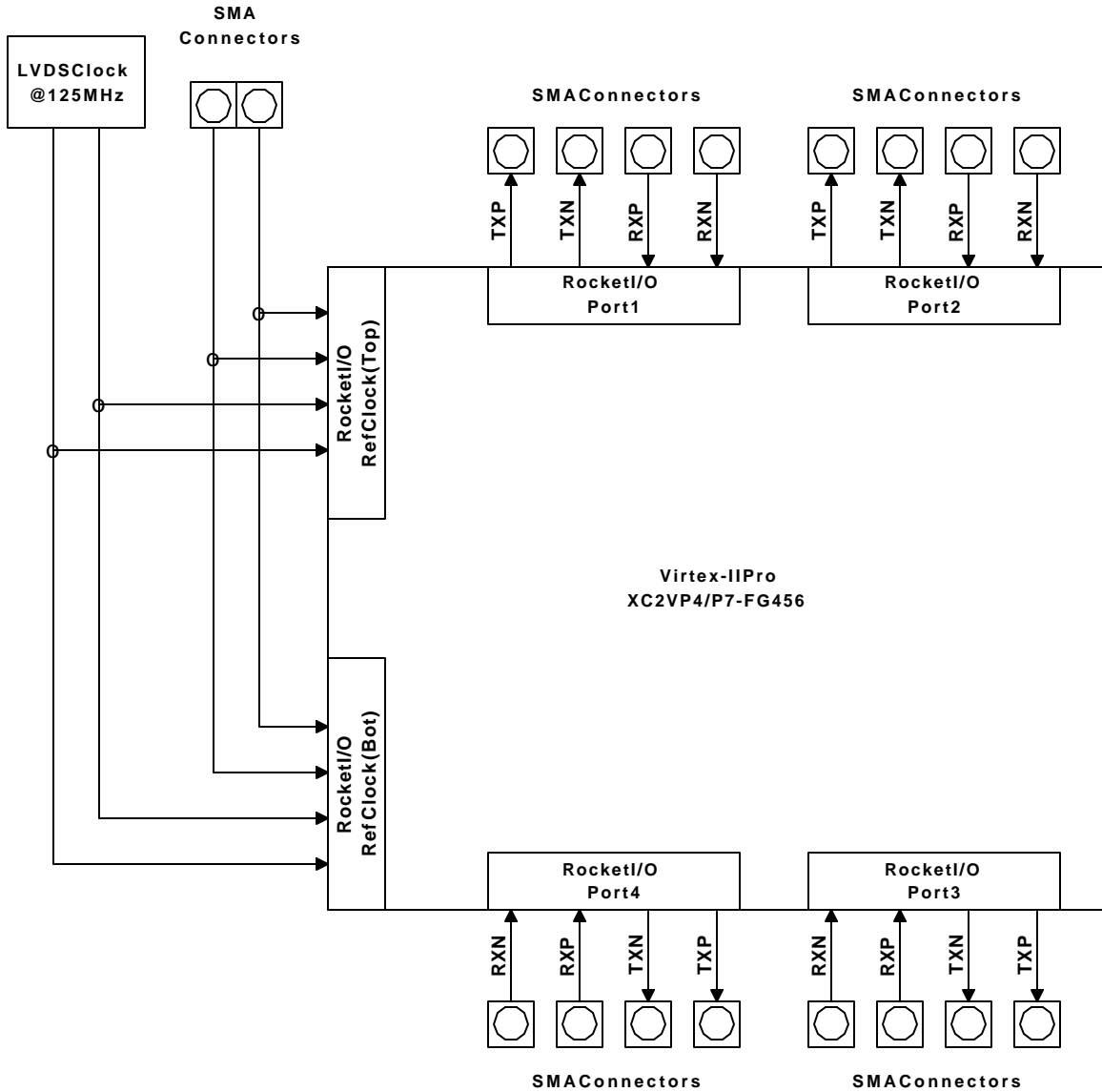
Figure 3 – MGT clocking Diagram

Table 3 - Rocket I/O Transceiver Ports Pin Assignments

Rocket I/O Port #	Signal Name	Virtex-II Pro Pin #	Description
1	AVCCAUXRX6	B10	Analog power supply for receive circuitry of the MGT (2.5V).
	VTRXPAD6	B9	Receive termination supply for the MGT (1.8V to 2.8V).
	RXNPAD6	A10	Negative differential receive port of the MGT.
	RXPPAD6	A9	Positive differential receive port of the MGT.
	GNDA6	C9	Ground for the analog circuitry of the MGT.
	TXNPAD6	A7	Negative differential transmit port of the MGT.
	TXPPAD6	A8	Positive differential transmit port of the MGT.
	AVCCAUXTX6	B8	Analog power supply for transmit circuitry of the MGT (2.5V).
	VTTXPAD6	B7	Transmit termination supply for the MGT (1.8V to 2.8V).
2	AVCCAUXRX7	B16	Analog power supply for receive circuitry of the MGT (2.5V).
	VTRXPAD7	B15	Receive termination supply for the MGT(1.8V to 2.8V).
	RXNPAD7	A16	Negative differential receive port of the MGT.
	RXPPAD7	A15	Positive differential receive port of the MGT.
	GNDA7	C14	Ground for the analog circuitry of the MGT.
	TXNPAD7	A13	Negitive differential transmit port of the MGT.
	TXPPAD7	A14	Positive differential transmit port of the MGT.
	AVCCAUXTX7	B14	Analog power supply for transmit circuitry of the MGT (2.5V).
	VTTXPAD7	B13	Transmit termination supply for the MGT (1.8V to 2.8V).

Table 4 - Rocket I/O Transceiver Ports Pin Assignments (Cont.)

Rocket I/O Port #	Signal Name	Virtex-II Pro Pin #	Description
3	AVCCAUXRX18	AA16	Analog power supply for receive circuitry of the MGT (2.5V).
	VTRXPAD18	AA15	Receive termination supply for the MGT (1.8V to 2.8V).
	RXNPAD18	AB16	Negative differential receive port of the MGT.
	RXPPAD18	AB15	Positive differential receive port of the MGT.
	GNDA18	Y14	Ground for the analog circuitry of the MGT.
	TXNPAD18	AB13	Negitive differential transmit port of the MGT.
	TXPPAD18	AB14	Positive differential transmit port of the MGT.
	AVCCAUXTX18	AA14	Analog power supply for transmit circuitry of the MGT (2.5V).
	VTTXPAD18	AA13	Transmit termination supply for the MGT (1.8V to 2.8V).
4	AVCCAUXRX19	AA10	Analog power supply for receive circuitry of the MGT (2.5V).
	VTRXPAD19	AA9	Receive termination supply for the MGT (1.8V to 2.8V).
	RXNPAD19	AB10	Negative differential receive port of the MGT.
	RXPPAD19	AB9	Positive differential receive port of the MGT.
	GNDA19	Y9	Ground for the analog circuitry of the MGT.
	TXNPAD19	AB7	Negitive differential transmit port of the MGT.
	TXPPAD19	AB8	Positive differential transmit port of the MGT.
	AVCCAUXTX19	AA8	Analog power supply for transmit circuitry of the MGT (2.5V).
	VTTXPAD19	AA7	Transmit termination supply for the MGT (1.8V to 2.8V).

2.3 SDRAM Memory

The Virtex-II Pro development board provides 32MB of SDRAM memory (Infineon Mobile SDRAM - HYB25L128160AC-8). The high-level block diagram of the SDRAM interface is shown below followed by a table describing the SDRAM memory interface signals.
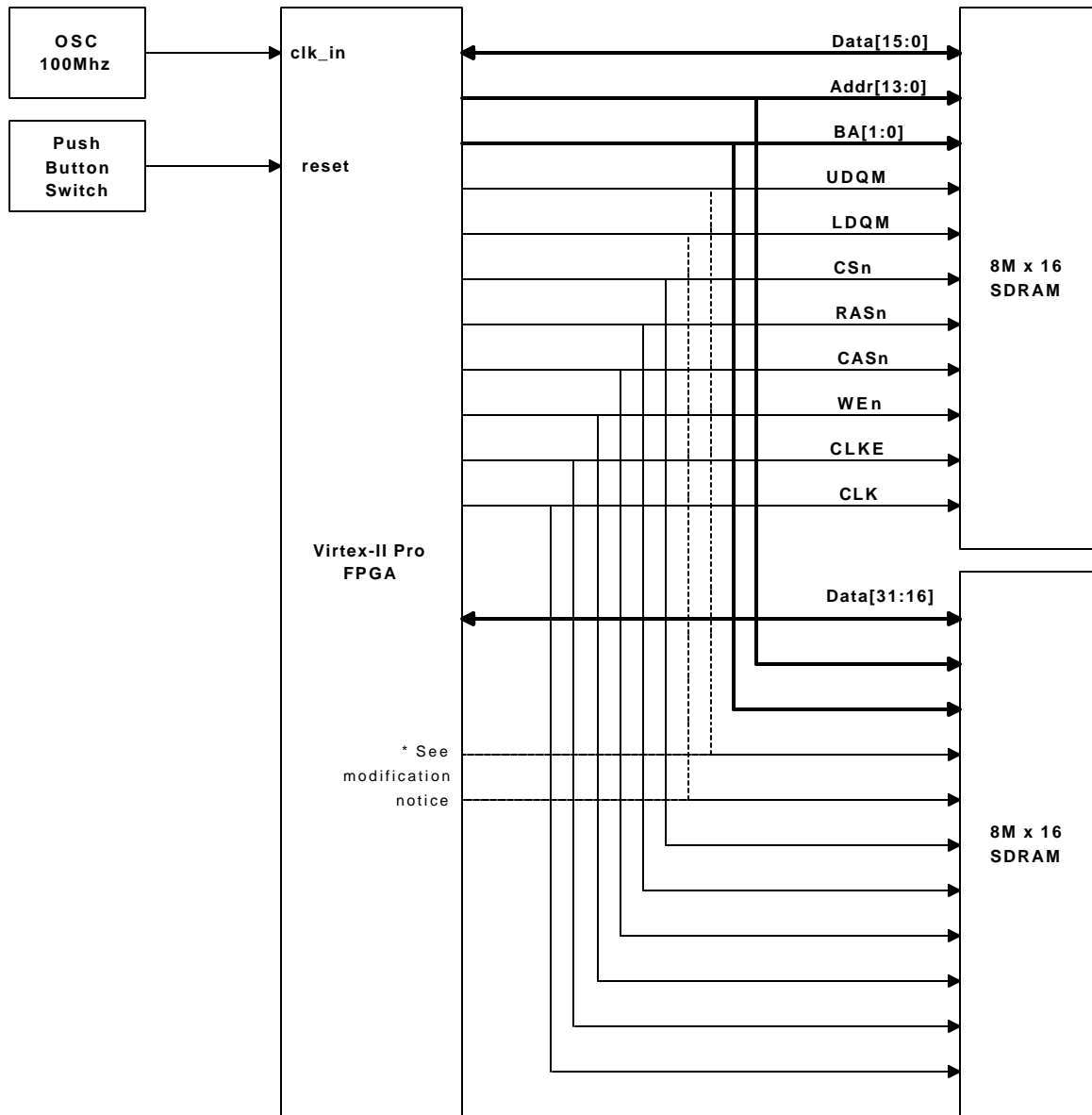
Figure 4- SDRAM Interface

Note: Only ADDR[11:0] are used with the Infineon Mobile RAM (HYB25L128).
ADDR[13:12] are not connected to the memory and are available for future
expansion.

**Some Rev 2 boards have been modified with fly wires to separate the upper
and lower data strobe signals for each memory. See the Rev 2 Board
Modification notice included in your kit for details of this change.**

Table 5- SDRAM Memory Interface Signal Descriptions

Signal Name	Description	FPGA Pin #
A0	Address 0	M4
A1	Address 1	P4
A2	Address 2	N4
A3	Address 3	M3
A4	Address 4	J4
A5	Address 5	H3
A6	Address 6	L3
A7	Address 7	G3
A8	Address 8	H4
A9	Address 9	K4
A10	Address 10	N3
A11	Address 11	F3
A12*	Address 12*	G4
A13*	Address 13*	E4
DQ0	Data 0	G2
DQ1	Data 1	H2
DQ2	Data 2	G1
DQ3	Data 3	J2
DQ4	Data 4	H1
DQ5	Data 5	K2
DQ6	Data 6	J1
DQ7	Data 7	K1
DQ8	Data 8	F5
DQ9	Data 9	F1
DQ10	Data 10	G5
DQ11	Data 11	F2
DQ12	Data 12	D2
DQ13	Data 13	E1
DQ14	Data 14	D1
DQ15	Data 15	E2
DQ16	Data 16	U1
DQ17	Data 17	V1
DQ18	Data 18	U2
DQ19	Data 19	W1
DQ20	Data 20	V2
DQ21	Data 21	Y1
DQ22	Data 22	W2
DQ23	Data 23	Y2
DQ24	Data 24	N1
DQ25	Data 25	T2
DQ26	Data 26	N2
DQ27	Data 27	T1
DQ28	Data 28	P1
DQ29	Data 29	R2
DQ30	Data 30	P2
DQ31	Data 31	R1
BA0	Bank Select 0	L4
BA1	Bank Select 1	R4
UDQM**	Write Mask0	T3**
LDQM**	Write Mask1	F4**
CSn	Chip Select	P3
RASn	Row Address Strobe	T4
CASn	Column Address Strobe	K3

WEn	Write Enable	R3
CLK	Clock	E3
CKE	Clock Enable	J3

* A12 and A13 are not used with the 128Mbit version of the Mobile RAM (HYB25L128)
** See separate Board Modification note for details of pin-out changes made (Appendix)

2.4   Liquid Crystal Display

The Virtex-II Pro development board provides an 8-bit interface to a 2x16 LCD panel (Varitronix MDL-16265-LV). The following table shows the LCD interface signals.

Table 6 - LCD Interface Signal Description

Signal Name	Virtex-II Pro Pin #	Description
D7	E8	LCD Data Bit 7
D6	C8	LCD Data Bit 6
D5	D8	LCD Data Bit 5
D4	C7	LCD Data Bit 4
D3	D6	LCD Data Bit 3
D2	D5	LCD Data Bit 2
D1	F9	LCD Data Bit 1
D0	D7	LCD Data Bit 0
EN	E7	LCD Enable Signal
RW		LCD Write Signal (this signal is connected to logic "0" on the Virtex-II Pro board, enabling write only cycles).
RS	E6	LCD Register Select Signal

2.5   User LED

The Virtex-II Pro development board provides four user LEDs that can be turned "ON" by driving the LEDx signal to a logic "0". The following table shows the user LEDs and their associated Virtex-II Pro FPGA pin assignments.

Table 7 - User LED

LED Designation	Virtex-II Pro Pin #
DS7 (LED1)	V8
DS8 (LED2)	W6
DS9 (LED3)	U10
DS10 (LED4)	V10

2.6   User Push Button Switches

The Virtex-II Pro development board provides four user push button switches as described in the following table. An active low signal is generated when a given switch is pressed. It should be noted that there are no pull-up resistors on the push button switch signals on the Virtex-II Pro board. Therefore, internal FPGA pull-up resistors must be used to force a given push button switch signal to a logic "1" when its associated switch is not pressed.

Table 8 - User Push Button Switches

Signal Name	FPGA Pin #	Description
FPGA.RESET	V15	User push button switch input used as Reset or general-purpose switch input (SW3)
PUSH1	V7	User push button switch input 1 (SW4)
PUSH2	W5	User push button switch input 2 (SW5)
PUSH3	AA12	User push button switch input 3 (SW6)

2.7 Program Switch

The Virtex-II Pro development board provides a push button program switch (SW2) for initiating the configuration of the Virtex-II Pro FPGA. This switch is used to force a re-configuration of the FPGA from the XC18V04 ISP PROMs. After programming of the XC18V04 ISP PROMs via the JTAG interface, this switch asserts the PROGn signal, thereby activating the Master Serial Mode of configuration. The mode jumpers (M0-M2) must be set to the Master Serial Mode for configuration to occur via the ISP PROMs. See section XX for further details of on setting the mode jumpers.

2.8 User DIP Switch

The Virtex-II Pro development board provides an 8-position user DIP switch. The switch input to the FPGA is set to logic "0" when a given DIP switch position is set to "ON". It should be noted that there are no pull-up resistors on the DIPx signals on the Virtex-II Pro development board. Hence, internal FPGA pull-up resistors must be used to force the DIPx signal to a logic "1" when its associated switch position is set to "OFF".
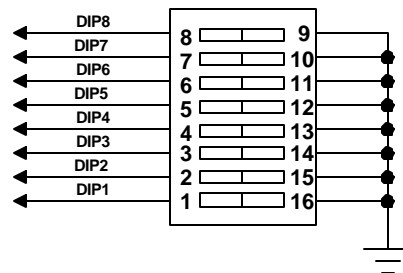
Figure 5 – User DIP Switch

The following table shows the user DIP switch inputs and their corresponding Virtex-II Pro FPGA pin assignments.

Table 9 - User DIP Switch

Signal Name	FPGA Pin #	Description
DIP8	V16	User Switch Input 8
DIP7	Y16	User Switch Input 7
DIP6	W16	User Switch Input 6
DIP5	Y15	User Switch Input 5
DIP4	W15	User Switch Input 4
DIP3	W14	User Switch Input 3
DIP2	Y13	User Switch Input 2
DIP1	W13	User Switch Input 1

2.9   RS232 Port

The Virtex-II Pro development board provides a DB-9 connection for a simple RS232 port. The board utilizes the TI MAX3223 device for driving the RD, TD, RTS, and CTS signals. The user must provide a UART core internal to the FPGA to enable serial communication.
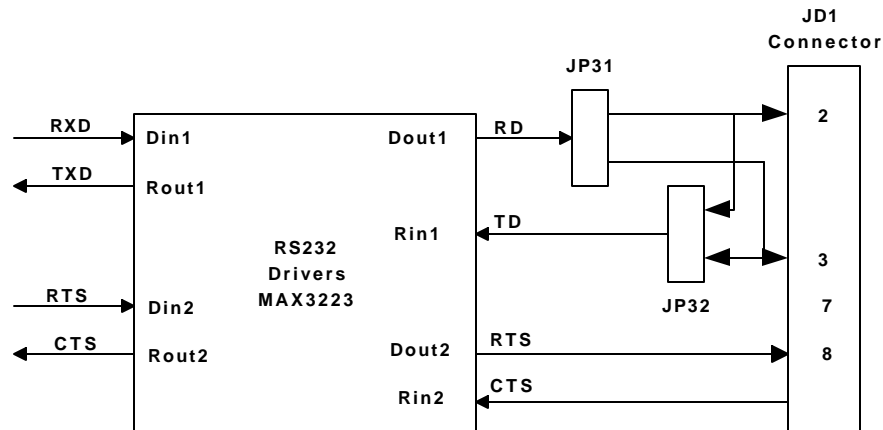
Figure 6 - RS232 Interface

The following table shows the RS232 interface signal names and their respective Virtex-II Pro FPGA pin assignments.

Table 10- RS232 Signal Description

Signal Name	FPGA Pin #	Description
RXD	W7	Received Data, RD
TXD	U9	Transmit Data, TD
RTS	Y7	Request To Send, RTS
CTS	V6	Clear To Send, CTS

Two jumpers, JP31 and JP32 allow the RD and TD signals to be swapped at the pin2 and pin 3 positions of the DB9 connector. This provides added flexibility for DCE and DTE types of configurations. Using the standard male-female straight through cable included in the kit, these jumpers should be configured for the DCE mode when connecting to a PC. Table 11 shows the different configuration options possible.

Table 11- DTE/DCE Configuration Jumpers

JP31	JP32	Description
1-2 Closed	2-3 Closed	DTE Configuration
2-3 Closed	1-2 Closed	DCE Configuration

2.10   Configuration/Debug Ports

Several configuration and debug methods are provided on the Virtex-II Pro development board to support the configuration of the Virtex-II Pro FPGA and the configuration/debug of the integrated PowerPC processor. In general, the FPGA can be configured in JTAG, Slave Serial, or Master

Serial modes. The on-board JTAG chain can also be used to configure/debug the PowerPC processor. In addition to the JTAG port, the CPU debug port can be used for the processor run-time debugging (BDM). The following sections provide a brief description of the FPGA/Processor configuration and debug methods used on the Virtex-II Pro development board.

2.10.1 JTAG Chain

The following figure shows the JTAG chain on the Virtex-II Pro development board and illustrates how four different sources can be used to drive this JTAG chain. The chain can be driven by the following sources:

- System ACE
- Parallel Cable IV
- JTAG Cable
- CPU JTAG Cable

The JTAG chain consists of one or two XC18V04 ISP PROMs, the Virtex-II Pro FPGA and the P160 module.
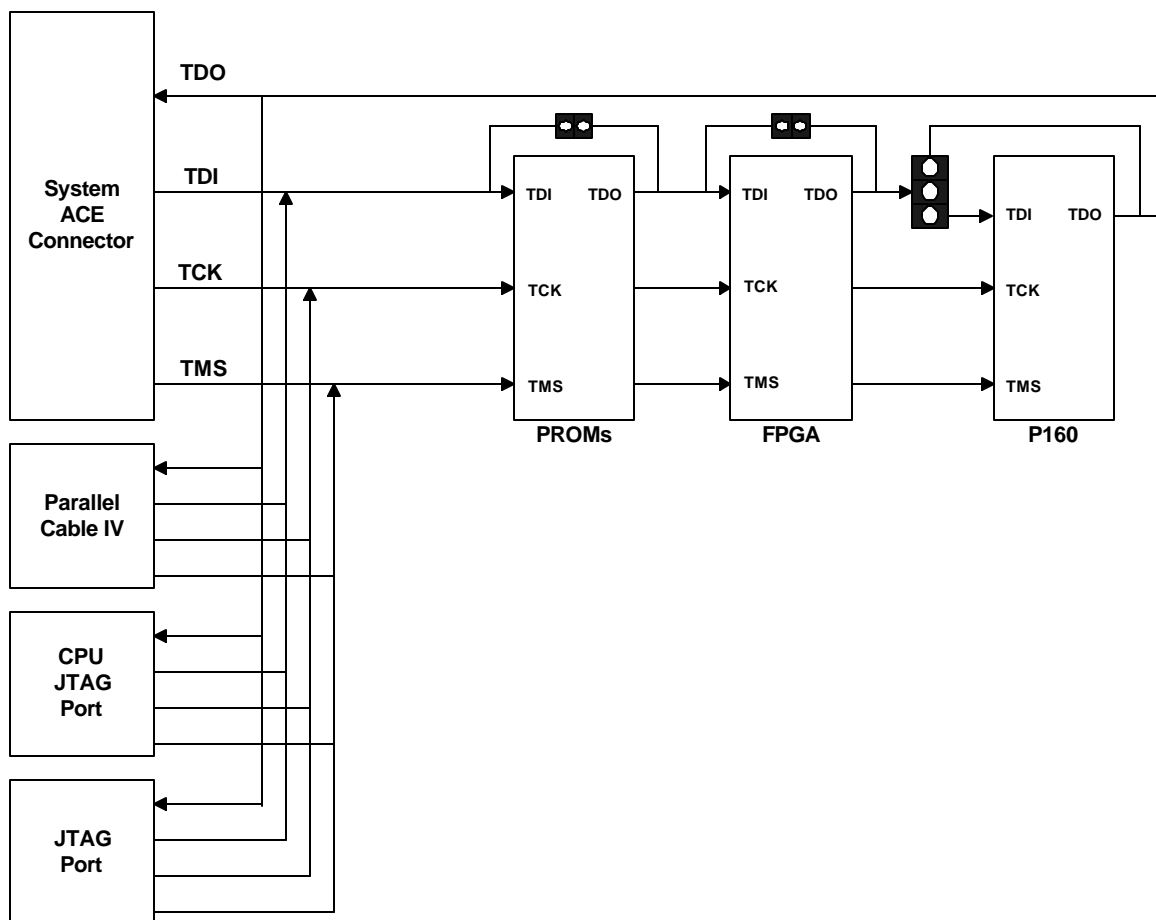
Figure 7 – JTAG Chain

2.10.2 JTAG Port

The Virtex-II Pro development board provides a JTAG connector that can be used to program the on-board ISP PROMs, configure the Virtex-II Pro FPGA, and program and/or configure JTAG devices located on the P160 Expansion module.

The JTAG chain on the board is designed for 2.5 V operation. Any P160 modules that connect to the board must be set for the 2.5 V JTAG mode.

The following figure shows the pin assignments for the JTAG connector on the Virtex-II Pro development board.
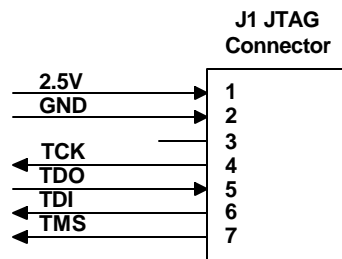
Figure 8 – J1 JTAG Connector

2.10.3 CPU JTAG Port

The Virtex-II Pro development board provides a CPU JTAG connector that can be used to download code into the Virtex-II Pro integrated PowerPC processor. This JTAG port can also be used as the processor debug port. The following figure shows the pin assignments for the CPU JTAG connector on the board.
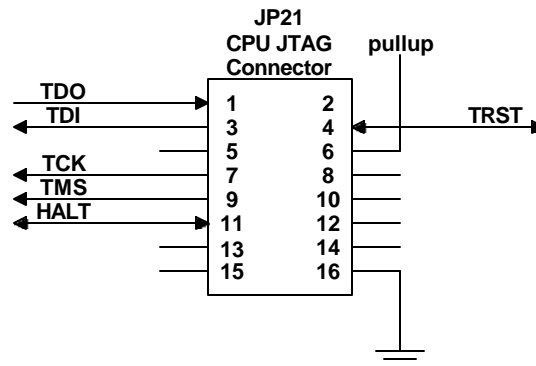
Figure 9 – J21 CPU JTAG Port

The HALT and TRST signals are connected to FPGA pins as shown in the table below:

Table 12- JP21 CPU JTAG Port

Signal Name	FPGA Pin #	Description
CPU.HALT	AA11	User defined
CPU.TRST	W10	User defined

2.10.4 Parallel Cable IV Port

The Virtex-II Pro development board provides a Parallel Cable IV connector (JP20) that can be used to program the on-board ISP PROM, configure the Virtex-II Pro FPGA and program JTAG devices located on the P160 Expansion module. The following figure shows the pin assignments for the Parallel Cable IV connector. The Parallel Cable IV can also be used to configure the FPGA via Slave Serial configuration mode.
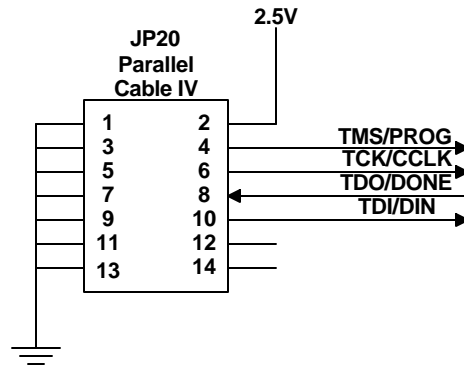
Figure 10 – J20 Parallel IV Port

The Parallel IV cable connects to JP20 as shown in the figure below.
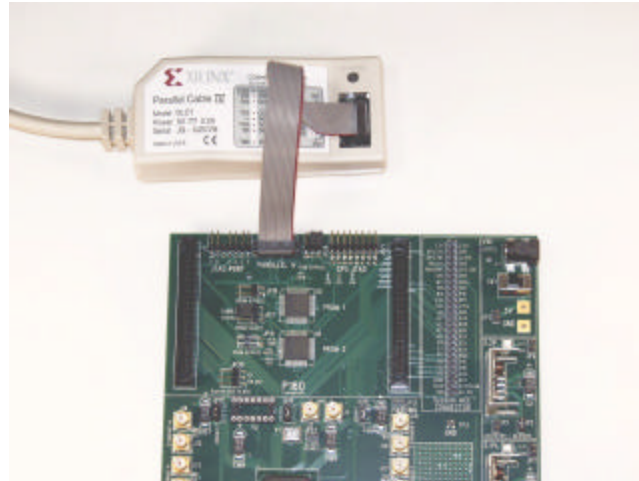
Figure 11 – Parallel IV Cable Hook-up

2.10.5 System ACE Connector

The Virtex-II Pro development board provides a System ACE interface that can be used to configure the Virtex-II Pro FPGA. The interface also gives software designers the ability to run real-time operating systems (RTOS) from removable CompactFlash cards. The Memec Design System ACE module (DS-KIT-SYSTEMACE) can be used to perform both of these functions. The figure below shows the System ACE module connected to the header on the Virtex-II Pro board.
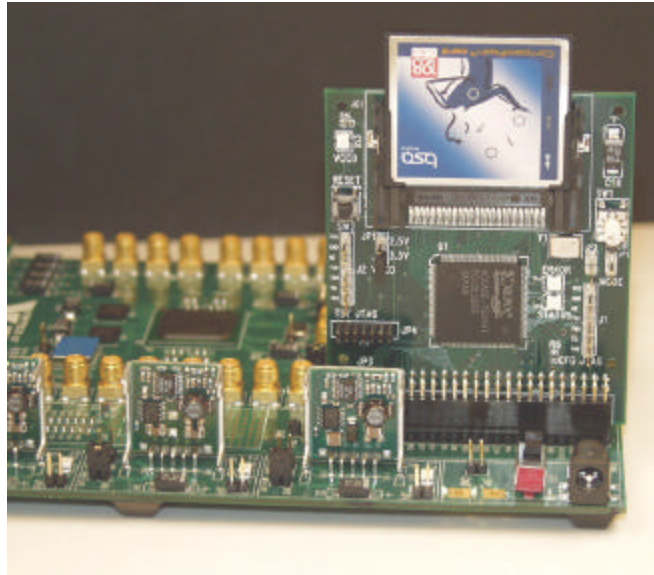
Figure 12 – System ACE Module Setup

The following figure shows a high-level block diagram of the Memec Design System ACE module. For more information, please refer to the Memec Design System ACE Module User's Guide.
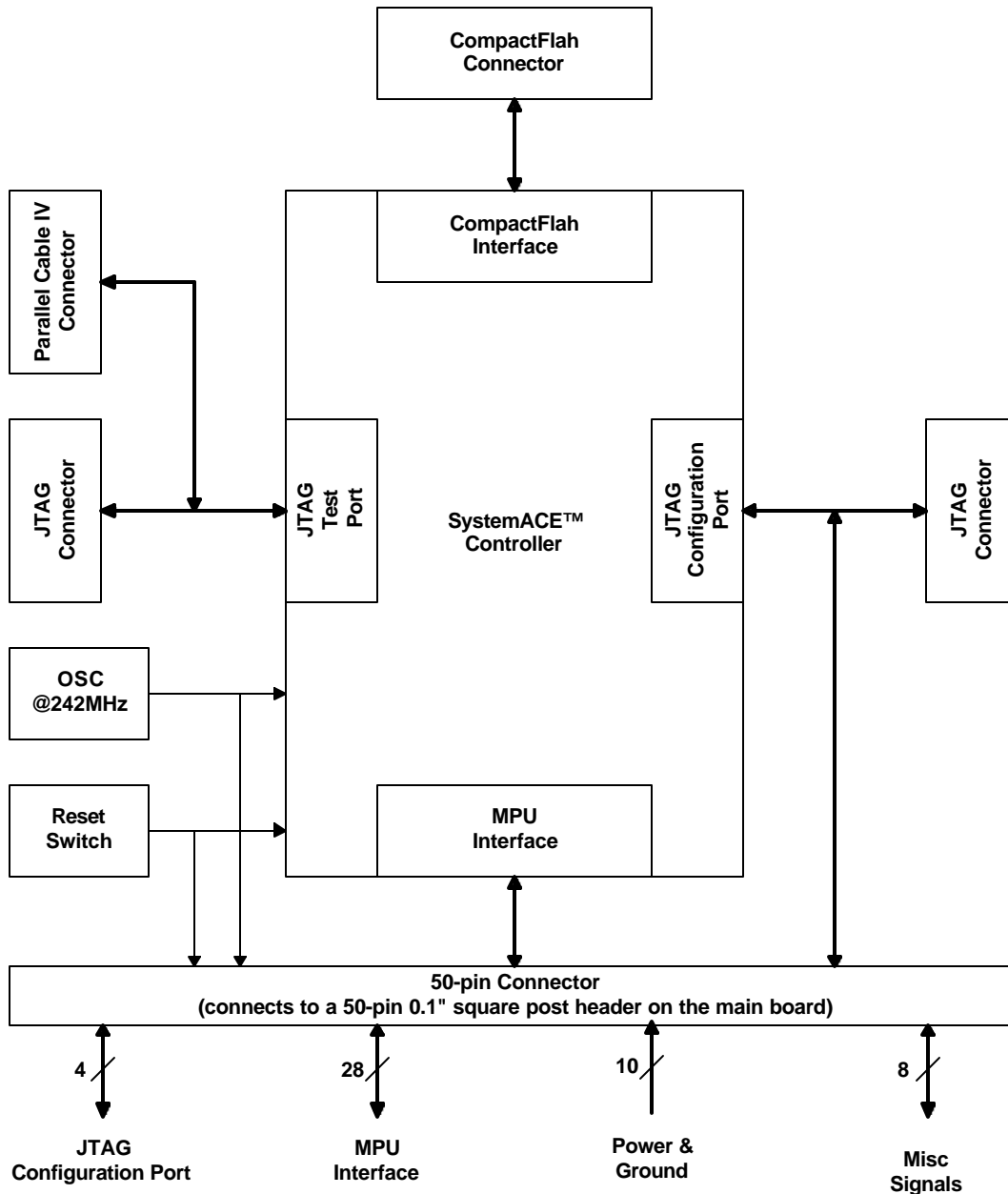
Figure 13- System ACE Module Block Diagram

The following figure shows the clocking scheme for the System ACE controller. When the MPU port of the System ACE controller is used, the Virtex-II Pro FPGA and the System ACE controller must use the same clock source. Hence, jumpers are provided on the Virtex-II Pro development board and the System ACE module to provide the clock input to both devices. Two clocking schemes are provided to ensure full synchronization of the MPU interface and also allow a variable clock input to the System ACE controller. The following table shows these two clocking options.

Table 13 – System ACE Controller Clock Source

Clock Source	Jumper Settings	
	JP30 (V2P board)	**JP5 (SAM board)**
System ACE module 24Mhz OSC	Place jumper on pins 2-3 (Pin D12 Position)	Open (24MHz osc enabled)
Virtex-II Pro board OSC socket **(OSC must not exceed 33Mhz)**	Place jumper on pins 1-2 (Y2 Position)	Closed (Disable 24MHz osc)
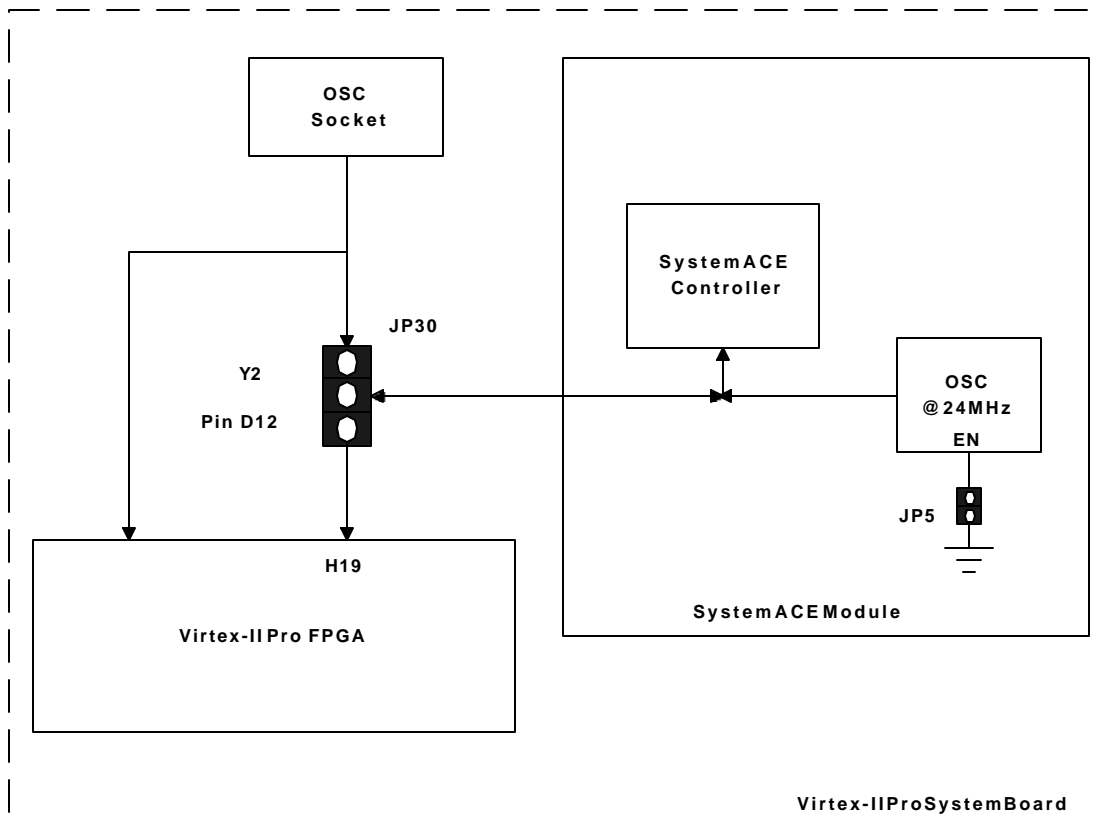
Figure 14- System ACE Controller Clock Source

The following table shows the System ACE interface signals. It should be noted that the System ACE controller's address, data and control signals are shared with the P160 module signals. A dedicated Chip Select signal (CEn, pin 44 of this connector) allows access to the P160 module resources such as SRAM and FLASH without the System ACE module driving the P160 module signals. This way, the System ACE and other memories can share a common bus. A 50-pin 0.1" square post header (JP29) is used to connect the System ACE module to the Virtex-II Pro development board.

Table 14 – System ACE Connector Signal Description

Virtex-II Pro Pin #	System ACE Signal Name	JP29 Pin #		System ACE Signal Name	Virtex-II Pro Pin #
	3.3V	1	2	**3.3V**	
	TDO	3	4	**GND**	
	TMS	5	6	CLOCK	
	TDI	7	8	**GND**	
B1	PROGRAMn	9	10	TCK	
	GND	11	12	**GND**	
W21	OEn	13	14	INITn	W17
N18	MPA0	15	16	WEn	H18
R18	MPA2	17	18	MPA1	P18
	2.5V	19	20	MPA3	N19
R22	MPD00	21	22	**2.5V**	
J19	MPD02	23	24	MPD01	J20
U21	MPD04	25	26	MPD03	T22
V22	MPD06	27	28	MPD05	K20
R21	MPD08	29	30	MPD07	K18
U22	MPD10	31	32	MPD09	P21
K19	MPD12	33	34	MPD11	T21
Y21	MPD14	35	36	MPD13	V21
P17	MPA4	37	38	MPD15	W22
U18	MPA6	39	40	MPA5	T18
F22	IRQ	41	42	**GND**	
E13	RESETn	43	44	CEn	G22
Y18	DONE	45	46	BRDY	N21
W20	CCLK	47	48	BITSTREAM	V17
	GND	49	50	**NC**	

2.10.6 CPU Debug Port

The Virtex-II Pro development board provides a dedicated CPU Debug connector that can be used to download code into the Virtex-II Pro integrated PowerPC processor. This JTAG port can also be used as the processor debug port. The figure below shows the pin assignments for the CPU Debug connector on the board and the table shows their connection to the FPGA I/O pins. The FPGA pins used are general purpose I/O, so connection to the PPC must be implemented within the FPGA design.
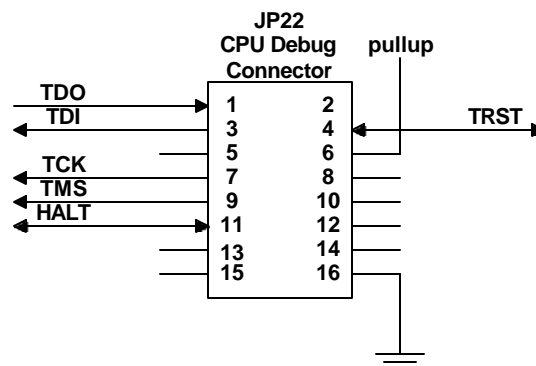
Figure 15- CPU Debug Port

Table 15- JP22 CPU Debug Port

Signal Name	FPGA Pin #	Description
CPU.TDO	Y8	CPU JTAG Data Out
CPU.TDI	W8	CPU JTAG Data In
CPU.TCK	Y10	CPU JTAG Clock
CPU.TMS	W9	CPU JTAG Mode
CPU.HALT	AA11	CPU Halt
CPU.TRST	W10	CPU Tristate

2.10.7 CPU TRACE Port

The processor uses the trace interface when operating in real-time trace-debug mode. Real-time trace-debug mode supports real-time tracing of the instruction stream executed by the processor. In this mode, debug events are used to cause external trigger events. An external trace tool (such as RISCTrace) uses the trigger events to control the collection of trace information. The broadcast of trace information on the trace interface occurs independently of external trigger events (trace information is always supplied by the processor). Real-time trace-debug does not affect processor performance. The following figure shows the Trace connector on the Virtex-II Pro development board followed by a table that provides a brief description of Trace interface signals.
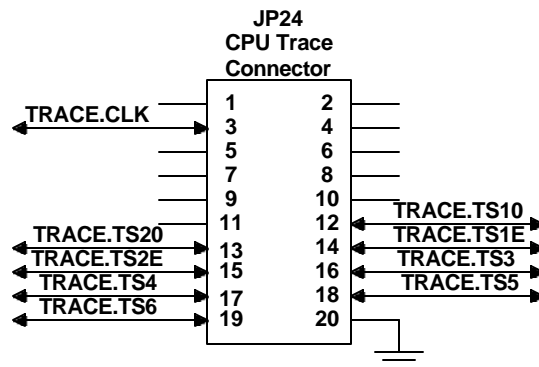
Figure 16- CPU Trace Port

Table 16 - CPU Trace Port Signal Assignments

Signal Name	FPGA Pin #	Description
TRACE.CLK	T5	Trace Clock
TRACE.TS3	U4	Trace Status
TRACE.TS4	N5	Trace Status
TRACE.TS5	V4	Trace Status
TRACE.TS6	M5	Trace Status
TRACE.TS10	U5	Execution status
TRACE.TS1E	U3	Execution status
TRACE.TS20	R5	Execution status
TRACE.TS2E	P5	Execution status

2.11 ISP PROM

The Virtex-II Pro development board utilizes one or two Xilinx XC18V04 ISP PROMs. The 2VP4 FPGA requires one PROM for configuration storage, while the 2VP7 FPGA needs two PROMs to hold the 4.4Mbits of configuration data. Therefore, for the 2VP7 version of the board, both of the PROMs need to be programmed with configuration data.

The JTAG port on the XC18V04 device is used to program the PROM with an .mcs file created by the Xilinx ISE software. Once the XC18V04 has been programmed, the user can configure the Virtex-II Pro device by asserting the PROGn signal (pressing the SW2 **Program** switch does this). Upon activation of the PROGn signal the XC18V04 device will use its FPGA Configuration Port to configure the FPGA. For this to occur, the FPGA must be set for the Master Serial mode via the mode select jumpers, M0, M1 and M2.

If the Virtex-II Pro configuration mode is set to Master Serial, the PROM's D0, CE, CCLK, RESET/OE, and the CF signals are used to configure the FPGA. The following figure shows the ISP PROM's interface to the JTAG port and the Virtex-II Pro FPGA configuration port.
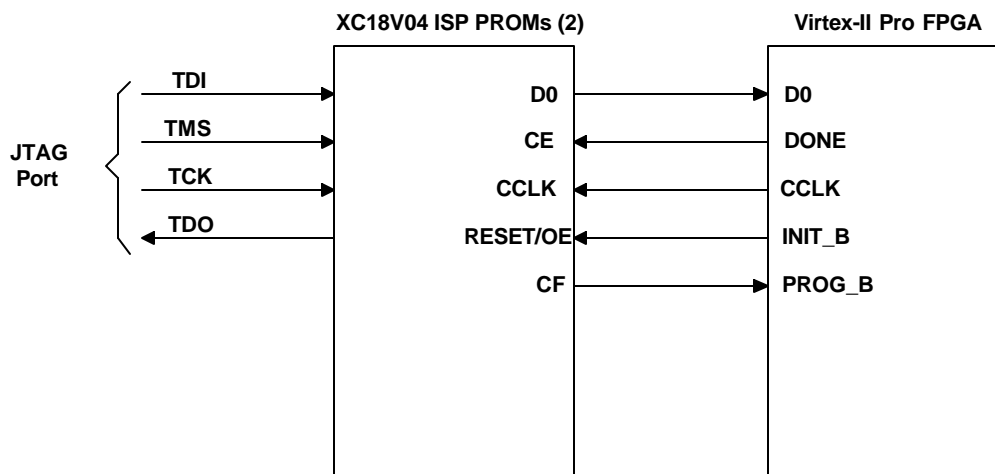
Figure 17 - Configuration PROM Interface

Jumper JP19 allows the ISP PROMs to be removed from the chain if desired. This can sometimes help when trouble shooting a JTAG chain error. The table below shows the setting for this jumper.

Table 17- JP19 Description

Jumper	Description
1-2 and 3-4	ISP PROMs in JTAG chain
2-3	ISP PROMs removed from JTAG chain

2.12 Bank I/O Voltage

The following table shows the jumper settings for the Virtex-II Pro bank I/O voltage (VCCO) selection. Banks 1, 2, and 3 can be set to 2.5V or 3.3V while all other banks are fixed at 2.5V.

Table 18- Bank I/O Voltage Jumper Settings

Bank #	Jumper		I/O Voltage
0	Fixed		2.5V
1	JP15		
	1-2	2-3	
	Closed	Open	2.5V
	Open	Closed	3.3V
2	JP16		
	1-2	2-3	
	Closed	Open	2.5V
	Open	Closed	3.3V
3	JP18		
	1-2	2-3	
	Closed	Open	2.5V
	Open	Closed	3.3V
4	Fixed		2.5V
5	Fixed		2.5V
6	Fixed		2.5V
7	Fixed		2.5V

2.13 Voltage Regulators

The following figure shows the voltage regulators that are used on Virtex-II Pro development board to provide various on-board voltage sources. As shown in the following figure, JP1 connector is used to provide the main 5.0V voltage to the board. This voltage source is provided to all on-board regulators to generate the 1.5V, 2.5V, and 3.3V voltages for the digital section of the board and the 2.5V for the Rocket I/O transceiver section.
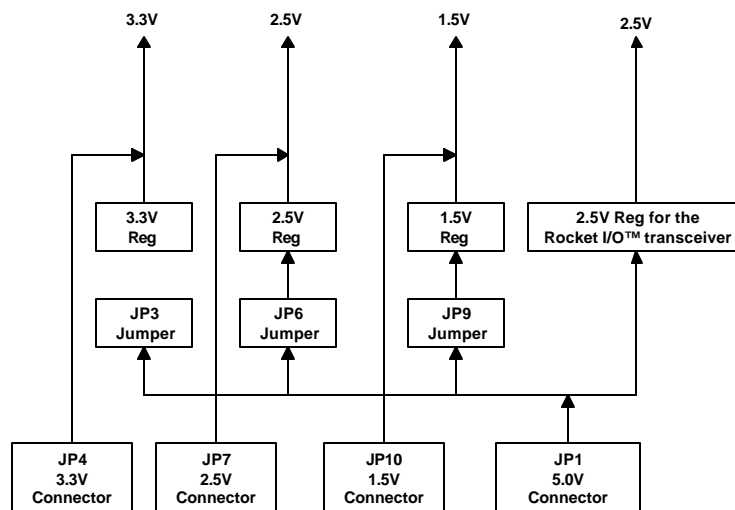
Figure 18 - Voltage Regulators

For the on-board digital voltages (1.5V, 2.5V, and 3.3V), if the current provided by the on-board regulator is not sufficient for some applications, the user can directly drive the voltage source and bypass the on-board regulators. This is accomplished by removing jumpers JP3, JP6 and JP9 and adding jumpers to JP5, JP8 and JP11.

Table 19 - Voltage Regulator Jumper Settings

| Jumper	Jumper Setting	3.3V Source (3A Maximum)	2.5V Source (1.5A Maximum)	1.5V Source (1.5A Maximum)
JP3	Open	External 3.3V supply via JP4 connector	NA	NA
	Closed	On-board 3.3V regulator	NA	NA
JP6	Open	NA	External 2.5V supply via JP7 connector	NA
	Closed	NA	On-board 2.5V regulator	NA
JP9	Open	NA	NA	External 1.5V supply via JP10 connector
	Closed	NA	NA	On-board 1.5V regulator

2.14 Configuration Mode

The following table shows the Virtex-II Pro configuration modes. It should be noted that the Master and Slave SelectMap mode of configurations are not supported on the Virtex-II Pro development board.

Table 20 – Configuration Mode Jumper Settings

Mode	PC Pull-up	JP12			
		1-2 (M2)	3-4 (M1)	5-6 (M0)	7-8 (HSWAP_EN)
Master Serial	Yes	Closed	Closed	Closed	Closed
Master Serial	No	Closed	Closed	Closed	Open
Slave Serial	Yes	Open	Open	Open	Closed
Slave Serial	No	Open	Open	Open	Open
Master SelectMap*	Yes	Closed	Open	Open	Closed
Master SelectMap*	No	Closed	Open	Open	Open
Slave SelectMap*	Yes	Open	Open	Closed	Closed
Slave SelectMap*	No	Open	Open	Closed	Open
JTAG	Yes	Open	Closed	Open	Closed
JTAG	No	Open	Closed	Open	Open

* Not supported on board

2.15 P160 Expansion Module

A P160 Expansion Module is included on the Virtex-II Pro development to support plug-in modules for various applications. The following tables show the Virtex-II Pro pin assignments to

the P160 Expansion Module connectors (JX1 & JX2) located on the Virtex-II Pro development board.

Table 21 - JX1 Signal Assignments

FPGA Pin #	I/O Connector Signal Name	JX1 Pin #		I/O Connector Signal Name	FPGA Pin #
	TCK	A1	B1	FPGA.BITSTREAM	
	GND	A2	B2	SM.DOUT/BUSY	
	TMS	A3	B3	FPGA.CCLK	
	Vin	A4	B4	DONE	
	TDI	A5	B5	INITn	
	GND	A6	B6	PROGRAMn	
	TDO	A7	B7	NC	
	3.3V	A8	B8	LIOB8	G18
F18	LIOA9	A9	B9	LIOB9	E17
	GND	A10	B10	LIOB10	E16
H20	LIOA11	A11	B11	LIOB11	E15
	2.5V	A12	B12	LIOB12	E14
E11	LIOA13	A13	B13	LIOB13	F14
	GND	A14	B14	LIOB14	F13
F11	LIOA15	A15	B15	LIOB15	F12
	Vin	A16	B16	LIOB16	H22
F10	LIOA17	A17	B17	LIOB17	H21
	GND	A18	B18	LIOB18	G22
D9	LIOA19	A19	B19	LIOB19	G21
	3.3V	A20	B20	LIOB20	F22
B11	LIOA21	A21	B21	LIOB21	F21
	GND	A22	B22	LIOB22	E22
E10	LIOA23	A23	B23	LIOB23	E21
	2.5V	A24	B24	LIOB24	D22
G19	LIOA25	A25	B25	LIOB25	D21
	GND	A26	B26	LIOB26	C22
F20	LIOA27	A27	B27	LIOB27	C21
	Vin	A28	B28	LIOB28	D18
F19	LIOA29	A29	B29	LIOB29	D17
	GND	A30	B30	LIOB30	D16
E20	LIOA31	A31	B31	LIOB31	C16
	3.3V	A32	B32	LIOB32	D15
C10	LIOA33	A33	B33	LIOB33	C15
	GND	A34	B34	LIOB34	D14
D10	LIOA35	A35	B35	LIOB35	D13
	2.5V	A36	B36	LIOB36	C13
E19	LIOA37	A37	B37	LIOB37	E13
	GND	A38	B38	LIOB38	B12
E12	LIOA39	A39	B39	LIOB39	C12
	Vin	A40	B40	LIOB40	D12

Table 22 - JX2 Signal Assignments

FPGA Pin #	I/O Connector Signal Name	JX2 Pin #		I/O Connector Signal Name	FPGA Pin #
J21	RIOA1	A1	B1	**GND**	
J22	RIOA2	A2	B2	RIOB2	J18
K21	RIOA3	A3	B3	**Vin**	
K22	RIOA4	A4	B4	RIOB4	J17
L21	RIOA5	A5	B5	**GND**	
M21	RIOA6	A6	B6	RIOB6	K17
N22	RIOA7	A7	B7	**3.3V**	
P22	RIOA8	A8	B8	RIOB8	L17
P21	RIOA9	A9	B9	**GND**	
R22	RIOA10	A10	B10	RIOB10	J19
R21	RIOA11	A11	B11	**2.5V**	
T22	RIOA12	A12	B12	RIOB12	J20
T21	RIOA13	A13	B13	**GND**	
U22	RIOA14	A14	B14	RIOB14	K19
U21	RIOA15	A15	B15	**Vin**	
V22	RIOA16	A16	B16	RIOB16	K20
V21	RIOA17	A17	B17	**GND**	
W22	RIOA18	A18	B18	RIOB18	K18
W21	RIOA19	A19	B19	**3.3V**	
Y22	RIOA20	A20	B20	RIOB20	L20
Y21	RIOA21	A21	B21	**GND**	
AA22	RIOA22	A22	B22	RIOB22	L19
R20	RIOA23	A23	B23	**2.5V**	
R19	RIOA24	A24	B24	RIOB24	L18
T20	RIOA25	A25	B25	**GND**	
T19	RIOA26	A26	B26	RIOB26	M18
U20	RIOA27	A27	B27	**Vin**	
U19	RIOA28	A28	B28	RIOB28	M19
V20	RIOA29	A29	B29	**GND**	
V19	RIOA30	A30	B30	RIOB30	M20
M17	RIOA31	A31	B31	**3.3V**	
N17	RIOA32	A32	B32	RIOB32	N18
P17	RIOA33	A33	B33	**GND**	
P18	RIOA34	A34	B34	RIOB34	N20
R18	RIOA35	A35	B35	**2.5V**	
T18	RIOA36	A36	B36	RIOB36	N19
U18	RIOA37	A37	B37	**GND**	
AB21	RIOA38	A38	B38	RIOB38	P20
N21	RIOA39	A39	B39	**Vin**	
H18	RIOA40	A40	B40	RIOB40	P19

3   Revisions

V2.0   Initial Release for Rev 2 board   August 28, 2002

V2.1   Update   October 7, 2002
        Corrected Table 21 for LIO.A13 and LIO.A15 pin connection
        Modified Figure 4 and Table 5 for SDRAM data strobe modification

V2.2   Update   November 13, 2002
        Changed V2PDK reference to EDK
        Updated RDC web link

4 Appendix - Rev 2 Board PCB Modification

The SDRAM interface provided on the revision 2 Virtex-II Pro board was originally design for x32 bit read and write accesses. The interface was designed using two separate x16 bit memories (U18 and U19), with U18 providing the lower 16-bits and U19 providing the upper 16-bits. This resulted in the SDRAM's upper data strobes and lower data strobes being tied together and driven by a single upper and lower strobe signal from the FPGA.

Original SDRAM Strobe Configuration

Signal Name	Description	FPGA Pin #
MRAM.UDQM	Upper Data Strobe (SDRAM pin F1 on U18 and U19)	F4
MRAM.LDQM	Lower Data Strobe (SDRAM pin E8 on U18 and U19)	T3

In order to enhance the functionality of the board for x8, x16, and x32 bit accesses, a modification was made to the PCB. The upper strobe is now split to two FPGA pins, one for U18 and one for U19. The same change was made to the lower strobe.

Revised SDRAM Strobe Configuration

Signal Name	Description	FPGA Pin #
MRAM2.UDQM	Upper Data Strobe (SDRAM pin F1 on U19)	U3
MRAM.UDQM	Upper Data Strobe (SDRAM pin F1 on U18)	F4
MRAM2.LDQM	Lower Data Strobe (SDRAM pin E8 on U19)	U4
MRAM.LDQM	Lower Data Strobe (SDRAM pin E8 on U18)	T3

The change described above was implemented by adding two fly wires to the PCB and cutting the two DQM traces going to U19. As a result, the CPU Trace connector signals TRACE.TS1E and TRACE.TS3 are now shared with the MRAM2.UDQM and MRAM2.LDQM

Not all Rev 2 boards include this modification. If your board does not contain visible wires around the SDRAM memory, then the data strobes are common to both SDRAMs.