Frequently asked questions regarding:

TDK Guide to ESD Capacitors

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Abstract
The damage caused by electrostatic discharge (ESD) can be severe. ESD can come from contact with the outside world or from within the system itself. The end customers are concerned with protecting the electrical circuits and there are a variety of test requirements out there. The Design Engineer is faced with the challenge of meeting module level ESD requirements and meeting design optimization for size, cost, etc. This paper answers some commonly asked questions regarding ESD and offers some insight to selecting the proper capacitor for ESD protection.

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TDK Guide to ESD Capacitors

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Q1. *What is ESD?*

A1. Electrostatic discharge (ESD) is an uncontrolled high voltage spike that is very short in duration. A common example of ESD is the static electricity build up a person stores when walking across carpet. The discharge in this example occurs when the person touches metal or another person. ESD is typically in the thousands of volts range and can cause severe damage to electrical circuits.

ESD can come from human contact as well as machine interface contact. These two sources are the basis of the industry ESD models.

Q2. *How can you protect against ESD?*

A2. The most common place to protect against ESD is at the interface sections of the circuit. This is where a connector is used to interface one module to another part of the system. Design Engineers typically use ceramic capacitors as ESD protection capacitors at connector pins and communication pins. The entire module may be subject to a module level ESD requirement while the capacitors may or may not also be required to meet a component level ESD requirement. The end customer is most concerned with the module level requirement since it is up to the Design Engineer to decide what component level requirements are needed to guarantee the module level requirements.

Q3. *What are the ESD models?*

A3. There are several ESD models including charged device model (CDM), machine model (MM), and human body model (HBM). Of these, the HBM is most commonly used to test and rate capacitors.

Q4. *What is the charged device model (CDM)?*

A4. The CDM is one of the most neglected models. This ESD event occurs when a device slides down a tube, bag, or similar source. This also can occur when connecting the device to a ground. A common discharge network consists of a 4 or 30pF capacitor.

Q5. *What is the machine model (MM)?*

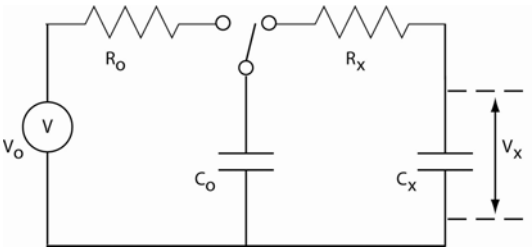
A5. Similar to the HMB is the Machine Model. This model originated in Japan as a worst case HBM. The Machine Model simulates a discharge from some conductive material such as a metal frame or tool. An example of this can be found in the pins of an automatic tester.

A common discharge network consists of 200pF capacitor, no resistor, and discharging through a 500nH series inductor.

Q6. *What is the human body model (HBM)?*

A6. The HBM is the oldest and most common form of ESD. As stated in Mil-Std 1686 section 5.2.1.1, the principal source of ESD damage is the human body, as modeled by the HBM standards. Although this is called the human body model, it really represents the discharge from the human body or *any* charged device into an ESD sensitive (ESDS) device. This is commonly represented as the discharge from a fingertip to the device.

The equivalent circuit as shown here contains a charged capacitor Co. When the switch is thrown, C_O discharges through R_X into the DUT (C_X).



This model was introduced under MIL-STD 883 method 3015 where C_O = 100pF and R_X = 1.5kohm. Also commonly used is IEC 61000-4-2 where C_O = 150pF and R_X = 330 ohms. For AEC-Q200, C_O = 150pF and R_X =

2kohm. In addition to these, there are countless variations of the HBM ESD test.

Q7. *What are some of the industry recognized ESD test specs?*
A7. There are a countless number of industry and customer specific ESD test specifications. There are specifications for the component level as well as the module level. Among all these specification, the most common include Mil-Std 883 method 3015, JESD22-A114, and AEC-Q200.

These specifications vary in several parameters including the values within the discharge network, ESD voltage level increments, number of ESD pulses (strikes) per test, sequence of polarity, and charge/discharge sequence.

Many of these specifications also have their own ESD level classification system to indicate the degree of ESD sensitivity. The automotive AEC-Q200, for example, shows one of the higher levels with ESD testing up to 25kV.

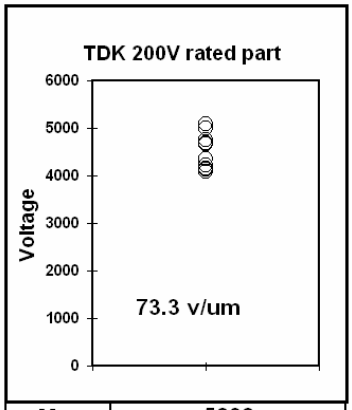
Q8. *How does TDK typically test for ESD?*
A8. Based on our most prevalent customer requirements, TDK follows the AEC-Q200 as the typical ESD test method. Existing family qualifications are conducted with this method.

The AEC-Q200 starts at 6kV and follows a progressive voltage test scale based on a progression tree. In an ideal situation the progression would be 6kV, 12kV, 16kV, and 25kV. A single charge/discharge at each polarity is triggered at each voltage level. Virgin parts are allowed at each voltage. It should be noted that proper and complete discharge is critical in obtaining accurate ESD results.

The highest level passed represents the ESD classification level (ESD sensitivity) for the component being tested. This classification level helps the design engineer determine the right capacitor for their application.

Q9. *How does TDK recommend selecting the right capacitor for ESD?*
A9. Through experimentation, TDK has determined that there are three critical parameters that help the design engineer determine the best value for an ESD capacitor: voltage breakdown, capacitance, and DC bias.

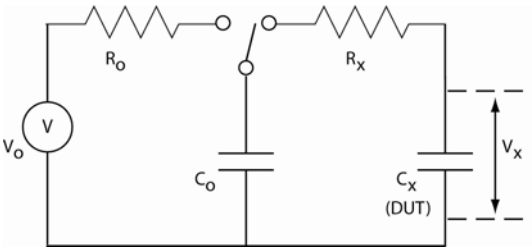
Q10. *What is voltage breakdown (V_{bd})?*
A10. Voltage breakdown is a test method used to quantify the voltage level strength of a capacitor. DC voltage is applied across the capacitor at a fixed voltage ramp rate (i.e. 100v/s) until the part fails. This determines the maximum sustained voltage the capacitor can withstand but does not directly indicate maximum ESD voltage level.



Max	5090
Min	4080
Ave	4520
Sig	368

Example of V_{bd} test results

Q11. *What is the capacitance (DUT) effect?*
A11. The DUT effect refers to the effective resultant voltage seen across the capacitor under test (DUT) in the ESD test circuit.



Nodal analysis shows that the relationship between the resultant voltage (V_X) across the DUT (C_X) as

$$V_X = \frac{C_O}{C_O + C_X} V_O$$

By keeping the source voltage (V_O) and charge capacitor (C_O) constant, the relationship between resultant voltage (V_X) and the DUT capacitor (C_X) are inversely proportional. This means that as you select a higher value C_X, V_X decreases.

To illustrate the DUT effect, take as an example a 4kV (V_O) ESD requirement for a 1000pF capacitor (C_X). Also assume we are using the AEC-Q200 test method which uses C_O = 150pF. The DUT effect relationship shows that with 4kV applied, C_X only sees 521.7V (V_X).

Q12. ***What is DC bias?***

A12. When DC voltage is applied to a ceramic capacitor, the effective capacitance may be different from the nominal capacitance. DC Bias is typically expressed in percent capacitance change from nominal.

$$\text{DC Bias (\%)} = \frac{C_{final} - C_{init}}{C_{init}}$$

DC Bias is largely due to the dielectric material. Of course other design and construction factors play a role as well. For Class I dielectrics such as C0G, the change is relatively flat. For Class II such as X7R and X5R, you may see a slight increase in capacitance initially which is immediately followed by a steady decrease as you approach the rated capacitance. Typically for Class II dielectrics, the DC bias is between -10% to -70%.

As the applied voltage increases, effective capacitance decreases. DC bias is repeatable and does not have any destructive effect on the performance or life of the capacitor as long as you do not exceed the rated voltage.

Q13. ***How does all of this help me select an ESD protection capacitor?***

A13. The first step is to confirm how much ESD protection is required. Keep in mind that a 12,000V module level requirement does not mean that the component requirement is also 12,000V. In many cases, the end customer sets a module level ESD requirement and lets the Design Engineer decide what component level requirements are necessary to meet the module level ESD.

ESD test rating alone is not the best way to select a capacitor value. Without looking at V_{bd}, DUT, and DC Bias affects, the Design Engineer could over-design or even under-design the protection circuit.

First, recall the relationship between the resultant voltage (V_X) across the DUT (C_X).

$$V_X = \frac{C_O}{C_O + C_X} V_O$$

As discussed earlier, DC bias causes a reduction in capacitance as much as 70% for Class II MLCCs. If we assume this as worst case,

$$V_X = \frac{C_O}{C_O + 0.3C_X} V_O$$

This relationship tells us how much voltage (V_X) our capacitor (C_X) will really see. Therefore we make our capacitor selection by choosing a capacitor with the voltage breakdown level (V_{bd}) greater than V_X.

$V_{bd} > V_X$, where

$$V_{bd} > \frac{C_O}{C_O + 0.3C_X} V_{\text{ESD level required}}$$

For example, assume C_O = 150pF, C_X = 1000pF and V_{ESD} = 12kV as we have been using in our previous examples. This results in a minimum V_{bd} of 4000V. The 1000pF capacitor we chose for C_X must have a minimum V_{bd} level of 4000V.

If we refer back to the example V_{bd} chart from question 10 above, we see that the average V_{bd} level is 4520V and the minimum is 4080V for this capacitor and therefore is a suitable choice.

Q14. ***How can the ESD rating be improved on a part?***

A14. There are times when TDK can evaluate the design of an item and redesign a part for improved ESD performance. There are several ways to accomplish this. A simple way is to alter the construction using a combination of increasing layer thickness, altering the active area, and changing the number of layers. Some improvements are also achieved through a finer processing of the raw material grain size or even a modification of the dielectric.
It is important to understand that if improved ESD performance is driven by a single customer's request, this may be a custom part. Custom parts often may come at a cost premium as well as extended lead times. Due to this, it is important that the Design Engineer look closely at the circuit needs and the design considerations discussed in this paper first to determine how much ESD sensitivity really is necessary before resorting to a custom part. Often there may be another part offered that will meet the design requirements.

Q15. ***What are some resources to learn more about ESD?***
A15. There are many resources to learn more about ESD and ESD testing requirements. Most of the references used in this paper focused on industry test methods. The following list of specifications and websites are a good place to start.

Mil-Std 1686
Mil-Std 883 method 3015
JESD22-A114
AEC-Q200
ESD-DS5.2-1996
ESDS5.2-1994
ESD-STM5.1-1998
ESDS5.3.1-1996
www.esda.org
www.keytek.com

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