# Microcontroller Training

Infineon Incore TC 1796

Controller: TC1796

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Never stop thinking

### PWM

In this exercise you will develop an application that generates a sinusodial complementary 3-phase PWM (Puls Width Modulation) signal with an update frequency of 20KHz using the General Purpose Timer Array (GPTA).

The GPTA provides a set of timer, compare and capture functionalities that can be flexibly combined to form signal measurement and signal generation units. They are optimized for tasks typical of engine, gearbox, and electrical motor control applications, but can also be used to generate simple and complex signal waveforms needed in other industrial applications.

The TC1796 contains two General Purpose Timer Arrays (GPTA0 and GPTA1) with identical functionality, plus an additional Local Timer Cell Array (LTCA2).







#### **GPTA Features**

Each of the General Purpose Timer Arrays (GPTA0 and GPTA1) provides a set of hardware modules required for high-speed digital signal processing:

Clock Generation Unit

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic units (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse-width measurement capabilities.
- A Digital Phase Locked Loop unit (PLL) generates a programmable number of GPTA module clock ticks during an input signal's period.

Signal Generation Unit

- Global Timer units (GT) driven by various clock sources are implemented to operate as a time base for the associated Global Timer Cells.
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an external or internal event. A GTC may also be used to control an external port pin depending on the result of an internal compare operation. GTCs can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs, enabled in Timer Mode or Capture Mode, can be clocked or triggered by various external or internal events.



Fig.1 GPTA Block Diagram



#### **LTC Functionality**

- Local Timer Cell (LTC)
- 64 independent units
- Three basic operating modes (Timer, Capture and Compare) for 63 units
- Special compare modes for one unit
- 16-bit data width
- $\blacksquare f_{\text{GPTA}}$  maximum resolution
- $\blacksquare f_{GPTA}/2$  maximum input signal frequency



#### Fig.2 Architecture of Local Timer Cells and Interconnections between LTCs





Fig.3 PWM Generation with Local Timer Cells

	Value	Cell	Output Control Mode	Port
Reset Timer	-	LTC0	-	-
Compare Period	Т	LTC1	Interrupt: adjust t <sub>off,H</sub> , t <sub>on,L</sub>	-
Compare Mid Period	T/2	LTC2	Interrupt: adjust t <sub>on,H</sub> , t <sub>off,L</sub>	-
Compare High side On	t <sub>on,H</sub>	LTC3	Set output by a local event	-
Compare High side Off	t <sub>off,H</sub>	LTC4	Reset output by a local event or copy the previous cell action	P2.8
Compare Low Side Off	t <sub>on,L</sub>	LTC5	Reset output by a local event	-
Compare Low Side On	t <sub>on,L</sub>	LTC6	Set output by a local event or copy the previous cell action	P2.9

Release 04/2007

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#### 1. Create a DAvE project

Open the Windows Explorer and create a new directory c:\infineon\pwm. Copy the isr.dav file from the previous exercise to the new directory and rename the file to pwm.dav.

#### 2. Open the GPTA clock properties

Click on **GPTA Clock** in the project window to open the GPTA Clock properties.





#### 3. Set up the GPTA clock properties

On the Module Clock page

- Select Select normal divider mode.
- **■** Enter **Required module clock [MHz]** to  $f_{GPTA} = 75$  MHz.

😨 GPTA Clock		×
Module Clock Timer Clock Control		
Module Disable Request	Sleep Mode Enable Control Disable the sleep mode for the GPTA module (EDIS)	
<ul> <li>Divider Mode Control (DM)</li> <li>Disable module clock</li> <li>Select normal divider mode</li> <li>Select fractional divider mode</li> </ul>	Disable Clock Control Dutput clock becomes inactive after initialization (DISCLK) Enable Hardware Clock Control Bit DISCLK is reset by HW while input signal ECEN (CAN_INT_015) is a high level (ENHW)	
Module Clock Control Required module clock [MHz] 75.000	Real module clock [MHz] 75.000	
Minimal module clock [KHz] 73.242	Percentage of deviation [%] 0.000	
Maximal module clock [MHz] 75.000	Step value (STEP) 0x3FF	



#### On the **Timer Clock Control** ■ Check **Enable GPTA0 timer clock (G0EN)**.



The GPTA clock is completely configured. Click the **Close** icon 🚵 on the dialog toolbar to close the **GPTA Clock** dialog.

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#### 4. Open the GPTA0 properties

Click on **GPTA0** in the project window to open the GPTA0 properties.





#### **5. Set up the GPTA0 properties**

On the **Clock Generation** page click **CDU** to open the Clock Distribution Unit properties.

😨 General Purpose Timer Array 0 (GPTAO)	X			
Input Pins Clock Generation Global Timer Local Timer Output Pins Functions SRN Parameters Notes				
Filter and Prescaler Cell (FPC)				
FPC 0         FPC 1         FPC 2         FPC 3         FPC 4         FPC 5				
Phase Discrimination Logic Cell (PDL)				
PDL 0 PDL 1				
Duty Cycle Measurement and Limit Checking Cell (DCM)				
DCM 0 DCM 1 DCM 2 DCM 3				
Digital Phase Locked Loop Cell (PLL)				
PLL				
Clock Distribution Unit (CDU)				
CDU				



#### On the Clock Bus 7-6 page

At Clock Bus Signal 7 (DFA07) select Divided GPTA0 clock and choose the Divide factor GPTA0 clock / 2^1. The maximum input frequency of the local timer cells is  $f_{GPTA}/2$ .

😨 Configure Clock Distribution Unit (CDU)
🖄 🕂 ?
Clock Bus 7-6 Clock Bus 5-4 Clock Bus 3-2 Clock Bus 1-0
Clock Bus Signal 7 (DFA07)
C Clock coming from FPC4 (= 75.0000 MHz)
Divided GPTA0 clock
Divide factor GPTA0 clock / 2^1 (= 37.500 MHz; 0.0267 μs)
Clock Bus Signal 6 (DFA06)
Clock coming from FPC1 (= 75.0000 MHz)
C Divided GPTA0 clock
Divide factor
bo Clock Distribution Unit is completely configured. Click the <b>Close</b> icon 🖄

The Clock Distribution Unit is completely configured. Click the **Close** icon **M** on the dialog toolbar to close the **Configure Clock Distribution Unit (CDU)** dialog.



#### 6. Set up the GPTA0 properties. Local Timer

On the Local Timer page click LTCO to open the Local Timer Cell 0 properties.

😨 General Purpose Timer Array 0 (GPTA0)							
A 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2							
Input Pins   Clock Generation   Global Timer   Local Timer   Output Pins   Functions   SRN   Para	neters Notes						
Local Timer Cell (LTC)							
LTCO LTC1 LTC2 LTC3 LTC4 LTC5 LTC6	LTC 7						
LTC 8 LTC 9 LTC 10 LTC 11 LTC 12 LTC 13 LTC 14	LTC 15						
LTC 16 LTC 17 LTC 18 LTC 19 LTC 20 LTC 21 LTC 22	LTC 23						
LTC 24 LTC 25 LTC 26 LTC 27 LTC 28 LTC 29 LTC 30 LTC 31							
LTC 32 LTC 33 LTC 34 LTC 35 LTC 36 LTC 37 LTC 38	LTC 39						
LTC 40 LTC 41 LTC 42 LTC 43 LTC 44 LTC 45 LTC 46	LTC 47						
LTC 48 LTC 49 LTC 50 LTC 51 LTC 52 LTC 53 LTC 54	LTC 55						
LTC 56 LTC 57 LTC 58 LTC 59 LTC 60 LTC 61 LTC 62	LTC 63						

On the **LTCO** page configure the cell as reset timer:

- Choose Enable LTC0 cell after initialization (CEN),
- Select Timer with reset from adjacent LTC with higher order number. When the timer value in LTC0 matches the compare value stored in LTC1, the Event Out signal from LTC1 is activated and passed upstream to LTC0 as the Event In signal which then resets the timer to the value of FFFF<sub>h</sub>.
- Check Connect the input line to LTCO (LIMENO). The cell will be connected to the clock bus line 7 which we configured in step 5.
- Check Enable rising edge of selected input signal (RED).







On the **Data Input** page of LTC0 and select the internal input **Clock7** as data input line for LTC0.

😨 Local Timer Cell 0 (LTC0)		×
1 🔁 🗊 🗸 💡		
LTC0 Data Input Output Selection		
Data input line selection for LTCO (LIMGO	and LIML0)	
Port Input's:	GTC Input's:	Internal Input's:
🔘 Use GPTA0_IN0 (= none)	Use output of GTC0	C CLOCKO
🔘 Use GPTA0_IN1 (= none)	O Use output of GTC1	C CLOCK1
C Use GPTA0_IN2 (= none)	Use output of GTC2	C CLOCK2
O Use GPTA0_IN3 (= none)	Use output of GTC3	C CLOCK3
O Use GPTA0_IN4 (= none)	Use output of GTC4	C CLOCK4
Use GPTA0_IN5 (= none)	Use output of GTC5	C CLOCK5
🔘 Use GPTA0_IN6 (= none)	Use output of GTC6	C CLOCK6
🔘 Use GPTA0_IN7 (= none)	Use output of GTC7	୍ CLOCK7
🔘 Use GPTA0_IN32 (= none)	Note:	
🔘 Use GPTA0_IN33 (= none)	CLOCK7 = GP1	'A0 clock / 2^1 (= 37.500 MHz; 0.0267 μs)
💭 Use GPTA0_IN34 (= none)		C PDL1 forward signal
🔘 Use GPTA0_IN35 (= none)		O PDL1 backward signal
🔘 Use GPTA0_IN36 (= none)		C CAN_INT_015
🔘 Use GPTA0_IN37 (= none)		C SCU_IOUT1
🔘 Use GPTA0_IN38 (= none)		C SCU_IOUT2
💭 Use GPTA0_IN39 (= none)		C SCU_IOUT3

The LTC0 is completely configured as reset timer running at  $f_{GPTA}/2 = 37.5$  MHz. Click the **Close** icon **M** on the dialog toolbar to close the **Local Timer Cell 0 (LTC0)** dialog.



Click LTC1 on the Local Timer page. On the LTC1 page configure the cell to compare mode:

- Choose Enable LTC1 cell after initialization (CEN),
- Select Compare with last timer (=LTC0),

■ Check Enable low level of 'Select Line input' Si (SOL) and Enable high level of 'Select Line input' Si (SOH) to enable Compare mode in all cases,

■ Set the LTC1 register value (X) to the period value. Since the timer LTC0 resets to -1 (FFFF<sub>h</sub>) and then counts through 0 up to (and including) the compare value, the compare value used to generate a periodic interval is somewhat different than what might be expected. To generate a periodic interval of P clocks, the compare value must be set to (P-2). To get a symmetric PWM P must be even. P = 37.5MHz/20KHz = 1875. The period P will be choosen as the next higher even value 1876. The register is set to 1874 = 752<sub>h</sub>. Enter **0x0752** in the text field and type **Return**.



The LTC1 is completely configured. Click the **Close** icon 🚵 on the dialog toolbar to close the **LTC1** dialog.



Click LTC2 on the Local Timer page. On the LTC2 page and configure the cell to compare mode:

- Choose Enable LTC2 cell after initialization (CEN),
- Select Compare with last timer (=LTC0),
- Check Enable low level of 'Select Line input' Si (SOL) and Enable high level of 'Select Line input' Si (SOH) to enable Compare mode in all cases,
- Set the LTC2 register value to the mid period value -1+1876/2 = 937 = 3A9<sub>h</sub>. Enter **0x03A9** in the text field and type Return.



The LTC2 is completely configured. Click the **Close** icon 🚵 on the dialog toolbar to close the **LTC2** dialog.



To configure the phase U using LTC3/LTC4 and LTC5/LTC6 click LTC3 on the Local Timer page. On the LTC3 page configure the cell to compare mode:

- Choose Enable LTC3 cell after initialization (CEN),
- Select Compare with last timer (=LTC0),
- Check Enable low level of 'Select Line input' Si (SOL) and Enable high level of 'Select Line input' Si (SOH) to enable Compare mode in all cases,
- Choose Set the LTC3 output by an local event only as the Output Control Mode to set the output to high on a compare match. The LTC3 register value will be calculated in the mid period interrupt routine.





Open the LTC4 to LTC6 and configure them also in compare mode

■ LTC4: Choose Reset the LTC4 output by an local event or copy the previous cell action to set the output to pas-

sive on a compare match.

LTC4 Output Control Mode (OCM) Reset the LTC4 output by an local event or copy the previous cell action	s Control nable bypass Inctionality (BYP)	
	T/2	t <sub>off.H</sub> t <sub>on,L</sub>

To configure the low side of phase U using LTC5/LTC6 configure the **Output Control Mode**:

■ LTC5: Choose Reset the LTC5 output by an local event to set the output to low on a compare match,

Reset the LTC5 output by an local event only	LTC5 Output Control Mode (OCM) Bypass Control		dead time	—	
	Reset the LTC5 output by an local event only	A I			

■ LTC6: Choose Set the LTC6 output by an local event or copy the previous cell action to set the output to high on a compare match.



The high side and the low side of phase U are configured. Close the **LTC3** to **LTC6** dialogs.



For phase V open cell LTC7 to LTC10 and configure them also in compare mode: ■ LTC7: Choose **Set the LTC7 output by an local event**,

LTC7 Output Control Mode (OCM)	Bypass Control
Set the LTC7 output by an local event only Force the selected action after initialization (OIA)	Enable bypass functionality (BYP)

■ LTC8: Choose Reset the LTC8 output by an local event or copy the previous cell action,



- LTC9 Output Control Mode (OCM)	-	- Bupass Control-
		Bypass control
Reset the LTC9 output by an local event only		🗕 Enable bypass
Force the selected action after initialization (OIA)		functionality (BYP)

#### ■ LTC10: Choose Set the LTC10 output by an local event or copy the previous cell action.



The high side (LTC7/LTC8) and the low side (LTC9/LTC10) of phase V are configured. Close the LTC7 to LTC10 dialogs.



#### For phase W open cell LTC11 to LTC14 and configure them also in compare mode: ■ LTC11: Choose **Set the LTC11 output by an local event**,

LTC11 Output Control Mode (OCM)	Bypass Control
Set the LTC11 output by an local event only	- Enable bypass
Force the selected action after initialization (OIA)	functionality (BYP)

■ LTC12: Choose Reset the LTC12 output by an local event or copy the previous cell action,

LTC12 Output Control Mode (OCM)	Bypass Control
Reset the LTC12 output by an local event or copy the previous cell action	— Enable bypass
Force the selected action after initialization (OIA)	functionality (BYP)

#### ■ LTC13: Choose Reset the LTC13 output by an local event,

LTC13 Output Control Mode (OCM)	Bypass Control
Reset the LTC13 output by an local event only	- Enable bypass
Force the selected action after initialization (OIA)	functionality (BYP)

■ LTC14: Choose Set the LTC14 output by an local event or copy the previous cell action.



The high side (LTC11/LTC12) and the low side (LTC13/LTC10) of phase W are configured. Close the LTC11 to LTC14 dialogs.

To connect the data out of the cells to the port the **Output Pins** has to be configured.



#### On the **Output Pins** page open the **OUT0**, **OUT1**, **OUT8**, **OUT9**, **OUT10**, **OUT11** properties.

😨 General Purpose T	imer Array 0 (GPT/	AO)			×
🖄 🗗 🖓					
Input Pins Clock Genera	ation   Global Timer   Lo	cal Timer Output Pir	SRN	Parameters Notes	
Configure GPTA0 Inpu	t Pins				
OUTO (= none)	OUT1 (= none)	OUT2 (= none)	OUT3 (= none)	OUT4 (= none)	
OUT9 (= none)	OUT6 (= none)	OUT7 (= none)	OUT8 (= none)	OUT9 (= none)	
OUT10 (= none)	OUT11 (= none)	OUT12 (= none)	OUT13 (= none)	OUT14 (= none)	
OUT15 (= none)	OUT16 (= none)	OUT17 (= none)	OUT18 (= none)	OUT19 (= none)	
OUT20 (= none)	OUT21 (= none)	OUT22 (= none)	OUT23 (= none)	OUT24 (= none)	
OUT25 (= none)	OUT26 (= none)	OUT27 (= none)	OUT28 (= none)	OUT29 (= none)	
OUT30 (= none)	OUT31 (= none)	OUT32 (= none)	OUT33 (= none)	OUT34 (= none)	
OUT35 (= none)	OUT36 (= none)	OUT37 (= none)	OUT38 (= none)	OUT39 (= none)	
OUT40 (= none)	OUT41 (= none)	OUT42 (= none)	OUT43 (= none)	OUT44 (= none)	
OUT45 (= none)	OUT46 (= none)	OUT47 (= none)	OUT48 (= none)	OUT49 (= none)	
OUT50 (= none)	OUT51 (= none)	OUT52 (= none)	OUT53 (= none)	OUT54 (= none)	
		OUT55 (= none)			

#### Configure the OUT0 pin to P2.8:

G	PTA0_OUTO
Г	- GPTA0_OUT0 Pin Selection
	O No pin as GPTA0_OUT0 selected
	Use pin P2.8 as GPTA0 output signal 0 (GPTA0_0UT0)
	- Driver Mede



#### Configure the OUT1 pin to P2.9:

# GPTA0\_OUT1

- O No pin as GPTA0\_0UT1 selected
- Use pin P2.9 as GPTA0 output signal 1 (GPTA0\_OUT1)

#### Configure the OUT8 pin to P3.0:

#### GPTA0\_OUT8

-GPTA0\_OUT8 Pin Selection-

- O No pin as GPTA0\_0UT8 selected
- Use pin P3.0 as GPTA0 output signal 8 (GPTA0\_OUT8)

#### Configure the OUT9 pin to P3.1:

#### GPTA0\_OUT9

- GPTA0\_OUT9 Pin Selection -
- O No pin as GPTA0\_OUT9 selected
- Use pin P3.1 as GPTA0 output signal 9 (GPTA0\_OUT9)

#### Configure the OUT10 pin to P3.2:

GPTA0\_OUT10

-GPTA0\_OUT10 Pin Selection-

- O No pin as GPTA0\_OUT10 selected
- Use pin P3.2 as GPTA0 output signal 10 (GPTA0\_OUT10)

#### Configure the OUT11 pin to P3.3:

#### GPTA0\_OUT11

-GPTA0\_OUT11 Pin Selection-

No pin as GPTA0\_OUT11 selected

Use pin P3.3 as GPTA0 output signal 11 (GPTA0\_0UT11)



#### Close the 6 **Configure Alternate Pin Functions** dialogs.

The **Output Pins** page displays the complete configuration of the output pins.

😨 General Purpose Ti	imer Array O (GPT	TAO)		×
🔼 🕶 🕹				
Input Pins Clock Genera	tion   Global Timer   L	ocal Timer Output Pin	S Functions SRN	Parameters Notes
Configure GPTA0 Input	t Pins			
OUT0 (= P2.8)	OUT1 (= P2.9)	OUT2 (= none)	OUT3 (= none)	OUT4 (= none)
OUT5 (= Hone)	OUT6 (= none)	OUT7 (= none)	OUT8 (= P3.0)	OUT9 (= P3.1)
OUT10 (= P3.2)	OUT11 (= P3.3)	OUT12 (= none)	OUT13 (= none)	OUT14 (= none)
OUT15 (= none)	OUT16 (= none)	OUT17 (= none)	OUT18 (= none)	OUT19 (= none)
OUT20 (= none)	OUT21 (= none)	OUT22 (= none)	OUT23 (= none)	OUT24 (= none)
OUT25 (= none)	OUT26 (= none)	OUT27 (= none)	OUT28 (= none)	OUT29 (= none)
OUT30 (= none)	OUT31 (= none)	OUT32 (= none)	OUT33 (= none)	OUT34 (= none)
OUT35 (= none)	OUT36 (= none)	OUT37 (= none)	OUT38 (= none)	OUT39 (= none)
OUT40 (= none)	OUT41 (= none)	OUT42 (= none)	OUT43 (= none)	OUT44 (= none)
OUT45 (= none)	OUT46 (= none)	OUT47 (= none)	OUT48 (= none)	OUT49 (= none)
OUT50 (= none)	OUT51 (= none)	OUT52 (= none)	OUT53 (= none)	OUT54 (= none)
		OUT55 (= none)		

Select the Local Timer page again and click LTC4, LTC6, LTC8, LTC10, LTC12, LTC14.

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### Exercise 7: PWM

#### On the **Output Selection** page of each dialog

■ Check Connect output to GPTA\_OUTO (=2.8) on dialog Local Timer Cell 4 for the high side of phase U.



Connect ouput to OUT68 (MSC0\_ALTIN0.12)

Close the Legal Timer Cell 4 (LTC4) and Legal Timer Cell 6 (LTC6)

Close the Local Timer Cell 4 (LTC4) and Local Timer Cell 6 (LTC6) dialogs.

Connect output to GPTA0\_OUT4 (= none)



■ Check **Connect output to GPTA\_OUT8 (=3.0)** on dialog **Local Timer Cell 8** for the high side of phase V.

😨 Local Timer Cell 8 (LTC8)	
🖄 🕂 ?	
LTC8 Data Input Output Selection	
Output Pin Selection Connect output to GPTA0_OUT8 (= P3.0) Connect output to GPTA0_OUT9 (= P3.1) Connect output to GPTA0_OUT10 (= P3.2) Connect output to GPTA0_OUT11 (= P3.3) Connect output to GPTA0_OUT12 (= none) Connect output to GPTA0_OUT13 (= none)	MSC Output Selection  Connect ouput to OUT72 (MSC0_ALTIN1.0) Connect ouput to OUT73 (MSC0_ALTIN1.1) Connect ouput to OUT74 (MSC0_ALTIN1.2) Connect ouput to OUT75 (MSC0_ALTIN1.3) Connect ouput to OUT76 (MSC0_ALTIN1.4) Connect ouput to OUT77 (MSC0_ALTIN1.5)  OUT9 (=3.1) on dialog Local Timer Cell 10 for the low side of phase V.
😨 Local Timer Cell 10 (LTC10)	
Martin 1	
LTC10 Data Input Output Selection	
Output Pin Selection	MSC Output Selection
Connect output to GPTA0_0UT8 (= P3.0)	Connect ouput to OUT72 (MSC0_ALTIN1.0)
Connect output to GPTA0_0UT9 (= P3.1)	Connect ouput to OUT73 (MSC0_ALTIN1.1)
応 Connect output to GPTA0_0UT10 (= P3.2)	Connect ouput to OUT74 (MSC0_ALTIN1.2)
Connect output to GPTA0_0UT11 (= P3.3)	Connect ouput to OUT75 (MSC0_ALTIN1.3)
Connect output to GPTA0_0UT12 (= none)	Connect ouput to OUT76 (MSC0_ALTIN1.4)
Connect output to GPTA0_0UT13 (= none)	Connect ouput to OUT77 (MSC0_ALTIN1.5)
Close the Local Timer Cell 8 (LTC8)	) and Local Timer Cell 10 (LTC10) dialogs.



■ Check Connect output to GPTA\_OUT10 (=3.2) on dialog Local Timer Cell 12 for the high side of phase W.





#### **7.** Set up the GPTA0 properties. Service Request Node.

LTC1 and LTC2 are configured in period and mid period compare mode. To generate an interrupt on a compare match, the appropriate Service Request Node (SRN) has to be configured.

On the SRN page click Service Request Node 22-23 (LTC0-7).

😨 General Purpose Timer Array 0 (GPTA0)	
🔁 🕂 🔋	
Input Pins Clock Generation Global Timer Local Timer	Output Pins Functions SRN Parameters Notes
Service Request Nodes	
Service Request Node 0 - 1 (DCM0 - 1)	Service Request Node 2 - 3 (DCM2 - 3)
Service Request Node 4 (PLL)	Service Request Node 5 (GT0 - 1)
Service Request Node 6 - 9 (GTC0 - 7)	Service Request Node 10 - 13 (GTC8 - 15)
Service Request Node 14 - 17 (GTC16 - 23)	Service Request Node 18 - 21 (GTC24 - 31)
Service Request Node 22 - 23 (LTC0 - 7)	Service Request Node 24 - 25 (LTC8 - 15)
Service Request Node 26 - 27 (LTC16 - 23)	Service Request Node 28 - 29 (LTC24 - 31)
Service Request Node 30 - 31 (LTC32 - 39)	Service Request Node 32 - 33 (LTC40 - 47)
Service Request Node 34 - 35 (LTC48 - 55)	Service Request Node 36 - 37 (LTC56 - 63)



On the **SRNs** page enable the interrupt generation on the period and on the mid period compare match.

- Check Enable service request on LTC1 event (=compare with last timer),
- Check Enable service request on LTC2 event (=compare with last timer),
- Check Enable service request node 22 (SRE22).





On the **Interrupts** page and drag **GPTA0 SRN 22** from Level 0 to the CPU Interrupt level 3.

Service	Request Node 22 - 23				X
🖄 🐔	D • 🖇				
CDNo Int	terrupts Eurotional				
3HN3 10					
	CDU Jahannah (man 255)	DCD (whereast (where 255)		Level 0 (new interrupting)	
1 115	CPU Interrupt (max.255)	PCP Interrupt (max.200)		Lever o (non interrupting)	
Level 15					
Level 14					
Level 13					
Level 12					
Level 11					
Level 10			[		
Level 9			[		
Level 8					
Level 7					
Level 6					
Level 5	STM SRN 0				
Level 4					
Level 3	GPTA0 SRN 22				
Level 2	1				
Level 1					
			-		
Note: To	change the level and the group.	of an interrupt source, click on i	t drag it to	ite new position and drop it	
To set an	) interrupt source to the non inter	rupting level (Level 0) click on it	, drag it to	the 'Level O' list and drop it.	

Close the Service Request Node 22-23 dialog.



#### On the **Functions** page

■ Check the GPTA0\_vInit function.

General Purpose Timer Array 0 (GPTA0)	
🏝 🚛 - 🤋	
Input Pins Clock Generation Global Timer Local Time	er Output Pins Functions SRN Parameters Notes
<ul> <li>Initialization Function</li> </ul>	Source File
GPTA0_vInit	File name GPTA0.c
Function Library (Part 1)	Function Library (Part 2)
GPTA0_ubGetFPCGlitchState	GPTA0_vEnableCoherentUpdate
GPTA0_vResetFPCGlitchState	GPTA0_vStartGTTimer
GPTA0_uwGetDCMCapture	GPTA0_vStopGTTimer
GPTA0_uwGetDCMCapcom	GPTA0_vEnableTimerClock
GPTA0_vSetDCMCapcom	GPTA0_vDisableTimerClock
GPTA0_vGenerateDCMClockPulse	
GPTA0_vSetGTReload	
GPTA0_uwGetGTReload	
GPTA0_vWriteTmr	
GPTA0_uwReadTmr	
GPTA0_vOutputMode	
GPTA0_ubReadOutput	
GPTA0_vReEnableTmr	

The GPTA is completely configured to generate a complementary 3-phase PWM signal. Click the **Close** icon **M** on the dialog toolbar to close the **General Purpose Timer Array 0 (GPTA0)** dialog.



#### 8. Modify the STM properties.

Open the System timer properties and select the CMPO page

■ Change the **Start Bit Location of CMP0** to 20

😨 System Timer (STM)
Module Clock Resolutions CMP0 CMP1 Interrupt Control Interrupts Functions Parameters Notes
Start Bit Location of CMP0
Lowest bit number (0 to 24) of STM which is compared with the content of register CMP0 bit 0 (MSTART0)
Compare Register Size of CMP0
Number of bits (1 to 32) in register CMP0 (starting from 0), which are used for the compare operation with STM (MSIZE0)
Compare Register 0
Required compare value (CMP0)     0x00000001     Real compare value (dependent of MSIZE0)     0x00000001

The system timer interrupt is used to update the PWM values.

#### 9. Generate the application framework

Click on the **Generate Code** icon  $\frac{1}{2}$  on the application toolbar to start the code generation process. Save and close the *DAvE* project.

#### 10. Add a new project to the Tasking Workspace

Open the *Tasking* EDE. Choose File > Configure Project Space... > Add new project and add a new project c:\infineon\pwm\pwm.pjt.

# infineon

## Exercise 7: PWM

### **11. Add the application framework**

In the **Project Properties** dialog click the **Scan** icon H. A dialog appears. In the Pattern field, enter \*.c;\*.h. This will select all generated files of the application framework. Select the project directory and click **OK**.

#### 12. Set current project

Use the context menu in the workspace window to make the pwm project the current project.

#### 13. Load the project options

Choose Project > Load Options. In the Filename field enter c:\infineon\tc1796\_intmem.opt.

#### 14. Build the application

Click the **Build** icon 🔠 on the Build toolbar. The Build process finishes successfully.

#### 15. Add the user code

Add the following code to GPTA0.c. Include the standard math library at (GPTA0\_General,2).

```
// USER CODE BEGIN (GPTA0_General,2)
#include <math.h>
// USER CODE END
```

Define the following constants at (GPTA0\_General,4).

// USER CODE BEGIN (GPTA0\_General,4)

#define	LTC_FREQ	37500000	// = 37.5MHz
#define	PWM_FREQ	20000	// = 20.0kHz
#define	DEADTIME	1E-6	// = 1µs
#define	DEADTIME_CNTS	((short)	(LTC_FREQ * DEADTIME))
#define	PWM_PERIOD_CENTER_CNTS	((short)	((LTC_FREQ / PWM_FREQ) / 2)) // same as GPTA0_LTCXR02

```
// USER CODE END
```

Release 04/2007



Declare the following global variables at (GPTA0\_General,7). For the sinus a look up table is used to save time. Three circular buffers pointers are used to step through the elements of the array. Incrementing a circular buffer pointer that points to the last element results in a pointer to the first element.

```
// USER CODE BEGIN (GPTA0_General,7)
#define SINE_STEPS 360
short ______near ____circ duty[SINE_STEPS]; // duty lookup table in a circular buffer
short ______near ____circ *dutyU, *dutyV, *dutyW;
const float pi = 3.14159;
// USER CODE END
```

In the GPTA\_vInit function disable the interrupt for LTC1 and LTC2 at (Init, 3). The PWM will be started by the first STM interrupt.

```
// USER CODE BEGIN (Init,3)
GPTA0_LTCCTR01_REN = 0; // disable period interrupt
GPTA0_LTCCTR02_REN = 0; // disable mid period interrupt
// USER CODE END
```

Fill the duty lookup table and initialize the circular buffer pointer at (Init, 4)

```
// USER CODE BEGIN (Init,4)
for (int i=0;i<SINE_STEPS;i++)
   duty[i] = (PWM_PERIOD_CENTER_CNTS + 1) * 0.5*(sinf(i * 2*pi/SINE_STEPS) + 1);
dutyU = &duty[0]; // set to sin(0°)
dutyV = &duty[SINE_STEPS/3]; // set to sin(120°)
dutyW = &duty[-SINE_STEPS/3]; // set to sin(240°)
// USER CODE END</pre>
```



Configure the period and mid period interrupts at GPTA0\_visrN22 in file GPTA.c. Add the code for the period and mid period interrupt at (SRN22, 2). At zero percent duty the low side must be set to active, i.e.  $t_{on,L}$  should be ignored. This is done by setting  $t_{on,L}$  to -2 (=FFFE<sub>H</sub>), a value that is never reached.

```
// USER CODE BEGIN (SRN22,2)
unsigned int n;
if (GPTA0 LTCCTR01 REN)
  GPTA0 LTCCTR01 REN = 0; // disable period interrupt
  STM ICR CMPOEN = 1; // enable the stm interrupt
  // update duty U
  n = PWM PERIOD CENTER CNTS + *dutyU;
  GPTA0 LTCXR04 = n;
  GPTA0 LTCXR06 = n + DEADTIME_CNTS;
  //update duty V
 n = PWM PERIOD CENTER CNTS + *dutyV;
  GPTA0 LTCXR08 = n;
  GPTA0 LTCXR10 = n + DEADTIME CNTS;
  //update duty W
  n = PWM PERIOD CENTER CNTS + *dutyW;
  GPTA0 LTCXR12 = n;
  GPTA0 LTCXR14 = n + DEADTIME CNTS;
```

}

. . .



#### else

{

```
GPTA0_LTCCTR02_REN = 0; // disable mid period interrupt
GPTA0 LTCCTR01 REN = 1; // enable period interrupt
// update duty U
n = PWM PERIOD CENTER CNTS - *dutyU;
GPTA0 LTCXR03 = n;
GPTA0 LTCXR05 = (n == PWM PERIOD CENTER CNTS) ? 0xfffe :
                         ((n < DEADTIME CNTS) ? Oxffff : n - DEADTIME CNTS);
// update duty V
n = PWM PERIOD CENTER CNTS - *dutyV;
GPTA0 LTCXR07 = n;
GPTA0 LTCXR09 = (n == PWM PERIOD CENTER CNTS) ? 0xfffe :
                         ((n < DEADTIME_CNTS) ? 0xffff : n - DEADTIME_CNTS);
// update duty W
n = PWM PERIOD CENTER CNTS - *dutyW;
GPTA0 LTCXR11 = n;
GPTA0_LTCXR13 = (n == PWM_PERIOD_CENTER_CNTS) ? 0xfffe :
                         ((n < DEADTIME CNTS) ? Oxffff : n - DEADTIME CNTS);
}
```

```
// USER CODE END
```



Enable the mid period interrupt in file MAIN.c before the forever loop at (Main,9):

```
// USER CODE BEGIN (Main,9)
STM_ICR_CMP0EN = 1; // enable the stm interrupt
for(;;) // forever
;
// USER CODE END
In file STM.c define the *dutyU, *dutyV, *dutyW as extern and add to function STM viSRN0 (SRN0,3):
```

```
// USER CODE BEGIN (SRN0,3)
STM_ICR_CMP0EN = 0; // disable the stm interrupt
GPTA0_LTCCTR02_REN = 1; // enable mid period interrupt
dutyU++; dutyV++; dutyW++; // circular step through the sinus lookup table
// USER CODE END
```



At 0% duty LTC3 and LTC4 have the same compare value and the output is following the action request of the higher cell LTC4, e.g. the high side is set to passive. LTC5 is -2 and therefor ignored, so that the low side is set to active. At 100% duty LTC5 has a compare value of -1 and is set immediately. LTC6 is larger than the period in LTC1, so that a reset is never happen. I.e. The low side is set to passive.



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#### 16. Build the application

Click the **Build** icon 📇 on the Build toolbar. The Build process finishes successfully.

#### 17. Debug the application

Click the **Debug** icon **(a)** on the Build toolbar to open the *CrossView Pro* debugger.

#### 18. Connect an Oscilloscope

Connect the pins P2.8, P2.9, P3.0, P3.1, P3.2, P3.3 to a logic analyzer. Connect P2.10 to the trigger input.



#### 19. Run the application

Click the **Run** icon **>** on the *CrossView Pro* toolbar and see the logic analyzer output.

The cursor is adjusted to measure the dead time.

📕 Intronix	LogicPo	ort Logic Analyze	r - E:\infineon\pwm\p	wm.LPF						
File Options	Setup /	Acquisition View H	elp	_						
Waveforms	State List	t Notes 🖉 🗗		▶ 🖵 🗖 T!	<mark>⊬ <del>₮</del> →</mark>	$ \oplus, \odot, \otimes $	Buffer Position:	)		
Samp	ole Rate	▼ 50MHz	Sample Period	d 🔽 20n	s 💌 🗌	Pre-Trigger Buffer	▼ 50%	Measureme	ent A Source 💌	D1 💽
•										
Signal	Wire ID	-40us . I	-30us -21	Dus -	-10us	. <sup>T+0</sup>	+10us ,   , , ,	+20us	+30us , I , , ,	+40us ,   ,
TRG	D6									
- PWM		100110Ь		100110Б		)10101Ь ∭	100110Ь		100110Ь	
AH	DO									
AL	D1									
BH	D2									
BL	D3									
CH	D4									
CL	D5									
						1				
		1								
Prefill complete,	Waiting fo	or trigger	Acquisition: 10.4K, Sample	s: 264K D1 Freq:	19,990Hz	D3 Period: 50	Dus	nterval T->C: 500ns	D1 Transition	is A->B: 0

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### Exercise 7: PWM

#### **PWM** with coherent update

The exercise above uses 2 interrupts to set-up the t<sub>on</sub> and t<sub>off</sub> values of the low and high side. This system setup might be critical when a interrupt is delayed by more than half a period and the interrupt routine set the new values in the deadtime period. Then only one side will be set to a new value and this might cause a short.

Therefor in systems with heavy interrupt load another configuration is needed. Instead of using shadow registers which are not available within the LTC a second set of LTCs can be set-up and the reset timer switches by HW from on set to the other. This is called coherent update (CUD). The exercise solutions contains a project pwm\_cud which implements such a solution. This solution uses twice as much LTCs for each PWM, so that for a complementary 3-phase PWM 26 cells are used instead of 15.





	Cell	SOL	SOH	Output Control Mode	Port
Reset Timer	LTC0		-	Toggle select line (SL) by HW on reset, Interrupt on reset to	-
				set-up t <sub>on,H</sub> ,t <sub>off,H</sub> ,t <sub>on,L</sub> ,t <sub>on,L</sub>	
Compare Period	LTC1	1	1	-	-
Compare High Side On	LTC2	1	0	Set output by a local event	-
Compare High Side Off	LTC3	1	0	Reset output by a local event or copy the previous cell action	-
Compare High Side On	LTC4	0	1	Set output by a local event or copy the previous cell action	-
Compare High Side Off	LTC5	0	1	Reset output by a local event or copy the previous cell action	P2.8
Compare Low Side Off	LTC6	1	0	Reset output by a local event	-
Compare Low Side On	LTC7	1	0	Set output by a local event or copy the previous cell action	-
Compare Low Side Off	LTC4	0	1	Reset output by a local event or copy the previous cell action	-
Compare Low Side On	LTC5	0	1	Set output by a local event or copy the previous cell action	P3.0