

LOGIC

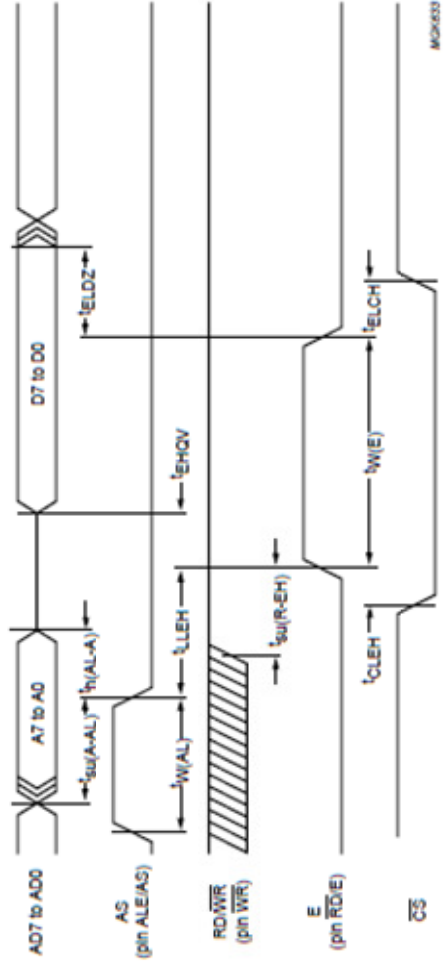
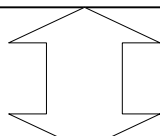
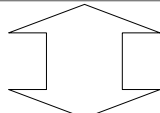


Fig.18 Read cycle timing diagram; Motorola mode.

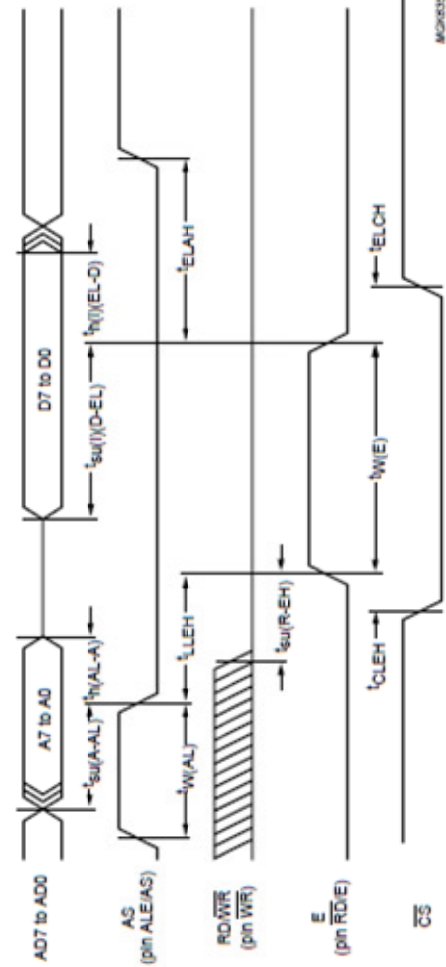


Fig.20 Write cycle timing diagram; Motorola mode.