Enabling Visual Communication

LEADIS®

LDS517

Data Sheet

128 Column X 128 Row 262k-Color / 56 Icons

OLED Controller & Driver

Jun. 01 2005 PRELIMINARY Ver1.2

Contents

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REVISION HISTORY

Date	Page	Contents	Version
Dec. 20 2004	3	Changed : VCC → VDC / VDR	Ver 0.1
	4	Inserted : VROW Generator Block in the Block Diagram	
	5	Changed : VCC → VDC, VDR pin description	
	14	Changed : VCC → VDR in display size	
	18	Inserted : VDR pin	
	21	Inserted : VROW power selection (3Ah) set command list	
	30, 41	Changed : VCC → VDR	
	46	Inserted : VROW power selection (3Ah) set command description	
	75	Changed : VCC → VDR	
	76, 77	Changed : VCC → VDC, VDR	
Dec. 27 2004		Revision : MPU/RGB interface data-bus (D[17:0]/VD[17:0]) format MPU interface - 9-bit interface mode : D[17:9] → D[8:0] - 8-bit interface mode : D[17:10] → D[7:0] - 6-bit interface mode : D[17:12] → D[5:0] RGB interface - 6-bit interface mode : VD[17:12] → VD[17:12] or VD[5:0] selectable mode	Ver 1.0
	5	Changed : MPU/RGB interface pins functions	
	6	Changed : MPU interface mode setting table	
	8, 9	Changed : MPU interface data format and DDRAM data write figures	
	19	Changed : Data Write command (DATARW :0Ch) list	
	20	Changed : Data Read command (DATARW : 0Ch) list	
	20	Changed : Register Read command (READREG :0Dh) list	
	22	Inserted : RB parameter in the RGB interface mode command (RGBIF : 2Fh) list - RB parameter select RGB 6-bit interface data bus VD[17:12] or VD[5:0]	
	30	Changed : 1 Pixel (RGB) display data format	
	33	Changed : Data Write command (DATARW :0Ch) description	
	34	Changed : Data Read command (DATARW : 0Ch) description	
	35	Changed : Register Read command (READREG : 0Dh) description	
	43, 44	Inserted : RB parameter in the RGB interface mode command (RGBIF : 2Fh) description - RB parameter select RGB 6-bit interface data bus VD[17:12] or VD[5:0]	

Dec. 27 2004	64-69	Changed : RGB interface data bus format - VD17-12 → VD5-0 or VD17-12	Ver 1.0
	68	Changed : RGB interface data bus format - VD11-0 → VD17-6 or VD11-0	
	68	Inserted : RGB interface data bus format - VD5/VD4/VD3/VD2/VD1/VD0	
	83	Inserted : RGB Interface Timing	
	85	Changed : MPU 6-bit interface data format - D17-12 → D5-0 - D11-0 → D17-6	
	86	Changed : MPU 8-bit interface data format - D17-10 → D7-0 - D9-0 → D17-8	
	87	Changed : MPU 9-bit interface data format - D17-9 → D8-0 - D10-0 → D17-9	
Dec. 28 2004	77	Changed FOSC1 (Oscillator Frequency for Dot Matrix) MIN/TYP/MAX value - 1.8/2.0/2.2 → 2.7/3.0/3.3 MHz	Ver 1.1
Apr. 19 2005		Revision : MPU interface data-bus (D[17:0]) format - 16-bit interface mode : D[17:13], D[11:1] → D[15:0] ICON Status register - ICON status in the ICON Initialize command (ICONINIT : 24h) : S[6:0] → S[5:0]	Ver 1.2
	6	Changed MPU interface Pins - 16-bit interface : D[17:13], D[11:1] → D[15:0]	
	7	Changed MPU 16-bit interface data format - D[17:13], D[11:1] → D[15:0]	
	10	Changed : MPU interface 16-bit data bus format and DDRAM data write figures	
	17	Changed : ICON Function - ICON status memory and register : 7-bit → 6-bit - ICON status range : 0~127 → 0-63	
	20	Changed : Data Write command (DATARW :0Ch) list about 16-bit data bus format	
	31	Changed : MPU Interface command (IFMODE :08h) description about 16-bit data bus format	
	34	Changed : Data Write command (DATARW :0Ch) description about 16-bit data bus format	
	60	Changed : ICON output current table in the ICON Initialize command (ICONINIT : 24h) - S[6:0] : 0 ~ 127 → S[5:0] : 0 ~ 63	
	62	Changed : ICON_ROW_HIGH_PERIOD (28h) - 0/64,…,7/64 → 0/56,..,7/56	
	88	Changed : MPU 16-bit interface data format - Open : D12, D0 → D17, D16 - D17-D13, D11-D1 → D15-D0	
Jun. 01 2005	9	Changed : MPU Interface mode setting - PS : 0 → 1, 1 →0	

DESCRIPTION

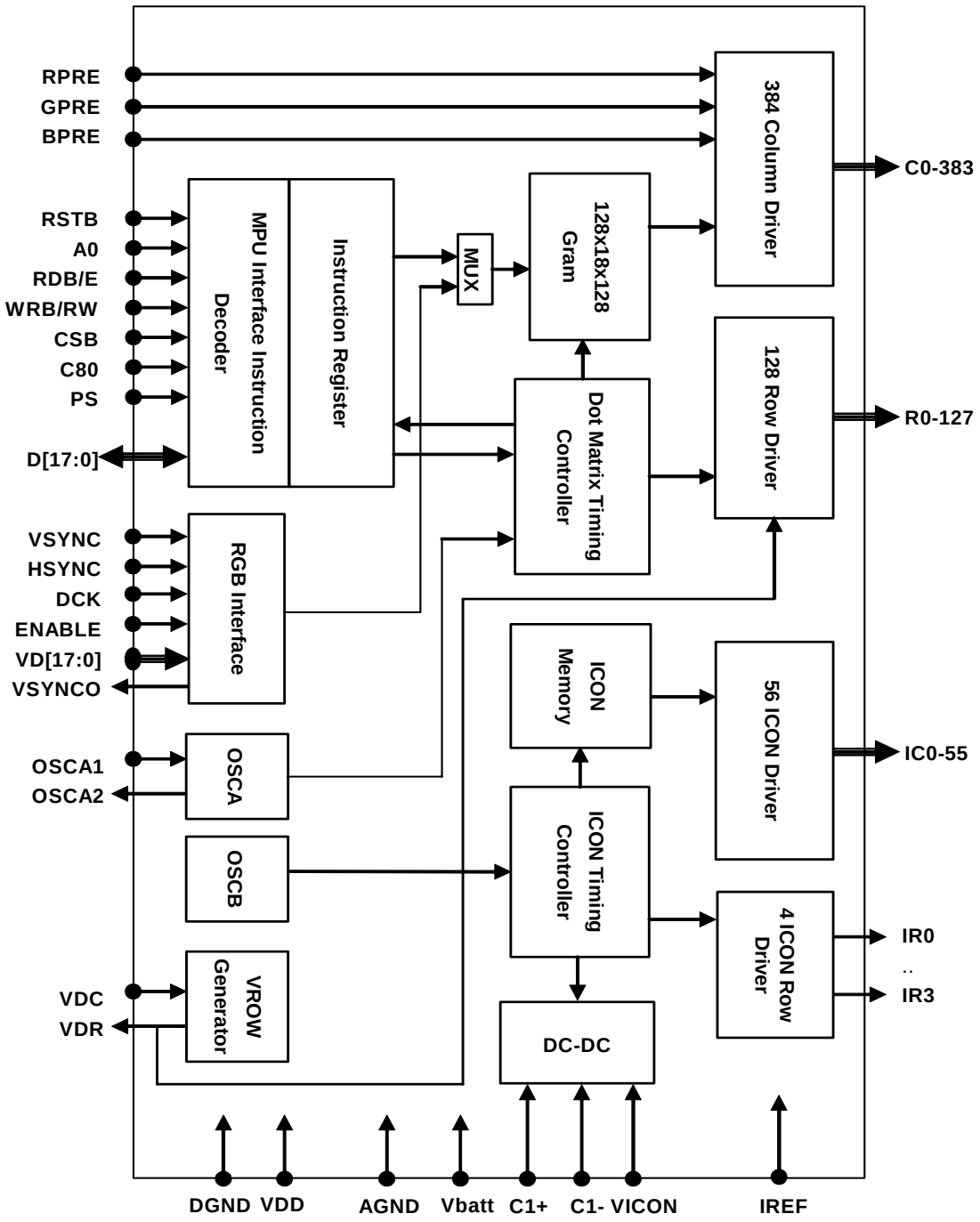
LDS517 is a 384–column(128xRGB) and 128-row dot driver & 56-column and 4-row icons driver & controller with RAM for the 262k-Color OLED panel.

As a MPU interface with a microcomputer, the LDS517 has 80/68-system MPU interfaces with 8/9/16/18-bit bus and Serial interface, which enable efficient data transmission with the microcomputer. The LDS517 also incorporates an External Display Interface, RGB interface and VSYNC interface (VSYNC, HSYNC, DCK, ENABLE, VD17-0 and VSYNCO), for displaying moving picture.

FEATURES

- Outputs:
  Dot Driver : 384 (128 x RGB) columns and 128 rows
  Icon Driver : 56 columns and 4 rows
- Internal Display Data RAM: 128 x 18-bit x 128 = 294,912 bits
- MPU Interface
  Serial interface
  Parallel interface for 80/68 series (6-bit/8-bit/9-bit/16-bit/18-bit mode)
  Address A0 (Select instruction and Parameter)
  Always 6-bit command mode (instruction and parameter) in MPU interface
- External Display Interface for displaying moving pictures
  RGB interface mode (6-bit/16-bit/18-bit)
  VSYNC interface mode
- Inner Charge Pump DC-DC for Icons
- Variety of Screen Saver
- Internal Oscillator Circuit A (external R component) for Dot Matrix
  Internal Oscillator Circuit B for Icon
- Adjustable Frame Frequency: 60/75/90/105/120/135/150 [frames/s]
- Operating Voltage
  - VDD = 1.65 ~ 3.3V (TYP=1.8/2.8V)
  - VDC/VDR = 10.0 ~ 21.0V
  - VBATT = 3.2 ~ 4.2V
  - VICON = 3.2 ~ 21.0V
- Package: Bumped chip

BLOCK DIAGRAM



CHIP PIN DESCRIPTION

Power Supply Pins

Name	Quantity	Pad No.	TYPE	Function
VDC	TBD	TBD	Power	OELD Dot Matrix Power Supply for Column Driver
VDR	TBD	TBD		OELD Dot Matrix Power Supply for Row Driver
VDD	TBD	TBD		Logic Power Supply
Vbatt	TBD	TBD		DC-DC Input Power Supply for ICON
AGND	TBD	TBD		Analog (Driver) GND
DGND	TBD	TBD		Digital Logic GND
C1+	1	TBD	Power	Capacitor for Charge Pump DC-DC, between C1+ and C1-, connect Capacitor.
C1-	1	TBD		
VICON	1	TBD		Capacitor for Charge Pump DC-DC, between VICON and AGND connect Capacitor. Directory imputable power supply for ICON to use this pin.

System Control Pins

Name	Quantity	Pad No.	TYPE	Function
OSCA1	1	TBD	I	Oscillator for Dot Matrix
OSCA2	1	TBD	O	
RPRE	1	TBD	I/O	Pre-Charge Voltage for Red
GPRE	1	TBD	I/O	Pre-Charge Voltage for Green
BPRE	1	TBD	I/O	Pre-Charge Voltage for Blue
IREF	1	TBD	O	Current Setting. Typ Resistance = TBD kΩ （Current adjustable range ±30%）
C80	1	TBD	I	H : 68-series CPU, L : 80-series CPU
PS	1	TBD	I	H : Parallel interface, L : Serial interface

MPU Interface Pins

Name	Quantity	Pad No.	TYPE	Function
CSB	1	TBD	I	Chip Select (Active Low)
RDB/E	1	TBD	I	80-Interface : Read (Active Low) 68-Interface : Enable (Falling Edge)
WRB/RW	1	TBD	I	80-Interface : Write (Active Low) 68-Interface : Read (High), Write (Low)
RSTB	1	TBD	I	Reset (Active Low)
A0	1	TBD	I	Address A0 (L : instruction, H : Parameter)
D[17:2]	16	TBD	I/O	MPU Data Bus 6-bit interface : D[5:0], 8-bit interface : D[7:0], 9-bit interface : D[8:0] 16-bit interface : D[15:0] 18-bit interface : D[17:0] Instructions & Parameters 6-bit : D[5:0]
D[1]	1	TBD	I/O	MPU Data [1] or Serial Data
D[0]	1	TBD	I/O	MPU Data [0] or Serial Clock

RGB Interface Pins

Name	Quantity	Pad No.	TYPE	Function	
VSYNC	1	TBD	I	RGB interface vertical sync input pin (Active Low).	The polarity of these signals is inverted by register setting (PV, PH, PC, PE, PO).
HSYNC	1	TBD	I	RGB interface horizontal sync input pin (Active Low).	
DCK	1	TBD	I	RGB interface Dot clock input pin (Rising Edge).	
ENABLE	1	TBD	I	RGB interface VD[17:0] data enable input pin (Active Low).	
VSYNCO	1	TBD	O	RGB interface vertical sync output pin (Active High).	
VD[17:0]	18	TBD	I	RGB interface data bus 6-bit interface : VD[5:0] or VD[17:12], 16-bit interface : VD[17:13], VD[11:1] 18-bit interface : VD[17:0]	

OLED Driver Pins

Name	Quantity	Pad No.	TYPE	Function
R0 to R127	128	TBD	O	OELD Dot Matrix Row Output
C0 to C383	384	TBD	O	OELD Dot Matrix Column Output
IR0 to IR3	4	TBD	O	OELD ICON Row Output
IC0 to IC55	56	TBD	O	OELD ICON Column Output

NOTICE: DUMMY– These pins should be open (float).

Functional description

MPU INTERFACE

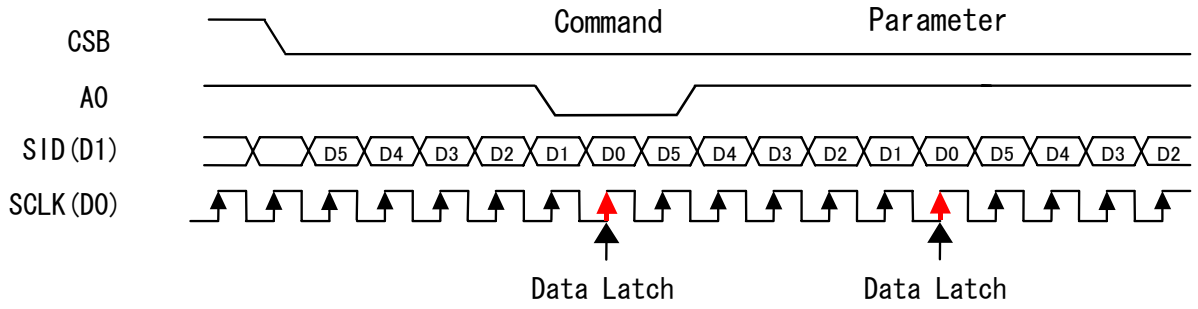
The LDS517 has 2 MPU interface modes : Parallel Interface (80/68-series mode with 18, 16, 9, 8 and 6-bit bus) and Serial Interface and selects the MPU interface mode by setting PS pin and IFMODE[2:0] register, it is set by “MPU_Interface_Mode Command”.

MPU interface mode setting

PS	C80	IFMODE[2:0]			MPU Interface		Instructions & Parameters (6-bit)		DDRAM Write Data		
		2	1	0			Data Bus Pins	Transfer times	Data Bus Pins	Transfer times	Setting Colors
1	0	0	0	0	80-series	6-bit	D[5:0]	1	D[5:0] + D[5:0] + D[5:0]	3	262,144
1	0	0	0	1		8-bit	D[5:0]	1	D[7:0] + D[7:0]	2	65,536
1	0	0	1	0		9-bit	D[5:0]	1	D[8:0] + D[8:0]	2	262,144
1	0	0	1	1		16-bit	D[5:0]	1	D[15:0]	1	65,536
1	0	1	0	0		18-bit	D[5:0]	1	D[17:0]	1	262,144
1	1	0	0	0	68-series	6-bit	D[5:0]	1	D[5:0] + D[5:0] + D[5:0]	3	262,144
1	1	0	0	1		8-bit	D[5:0]	1	D[7:0] + D[7:0]	2	65,536
1	1	0	1	0		9-bit	D[5:0]	1	D[8:0] + D[8:0]	2	262,144
1	1	0	1	1		16-bit	D[5:0]	1	D[15:0]	1	65,536
1	1	1	0	0		18-bit	D[5:0]	1	D[17:0]	1	262,144
0	-	0	0	0	Serial interface 6-bit		D[1]	6	D[1]	6 x 3	262,144

SERIAL INTERFACE

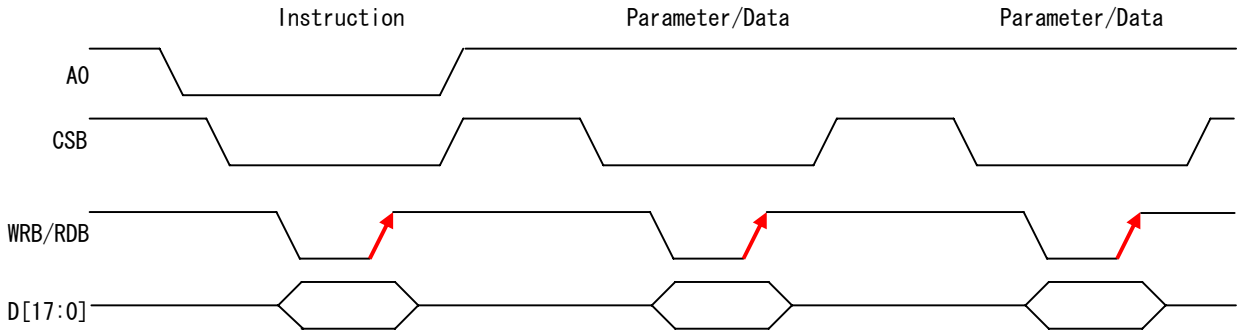
Function	CSB	Clock	A0	Data
Write Instruction	L	D0	L	D1
Write Parameter	L	D0	H	D1



PARALLEL INTERFACE

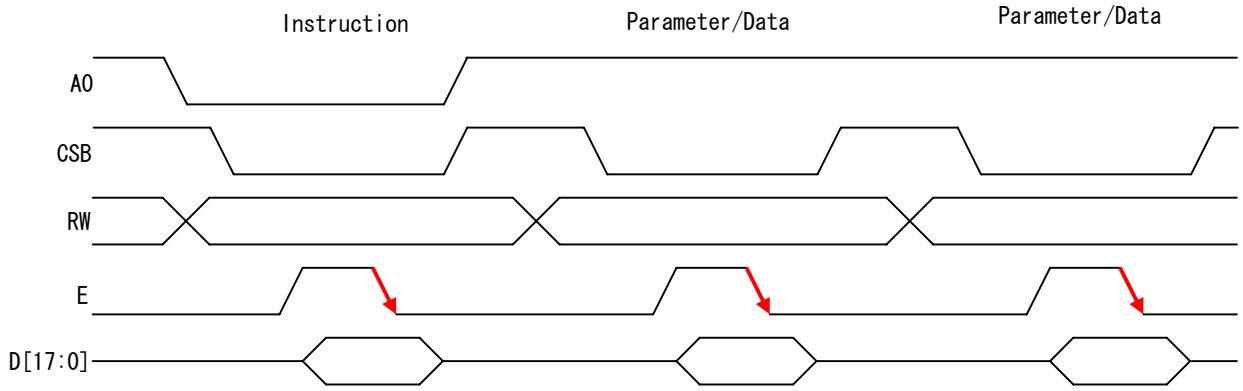
80-SERIES MPU

Function	CSB	WRB	RDB	A0	D[17:0]
Write Instruction	L	↑	H	L	Instruction D[5:0]
Write Parameter or Data	L	↑	H	H	Parameter D[5:0] or Data [17:0]
Read Parameter or Data	L	H	↑	H	

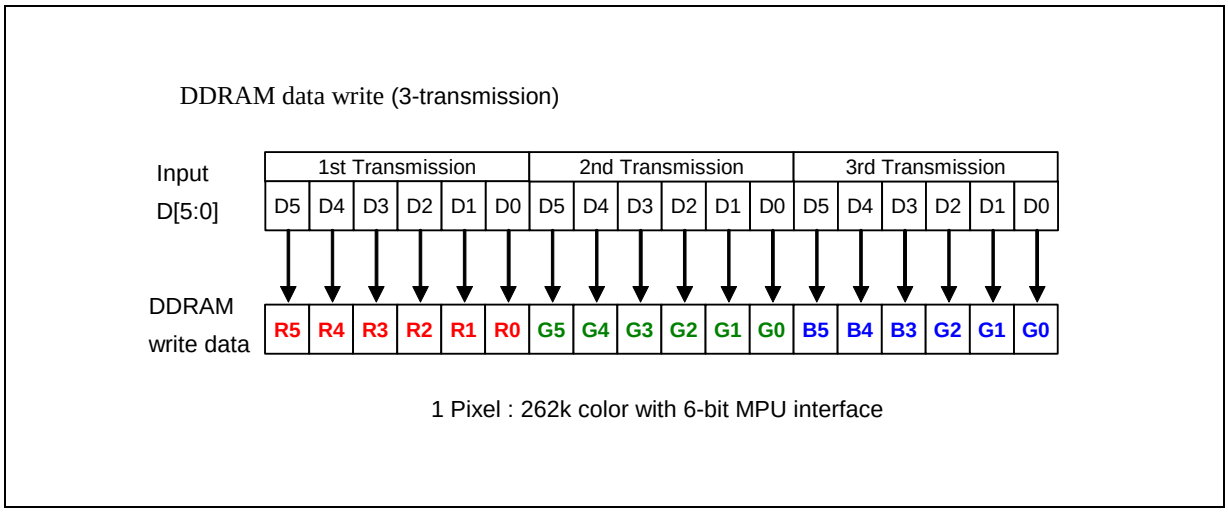


68-SERIES MPU

Function	CSB	RW	E	A0	D[17:0]
Write Instruction	L	L	↓	L	Instruction D[5:0]
Write Parameter or Data	L	L	↓	H	Parameter D[5:0] or Data [17:0]
Read Parameter or Data	L	H	↓	H	

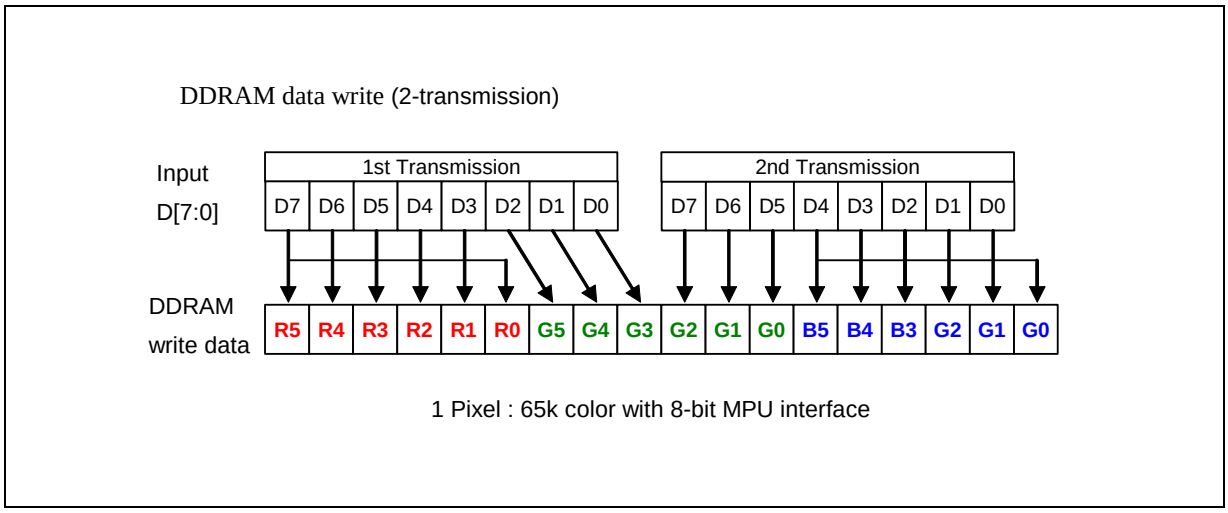


80/68-Series MPU, 6-bit interface (IFMODE[2:0] = " 000")



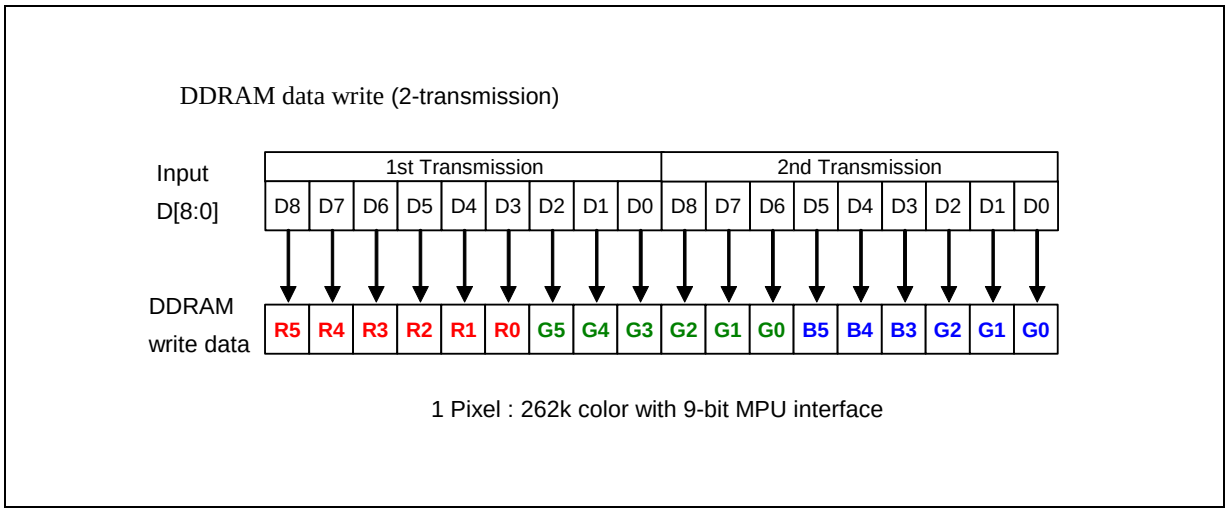
8-bit MPU interface data format, DDRAM data write (3-transmission mode)

80/68-Series MPU, 8-bit interface (IFMODE[2:0] = " 001")



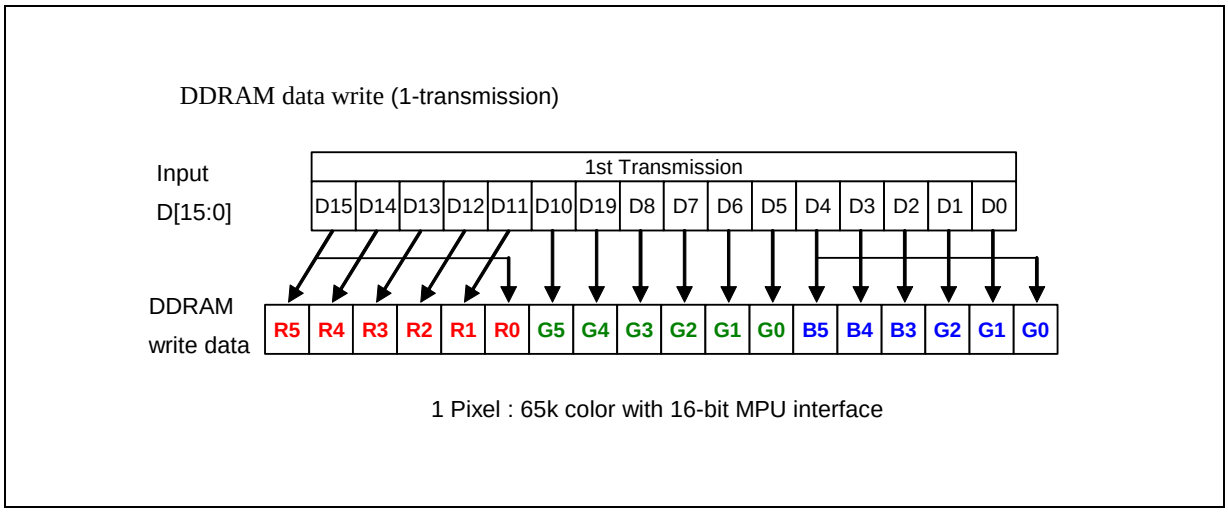
8-bit MPU interface data format, DDRAM data write (2-transmission mode)

80/68-Series MPU, 9-bit interface (IFMODE[2:0] = " 010")



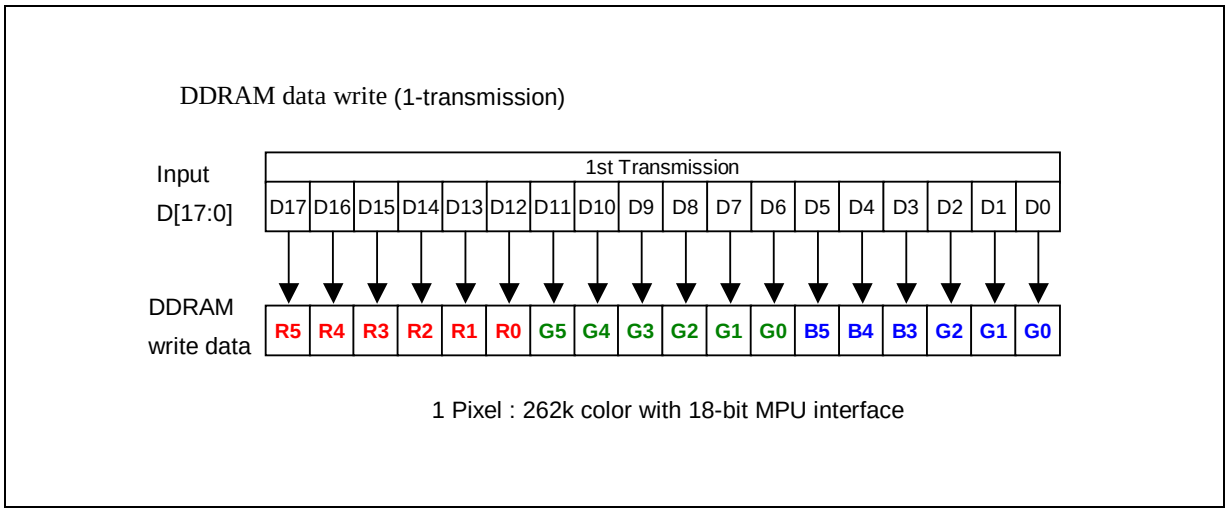
9-bit MPU interface data format, DDRAM data write (2-transmission mode)

80/68-Series MPU, 16-bit interface (IFMODE[2:0] = " 011")



16-bit MPU interface data format, DDRAM data write (1-transmission mode)

80/68-Series MPU, 18-bit interface (IFMODE[2:0] = " 100")



18-bit MPU interface data format, DDRAM data write (1-transmission mode)

EXTERNAL DISPLAY INTERFACE

LDS517 has a MPU interface to make an instruction setting and an external display interface to display a moving picture. The LDS517 selects an optimum interface according to the kind of display (moving or still picture, or both) to transmit data efficiently.

As an external display interface, the LDS517 has an RGB interface and a VSYNC interface, which update screens without flicker.

In the RGB interface, display operations are executed in synchronization with VSYNC, HSYNC, and DCK. Display data are written according to the values of data enable signal (ENABLE), and display data in VD17-0 in synchronization with VSYNC, HSYNC, and DCK. By writing display data to DDRAM, data transmission is minimized to only when screen switching is required. The use of window addressed enables to overwrite only the RAM area for a moving picture display, and therefore makes it possible to display a moving picture and the pre-written RAM data in the area other than moving picture areas simultaneously.

In VSYNC interface mode, the frame synchronization signal (VSYNC) synchronizes internal display operations. The VSYNC interface enables a moving picture display while using a MPU interface by writing data to DDRAM through a MPU interface at a fixed speed in synchronization with the falling edge of VSYNC. In this case, there are constraints in the speed and method to write data to RAM.

For details, see the “External Display Interface” section.

The LDS517 handles the following operating modes according to the type of display.

Operation Mode	RAM Access Setting (RA)	Display Operation Mode(DM[1:0])
Internal operating clock only (Displaying still picture)	MPU Interface (RA = 0)	Internal operating clock (DM[1:0] = “00”)
RGB Interface (1) (Display moving picture)	RGB Interface (RA = 1)	RGB Interface (DM[1:0] = “01”)
RGB Interface (2) (Rewriting still picture while displaying moving pictures)	MPU Interface (RA = 0)	RGB Interface (DM[1:0] = “00”)
VSYNC Interface (Displaying moving pictures)	MPU Interface (RA = 0)	VSYNC Interface (DM[1:0] = “10”)

Note 1) Instruction settings are made only through a MPU interface.

Note 2) The RGB Interface and the VSYNC Interface are not used simultaneously.

Note 3) Do not make changes to the setting of RGB Interface Mode (RM[1:0]) while the RGB Interface is in operation

Note 4) When switching between different operating modes, see the transitional flowcharts in the “External Display Interface” section.

LDS517 has a VSYNCO output pin for external display interface. VSYNCO is high-level output during 128th line in the internal operating clock mode and VSYNC Interface mode of LDS517. It’s polarity is active high, default mode, is controlled by “RGB_Signal_Polarity (RGBPOL)” command’s PO parameter.

VSYNCO output signal is useful for frame sync control and RAM data writing between MPU Interface mode and RGB interface or VSYNC Interface mode.

DOT DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the display. It is composed of 128-row by 128-column x 18-bit addressable array. Address counter provides row and column address to DDRAM for access display pixel data from MPU. It is set by "Data_Write command" to the predetermined start address (Data_R/W_Box_Size and Display_Direction Command). And it is increased or decreased by one, after "Data_Write parameter" operations. After both the column and row address counter are reached at the predetermined column and row end address, the counter is not counting any more and the " Data_Write parameter " operation is not valid until " Data_Write command " is being issued.

Display Data RAM Map

C0 to C383	C0						C1						C2						C3						C4						C5						---	C381						C382						C383					
COLUMN	0																		1																		---	127																	
ROW(RGB)	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	---	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
ROW(BGR)	B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0	B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0	---	B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0
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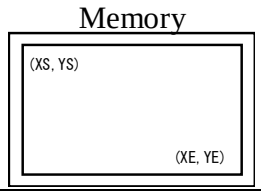
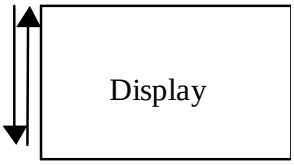
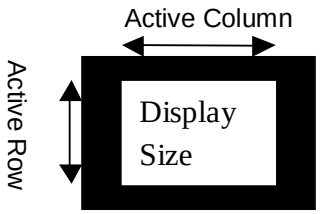
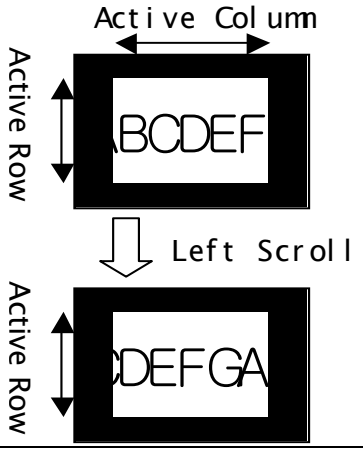
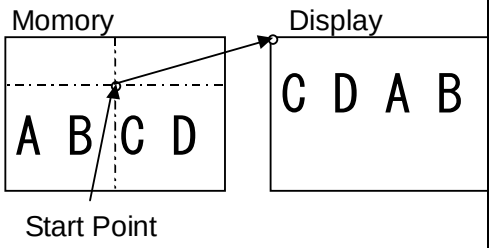
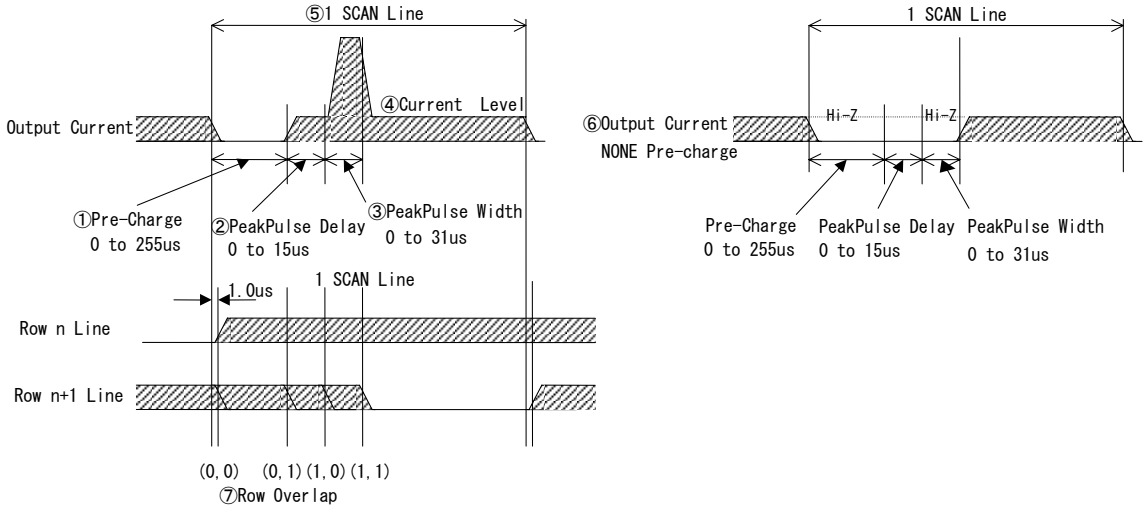
When “Data_Write_Control command”(WRITEDIR : 05h)’s 1st parameter D3 bit is control the RGB-BGR order.

- “0” = Row(RGB)
- “1” = Row(BGR)

Correspondence Memory and Display

Memory Data Write	"Data_R/W_Box_Set command" indicate memory writing area. "Data_Writing_Control command" indicate writing direction(auto address increment or decrement)	
Display Direction	"Display_Direction command" indicate display direction.	
Display Size	"Display_Size command" indicate active outputs. The column outputs out of active area always Hi-z. The row outputs out of active area always VDR excluding display off. Scan is repeated within active area. Frame frequency is set for maximum display area. Rows out of active row are VDR.	
Scroll Area	In scroll mode, display all memory area regardless display size.	
Memory Reading Start Address	"Memory_Read_Start_Address command" fix the relation of memory and display coordinates.	

Dot Matrix Output Wave Form



□ Related Command

① Pre-Charge_Width(PRCWIDTH), Pre-Charge_Mode(PRCSELECT)
② Peak_Pulse_Delay(PEAKDELAY)
③ Pre-Charge_Width(PRCWIDTH), Pre-Charge_Mode(PRCSELECT)
④ Dot_Current(DOTCURRENT)
⑤ Dot_Matrix_Frame_Frequency(DFRAME)
⑥ Pre-Charge_Mode(PRCSELECT)
⑦ Row_Overlap_Scan(ROWSCAN)

Pre-charge

When Pre-Charge, each column output is connected the each color pre-charge pin in the IC. Therefore all dot matrix column outputs have the switch between driver and pre-charge pin.

External pre-charge pins are tied with “Zener Diode”.

External pre-charge pins have outer circuit for every colors.

Dot Matrix Power Save

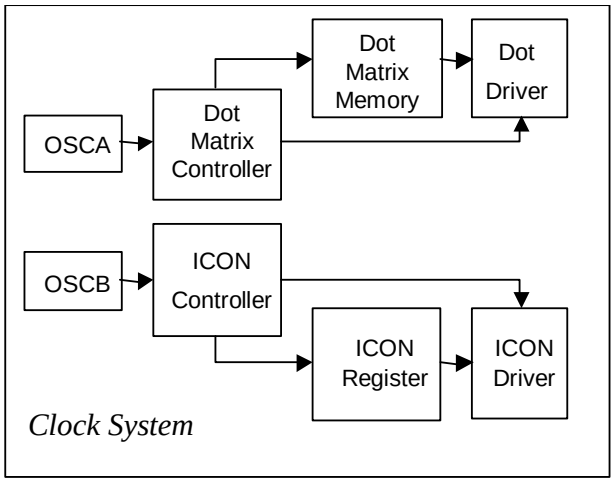
Function	Display ON/OFF	Stand-by	Soft Reset
Command	Dot_Matrix_Display_On/Off (DDISPONOFF : 02h)	Dot_Matrix_Stand-By_On/Off (DSTBYONOFF : 03h)	Software_Reset (SWRESET : 01h)
Execute	Display ON/Off	Display ON/OFF OSC Start/Stop	Register Clear Display OFF Stand-by ON

Reset

When RSTB Input becomes 'L', all Register is set Default.
When Software_Reset (SWRESET) command is inputted, all Register is set Default.

Oscillator

Oscillators are separated between Dot Matrix and ICONs.



LDS517 has On-chip oscillator A with external resistor for dot matrix, The frequency is controlled by external resistor value between OSC1 and OSC2. This oscillator signal is used for system clock generation. Frame frequency is adjusted by "Dot_Matrix_Frame_Frequency(DFRAME)" command.
And On-chip oscillator B for ICON with internal resistor.

In stand-by mode, oscillators are stopped.

ICON Function

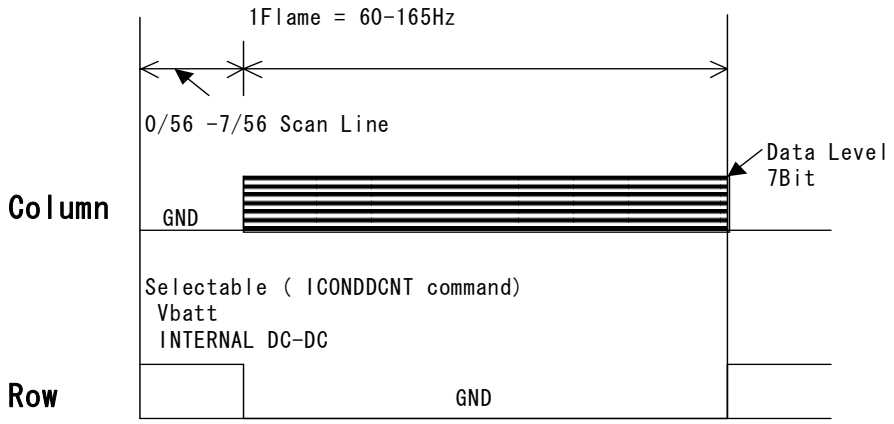
STATUS/DATA REGISTER MAP

Status Memory = 56 x 6 Bit
Data Memory = 56 x 1 Bit

IC0 to IC55	Status Reg						Data Reg
	S5	S4	S3	S2	S1	S0	D0
0	0-63						ON/OFF
1							
2							
:							
55							

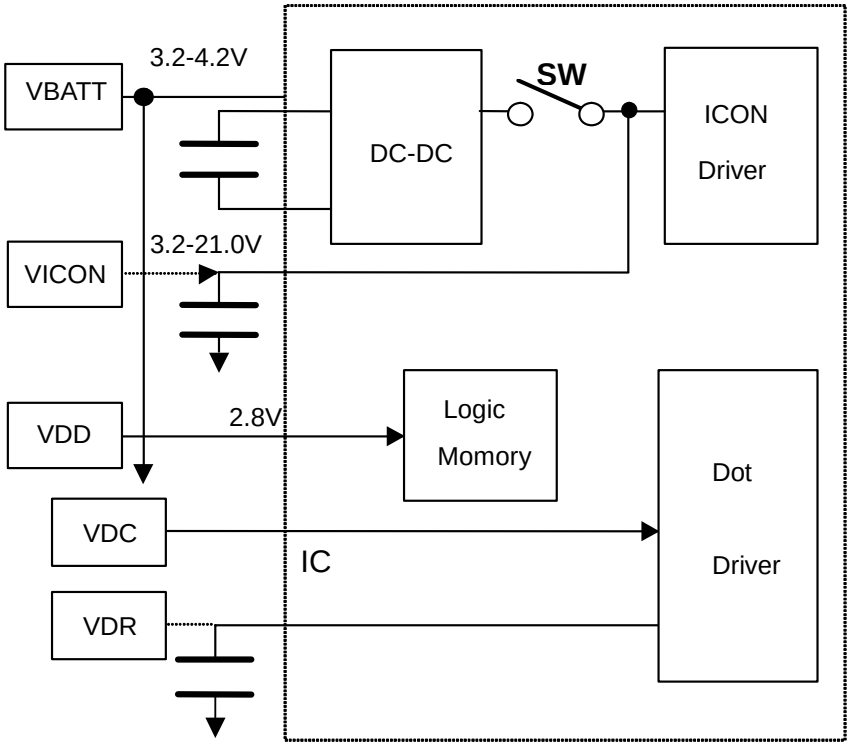
Icon_Initialize(ICONINIT) command is used for Status Resistor setting.
Icon_Data_Write(IDATAWR) command is used for Data Resistor setting.

ICON DRIVE WAVEFORM



When ICON display off (Icon_Display_On/Off command : instruction -20h, parameter-00h), ICON Columns and Rows are GND level.

POWER SUPPLY AND DC-DC



MODE	SW	DC-DC	ICON Power
01b	OFF(Default)	STOP	VICON
10b	ON	ON	VBATTX2

Voltage supply for ICON Drivers is selected from internal DC-DC or external power supply through VICON.

ICON POWER SAVE

Command	Icon_Display_On/Off (IDSPONOFF)	Icon_Stand-By_On/Ofl (ISTBYONOFF)	Software_Reset (SWRESET)
Function	ALL ICON ON/OFF Normal Display	OSCB start/stop Internal DC-DC Start/Stop ALL ICON OFF	SOFT Reset Register Clear

Instruction Table

Main command

"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
Software_Reset											
SWRESET	W	L	-	01h						Display Off	-
Dot_Matrix_Display_On/Off											
DDISPONOFF	W	L	-	02h						Dot Matrix Display ON/OFF	-
1st parameter	W	H	-	**0**	**0**	**0**	**0**	**0**	D0	D0=0:Display Off, D0=1:Display On	00h
Dot_Matrix_Stand-By_On/Off											
DSTBYONOFF	W	L	-	03h						Dot Matrix Stand-By ON/OFF	-
1st parameter	W	H	-	**0**	**0**	**0**	**0**	**0**	D0	D0=0:OSCA start, D0=1:Run DDISPOFF,OSCA stop	01h
Dot_Matrix_Frame_Frequency											
DFRAME	W	L	-	04h						Dot Matrix Frame frequency set	-
1st parameter	W	H	-	-	-	-	F2	F1	F0	60 ~ 150 Hz	02h
Data_Write_Control											
WRITEDIR	W	L	-	05h						Data Write Control	-
1st parameter	W	H	-	-	-	D3	D2	D1	D0	D2=0;Horizontal, D2=1:Vertical	00h
Display_Direction											
DISPDIR	W	L	-	06h						Display Direction Control	-
1st parameter	W	H	-	-	-	-	-	DV	**0**	Display direction	00h
Display_Size											
DISPSIZE	W	L	-	07h						Display Size Set	-
1st parameter	W	H	-	-	-	-	FX6	FX5	FX4	Display Size X From	00h
2nd parameter	W	H	-	-	-	FX3	FX2	FX1	FX0		00h
3rd parameter	W	H	-	-	-	-	TX6	TX5	TX4	Display Size X to	07h
4th parameter	W	H	-	-	-	TX3	TX2	TX1	TX0		0Fh
5th parameter	W	H	-	-	-	-	FY6	FY5	FY4	Display Size Y From	00h
6th parameter	W	H	-	-	-	FY3	FY2	FY1	FY0		00h
7th parameter	W	H	-	-	-	-	TY6	TY5	TY4	Display Size Y to	07h
8th parameter	W	H	-	-	-	TY3	TY2	TY1	TY0		0Fh
MPU_Interface_Mode											
IFMODE	W	L	-	08h						6/9/18 Bit Interface Select	-
1st parameter	W	H	-	-	-	-	D2	D1	D0	"000" : 6-bit, "001" : 8-bit "010" : 9-bit "011" : 16-bit "100" : 18-bit	00h
Data_Reverse_Color_Masking											
DATAMASK	W	L	-	09h						Data Reverse & Color Masking	-
1st parameter	W	H	-	-	RV	-	R	G	B	RV=0:Origin, RV=1:Reverse	07h

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
Data_R/W_Box_Size											
RWBOXSIZE	W	L	-	0Ah						R/W Box Set	-
1st parameter	W	H	-	-	-	-	XS6	XS5	XS4	R/W Box Column Start Address	00h
2nd parameter	W	H	-	-	-	XS3	XS2	XS1	XS0		00h
3rd parameter	W	H	-	-	-	-	XE6	XE5	XE4	R/W Box Column End Address	07h
4th parameter	W	H	-	-	-	XE3	XE2	XE1	XE0		0Fh
5th parameter	W	H	-	-	-	-	YS6	YS5	YS4	R/W Box Row Start Address	00h
6th parameter	W	H	-	-	-	YS3	YS2	YS1	YS0		00h
7th parameter	W	H	-	-	-	-	YE6	YE5	YE4	R/W Box Row End Address	07h
8th parameter	W	H	-	-	-	YE3	YE2	YE1	YE0		0Fh
Memory_Read_Start_Address											
DISPSTART	W	L	-	0Bh						Memory Read Start Set	-
1st parameter	W	H	-	-	-	-	XS6	XS5	XS4	Memory Read Column Start Address	00h
2nd parameter	W	H	-	-	-	XS3	XS2	XS1	XS0		00h
3rd parameter	W	H	-	-	-	-	YS6	YS5	YS4	Memory Read Row Start Address	00h
4th parameter	W	H	-	-	-	YS3	YS2	YS1	YS0		00h
Data_Write											
DATARW	W	L	-			0Ch				Dot Matrix Data Write	
18-bit Mode (262k color)	W	H	R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0			B5	B4	B3	B2	B1	B0	1st Data	
	:	:	: : : : : : : : : : : :			:	:	:	:	:	:		
	W	H	R5 R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0			B5	B4	B3	B2	B1	B0	Nth Data	
16-bit Mode (65k color)	W	H	- R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0			B4	B3	B2	B1	B0		1st Data	
	:	:	: : : : : : : : : : : :			:	:	:	:	:	:		
	W	H	- R4 R3 R2 R1 R0 G5 G4 G3 G2 G1 G0			B4	B3	B2	B1	B0		Nth Data	
9-bit Mode (262k color)	W	H	-	R5	R4	R3	R2	R1	R0	G5	G4	G3	1st Data
	W	H	-	G2	G1	G0	B5	B4	B3	B2	B1	B0	
	:	:	:	:	:	:	:	:	:	:	:	:	
	W	H	-	R5	R4	R3	R2	R1	R0	G5	G4	G3	Nth Data
	W	H	-	G2	G1	G0	B5	B4	B3	B2	B1	B0	
8-bit Mode (65k color)	W	H	-		R4	R3	R2	R1	R0	G5	G4	G3	1st Data
	W	H	-		G2	G1	G0	B4	B3	B2	B1	B0	
	:	:	:		:	:	:	:	:	:	:	:	
	W	H	-		R4	R3	R2	R1	R0	G5	G4	G3	Nth Data
	W	H	-		G2	G1	G0	B4	B3	B2	B1	B0	
6-bit Mode (262k color)	W	H	-			R5	R4	R3	R2	R1	R0	1st Data	
	W	H	-			G5	G4	G3	G2	G1	G0		
	W	H	-			B5	B4	B3	B2	B1	B0		
	:	:	:			:	:	:	:	:	:		
	W	H	-			R5	R4	R3	R2	R1	R0	Nth Data	
	W	H	-			G5	G4	G3	G2	G1	G0		
	W	H	-			B5	B4	B3	B2	B1	B0		

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
Data_Read											
DATARW	W	L	-			0Ch				Dot Matrix Data Read	
18-bit Mode	R	H	X X X X X X X X X X	X	X	X	X	X	X	Dummy Data	
	R	H	R5 R4 R3 R2 R1 R0 G5 G4 G3	G2	G1	G0	B5	B4	B3	1st Data	
	:	:	: : : : : : : : : :	:	:	:	:	:	:		
	R	H	R5 R4 R3 R2 R1 R0 G5 G4 G3	G2	G1	G0	B5	B4	B3	Nth Data	
9-bit Mode	R	H	-	X	X	X	X	X	X	Dummy Data	
	R	H	-	R5	R4	R3	R2	R1	R0	1st Data	
	R	H	-	G2	G1	G0	B5	B4	B3		
	:	:	:	:	:	:	:	:	:		
	R	H	-	R5	R4	R3	R2	R1	R0	Nth Data	
	R	H	-	G2	G1	G0	B5	B4	B3		
6-bit Mode	R	H	-			X	X	X	X	Dummy Data	
	R	H	-			R5	R4	R3	R2	1st Data	
	R	H				G5	G4	G3	G2		
	R	H	-			B5	B4	B3	B2		
	:	:	:			:	:	:	:		
	R	H	-			R5	R4	R3	R2	Nth Data	
	R	H				G5	G4	G3	G2		
	R	H	-			B5	B4	B3	B2		
Register_Read											
REGREAD	W	L	-			0Dh				Register Read	
1st parameter	R	H	-			D5	D4	D3	D2	1st parameter	
:	:	:	-			:	:	:	:		
Nth parameter	R	H	-			D5	D4	D3	D2	Nth parameter	
Dot_Current											
DOTCURRENT	W	L	-			0Eh				Dot Current Set	
1st parameter	W	H	-	-	-	IR7	IR6	IR5	IR4	Red Level = 0 ~ 255uA	00h
2nd parameter	W	H	-	-	-	IR3	IR2	IR1	IR0		00h
3rd parameter	W	H	-	-	-	IG7	IG6	IG5	IG4	Green Level = 0 ~ 255uA	00h
4th parameter	W	H	-	-	-	IG3	IG2	IG1	IG0		00h
5th parameter	W	H	-	-	-	IB7	IB6	IB5	IB4	Blue Level = 0 ~ 255uA	00h
6th parameter	W	H	-	-	-	IB3	IB2	IB1	IB0		00h
Pre-Charge_Mode											
PRCSELECT	W	L	-			1Bh				Pre-Charge Mode Set	
1st parameter	W	H	-	-	-	-	-	D1	D0		01h
Pre-Charge_Pulse_Width											
PRCWIDTH	W	L	-			1Ch				Pre-Charge Width Set	
1st parameter	W	H	-	-	-	T7	T6	T5	T4	Width = 0 ~ 255us	00h
2nd parameter	W	H	-	-	-	T3	T2	T1	T0		08h

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
Peak_Pulse_Width											
PEAKWIDTH	W	L	-	1Dh						Peak Pulse Width Set	
1st parameter	W	H	-	-	W4	W3	W2	W1	W0	Red Width = 0 ~ 31us	05h
2nd parameter	W	H	-	-	W4	W3	W2	W1	W0	Green Width = 0 ~ 31us	05h
3rd parameter	W	H	-	-	W4	W3	W2	W1	W0	Blue Width = 0 ~ 31us	05h
Peak_Pulse_Delay											
PEAKDELAY	W	L	-	1Eh						Peak Pulse Delay Set	
1st parameter	W	H	-	-	-	W3	W2	W1	W0	Delay = 0 ~ 15us	05h
Row_Overlap_Scan											
ROWSCAN	W	L	-	1Fh						Row Scan Set	
1st parameter	W	H	-	D5	D4	D3	-	D1	D0	D[5:4] : Row Overlap Timing Set D[3] : Row Scan Mode Set D[1:0] : Row Scan Sequence Set	00h
RGB_Interface_Mode											
RGBIF	W	L	-	2Dh						RGB Interface Set	
1st parameter	W	H	-	RB	RA	DM1	DM0	RM1	RM0	RGB Interface Mode set	00h
Display_Clock_Condition											
DISPCLK	W	L	-	2Eh						Display Clock condition set	
1st parameter	W	L	-	-	-	-	-	HN7	HN6	Number of pixels during 1H	02h
2nd parameter	W	L	-	HN5	HN4	HN3	HN2	HN1	HN0		08h
3rd parameter	W	H	-	-	-	BP3	BP2	BP1	BP0	Number of lines for Back Porch	0Eh
4th parameter	W	L	-	-	-	FP3	FP2	FP1	FP0	Number of lines for Front Porch	02h
RGB_Signal_Polarity											
RGBPOL	W	L	-	2Fh						RGB Interface Signal Set	
1st parameter	W	H	-	-	PV	PH	PC	PE	PO	RGB Interface Polarity	00h
Row Power Selection Set											
VROWSEL	W	L	-	3Ah						Row Power Level Set	
1st parameter	W	H	-	-	EN	S3	S2	S1	S0		04h

Screen Saver command

SS : Screen Saver ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
Screen_Saver_Sleep_Timer											
SSLPTIM	W	L	-	10h						**SS** Sleep Timer Set	-
1st parameter	W	H	-	-	-	T7	T6	T5	T4	Timer = 0 ~ 255s	00h
2nd parameter	W	H	-	-	-	T3	T2	T1	T0		00h
Screen_Saver_Sleep_Start											
SSLPSTRT	W	L	-	11h						**SS** Auto Sleep Timer Start	-
1st parameter	W	H	-	-	-	-	-	-	D0		00h
Screen_Saver_Step_Timer											
SSTEPTIMER	W	L	-	12h						**SS** Step Timer Set	-
1st parameter	W	H	-	-	-	T7	T6	T5	T4	Timer = 0 ~ 25.5s	00h
2nd parameter	W	H	-	-	-	T3	T2	T1	T0		
Screen_Saver_Step_Unit											
SSTEPUNIT	W	L	-	13h						**SS** Step Timer Unit Set	-
1st parameter	W	H	-	-	-	-	-	S1	S0		00h
Screen_Saver_Box_Area											
SBOXSIZE	W	L	-	14h						**SS** Box Column & Row Set	-
1st parameter	W	H	-	-	-	-	SX6	SX5	SX4	**SS** Box Column Start Address	00h
2nd parameter	W	H	-	-	-	SX3	SX2	SX1	SX0		00h
3rd parameter	W	H	-	-	-	-	EX6	EX5	EX4	**SS** Box Column End Address	07h
4th parameter	W	H	-	-	-	EX3	EX2	EX1	EX0		0Fh
5th parameter	W	H	-	-	-	-	SY6	SY5	SY4	**SS** Box Row Start Address	00h
6th parameter	W	H	-	-	-	SY3	SY2	SY1	SY0		00h
7th parameter	W	H	-	-	-	-	EY6	EY5	EY4	**SS** Box Row End Address	07h
8th parameter	W	H	-	-	-	EY3	EY2	EY1	EY0		0Fh
Screen_Saver_Changing_Moving_Step											
SSTEPSET	W	L	-	15h						**SS** Changing or Moving Step Set	-
1st parameter	W	H	-	-	-	SX3	SX2	SX1	SX0	X Step	01h
2nd parameter	W	H	-	-	-	SY3	SY2	SY1	SY0	Y Step	01h
Screen_Saver_Condition											
SCONDI	W	L	-	16h						**SS** Condition Set	-
1st parameter	W	H	-	-	LO	U	D	R	L		00h
Screen_Saver_Start/Stop											
SSTTSTP	W	L	-	17h						**SS** Start/Stop	-
1st parameter	W	H	-	-	-	-	-	-	SS		00h
Screen_Saver_Select											
SSELECT	W	L	-	18h						**SS** Select Common Command	-
1st parameter	W	H	-	-	-	SS3	SS2	SS1	SS0	**SS** 0=ZIGZAG **SS** 1=RANDOM **SS** 2=MultiScroll **SS** 3=FadeInOut **SS** 4=FadeBox **SS** 5=FadeMask **SS** 6=FadeScroll **SS** 7=AutoColor	00h

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
Screen_Saver_Color_Stage											
SCOLSTG	W	L	-	19h						**SS** Color Stage Set	-
1st parameter	W	H	-	-	-	-	S2	S1	S0		00h
Screen_Saver_Color_Pallet											
SCOLPAL	W	L	-	1Ah						**SS** Pallet Set	-
1st parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet0	07h
2nd parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet1	06h
3rd parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet2	05h
4th parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet3	04h
5th parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet4	03h
6th parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet5	02h
7th parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet6	01h
8th parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet7	00h

Icon command

IC : Icon ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
Icon_Display_On/Off											
IDSPONOFF	W	L	-	20h						**IC** Display On/Off or Normal	-
1st parameter	W	H	-	-	-	-	-	D1	D0		00h
Icon_Stand-By_On/Off											
ISTBYONOFF	W	L	-	21h						**IC** Stand-by Setting	-
1st parameter	W	H	-	-	-	-	-	-	D0		01h
Icon_Register_Set/Reset											
IREGSETRST	W	L	-	22h						**IC** Register Set/Reset	-
1st parameter	W	H	-	-	-	-	-	AD	SR		00h
Icon_Reference_Current											
ICONIREF	W	L	-	23h						**IC** Reference Current Set	-
1st parameter	W	H	-	-	-	I7	I6	I5	I4		00h
2nd parameter	W	H	-	-	-	I3	I2	I1	I0		00h
Icon_Initisalize											
ICONINIT	W	L	-	24h						**IC** Initialize	-
1st parameter	W	H	-	S5	S4	S3	S2	S1	S0	**IC** Status	00h
:	W	H	-	:	:	:	:	:	:		
56th parameter	W	H	-	S5	S4	S3	S2	S1	S0	**IC** Status	00h
Icon_Data_Write											
IDATAWR	W	L	-	25h						**IC** Data Write	-
1st parameter	W	H	-	-	-	-	-	-	D0		00h
2nd parameter	W	H	-	N5	N4	N3	N2	N1	N0		00h
Icon_Blink_Time											
IBLINKTIME	W	L	-	26h						**IC** Blink time	-
1st parameter	W	H	-	-	-	-	-	-	BS	**IC** Blink time set	00h
2nd parameter	W	H	-	T5	T4	T3	T2	T1	T0		00h
Icon_Blink_Data											
IBLINKDATA	W	L	-	27h						**IC** Blink data	-
1st parameter	W	H	-	-	-	-	-	-	BD	**IC** Blink data set	00h
2nd parameter	W	H	-	B5	B4	B3	B2	B1	B0		00h
Icon_Row_High_Period											
IROWHIGH	W	L	-	28h						**IC** Row High Period Set	-
1st parameter	W	H	-	-	-	-	L2	L1	L0		00h
Icon_DC-DC_Control											
ICONDCDC	W	L	-	29h						**IC** DC-DC Control Set	-
1st parameter	W	H	-	-	-	-	-	M1	M0		01h
Icon_Frame_Frequency											
IFRAME	W	L	-	2Ah						**IC** Frame Frequency Set	-
1st parameter	W	H	-	-	-	-	F2	F1	F0		02h

Instruction Description

MAIN

SOFTWARE_RESET (01H)

Software reset

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
SWRESET	W	L	-	01h						Display Off	-

All registers are cleared default (except for ICON Area and Data Register).

Dot matrix and All ICON are OFF.

OSCA , OSCB and internal DC-DC are stopped.

Graphic memory is kept.

DOT_MATRIX_DISPLAY_ON/OFF (02H)

Dot display on/off

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
DDISPONOFF	W	L	-	02h						Dot Matrix Display ON/OFF	-
1st parameter	W	H	-	**0**	**0**	**0**	**0**	**0**	D0	D0=0:Display Off, D0=1:Display On	00h

When D="00h" :

Turns the dot matrix Display OFF (Default).

Display OFF means

All Column Output become Hi-Z

All Row Output become GND

Stop Data transfer from memory to Dot Matrix Driver.

When D="01h" :

Turns the dot matrix Display ON.

DOT_MATRIX_STAND-BY_ON/OFF (03H)

Dot matrix stand-by on/off

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
DSTBYONOFF	W	L	-	03h						Dot Matrix Stand-By ON/OFF	-
1st parameter	W	H	-	**0**	**0**	**0**	**0**	**0**	D0	D0=0:OSCA start, D0=1:Run DDISPOFF,OSCA stop	01h

When D=”00h”

OSCA Start. (Don’t turn the dot matrix display on)

When D=”01h”

Execute Dot_Matrix_displzy_On/Off (DDISPOFF) command

OSCA Stop. (Default).

This command can’t clear Graphics memory and Register.

After software and hardware Reset, stay “Dot_Matrix_Stand-By_On/Off (DSTBYON)” Mode.

Column Driver latched data are reset.

DOT_MATRIX_FRAME_FREQUENCY (04H)

Dot matrix frame frequency

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
DFRAME	W	L	-	04h						Dot Matrix Frame frequency set	-
1st parameter	W	H	-	-	-	-	F2	F1	F0	60 ~ 150 Hz	02h

F[2:0]	Frame Frequency
0	60Hz
1	75Hz
2	90Hz(Default)
3	105Hz
4	120Hz
5	135Hz
6	150Hz
7	150Hz

DATA_WRITE_CONTROL (05H)

Graphic memory writing control setting

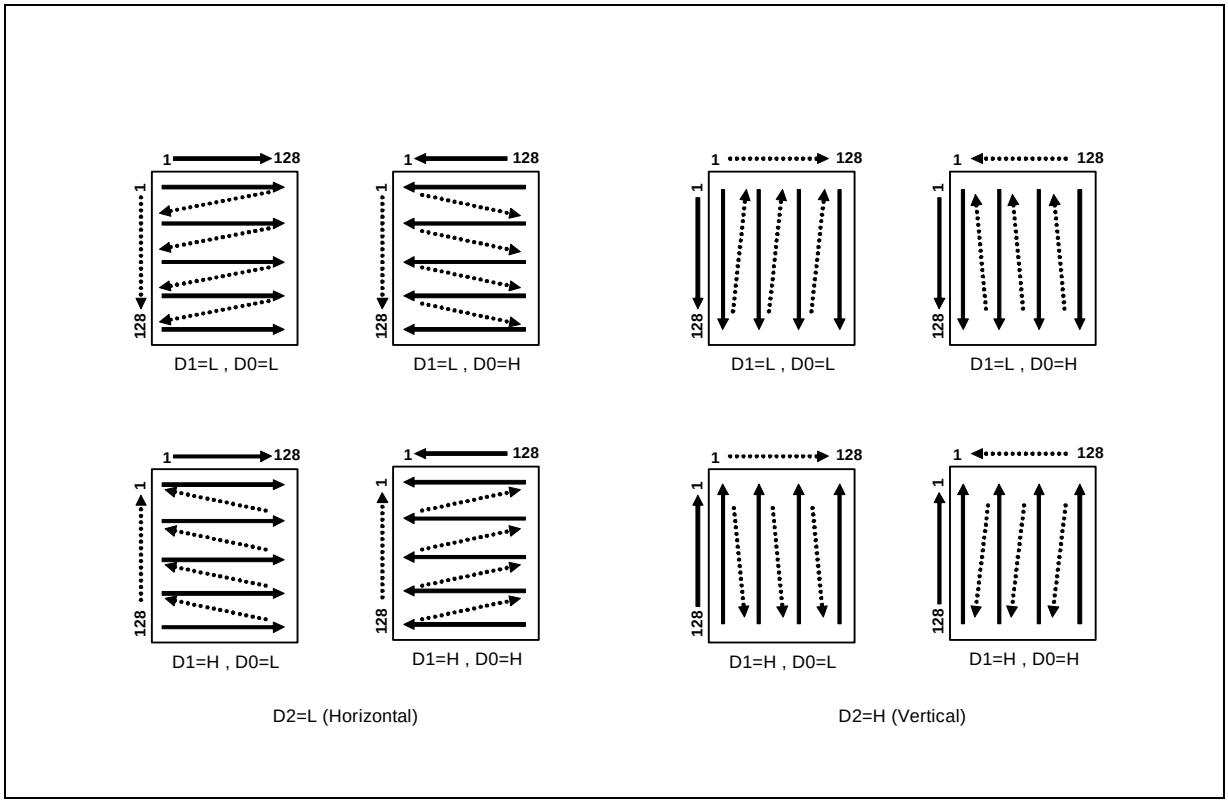
Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
WRITEDIR	W	L	-	05h						Data Write Control	-
1st parameter	W	H	-	-	-	D3	D2	D1	D0	VH=0;Horizontal, VH=1:Vertical	00h

D3= "L": Write memory cell RGB-order. (Default)
D3= "H". Write memory cell BGR-order.

D2 = "L": Write Direction is "Horizontal. (Default)
D2 = "H": Write Direction is "Vertical".

D1 = "L": Row Address Counter is "Increment". (From Top to Bottom). (Default)
D1 = "H": Row Address Counter is "Decrement". (From Bottom to Top)

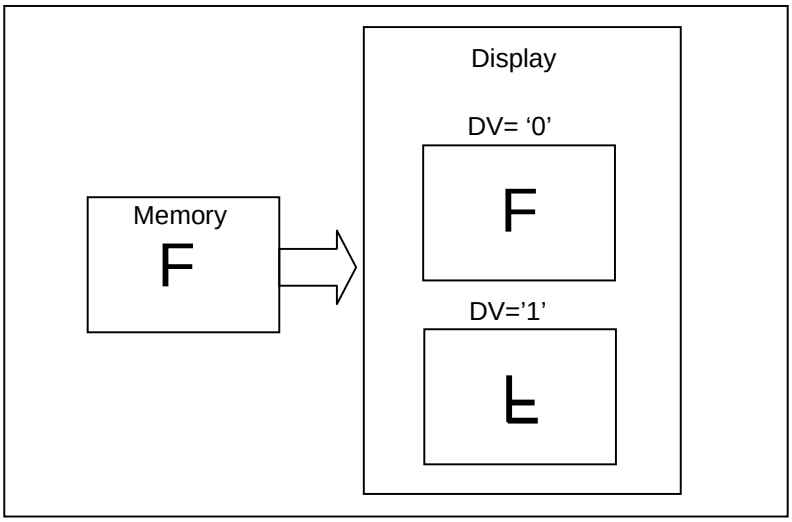
D0 = "L": Column Address Counter is "Increment". (From Left to Right). (Default)
D0 = "H": Column Address Counter is "Decrement". (From Right to Left)



DISPLAY_DIRECTION (06H)

Display direction set.

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
DISPDIR	W	L	-	06h						Display Direction Control	-
1st parameter	W	H	-	-	-	-	-	DV	**0**	Display direction	00h



DISPLAY_SIZE (07H)

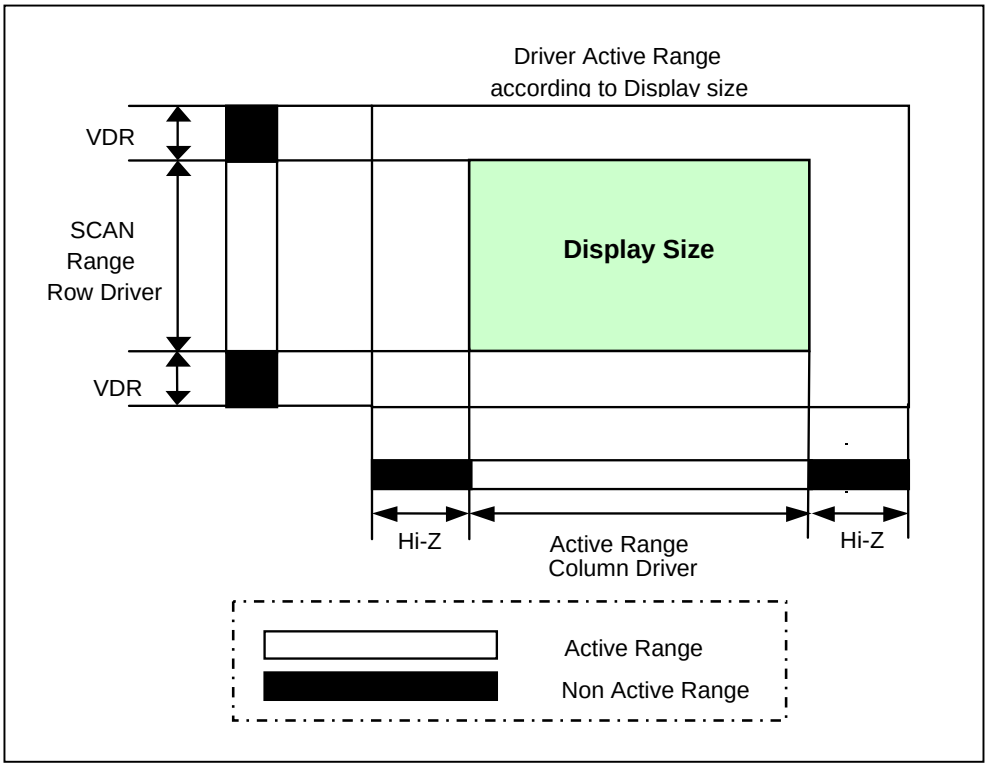
Setting Row and Column Outputs Range.

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
DISPSIZE	W	L	-	07h						Display size Set	-
1st parameter	W	H	-	-	-	-	FX6	FX5	FX4	Display size X From	00h
2nd parameter	W	H	-	-	-	FX3	FX2	FX1	FX0		00h
3rd parameter	W	H	-	-	-	-	TX6	TX5	TX4	Display size X to	07h
4th parameter	W	H	-	-	-	TX3	TX2	TX1	TX0		0Fh
5th parameter	W	H	-	-	-	-	FY6	FY5	FY4	Display size Y From	00h
6th parameter	W	H	-	-	-	FY3	FY2	FY1	FY0		00h
7th parameter	W	H	-	-	-	-	TY6	TY5	TY4	Display size Y to	07h
8th parameter	W	H	-	-	-	TY3	TY2	TY1	TY0		0Fh

From FX to TX ：The range of active Column Outputs (Range：0h~7Fh)
XE＜XS" is inhibited.

From FY to TY ：The range of active Row Outputs setting(Range：00h~7Fh)
YE＜YS" is inhibited.

The outputs out of settng range, set Hi-Z(Column) and VDR(Row).
Screen Saver Area is moved in all memory Size.
Line scan frequency isn't related with DISPSIZE command.



MPU_INTERFACE_MODE (08H)

Display data interface select

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
IFMode	W	L	-	08h						Data bus Interface bit Select	-
1st parameter	W	H	-	-	-	-	D2	D1	D0	6/8/9/16/18 bit	00h

When D[2:0]="000" 6-Bit display data Interface for 262k color.
When D[2:0]="001" 8-Bit display data Interface for 65k color.
When D[2:0]="010" 9-Bit display data Interface for 262k color.
When D[2:0]="011" 16-Bit display data Interface for 65k color.
When D[2:0]="100" 18-Bit display data Interface for 262k color.

1 Pixel(RGB) display data format

Data bus width	W/R	A0	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Display colors	D[2:0]
6-Bit Mode	W	L	-												R5	R4	R3	R2	R1	R0	262k color	000
	W	L	-												G5	G4	G3	G2	G1	G0		
	W	L	-												B5	B4	B3	B2	B1	B0		
8-Bit Mode	W	L	-										R4	R3	R2	R1	R0	G5	G4	G3	65k color	001
	W	L	-										G3	G2	G1	B4	B3	B2	B1	B0		
9-Bit Mode	W	L	-									R5	R4	R3	R2	R1	R0	G5	G4	G3	262k color	010
	W	L	-									G2	G1	G0	B5	B4	B3	B2	B1	B0		
16-Bit Mode	W	L	-	-	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65k color	011
18-Bit Mode	W	L	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262k color	100

DATA_REVERSE_COLOR_MASKING (09H)

Data reverse and RGB color masking

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
DATAMASK	W	L	-	09h						Data Reverse & Color Masking	-
1st parameter	W	H	-	-	RV	-	R	G	B	RV=0:Origin, RV=1:Reverse	07h

When RV ="1" : (Data EXOR "FFFFh") AND Pallet(RGB) ⇒ Output Data

When RV ="0" : Data AND Pallet(RGB) ⇒ Output Data

When R = '0' : Red output data is masking.

When B = '0' : Blue output data is masking.

When G = '0' : Green output data is masking.

DATA_R/W_BOX_SIZE (0AH)

Read & write box size set

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
RWBOXSIZE	W	L	-	0Ah						Read & Write Box Size Set	-
1st parameter	W	H	-	-	-	-	XS6	XS5	XS4	R/W Box Column Start Address	00h
2nd parameter	W	H	-	-	-	XS3	XS2	XS1	XS0		00h
3rd parameter	W	H	-	-	-	-	XE6	XE5	XE4	R/W Box Column End Address	07h
4th parameter	W	H	-	-	-	XE3	XE2	XE1	XE0		0Fh
5th parameter	W	H	-	-	-	-	YS6	YS5	YS4	R/W Box Row Start Address	00h
6th parameter	W	H	-	-	-	YS3	YS2	YS1	YS0		00h
7th parameter	W	H	-	-	-	-	YE6	YE5	YE4	R/W Box Row End Address	07h
8th parameter	W	H	-	-	-	YE3	YE2	YE1	YE0		0Fh

XS6-XS0 ：X axis Reading/Writing Start Point (Range : 00h~7Fh)
XE6-XE0 ：X axis Reading/Writing End Point (Range : 00h~7Fh)

”XE＜XS” is inhibited.

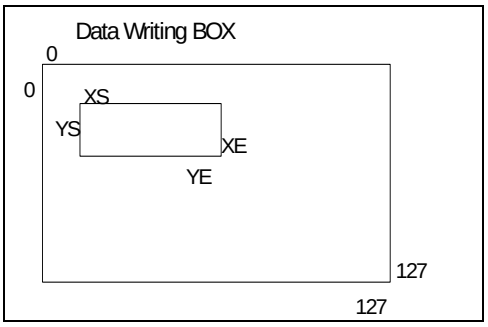
YS6-YS0 ：Y axis Reading/Writing Start Point (Range : 00h~7Fh)
YE6-YE0 ：Y axis Reading/Writing End Point (Range : 00h~7Fh)

”YE＜YS” is inhibited.

After this command executes, writing address is set like under table**.**

Writing Direction Mode	X address	Y address
00	XS	YS
01	XE	YS
10	XS	YE
11	XE	YE

See Writing Direction Set Command.

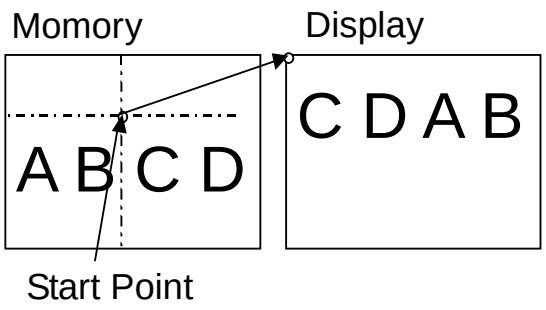


MEMORY_READ_START_ADDRESS (0BH)

Memory reading start address set

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
DISPSTART	W	L	-	0Bh						Memory Read Start Set	-
1st parameter	W	H	-	-	-	-	DX6	DX5	DX4	Memory read column start address	00h
2nd parameter	W	H	-	-	-	DX3	DX2	DX1	DX0		00h
3rd parameter	W	H	-	-	-	-	DY6	DY5	DY4	Memory read row start address	00h
4th parameter	W	H	-	-	-	DY3	DY2	DY1	DY0		00h

DX6-DX0 ：X axis Reading Start address (Range : 00h~7Fh)
DY6-DY0 ：Y axis Reading Start address (Range : 00h~7Fh)

Memory Reading Start Address	“Memory_Read_Start_Address (DISPSTART)” command fix the relation of memory and display coordinates.	

DATA_WRITE/READ (0CH)

Dot matrix display data write and read.

Instruction	W/R	A0	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default
Data Write																						
DATARW	W	L	-												0Ch						Dot Matrix Data Write	-
6-bit Mode (262k color)	W	H	-												R5	R4	R3	R2	R1	R0	1st Data	
	W	H	-												G5	G4	G3	G2	G1	G0		
	W	H	-												B5	B4	B3	B2	B1	B0		
	:	:	:												:	:	:	:	:	:		
	W	H	-												R5	R4	R3	R2	R1	R0	Nth Data	
	W	H	-												G5	G4	G3	G2	G1	G0		
	W	H	-												B5	B4	B3	B2	B1	B0		
8-bit Mode (65k color)	W	H	-										R4	R3	R2	R1	R0	G5	G4	G3	1st Data	
	W	H	-										G2	G1	G0	B4	B3	B2	B1	B0		
	:	:	:										:	:	:	:	:	:	:	:		
	W	H	-										R4	R3	R2	R1	R0	G5	G4	G3	Nth Data	
	W	H	-										G2	G1	G0	B4	B3	B2	B1	B0		
9-bit Mode (262k color)	W	H	-									R5	R4	R3	R2	R1	R0	G5	G4	G3	1st Data	
	W	H	-									G2	G1	G0	B5	B4	B3	B2	B1	B0		
	:	:	:									:	:	:	:	:	:	:	:	:		
	W	H	-									R5	R4	R3	R2	R1	R0	G5	G4	G3	Nth Data	
	W	H	-									G2	G1	G0	B5	B4	B3	B2	B1	B0		
16-bit Mode (65k color)	W	H	-	-	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1st Data	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	W	H	-	-	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	Nth Data	
18-bit Mode (262k color)	W	H	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	1st Data	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	W	H	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	Nth Data	

Instruction	W/R	A0	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default
Data Read																						
DATARW	W	L	-												0Ch						Dot Matrix Data Write	
18-bit Mode	R	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	dummy	
	R	H	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	1st Data	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:				
	R	H	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	Nth Data	
16-bit Mode & 9-bit Mode	R	H	-									X	X	X	X	X	X	X	X	X	dummy	
	R	H	-									R5	R4	R3	R2	R1	R0	G5	G4	G3	1st Data	
	R	H	-									G2	G1	G0	B5	B4	B3	B2	B1	B0		
	:	:	:									:	:	:	:	:	:	:	:	:		
	R	H	-									R5	R4	R3	R2	R1	R0	G5	G4	G3	Nth Data	
	R	H	-									G2	G1	G0	B5	B4	B3	B2	B1	B0		
8-bit Mode & 6-bit Mode	R	H	-												X	X	X	X	X	X	dummy	
	R	H	-												R5	R4	R3	R2	R1	R0	1st Data	
	R	H	-												G5	G4	G3	G2	G1	G0		
	R	H	-												B5	B4	B3	B2	B1	B0		
	:	:	:												:	:	:	:	:	:		
	R	H	-												R5	R4	R3	R2	R1	R0	Nth Data	
	R	H	-												G5	G4	G3	G2	G1	G0		
	R	H	-												B5	B4	B3	B2	B1	B0		

In the area out of reading / writing-box , this command can't write data.

Address auto increment acceding to WRITEDIR setting direction.

When memory address increment/decrement is reached at the end of reading / writing-box, memory write finish.

If you read / write again, re-enter "Data_Write/Read (DATARW)" command.

REGISTER_READ (0DH)

Resigter read.

Instruction	W/R	A0	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default
Register Read																						
REGREAD	W	L	-												0Dh						Register Read	
1st parameter	R	H	-												D5	D4	D3	D2	D1	D0	1st parameter	
:	:	:	-												:	:	:	:	:	:		
16th parameter	R	H	-												D5	D4	D3	D2	D1	D0	16th parameter	

Read out registers.

Order	Register
1	Dot_Matrix_Display_On/Off (DDISPON/OFF)
2	Dot_Matrix_Stand-By_On/Off (DSTBYON/OFF)
3	Display_Size (DISPSIZE XS[6:4])
4	Display_Size (DISPSIZE XS[3:0])
5	Display_Size (DISPSIZE XE[6:4])
6	Display_Size (DISPSIZE XE[3:0])
7	Display_Size (DISPSIZE YS[6:4])
8	Display_Size (DISPSIZE YS[3:0])
9	Display_Size (DISPSIZE YE[6:4])
10	Display_Size (DISPSIZE YE[3:0])
11	Row_Overlap_Scan (SCANMODE[1:0])
12	Icon_Display_On/Off (IDSPONOFF)
13	Icon_DC-DC_Control (ICONDCDC)
14	Screen_Saver_Sleep_Start (SSLPSTRT)
15	Screen_Saver_Start/Stop (SSTTSTP)
16	Screen_Saver_Select (SSELECT)

DOT_CURRENT (0EH)

Dot matrix current level set.

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
DOTCURRENT	W	L	-	0Eh						Dot Current Set	-
1st parameter	W	H	-	-	-	IR7	IR6	IR5	IR4	Red Level = 0 ~ 255uA	00h
2nd parameter	W	H	-	-	-	IR3	IR2	IR1	IR0		00h
3rd parameter	W	H	-	-	-	IG7	IG6	IG5	IG4	Green Level = 0 ~ 255uA	00h
4th parameter	W	H	-	-	-	IG3	IG2	IG1	IG0		00h
5th parameter	W	H	-	-	-	IB7	IB6	IB5	IB4	Blue Level = 0 ~ 255uA	00h
6th parameter	W	H	-	-	-	IB3	IB2	IB1	IB0		00h

IR[7:0] / IG[7:0] / IB[7:0]		Reference Current Value (1.0u step)		
Hex	Dec	Red (IR)	Green (IG)	Blue (IB)
00	0	0.0 uA	0.0 uA	0.0 uA
01	1	1.0 uA	1.0 uA	1.0 uA
02	2	2.0 uA	2.0 uA	2.0 uA
03	3	3.0 uA	3.0 uA	3.0 uA
04	4	4.0 uA	4.0 uA	4.0 uA
05	5	5.0 uA	5.0 uA	5.0 uA
06	6	6.0 uA	6.0 uA	6.0 uA
:	:	:	:	:
:	:	:	:	:
F9	249	249.0 uA	249.0 uA	249.0 uA
FA	250	250.0 uA	250.0 uA	250.0 uA
FB	251	251.0 uA	251.0 uA	251.0 uA
FC	252	252.0 uA	252.0 uA	252.0 uA
FD	253	253.0 uA	253.0 uA	253.0 uA
FE	254	254.0 uA	254.0 uA	254.0 uA
FF	255	255.0 uA	255.0 uA	255.0 uA

Gray scale			Normal Current			Peak Current		
Red	Green	Blue	Red	Green	Blue	Red	Green	Blue
0	0	0	0	0	0	0	0	0
1	1	1	1/63xIR	1/63xIG	1/63xIB	1/63xIRx10	1/63xIGx10	1/63xIBx10
2	2	2	2/63xIR	2/63xIG	2/63xIB	2/63xIRx10	2/63xIGx10	2/63xIBx10
3	3	3	3/63xIR	3/63xIG	3/63xIB	3/63xIRx10	3/63xIGx10	3/63xIBx10
4	4	4	4/63xIR	4/63xIG	4/63xIB	4/63xIRx10	4/63xIGx10	4/63xIBx10
:	:	:	:	:	:	:	:	:
59	59	59	59/63xIR	59/63xIG	59/63xIB	59/63xIRx10	59/63xIGx10	59/63xIBx10
60	60	60	60/63xIR	60/63xIG	60/63xIB	60/63xIRx10	60/63xIGx10	60/63xIBx10
61	61	61	61/63xIR	61/63xIG	61/63xIB	61/63xIRx10	61/63xIGx10	61/63xIBx10
62	62	62	62/63xIR	62/63xIG	62/63xIB	62/63xIRx10	62/63xIGx10	62/63xIBx10
63	63	63	63/63xIR	63/63xIG	63/63xIB	63/63xIRx10	63/63xIGx10	63/63xIBx10

* 10 times Peak current is guaranteed under TBD μA but the peak current over TBD μA, the deviation is lower 4.0%.

PRE-CHARGE_MODE (1BH)

Pre-charge mode selection and compare bit set.

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
PRCSELECT	W	L	-	1Bh						Pre-Charge Mode Set	-
1st parameter	W	H	-	-	-	-	-	D1	D0	Width = 0 ~ 255us	01h

D1 and D0 used for Pre-Charge and Peak boot Selection Mode.

Default = 01h.

D1	D0	Pre-charge	Peak Boot
0	0	None	None
1	0	Every time	Every time
0	1	Selective (All Data)	Selective (All Data)
1	1	Selective (Data=max)	Selective (Data=max)

In case of PreC_Select **D[1:0] = “11”**

If (dataR(n) ≠ ”3Fh” or dataR(n-1) ≠”3Fh”) then do pre-charge and peak boot at that pixel.
If (dataG(n) ≠ ”3Fh” or dataG(n-1) ≠”3Fh”) then do pre-charge and peak boot at that pixel.
If (dataB(n) ≠ ”3Fh” or dataB(n-1) ≠”3Fh”) then do pre-charge and peak boot at that pixel.

If (dataR(n) = ”3Fh” and dataR(n-1)=”3Fh”) then Hi-z pre-charge and peak boot at that pixel.
If (dataG(n) = ”3Fh” and dataG(n-1)=”3Fh”) then Hi-z pre-charge and peak boot at that pixel.
If (dataB(n) = ”3Fh” and dataB(n-1)=”3Fh”) then Hi-z pre-charge and peak boot at that pixel.

PRE-CHARGE_PULSE_WIDTH (1CH)

Pre-charge pulse width set.

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
PRCWIDTH	W	L	-	1Ch						Pre-Charge Width Set	-
1st parameter	W	H	-	-	-	T7	T6	T5	T4	Width = 0 ~ 255us	00h
2nd parameter	W	H	-	-	-	T3	T2	T1	T0		08h

T[7:0]		Pre-Charge Pulse Width Value (Default = 08h)
Hex	Dec	
0	0	0 us
1	1	1 us
2	2	2 us
3	3	3 us
4	4	4 us
5	5	5 us
6	6	6 us
7	7	7 us
8	8	8 us
: :	: :	: :
FC	252	252 us
FD	253	253 us
FE	254	254 us
FF	255	255 us

If the pre-charge pulse width is longer than one line period, the column driving is pre-charge all the time.

PEAK_PULSE_WIDTH (1DH)

Peak pulse width set.

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
PEAKWIDTH	W	L	-	1Dh						Peak Pulse Width Set	-
1st parameter	W	H	-	-	W4	W3	W2	W1	W0	Red Width = 0 ~ 31us	05h
2nd parameter	W	H	-	-	W4	W3	W2	W1	W0	Green Width = 0 ~ 31us	05h
3rd parameter	W	H	-	-	W4	W3	W2	W1	W0	Blue Width = 0 ~ 31us	05h

W [4:0]		Peak Pulse Width Value (Default = 05h)
Hex	Dec	
0	0	0 us
1	1	1 us
2	2	2 us
3	3	3 us
4	4	4 us
5	5	5 us
:	:	:
1C	28	28 us
1D	29	29 us
1E	30	30 us
1F	31	31 us

PEAK_PULSE_DELAY (1EH)

Peak pulse delay set.

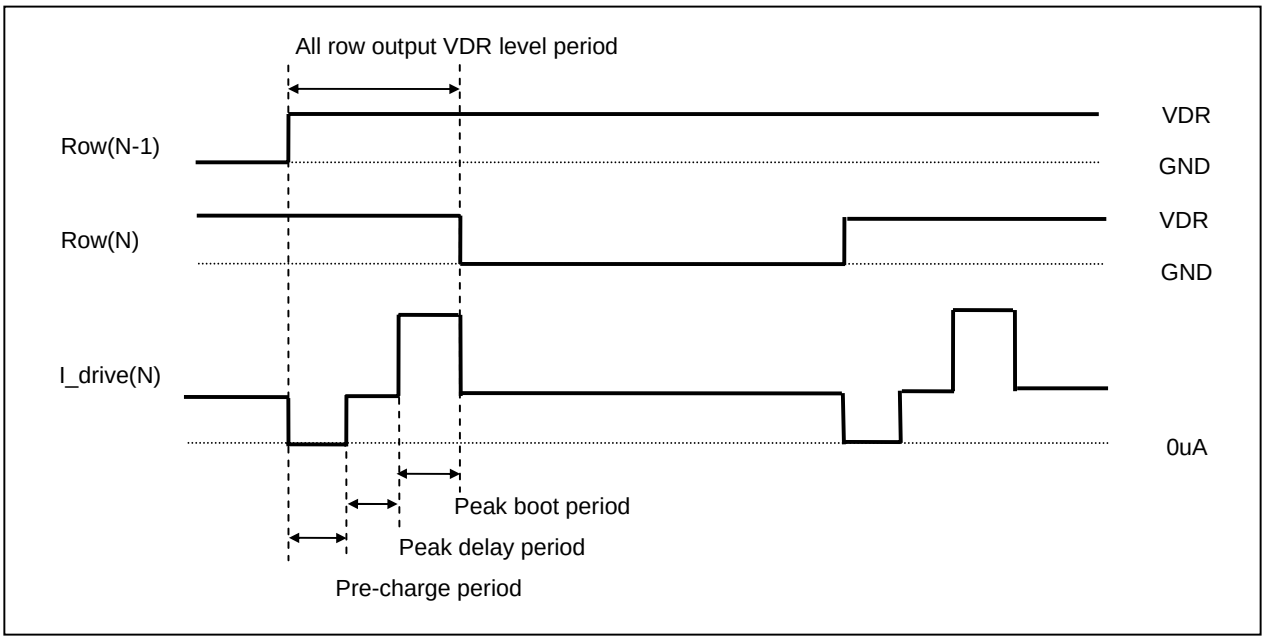
Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
PEAKDELAY	W	L	-	1Eh						Peak Pulse Delay Set	-
1st parameter	W	H	-	-	-	W3	W2	W1	W0	Delay = 0 ~ 15us	05h

W[3:0]		Peak Pulse Delay Time Value (Default = 08h)
Hex	Dec	
0	0	0.0 us
1	1	1.0 us
2	2	2.0 us
3	3	3.0 us
4	4	4.0 us
5	5	5.0 us
6	6	6.0 us
7	7	7.0 us
8	8	8.0 us
9	9	9.0 us
A	10	10.0 us
B	11	11.0 us
C	12	12.0 us
D	13	13.0 us
E	14	14.0 us
F	15	15.0 us

ROW_OVERLAP_SCAN (1FH)

Row output enable mode set

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
ROWSCAN	W	L	-	1Fh						Row Scan Set	-
1st parameter	W	H	-	D5	D4	D3	-	D1	D0	D[5:4] : Row Overlap Timing Set D[3] : Row Scan Mode Set D[1:0] : Row Scan Sequence Set	00h



Row output VDR timing setting table.

D5	D4	All Row VDR Time
0	0	None (Default)
0	1	Pre-Charge Timing
1	0	Pre-Charge + Peak Delay Timing
1	1	Pre-Charge + Peak Delay + Max(RGB) Peak boot Timing

Row scan mode set.

D3=”0” normal Scan.

D3=”1” All Row are in GND.

Row scan sequence set.

D[1:0]	SCAN Mode
0	Mode 1 : alternate scan mode. (Default)
1	Mode 2 : sequential scan mode.
2	Mode 3 : simultaneous scan mode.(half piriod)

D[1:0]	DispDirection	Case of 128 Line Scan
0	0	R0,R1,R2…R126,R127
	2	R127,R126,R125…R1,R0
1	0	R0,R2…R126,R1,R3,…R127
	2	R127,R1253…R1,R126,R124…R0
2	0	R0,R2…R126 R1,R3…R127
	2	R127,R125…R1 R126,R124…R0

In Mode 3, maximun Row number is 64 line at Display Size setting.

RGB_INTERFACE_MODE (2DH)

RGB interface Mode set.

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
RGBIF	W	L	-	2Dh						RGB Interface Set	-
1st parameter	W	H	-	RB	RA	DM1	DM0	RM1	RM0	RGB Interface mode set	00h

1st parameter : RGB Interface Mode set

RB is determined the RGB 6-bit interface data bus
- When RB=”0” VD[5:0]
- When RB=”1” VD[17:12]

RA is determined the RAM access
- When RA=”0” MPU Interface
- When RA=”1” RGB Interface

DM[1:0] is determined the Display Operation Mode.
- When DM[1:0]=”00” Internal operating clock.
- When DM[1:0]=”01” RGB interface.
- When DM[1:0]=”10” VSYNC interface.
- When DM[1:0]=”11” not used.

RM[1:0] select the 6-bit/16-bit/18-bit RGB interface data bus.
- When RM[1:0]=”10” 6-Bit RGB interface data bus for 262k color.
- When RM[1:0]=”01” 16-Bit RGB interface data bus for 65k color.
- When RM[1:0]=”00” 18-Bit RGB interface data bus for 262k color.

RGB Interface Operation Mode

Operation Mode	RAM Access Operation Mode (RA)	Display Operation Mode(DM[1:0])
Internal operating clock only (Displaying still picture)	MPU Interface (RA = 0)	Internal operating clock(DM[1:0] = “00”)
RGB Interface (1) (Display moving picture)	RGB Interface (RA = 1)	RGB Interface (DM[1:0] = “01”)
RGB Interface (2) (Rewriting still picture while displaying moving	MPU Interface (RA = 0)	RGB Interface (DM[1:0] = “00”)
VSYNC Interface (Displaying moving pictures)	MPU Interface (RA = 0)	VSYNC Interface(DM[1:0] = “10”)

RGB Interface data bus width Selection

RM1	RM0	RGB Interface	VD Pin
0	0	18-bit RGB Interface	VD17-0
0	1	16-bit RGB Interface	VD17-13, VD11-1
1	0	6-bit RGB Interface	VD5-0
		6-bit RGB Interface	VD17-12
1	1	Setting disabled	-

RGB interface data format

Data bus width	W/R	A0	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Display colors	
18-Bit Mode	W	L	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262k color	
16-Bit A Mode	W	L	R4	R3	R2	R1	R0	-	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	-	65k color	
6-Bit Mode	W	L	-												R5	R4	R3	R2	R1	R0	262k color	
	W	L	-												G5	G4	G3	G2	G1	G0		
	W	L	-												B5	B4	B3	B2	B1	B0		
6-Bit Mode	W	L	R5	R4	R3	R2	R1	R0	-													
	W	L	G5	G4	G3	G2	G1	G0	-													
	W	L	B5	B4	B3	B2	B1	B0	-													

DISPLAY_CLOCK_CONDITION (2EH)

Display Clock condition set

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
DISPCLK	W	L	-	2Eh						Display Clock condition set	-
1st parameter	W	H	-	-	-	-	-	HN7	HN6	Number of pixels during 1H	02h
2nd parameter	W	H	-	HN5	HN4	HN3	HN2	HN1	HN0		08h
3rd parameter	W	H	-	-	-	BP3	BP2	BP1	BP0	Number of lines for Back Porch	0Eh
4th parameter	W	H	-	-	-	FP3	FP2	FP1	FP0	Number of lines for Front Porch	02h

Display clock condition set.
1st to 4th parameter: Display clock set for full colour display mode.
HN [7:0]: Number of pixels during 1H
HN >= 132 (84h)
BP [3:0]: Number of lines for vertical back porch
FP [3:0]: Number of lines for vertical front porch

RGB_SIGNAL_POLARITY (2FH)

RGB interface signal polarity set.

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
RGBPOL	W	L	-	2Fh						RGB Polarity Set	-
1st parameter	W	H	-	-	PV	PH	PC	PE	PO	RGB Interface signal Polarity set	00h

1st parameter (PV,PH,PC,PE,PO) determines that the polarity of RGB interface control signals.

When PV="0" The polarity of **VSYNC** input is "Low active".
When PV="1" The polarity of **VSYNC** input is "High active"

When PH="0" The polarity of **HSYNC** input is "Low active".
When PH="1" The polarity of **HSYNC** input is "High active"

When PC="0" The Timing of VD[17:0] data input is determined on rising edge of **DCK**.
When PC="1" The Timing of VD[17:0] data input is determined on falling edge of **DCK**

When PE="0" The polarity of **Enable** input is "Low active".
When PE="1" The polarity of **Enable** input is "High active"

When PO="0" The polarity of **VSYNCO** output is "High active".
When PO="1" The polarity of **VSYNCO** output is "Low active"

VROW_SEL (3AH)

Row power selection set

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
VROWSEL	W	L	-	3Ah						Row Power Level Set	-
1st parameter	W	H	-	-	EN	S3	S2	S1	S0		04h

EN	Row Driving Voltage Generator On/Off
0	Off (Default) : External Row Power is using
1	On : Internal Row Power Generator. Connect Power Capacitor to GND

S[3:0]	Level of VDR
0000	VDC x 0.95
0001	VDC x 0.90
0010	VDC x 0.85
0011	VDC x 0.80
0100	VDC x 0.75
0101	VDC x 0.70
0110	VDC x 0.65
0111	VDC x 0.60
1000	VDC x 0.55
1001	VDC x 0.50

SCREEN SAVER

SCREEN_SAVER _SLEEP_TIMER & SCREEN_SAVER _SLEEP_START (10, 11H)

Screen saver stop and display off after setting time.

SS : Screen Saver ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
SSLPTIM	W	L	-	10h						**SS** Sleep Timer Set	-
1st parameter	W	H	-	-	-	T7	T6	T5	T4	Timer = 0 ~ 255s	00h
2nd parameter	W	H	-	-	-	T3	T2	T1	T0		00h
SSLPSTRT	W	L	-	11h						**SS** Auto Sleep Timer Start	-
1st parameter	W	H	-	-	-	-	-	-	D0		00h

S_Sleep_Timer(SSLPTIM) is setting Time period from 0 to 255sec. (Default = 0h)

D0='0' : Sleep Stop. (Default)
D0='1' : Sleep Start.

S_Sleep_Start(SSLPSTRT) is execute the follows after setting time will gone.
S_Start/Stop(SSTTSTP) : stop
S_Sleep_Start(SSLPSTRT) : start
Dot_Display_On/Off(DDISPONOFF) : off

SCREEN_SAVER_STEP_TIMER & SCREEN_SAVER_STEP_UNIT (12, 13H)

Screen saver step timer set.

SS : Screen Saver ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
SSTEPTIMER	W	L	-	12h						**SS** Step Timer Set	-
1st parameter	W	H	-	-	-	T7	T6	T5	T4	Timer = 0 ~ 255ms or 25.5s	00h
2nd parameter	W	H	-	-	-	T3	T2	T1	T0		00h
SSTEPUNIT	W	L	-	13h						**SS** Step Timer Unit Set	-
1st parameter	W	H	-	-	-	-	-	S1	S0		00h

S_Step_Timer is setting time period from 0 to 255 msec or to 25.5 sec. (Default = 0h)

S_Step_Unit is setting

S = 0 : Timer Stop (Default)
S = 1 : 1ms Unit
S = 2 : 0.1s Unit

SCREEN_SAVER_BOX_AREA (14H)

Box area for screen saver.

SS : Screen Saver ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
SBOXSIZE	W	L	-	14h						**SS** Box Column & Row Set	-
1st parameter	W	H	-	-	-	-	SX6	SX5	SX4	**SS** Box Column Start Address	00h
2nd parameter	W	H	-	-	-	SX3	SX2	SX1	SX0		00h
3rd parameter	W	H	-	-	-	-	EX6	EX5	EX4	**SS** Box Column Start Address	07h
4th parameter	W	H	-	-	-	EX3	EX2	EX1	EX0		0Fh
5th parameter	W	H	-	-	-	-	SY6	SY5	SY4	**SS** Box Column Start Address	00h
6th parameter	W	H	-	-	-	SY3	SY2	SY1	SY0		00h
7th parameter	W	H	-	-	-	-	EY6	EY5	EY4	**SS** Box Column Start Address	07h
8th parameter	W	H	-	-	-	EY3	EY2	EY1	EY0		0Fh

SX：Box Start Column Point : 00h－7Fh (Default=00h)
EX：Box End Column Point : 00h－7Fh (Default=7Fh)
Always SX < EX

SY：Box Start Row Point : 00h－7Fh (Default=00h)
EY：Box End Row Point : 00h－7Fh (Default=7Fh)
Always SY < EY

SCREEN_SAVER_CHANGING_MOVING_STEP (15H)

Step value set for screen saver.

SS : Screen Saver ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
SSTEPSET	W	L	-	15h						**SS** Changing or Moving Step Set	-
1st parameter	W	H	-	-	-	SX3	SX2	SX1	SX0	X Step	01h
2nd parameter	W	H	-	-	-	SY3	SY2	SY1	SY0	Y Step	01h

SX：Moving Step for Column Point : 00h－0fh (Default=01h)
SY：Moving Step for Row Point : 00h－0fh (Default=01h)

SCREEN_SAVER_CONDITION (16H)

One time or repeat action, direction condition setting for screen saver.

SS : Screen Saver ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
SCONDI	W	L	-	16h						**SS** Condition Set	-
1st parameter	W	H	-	-	LO	U	D	R	L	X Step	00h

LO= "0": One time (Default)
LO= "1": repeat

UDRL: Upper/Down/Right/Left Direction (Default = 0h)

SCREEN_SAVER_START/STOP (17H)

Start/stop Screen Saver

SS : Screen Saver ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
SSTTSTP	W	L	-	17h						**SS** Start/Stop	-
1st parameter	W	H	-	-	-	-	-	-	SS	X Step	00h

SS="0": Stop (Default)
SS="1": Start

SCREEN_SAVER_SELECT (18H)

Screen saver select

SS : Screen Saver ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
SSELECT	W	L	-	18h						**SS** Select Common Command	-
1st parameter	W	H	-	-	-	SS3	SS2	SS1	SS0	**SS** 0=ZIGZAG **SS** 1=RANDOM **SS** 2=MultiScroll **SS** 4=FadeInOut **SS** 5=FadeBox **SS** 6=FadeMask **SS** 7=FadeScroll **SS** 8=AutoColor	00h

Before screen saver select, do follow commands.

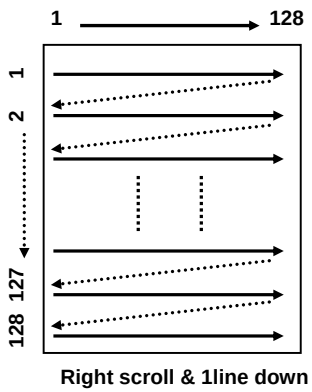
Time Step : S_Step_Timer and S_Step_Unit.
Move Step : S_Changing_Moviong_Step (X, Y).
Box : S_Box_Area (SX, SY, EX, EY).
Condition : S_Condition.

S_ZIGZAG

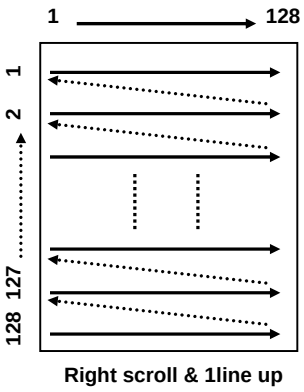
Zigzag mode screen saver.

Time Step	Move Step	Box	LO
Moving by pixel	1 pixel fixed	No relation	No relation

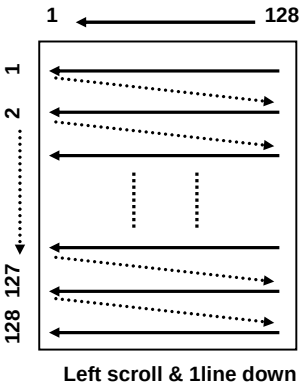
U	D	R	L	Meaning
1	-	1	-	Right Scroll and 1Line up
1	-	0	-	Left Scroll and 1Line up
0	-	1	-	Right Scroll and 1Line down
0	-	0	-	Left Scroll and 1Line down



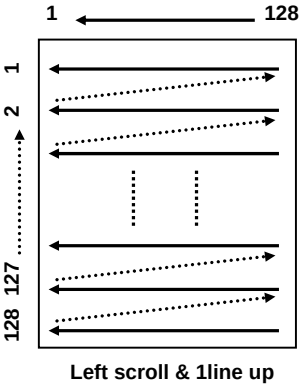
Right scroll & 1line down



Right scroll & 1line up



Left scroll & 1line down



Left scroll & 1line up

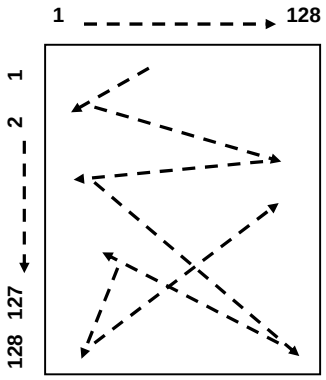
S_RANDOM

Random mode screen saver.

Time Step	Move Step	Box	LO
Moving by event	No relation	No relation	No relation

U	D	R	L	Meaning
-	-	-	-	-

Memory read address is randomized.



S_MULTISCROLL

Up/down/right/left scroll.

Time Step	Move Step	Box	LO
Moving by pixel	1 pixel fixed	No relation	No relation

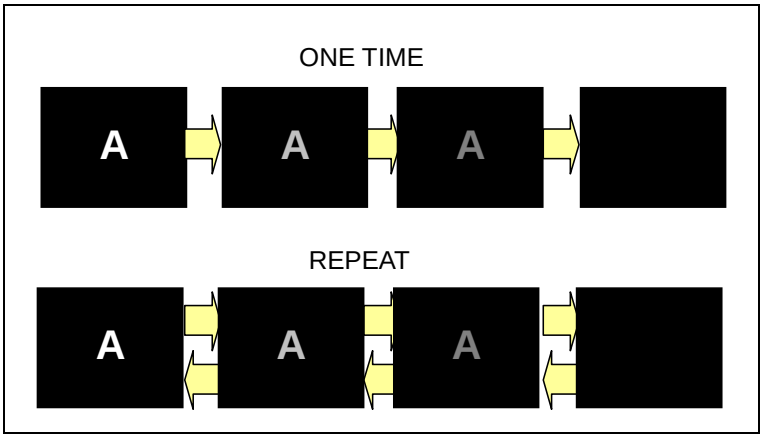
U	D	R	L	Meaning
1	0	0	0	Up Scroll
-	1	0	0	Down Scroll
-	-	1	0	Right Scroll
-	-	-	1	Left Scroll

S_FADEINOUT

Fade In means display become from dark to bright gradually.
Fade Out means display become from bright to dark gradually.

Time Step	Move Step (Current Step)	Box	LO
Changing Event period	0≤Iref≤3Fh 1 current step 40≤Iref≤7Fh 2 current step 80≤Iref≤BFh 3 current step C0≤Iref≤FFh 4 current step	No relation	0: One time 1: Repeat

U	D	R	L	Meaning
No relation				-

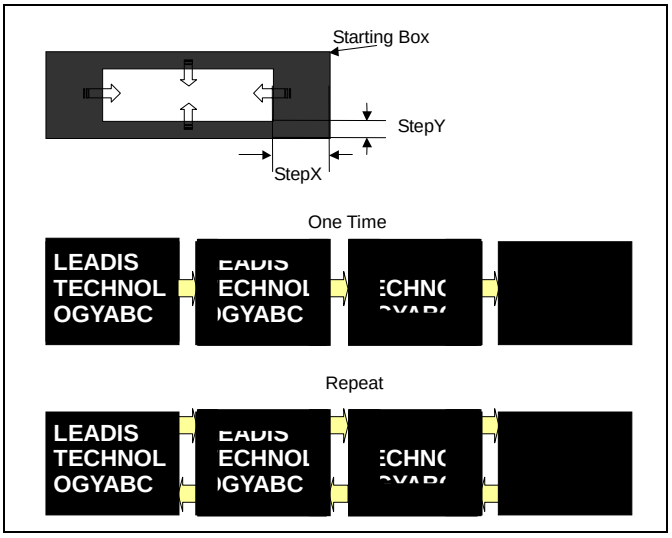


S_FADEBOX

"Fade Box" means display area is changing in box shape gradually.

Time Step	Move Step	Box	LO
Changing by event	Spreading or Shrinking Step	Starting Area or Point (Outside is black)	0: One time 1: Repeat

U	D	R	L	Meaning
No relation				-



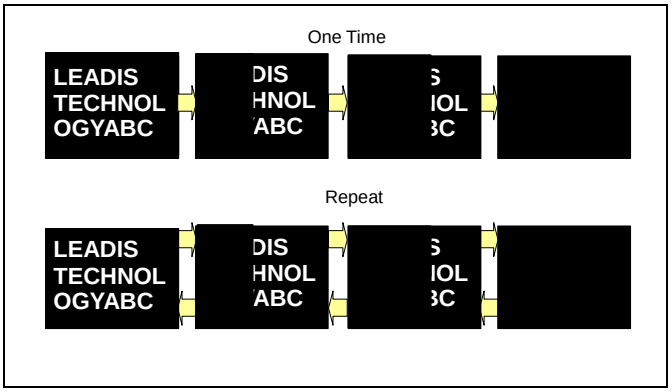
S_FADEMASK

Time Step	Move Step	Box	LO
Changing by event	1 Pixel pixed	No relation	0: One time 1: Repeat

Box is normally set display size.

U	D	R	L	Meaning
1	0	0	0	Up Scroll
-	1	0	0	Down Scroll
-	-	1	0	Right Scroll
-	-	-	1	Left Scroll

Display Sample

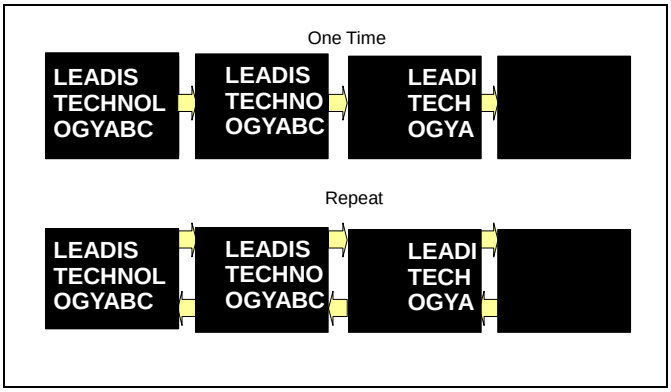


S_FADESCROLL

Time Step	Move Step	Box	LO
Changing by event	1 Pixel pixed	No relation	0: One time 1: Repeat

U	D	R	L	Meaning
1	0	0	0	Up Scroll
-	1	0	0	Down Scroll
-	-	1	0	Right Scroll
-	-	-	1	Left Scroll

Display Sample



S_AUTOCOLOR

Time Step	Move Step	Box	LO
Changing by event	No relation	No relation	No relation

U	D	R	L	Meaning
No relation				-

See color pallet and stage setting

SCREEN_SAVER_COLOR_STAGE & SCREEN_SAVER_COLOR_PALLET (19,1AH)

ColorPallet setting command for S_AutoColor.

SS : Screen Saver ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
SCOLSTG	W	L	-	19h						**SS** Color Stage Set	-
1st parameter	W	H	-	-	-	-	S2	S1	S0		00h
SCOLPAL	W	L	-	1Ah						**SS** Pallet Set	-
1st parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet0	07h
2nd parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet1	06h
3rd parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet2	05h
4th parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet3	04h
5th parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet4	03h
6th parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet5	02h
7th parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet6	01h
8th parameter	W	H	-	-	RV	-	R	G	B	RGB pallet data for pallet7	00h

S : Number of used color pallets, colors change loop in this pallet range .
Example) If S=2, then : Normal ⇒Pallet0⇒Pallet1⇒Pallet2⇒Normal…

Pallet Defaults

	(RV, R, G, B)
Pallet 0:	(0, 1, 1, 1)
Pallet 1:	(0, 1, 1, 0)
Pallet 2:	(0, 1, 0, 1)
Pallet 3:	(0, 1, 0, 0)
Pallet 4:	(0, 0, 1, 1)
Pallet 5:	(0, 0, 1, 0)
Pallet 6:	(0, 0, 0, 1)
Pallet 7:	(0, 0, 0, 0)

When RV ="1" : (Data EXOR "FFFFh") AND Pallet(RGB) ⇒ Output Data
When RV ="0" : Data AND Pallet(RGB) ⇒ Output Data

This command has priority than Data Reverse and Color Masking Command.

Sample:

Original Data (R, G, B)	Pallet (RV, R, G, B)	Output (R, G, B)
(1, 1, 1)	(0, 0, 0, 1)	(0, 0, 1)
(1, 1, 1)	(1, 0, 0, 1)	(0, 0, 0)
(1, 1, 0)	(0, 1, 0, 1)	(1, 0, 0)
(0, 0, 0)	(1, 1, 0, 1)	(1, 0, 1)

After data reversed, this command do color Masking.

ICON

ICON_DISPLAY_ON/OFF (20H)

ICON display on/off control.

IC : Icon ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
IDSPONOFF	W	L	-	20h						**IC** Display On/Off or Normal	-
1st parameter	W	H	-	-	-	-	-	D1	D0		00h

Parameter Definition

D[1:0]	Function	Initial
0	All ICON OFF.	Default
1	All ICON ON.	
2,3	Normal Display (depends on ICON DATA)	

ICON_STAND-BY_ON/OFF (21H)

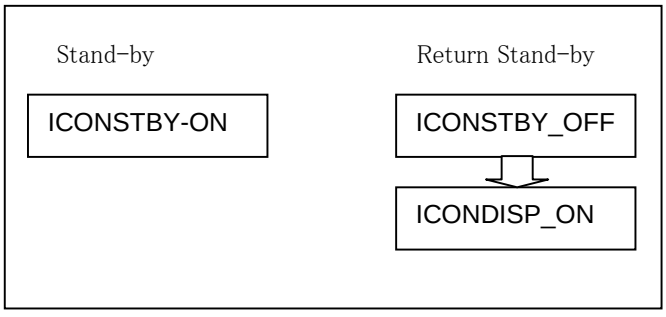
ICON stand-by on/off control.

IC : Icon ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
ISTBYONOFF	W	L	-	21h						**IC** Stand-by Setting	-
1st parameter	W	H	-	-	-	-	-	-	D0		01h

Parameter Definition

D0	Function	Initial
0	Start OSCB oscillation	
1	All ICON Display OFF Stop OSCB oscillation Stop inter DC-DC	Default



ICON_REG_SET/RESET (22H)

Set/reset the register for the ICONs.

IC : Icon ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
IREGSETRST	W	L	-	22h						**IC** Register Set/Reset	-
1st parameter	W	H	-	-	-	-	-	AD	SR		00h

AD is used for register selection.
AD = "0" Status Register. AD="1" Data Register

SR is used for Set/Reset selection.
SR = "0" Resister Reset. SR="1" Register Set.

ICON_REFERENCE_CURRENT (23H)

ICON current level set.

IC : Icon ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
ICONIREF	W	L	-	23h						**IC** Reference Current Set	-
1st parameter	W	H	-	-	-	I7	I6	I5	I4		00h
2nd parameter	W	H	-	-	-	I3	I2	I1	I0		00h

Current Setting Table

I[7：0]	ICON Current	UNIT
00h	0 (Default)	uA
01h	0.5	
02h	1.0	
:	:	
FEh	127.0	
FFh	127.5	

ICON_INITIALIZE (24H)

IC : Icon ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
ICONINIT	W	L	-	24h						**IC** Initialize	-
1st parameter	W	H	-	S5	S4	S3	S2	S1	S0	**IC** Status	00h
:	:	:	-	:	:	:	:	:	:		
56th parameter	W	H	-	S5	S4	S3	S2	S1	S0	**IC** Status	00h

This command set maximum current level to each Icon's Status and color.

If another command executes before all register input is done, it is effective at that point.

ICON output current table

S[5：0]	Output Current	UNIT
0	0 (Default)	uA
1	ICON_IREF * 1/63	
2	ICON_IREF * 2/63	
:	:	
62	ICON_IREF * 62/63	
63	ICON_IREF * 63/63	

ICONIREF is set value by setting "Icon_Reference_Current" command.

ICON_DATA_WRITE (25H)

IC : Icon ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
IDATAWR	W	L	-	25h						**IC** Data Write	-
1st parameter	W	H	-	-	-	-	-	-	D0		00h
2nd parameter	W	H	-	N5	N4	N3	N2	N1	N0		00h

Parameter	function	Range
N[5：0]	Register Indicate	0h~37h
D0	1⇒ON, 0⇒Off	0 or 1

Data register is initialized 0h.

ICON_BLINK_TIME (26H)

IC : Icon ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
IBLINKTIME	W	L	-	26h						**IC** Blink time	-
1st parameter	W	H	-	-	-	-	-	-	BS	**IC** Blink time set	00h
2nd parameter	W	H	-	T5	T4	T3	T2	T1	T0		00h

Parameter	Function	Range
BS	0 ⇒ Blinking disable (default) 1 ⇒ Blinking start	0 or 1

T[5 : 0]	1 Cycle Blinking Time	UNIT
0	0.1 (Default)	sec
1	0.2	
2	0.3	
:	:	
62	6.3	
63	6.4	

If BS=1(Blinking Start), no relation to the state of data register.
Refer to the command, Icon_Data_Write(25h).

If the number of blinking ICONs is more than one at BS=1,
Blinking timing of them must be synchronized.

After blinking disable, ICON display of disabled blink data must return to the state of data register.

ICON_BLINK_DATA (27H)

IC : Icon ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
IBLINKDATA	W	L	-	27h						**IC** Blink data	-
1st parameter	W	H	-	-	-	-	-	-	BD	**IC** Blink data set	00h
2nd parameter	W	H	-	B5	B4	B3	B2	B1	B0		00h

Parameter	Function	Range
BD	0⇒Blinking data disable (default) 1⇒Blinking data enabel	0 or 1
B [5:0]	Blink data register indication	00 ~ 37h

ICON_ROW_HIGH_PERIOD (28H)

IC : Icon ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
IROWHIGH	W	L	-	28h						**IC** Row High Period Set	-
1st parameter	W	H	-	-	-	-	L2	L1	L0		00h

L[2：0]	Period	UNIT
0	0/64 (Default)	cycle
1	1/64	
2	2/64	
:	:	
6	6/64	
7	7/64	

One Cycle is 1/(Frame Frequency) set ICON Frame command.

ICON_DC-DC_CONTROL (29H)

IC : Icon ,"-": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
ICONDCDC	W	L	-	29h						**IC** DC-DC Control Set	-
1st parameter	W	H	-	-	-	-	-	M1	M0		01h

M[1:0]	FUNCTION	INIT
01	Stop DC-DC Supply power from VICON directly	Default
10	Start DC-DC Supply power from inner DC-DC	
00/11	Don't use	

ICON_FRAME_FREQUENCY (2AH)

IC : Icon ,"**-**": Don't care

Instruction	W/R	A0	D17 - D6	D5	D4	D3	D2	D1	D0	Function	Default
IFRAME	W	L	-	2Ah						**IC** Frame Frequency Set	-
1st parameter	W	H	-	-	-	-	F2	F1	F0	**IC** Blink data set	02h

F[2 : 0]	Frame Frequency	UNIT
0	60	Hz
1	75	
2	90 (Default)	
3	105	
4	120	
5	135	
6	150	
7	165	

External Display Interface

RGB INTERFACE

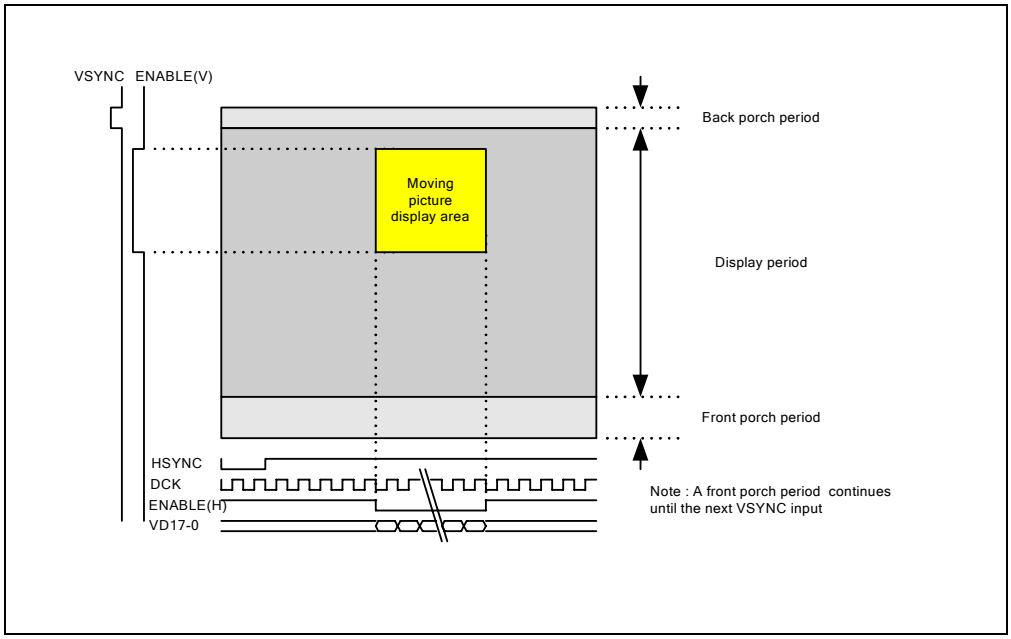
The following interfaces are available as an external display interface(RGB interface). The RGB interface is selected by setting RM1-0 registers. RAM is accessible through RGB interface.

RGB Interface Selection

RM1	RM0	RGB Interface	VD Pin
0	0	18-bit RGB Interface	VD17-0
0	1	16-bit RGB Interface	VD17-13, VD11-1
1	0	6-bit RGB Interface	VD5-0 or VD17-12
1	1	Setting disabled	-

Note 1) RGB interface are not able to be used simultaneously.

Display operation through the RGB Interface are synchronized with VSYNC, HSYNC, and DCK. With combined use of window addresses, RGB interfaces are able to transmit display data and only overwrite a moving picture display area in high speed with low power consumption. RGB interfaces require settings of front, back porch periods and display periods.



Timing example of External Display Interface

Note)

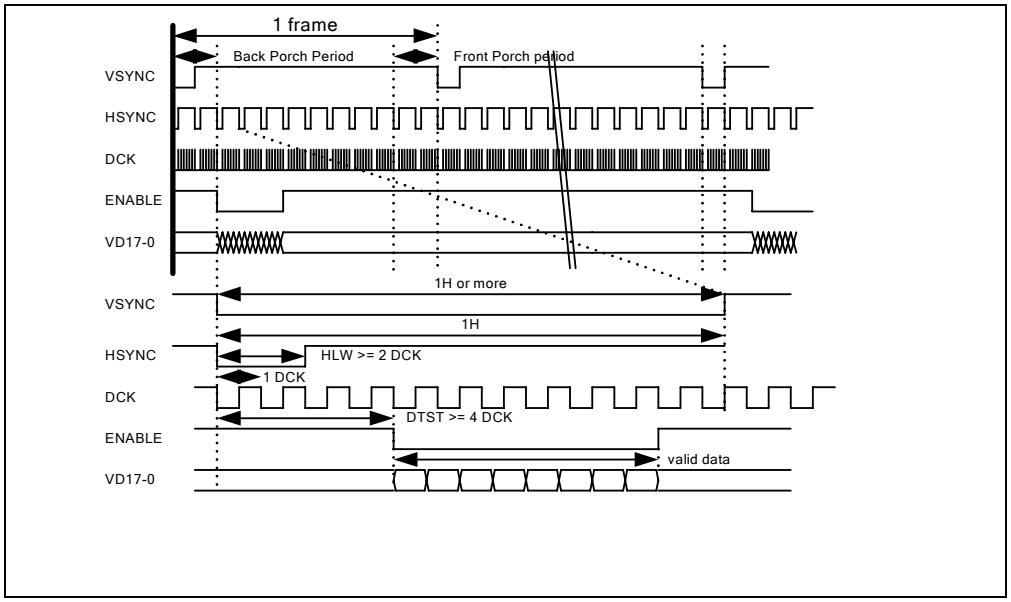
VSYNC : Frame synchronization signal
HSYNC : Raster-row synchronization signal
DCK : Dot clock
ENABLE : Data enable signal
VD17-0 : RGB(6:6:6)display data

Back porch period (BPP) : 14H >= BP >= 2H
Front porch period (FPP) : 14H >= FP >= 2H
FPP+BPP = 16H
Display Period 128H + BPP + FPP

Polarities of VSYNC, HSYNC, ENABLE, DCK signals

The polarities of VSYNC, HSYNC, DCK, ENABLE signals are changeable by instruction settings(PV, PH, PC, PE, and PO) according to a system in use.

Timing chart of 16/18-bit RGB interface mode



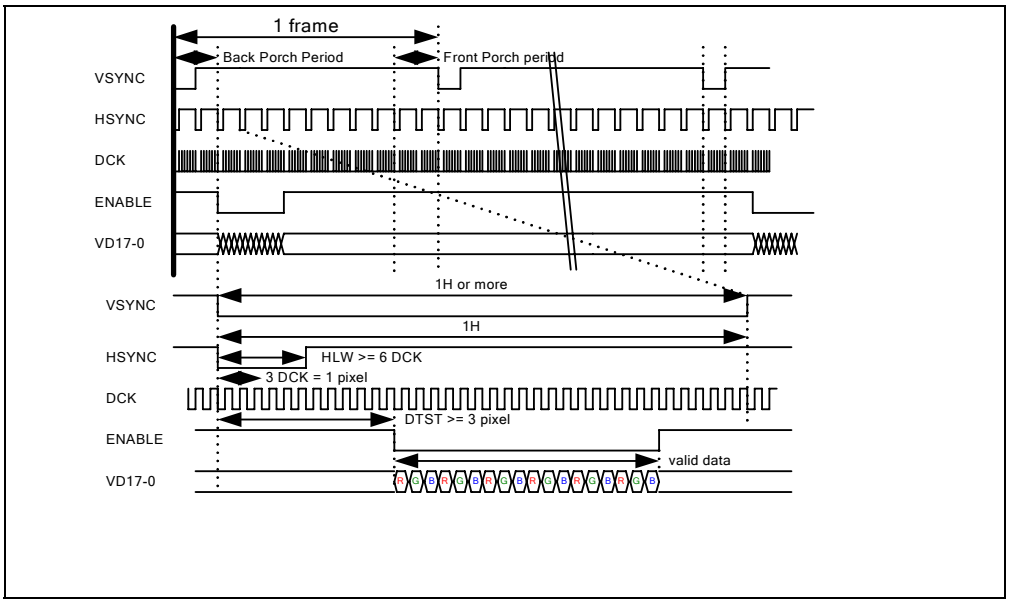
Timing chart for 16/18 bit RGB interface

Note 1) VLW: VSYNC "Low" period

HLW: HSYNC "Low" period

DTST: set up time for data transfer

Timing of 6-bit RGB Interface mode



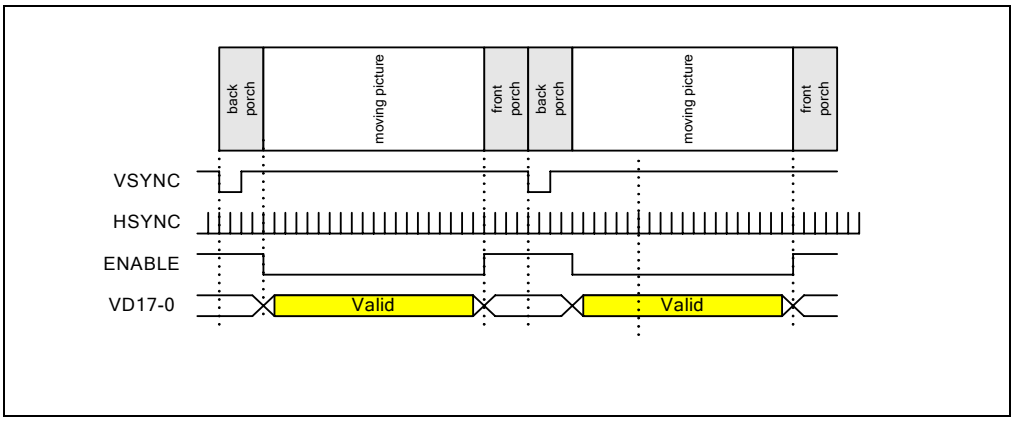
Timing chart for 6-bit RGB interface

Note 1) VLW: VSYNC "Low" period

HLW: HSYNC "Low" period

DTST: set up time for data transfer

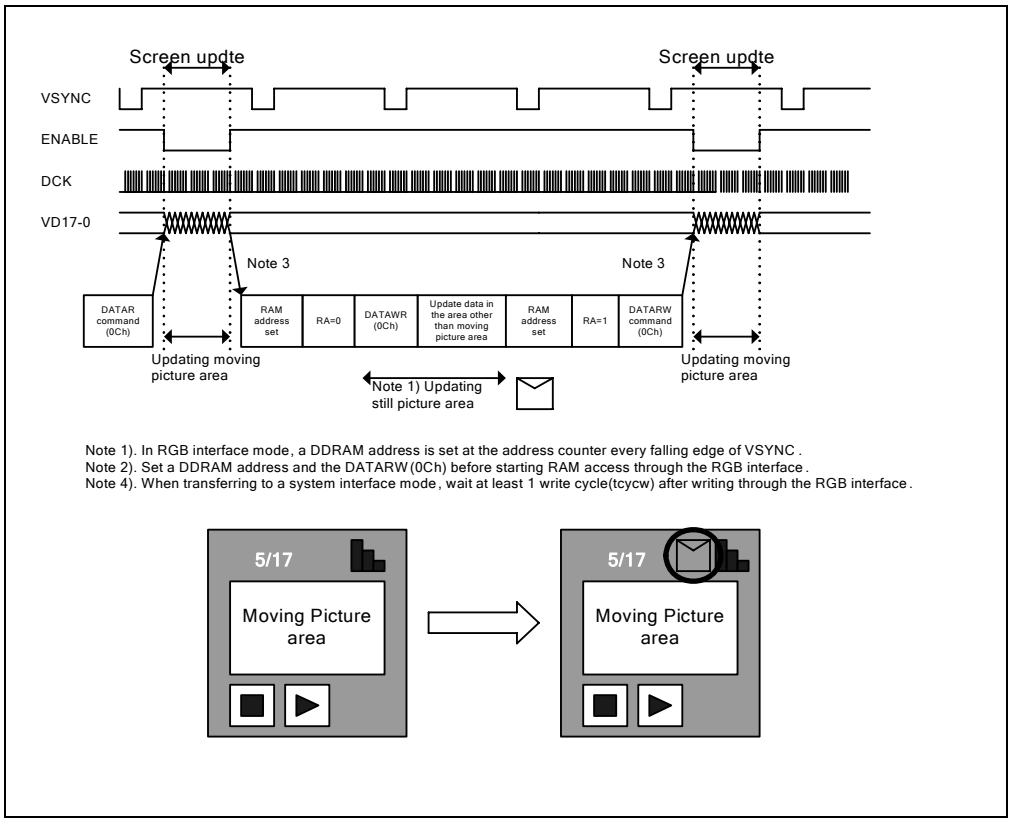
Note 2) Transmit each VSYNC, HSYNC, ENABLE, DCK, and VD5-0 or VD17-12 in 3 clocks



RAM access through a MPU interface in RGB-I/F mode

RAM is accessible through a MPU interface while using an RGB interface. In RGB interface mode, data are written to RAM in synchronization with DCK inputs while ENABLE is “Low”. When writing data to RAM through a MPU interface, it is necessary to set ENABLE “High” to stop writing data through the RGB interface. To set RA=0, RAM is accessible through a MPU interface. When reverting to the RGB interface mode, wait for a read/write bus cycle. Then, set RA = 1 and the instruction command DATARW (0Ch) to start RAM access though the RGB interface. When RAM write operations through the RGB and MPU interfaces conflict. There is no guarantee that data are properly written to RAM.

The following is an example of a moving picture display through the RGB interface while updating a still picture area through the MPU interface.

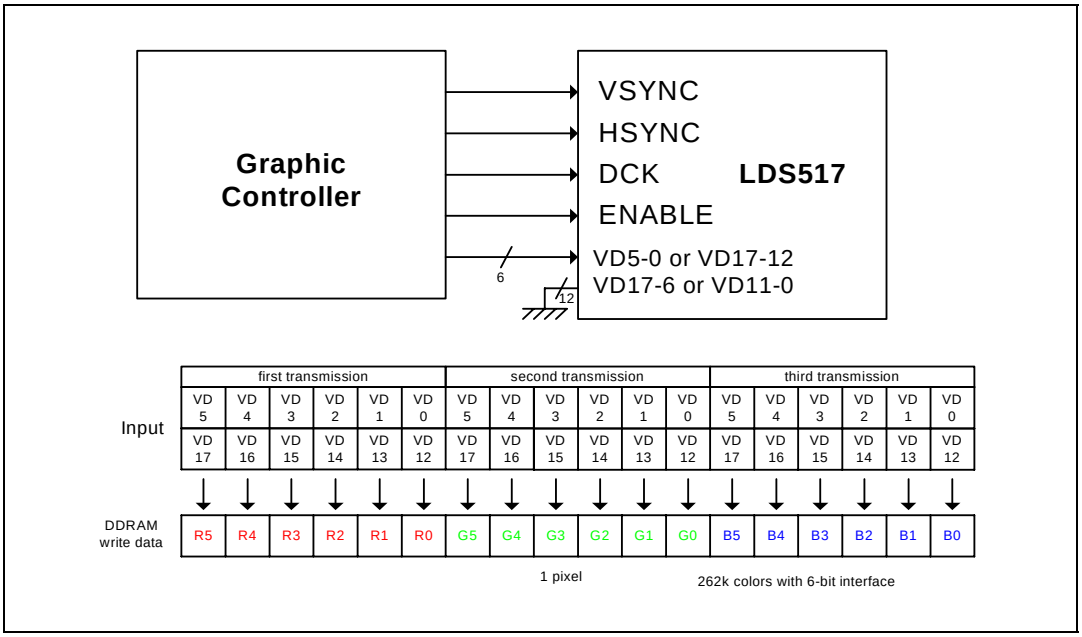


Updating still picture area during moving picture display

6-bit RGB Interface

The 6-bit RGB interface is selected by setting RM1-0 bits to “00”. Display operations are synchronized with VSYNC, HSYNC, and DCK signals. Display data are transmitted to RAM in synchronization with display operation through 6-bit RGB data bus(VD5-0 or VD17-12) according to the data enable signal(ENABLE). Unused pins(VD17-6 or VD11-0) must be fixed to either VDD or GND level.

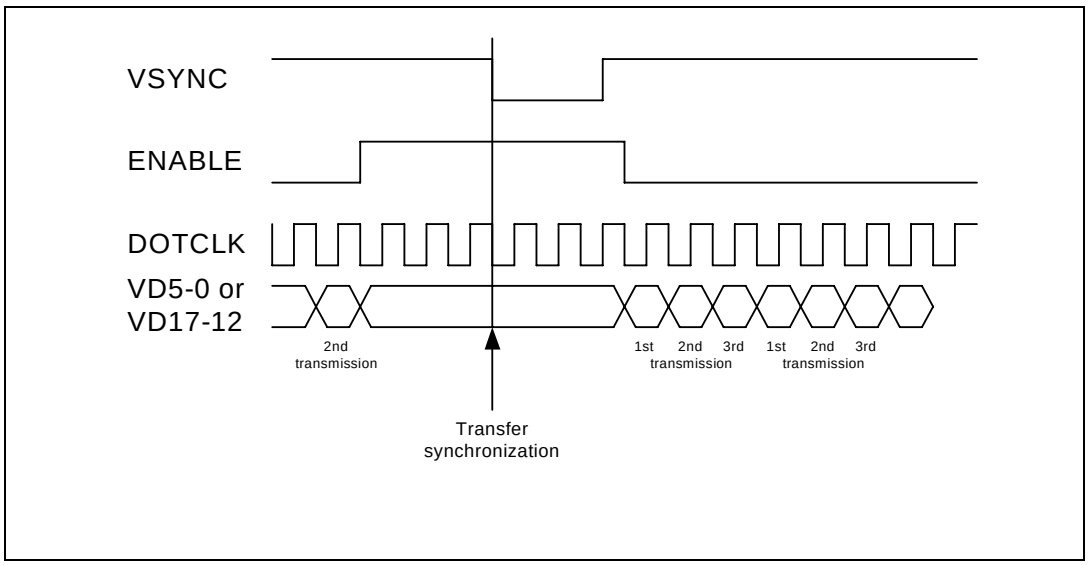
Instructions are set only through a MPU interface.



Example of 6-bit RGB Interface and data format

Transfer synchronization function for a 6-bit bus interface

The LDS517 incorporates a transmission counter to count the first, second, third data transmissions in 6-bit RGB interface mode. The transmission counter is always reset to the first transmission on falling edge of the VSYNC. If there are discrepancies in the timing of transferring first, second and third data, the counter is reset to the first data transmission at the start of each frame (falling edge of VSYNC and data transmission restarts in the correct timing from the next frame. In case of displaying moving pictures, which requires consecutive data transfer, this function minimizes the effect from discrepancies in the data transfer timing and facilitates the display system to return to normal.

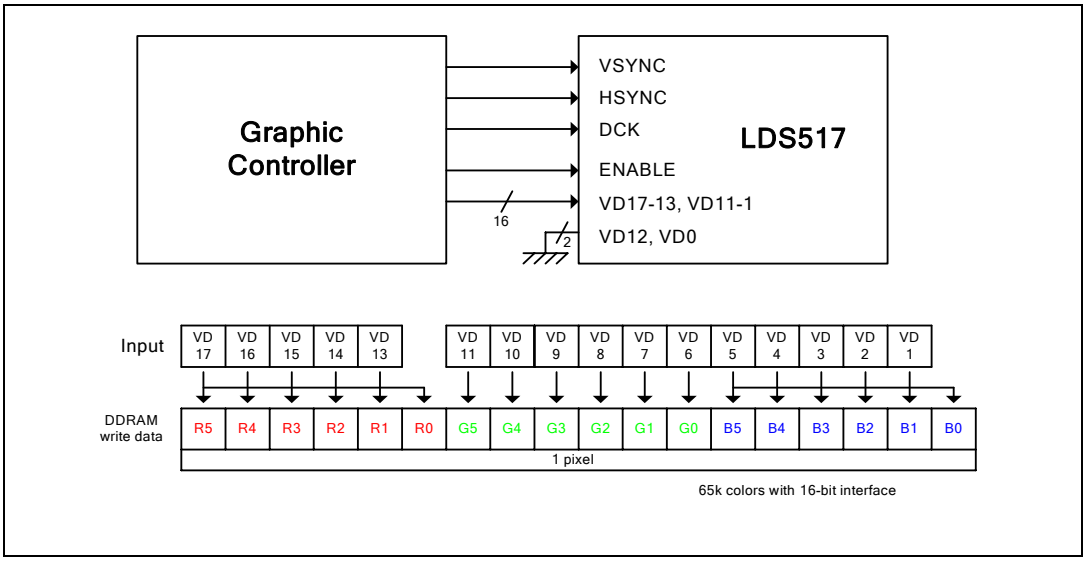


6-bit Transfer Synchronization

16-bit RGB Interface

The 16-bit RGB interface is selected by setting RM1-0 bits to “01”. Display operations are synchronized with VSYNC, HSYNC, and DCK signals. Display data are transmitted to RAM in synchronization with display operation through 16-bit RGB data bus(VD17-13, VD11-1) according to the data enable signal(ENABLE).

Instructions are set only through a MPU interface.

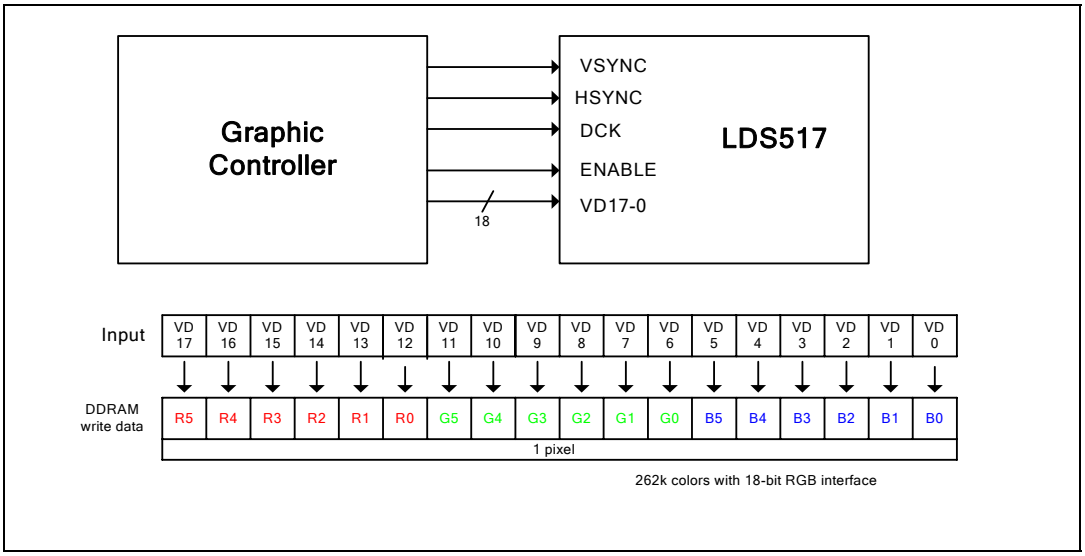


Example of 16-bit RGB Interface and data format

18-bit RGB Interface

The 18ps-bit RGB interface is selected by setting RM1-0 bits to “10”. Display operations are synchronized with VSYNC, HSYNC, and DCK signals. Display data are transmitted to RAM in synchronization with display operation through 18-bit RGB data bus(VD17-0) according to the data enable signal(ENABLE).

Instructions are set only through a MPU interface.

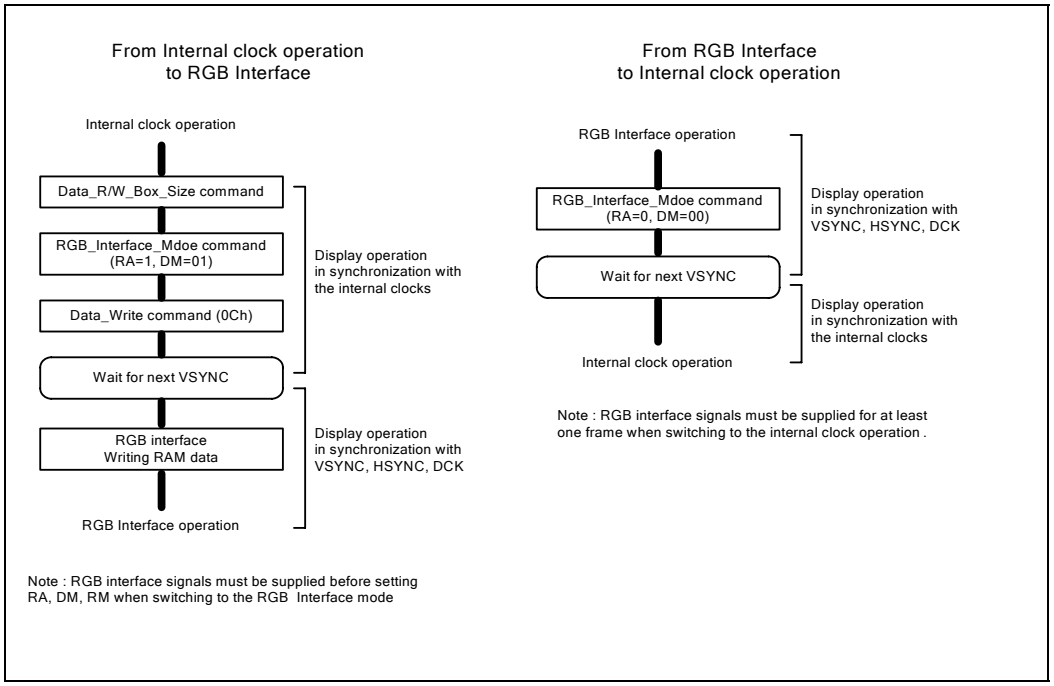


Example of 18-bit RGB Interface and data format

Notes to the external display interface

1. VSYNC, HSYNC, and DCK signals must be supplied throughout display operations using an RGB interface.
2. In RGB Interface mode, the reference clocks are all DCK, not internal operation clocks.
3. In 6-bit RGB Interface mode, transmission of RGB (pixel) is executed in three clocks.
4. To switch between internal operation mode and external display interface mode, follow the sequences of the following transitional flowcharts.
5. In RGB Interface mode, a front porch period continues after completion of one frame until the next VSYNC input.
6. In RGB Interface mode, RAM address set is executed every frame on falling edge of VSYNC.

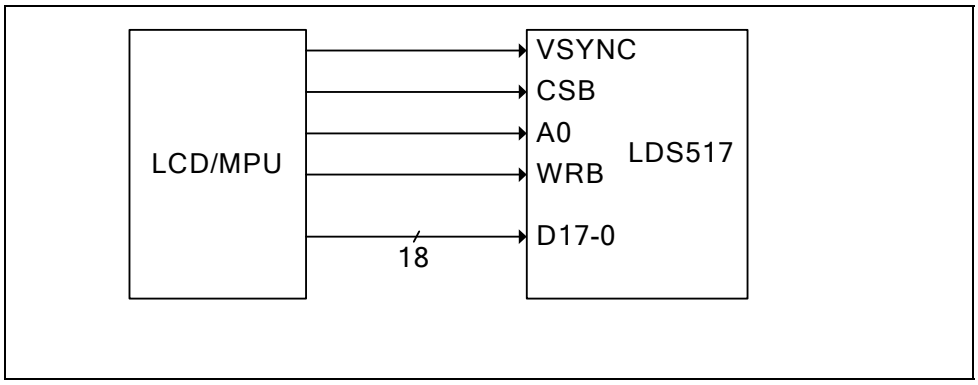
The sequences of transitional flowchart



The sequences of transitional flowchart

VSYNC Interface

The LDS517 incorporates a VSYNC Interface, which enables a MPU interface to display a moving picture by using only a frame synchronization signal (VSYNC). In other words, the VSYNC interface facilitates moving picture display with minimum modification to a conventional system.



VSYNC Interface

VSYNC interface mode is selected by setting DM1-0 = 10 and RA = 0. In VSYNC interface mode, internal display operations are synchronized with VSYNC. The VYSNC interface enables to display a moving picture through a MPU interface and update screens without flicker by writing data to RAM through a MPU interface in higher speed than the internal display operations by some degree.

The VSYNC interface executes display operations only with internal clocks generated by internal oscillators and VSYNC input. All display data are stored in RAM so that only the data relevant to updating a screen are transferred to minimize data transmission while displaying a moving picture.

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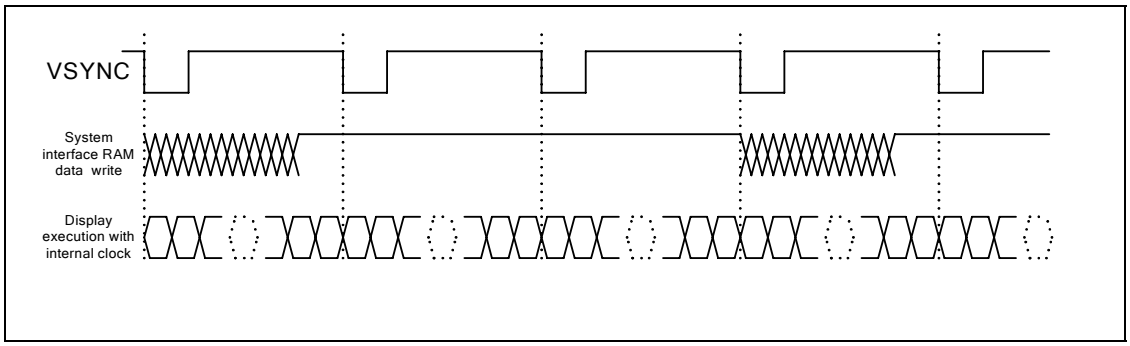
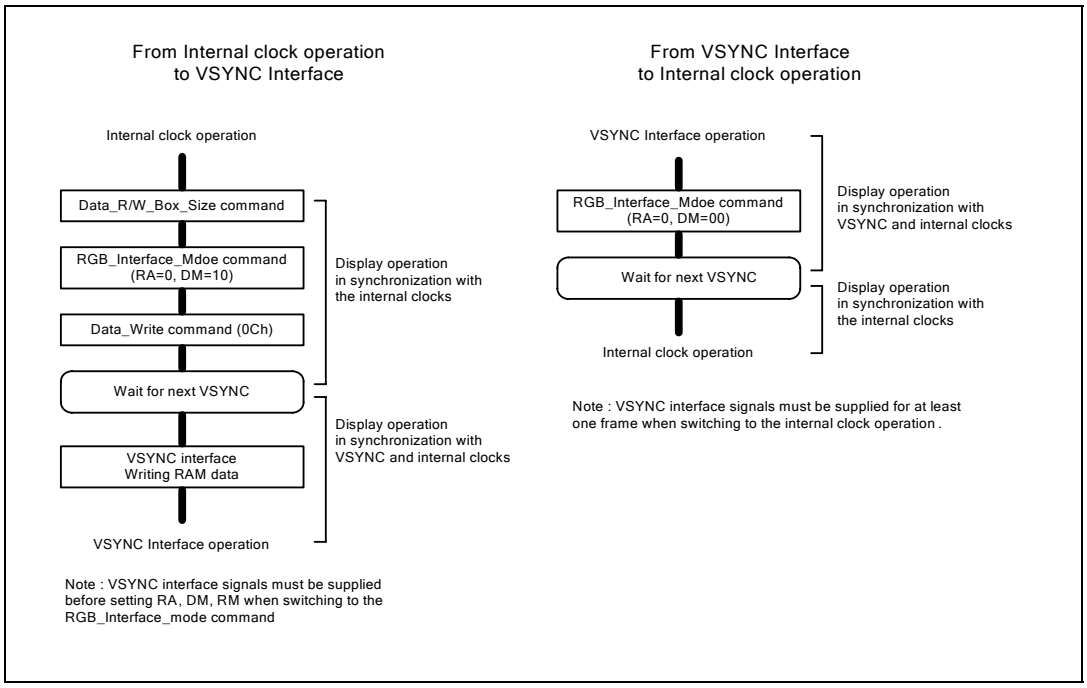


Moving picture data transmission through VSYNC interface

The sequences of transitional flowchart



Transition between VSYNC and Internal clock operation modes

DRIVER TIMING

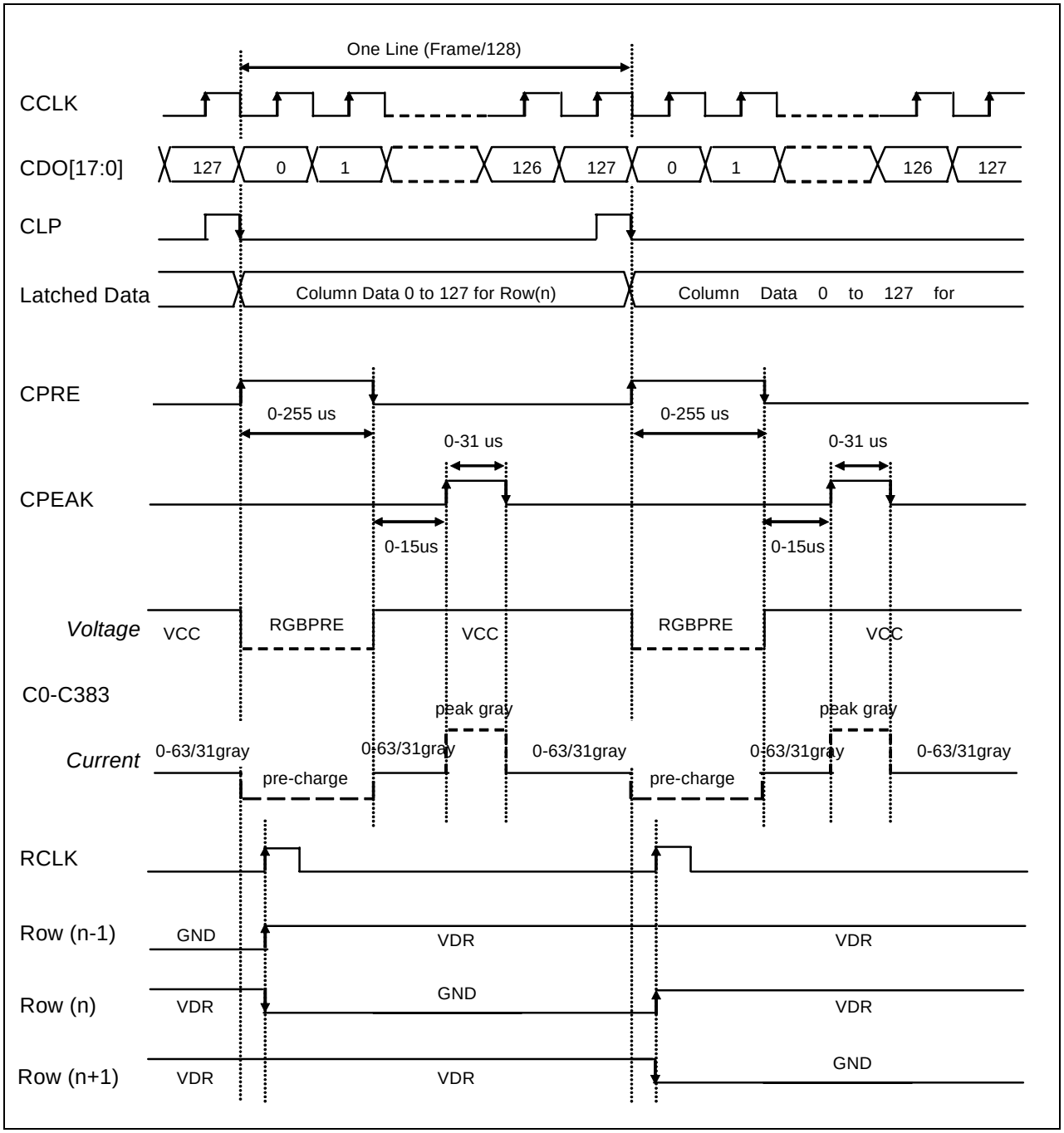


Figure 5. Driver timing diagram

SPECIFICATIONS

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage (1)	V_{DD}	- 0.3 ~ + 4.0	V
Supply voltage (2)	V_{DC}	- 0.3 ~ + 23.0	V
	VDR		
Supply voltage (3)	V_{BATT}	- 0.3 ~ + 5.0*1)	V
	V_{ICON}	- 0.3 ~ + 23.0*2)	V
Input voltage range	V_{IN}	- 0.3 ~ V_{DD} + 0.3	V
Output voltage range	V_{OUT}	- 0.3 ~ V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 40 ~ + 85	°C
Storage temperature range	T_{STG}	- 50 ~ + 100	°C

NOTICE:

1. VDD, VDC, VDR are based on VSS = 0V.

2. Voltage relationship VCC/VDR ≥ VDD ≥ VSS must always be satisfied.

*3. *1): When using the inner DC-DC (two times VBATT) for ICON driver.*

**2): When using the external VICON directly for ICON driver.*

DC Characteristics

BASIC CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 1.65 to 2.0V/2.3 to 3.3V, Ta = 25°C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
V_{DD}	Logic operating voltage	-	VDD	1.65	1.8	2.0	V
				2.3	2.8	3.3	
V_{DC}	Column operating voltage	-	VDC	10	15	21.0	
V_{DR}	Row operating voltage		VDR	10	15	21.0	
V_{BATT}	ICON operating voltage1	When using the inner DC-DC for ICON	VBATT	3.2	3.8	4.2	
V_{ICON}	ICON operating voltage2	When using the external V_{ICON} directly for ICON	VICON	3.2	6	21.0	
V_{IH}	High logic input voltage	-	*1)	0.7V_{DD}	-	V_{DD}	
V_{IL}	Low logic input voltage	-	*1)	V_{SS}	-	0.3V_{DD}	
V_{OH}	High logic output voltage	I_{OH} = -0.1mA	*2)	0.85V_{DD}	-	V_{DD}	
V_{OL}	Low logic output voltage	I_{OL} = +0.1mA	*2)	V_{SS}	-	0.15V_{DD}	
I_{IL}	Input leakage voltage	V_{IN} = V_{DD} or V_{SS}	*1)	-1.0	-	+1.0	μA
F_{OSC1}	Oscillator frequency for Dot matrix	VDD =2.8V	OSCA2	2.7	3	3.3	MHz
F_{OSC2}	Oscillator frequency for ICON	VDD =2.8V	IC Test Pin	9.2	11.5*3)	13.8	KHz

NOTICE:

**1) Applies to PS, C80, RSTB, A0 CSB, WRB, RDB and D17 to D0 pins.*

**2) Applies to D17 to D0 pins.*

**3) ICON Frame frequency = 90Hz.*

DRIVER CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 1.65 to 2.0V/2.3 to 3.3V, V_{CC} =15V, Ta = 25°C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
RPRE	Dot column driver pre-charge on resistance	*1)	C0 to C383	-	0.2	0.5	kΩ
RICONL	ICON column driver low level on resistance	-	IC0 to IC55	-	0.2	0.5	kΩ
RROWL	Row driver low level on resistance	IOL = 50mA	R0 to R127 IR0 to IR3	-	10	20	Ω
RROWH	Row driver high level on resistance	IOH = -1mA		-	1	3	kΩ
ICPTP1	Output current pin to pin deviation*2)	REFCNT = 63'd IREFCNT =127'd	C0 to C383 IC0 to IC55	T.B.D	-	T.B.D	%
ICPTP2	Output current pin to pin deviation*2)	REFCNT = 191'd	C0 to C383	T.B.D	-	T.B.D	%
ICPTP3	Peak current pin to pin deviation*2)	IOUTPeak = T.B.D uA	C0 to C383	T.B.D	-	T.B.D	%
ICALP1	Output current all pin deviation*3)	REFCNT = 63'd IREFCNT =127'd	C0 to C383 IC0 to IC55	T.B.D	-	T.B.D	%
ICALP2	Output current all pin deviation*3)	REFCNT = 191'd	C0 to C383	T.B.D	-	T.B.D	%
ICALP3	Peak current all pin deviation*3)	IOUTPeak = T.B.D uA	C0 to C383	T.B.D	-	T.B.D	%
ICALP4	Peak current all pin relative deviation*4)	IOUTPeak = T.B.D uA	C0 to C383	T.B.D	-	T.B.D	%
ICCHIP1	Output current absolute correctness*5)	REFCNT = 63'd IREFCNT = 127'd	C0 to C383 IC0 to IC55	T.B.D	-	T.B.D	%
ICCHIP2	Peak current absolute correctness*5)	IOUTPeak = T.B.D uA	C0 to C383	T.B.D	-	T.B.D	%
IDD1	Stand-by current	-	VDD(1.65-2.0)	-	1	5	μA
			VDD(2.3-3.3)	-	1	5	
ICC1			VCC	-	1	5	
IBATT1			VBATT	-	1	5	
IDD2	Normal operating current	*6)	VDD(1.65-2.0)	T.B.D	-	T.B.D	mA
			VDD(2.3-3.3)				
ICC2			VCC	T.B.D	-	T.B.D	
IBATT2			VBATT	T.B.D	-	T.B.D	
VICON	VICON output voltage	VBATT=3.8V, IICON=4mA	VICON	6.0	-	-	V
		VBATT=3.2V, IICON=4mA		5.0	-	-	

NOTICE:

**1) Pre-charge voltage = T.B.D V.*

**2) RED ~ DOT: (IN – IN+1) / IREF (SPEC): N = 0,3,…, 381*
GREEN ~ DOT: (IN – IN+1) / IREF (SPEC): N = 1,4,…, 382
BLUE ~ DOT: (IN – IN+1) / IREF (SPEC): N = 2,5,…, 383
ICON: (IN – IN+1) / IREF (SPEC): N = 0 to 55

**3) RED ~ (IMAX[RED] – IMIN[RED]) / IREF (SPEC)*
GREEN ~ (IMAX[GREEN] – IMIN[GREEN]) / IREF (SPEC)
BLUE~ (IMAX[BLUE] – IMIN[BLUE]) / IREF (SPEC)

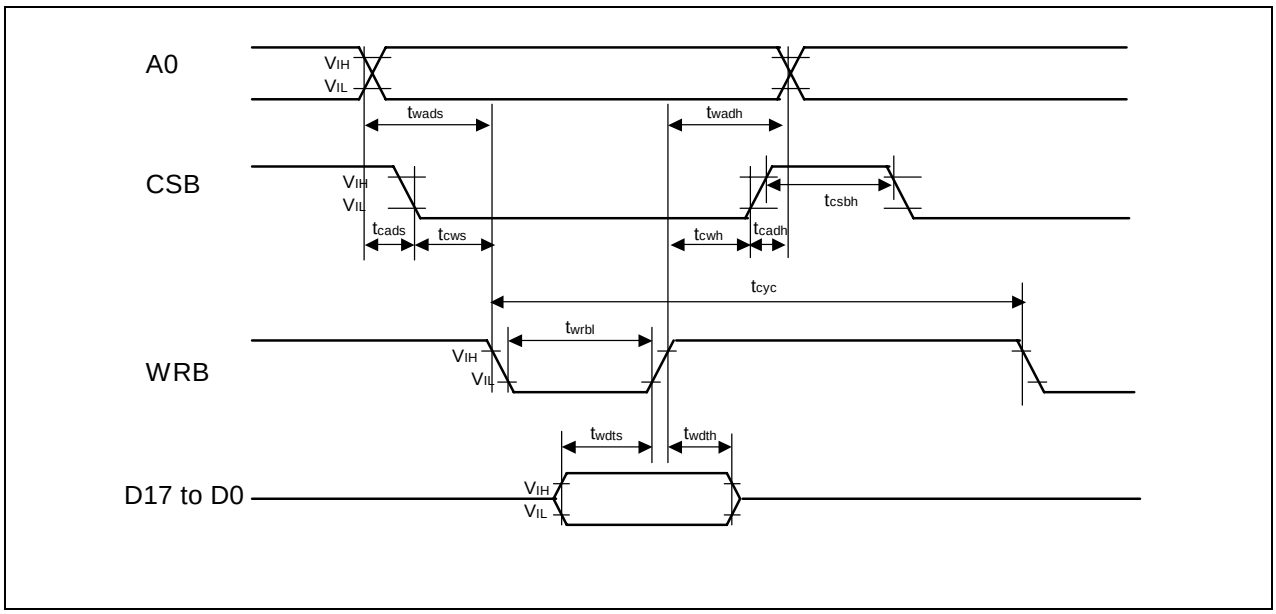
**4) RED ~ Max {(IN – IAVG) / IAVG}: N = 0,3,…, 381, IAVG = Σ (IN) / 128: N = 0,3,…, 381*
GREEN ~ Max {(IN – IAVG) / IAVG}: N = 1,4,…, 382, IAVG = Σ (IN) / 128: N = 1,4,…, 382
BLUE ~ Max {(IN – IAVG) / IAVG}: N = 2,5,…, 383, IAVG = Σ (IN) / 128: N = 2,5,…, 383

**5) (IAVG – IREF (SPEC)) / IREF (SPEC)*

**6) Iout = 10μA, Dot display data = 111111_111111_11111b, All ICON ON, Frame Frequency 120Hz,*
VDD=1.8V/2.8V, VBATT=3.8V,
Output all open, Display size full, Others Default

AC Characteristics

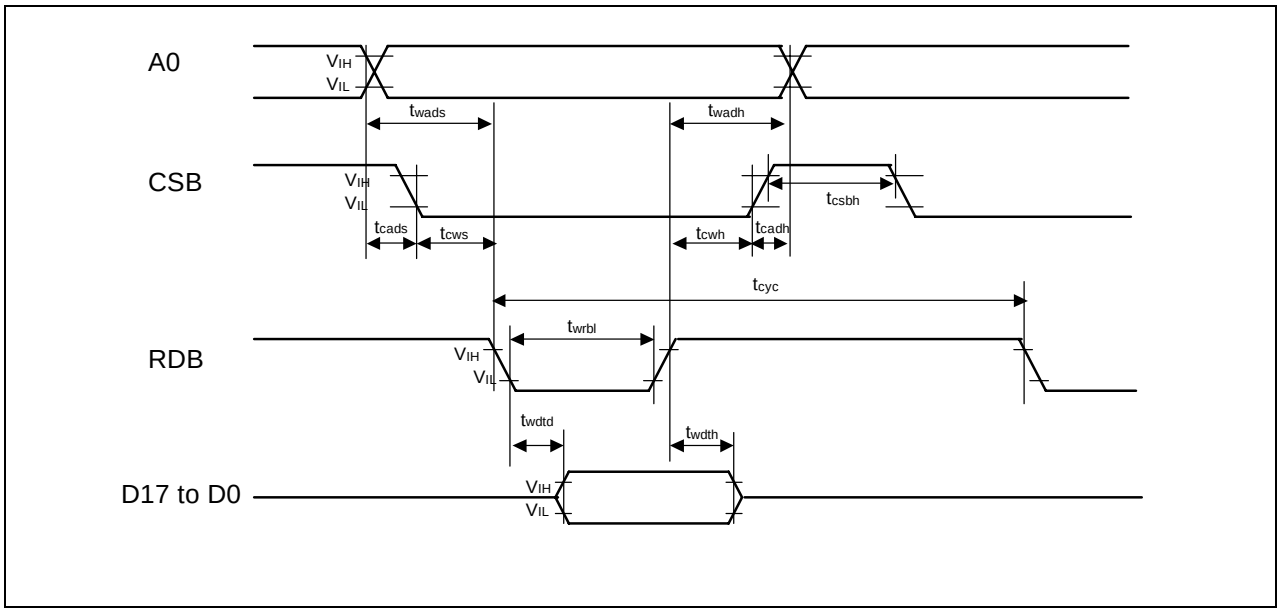
WRITE CHARACTERISTICS



(VDD = 1.8V/2.8V, Ta = 25 °C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{cyc}	Write cycle time	-	WRB	100	-	-	ns
t_{cads} t_{cadh}	Address and Select setup time Address and Select hold time	-	CSB,A0	0 0	- -	- -	ns
t_{wads} t_{wadh}	Address setup time Address hold time	-	A0	50 20	- -	- -	ns
t_{cws} t_{cwh}	Select setup time Select hold time	-	CSB	10 10	- -	- -	ns
t_{wrbl}	Write Low pulse width	-	WRB	30	-	-	ns
t_{csbh}	Select High pulse width	-	CSB	10	-	-	ns
t_{wdts} t_{wdth}	Data setup time Data hold time	-	D17 to D0	10 20	- -	- -	ns

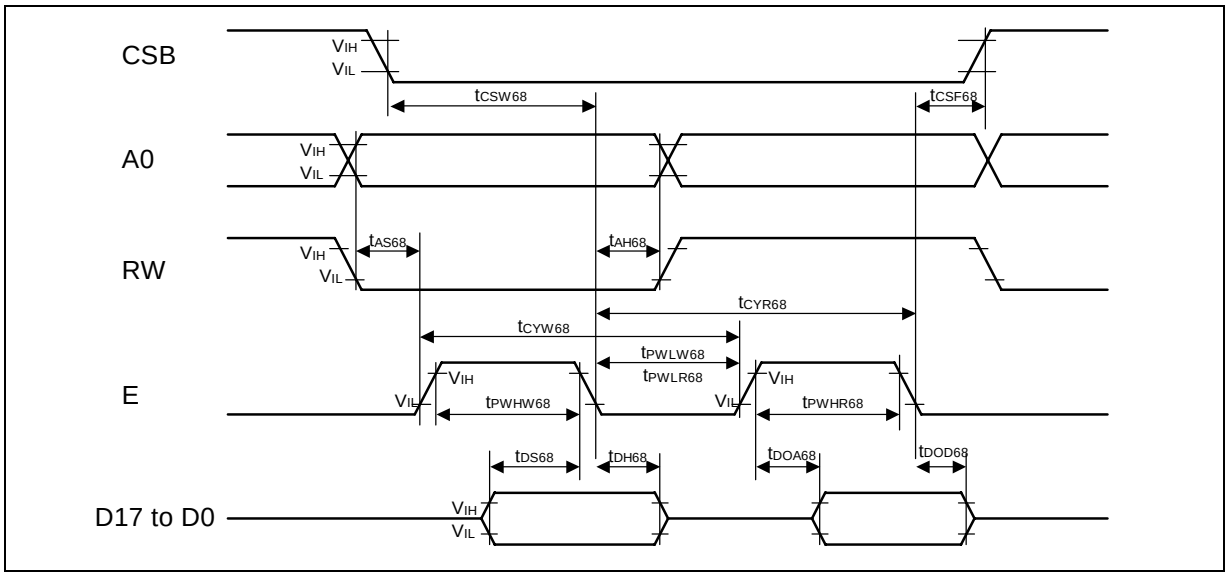
READ CHARACTERISTICS



(VDD = 1.8V/2.8V, Ta = 25 °C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{cyc}	Read cycle time	-	RDB	500	-	-	ns
t_{cads} t_{cadh}	Address and Select setup time Address and Select hold time	-	CSB,A0	0 0	- -	- -	ns
t_{rads} t_{radh}	Address setup time Address hold time	-	A0	50 20	- -	- -	ns
t_{crs} t_{crh}	Select setup time Select hold time	-	CSB	10 10	- -	- -	ns
t_{rdbl}	Read Low pulse width	-	RDB	250	-	-	ns
t_{csbh}	Select High pulse width	-	CSB	10	-	-	ns
t_{rdtd} t_{rdth}	Data output delay time Data output hold time	CL = 100pF	D17 to D0	- 5	- -	200 -	ns

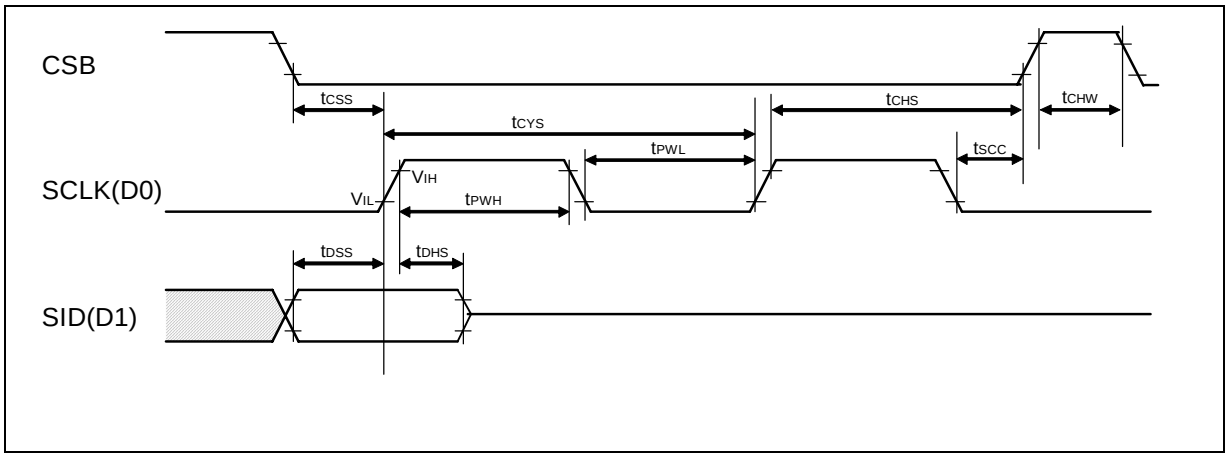
PARALLEL INTERFACE CHARACTERISTICS (6800-SERIES MPU)



(VSS=0V, VDD=1.8V/2.8V,Ta = 25°C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CSW68} t_{CSF68}	Chip select setup time Chip select hold time	-	CSB	10 10	- -	- -	ns
t_{AS68} t_{AH68}	Address setup time Address hold time	-	A0 RW	50 20	- -	- -	ns
t_{CYW68} t_{PWHW68} t_{PWLW68}	Write cycle time Write High Time Write Low Time	-	E	160 40 90	-	-	ns
t_{CYR68} t_{PWHR68} t_{PWLR68}	Read cycle time (Parameter read) Read High (Parameter read) Read Low (Parameter read)	-	E	160 40 90	-	-	ns
t_{CYR68} t_{PWHR68} t_{PWLR68}	Read cycle time (Data read) Read High (Data read) Read Low (Data read)	-	E	450 355 90	-	-	ns
t_{DS68} t_{DH68}	Data setup time Data hold time	-	D17 to D0	10 20	- -	- -	ns
t_{DOA68} t_{DOD68}	Data output access time Data output disable time	CL = 30pF		- 40	- -	40 80	ns

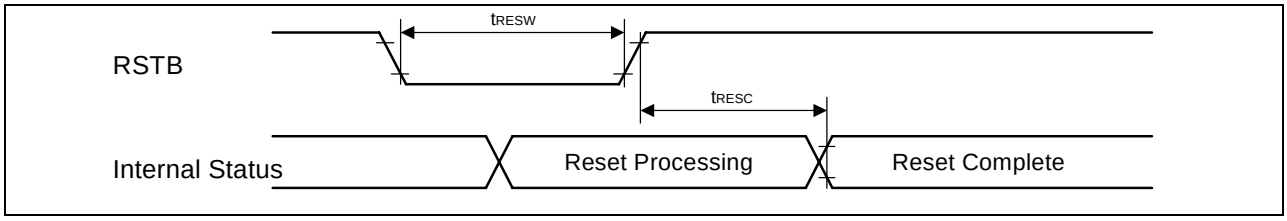
SERIAL INTERFACE CHARACTERISTICS



(VSS=0V, VDD=1.8V/2.8V,Ta = 25°C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CYS} t_{WHS} t_{WLS}	Serial clock cycle High pulse width Low pulse width	-	SCLK(D0)	160 60 60	- -	- -	ns
t_{DSS} t_{DHS}	Data setup time Data hold time		SID (D1)	60 60	- -	- -	ns
t_{CSS} t_{CHS} t_{CHW}	Chip select setup time Chip select hold time Chip select high pulse width	-	CSB	60 65 45	- - -	- - -	ns
t_{SCC}	SCLK to Chip select	-	SCLK, CSB	20	-	-	ns

RESET INPUT TIMING



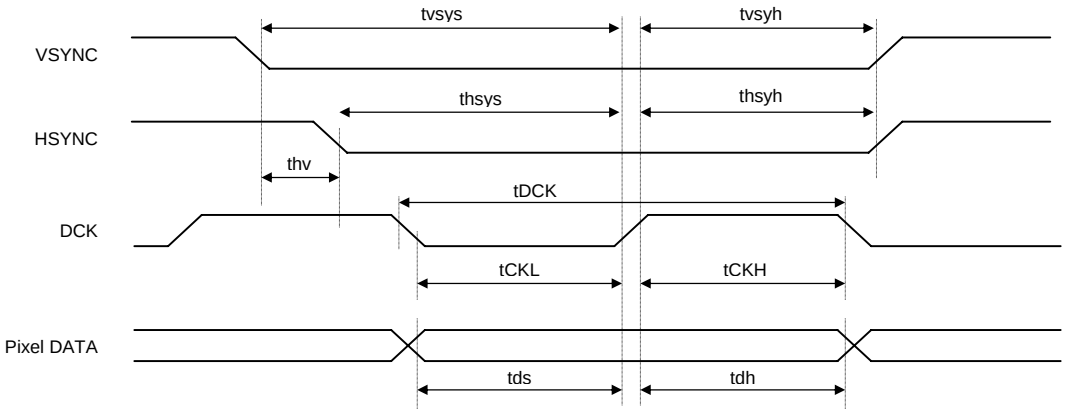
(VDD = 1.8V/2.8V, Ta = 25 °C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{RESW}	Reset low pulse width	-	RSTB	1000	-	-	ns
t_{RESC}	Reset complete time	-	-	-	-	1000	ns

RGB INTERFACE TIMING

Characteristics	Symbol	Min.	Typ.	Max.	Unit
DCK Frequency	fDCK	2.51	2.64	2.77	MHz
DCK Period	tDCK	398	379	361	nSec
DCK Low Period	tCKL	150			nSec
DCK High Period	tCKH	150			nSec
Vertical Sync Setup Time	tvsys	30			nSec
Vertical Sync Hold Time	tvsyh	30			nSec
Horizontal Sync Setup Time	thsys	30			nSec
Horizontal Sync Hold Time	thsyh	30			nSec
Phase difference of Sync Signal Falling Edge	thv	0		176	tDCK
Data Setup Time	tds	40			nSec
Data Hold Time	tdh	40			nSec
Reset pulse width	tRES	10			nSec

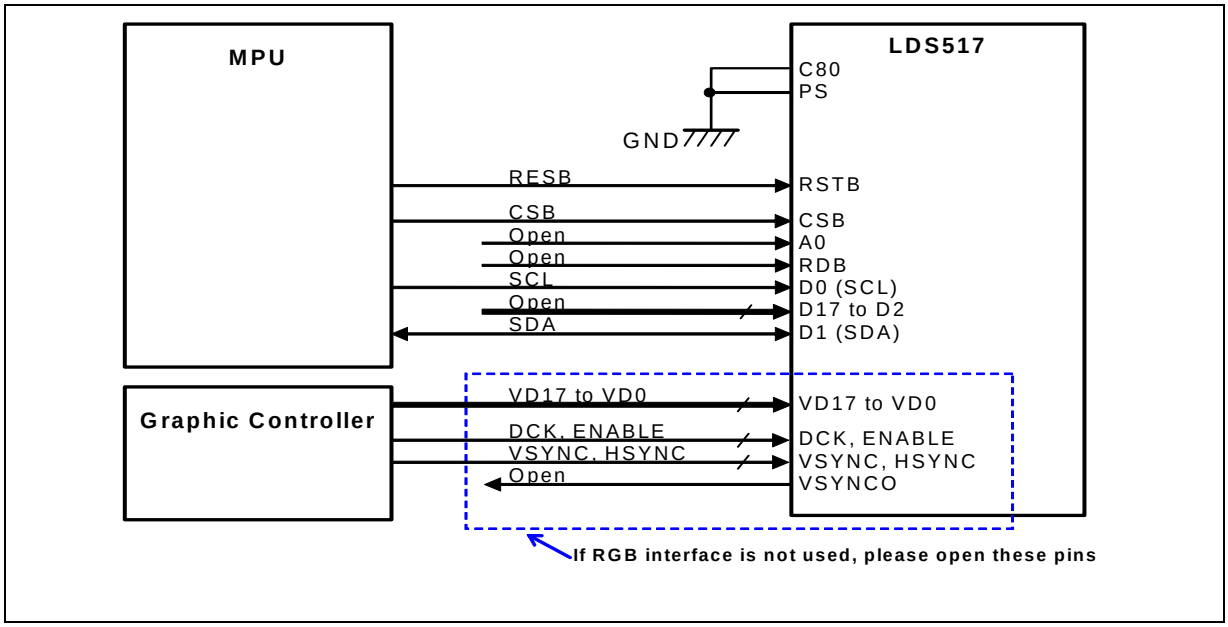
PIXEL CLOCK TIMING



REFERENCE APPLICATIONS

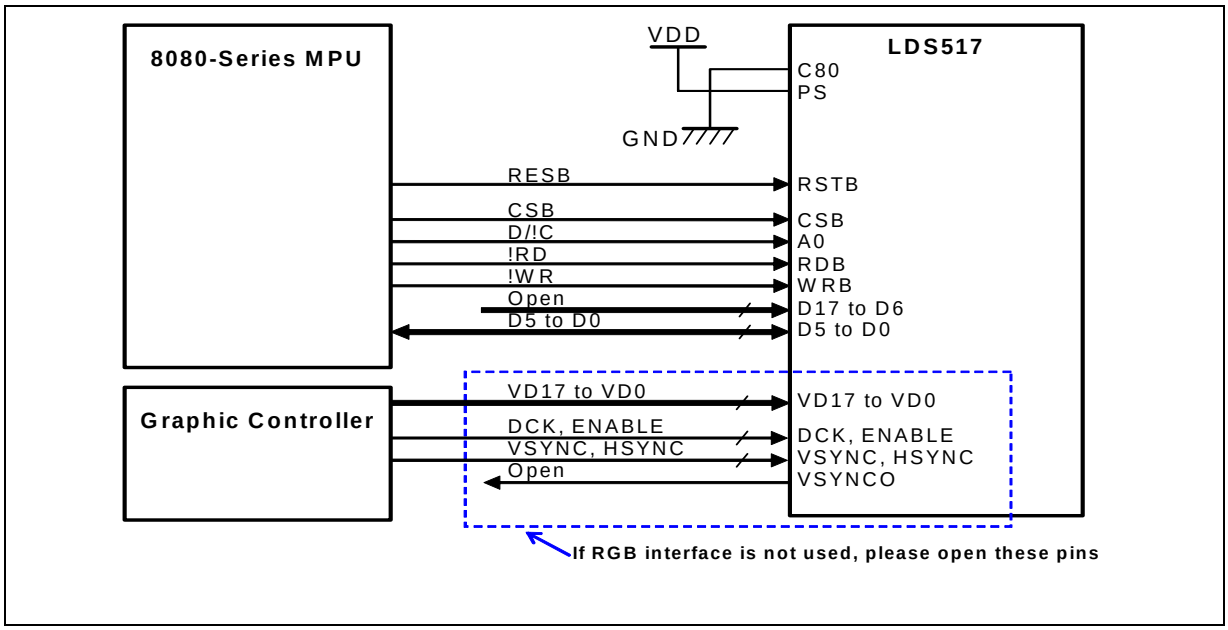
Microprocessor Interface

Interfacing with Serial Mode (PS = "L", C80 = "X", IFMODE[2:0] = "LLL")



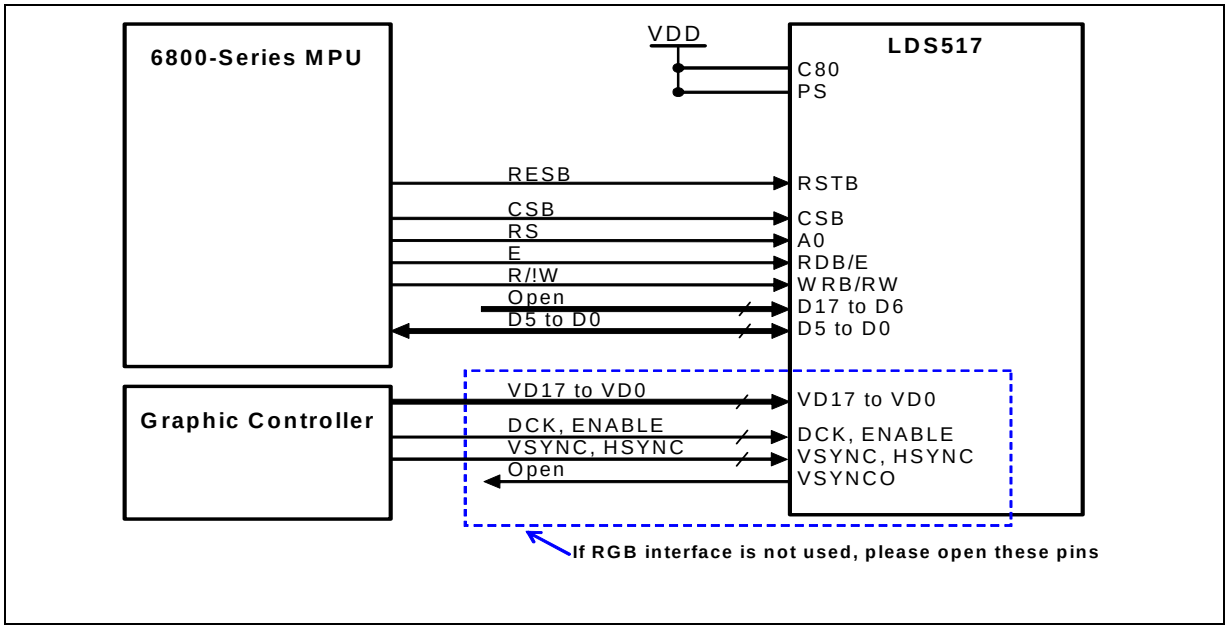
Interfacing with Serial Mode

Interfacing with 80-series MPU 6-Bit Bus (PS=”H”, C80 = "L", IFMODE[2:0] = "LLL”)



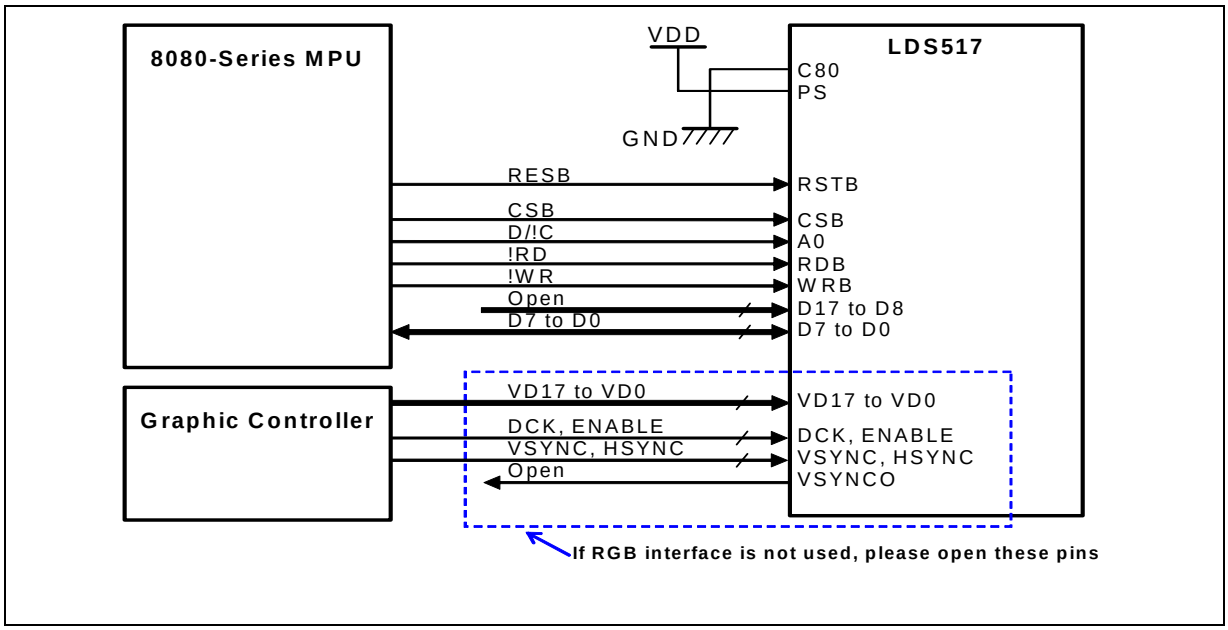
Interfacing with 6-bit 80-series

Interfacing with 68-series MPU 6-Bit Bus (PS=”H”, C80 = "H", IFMODE[2:0] = "LLL”)



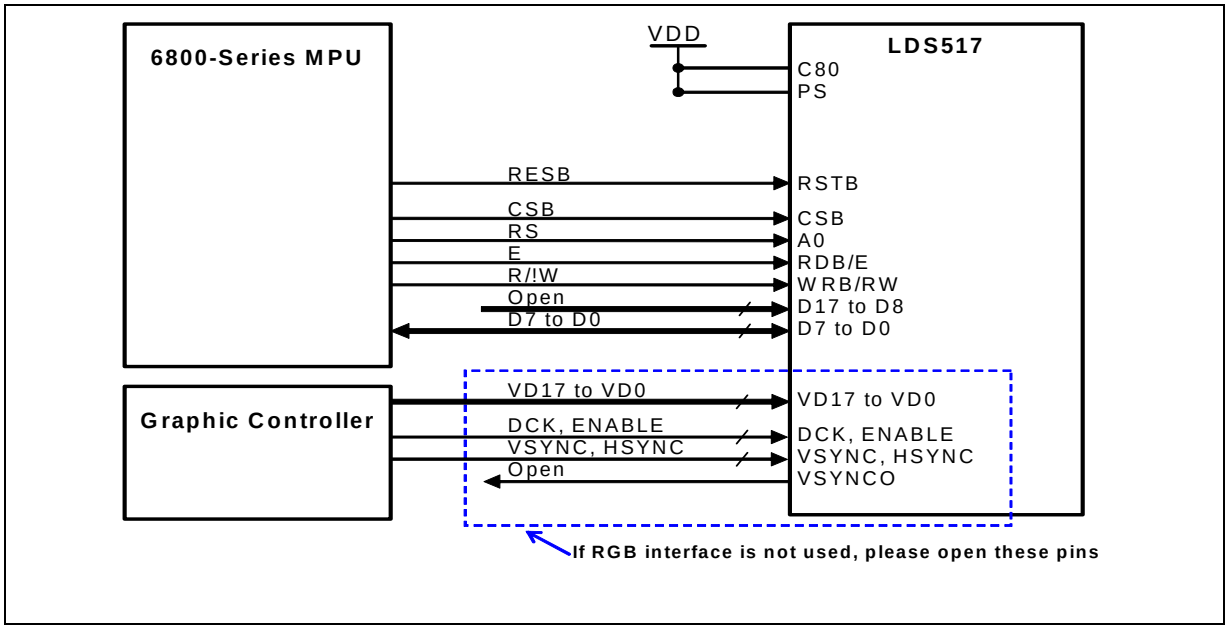
Interfacing with 6-bit 68-series

Interfacing with 80-series MPU 8-Bit Bus (PS=”H”, C80 = "L", IFMODE[2:0] = "LLH”)



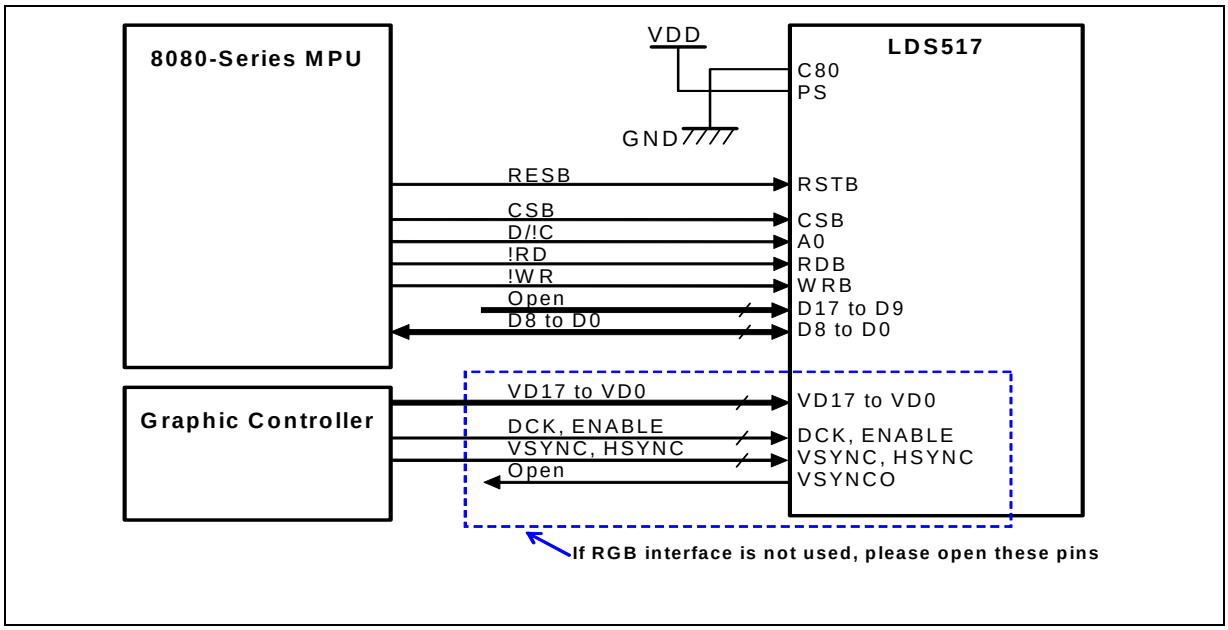
Interfacing with 8-bit 80-series

Interfacing with 68-series MPU 8-Bit Bus (PS=”H”, C80 = "H", IFMODE[2:0] = "LLH”)



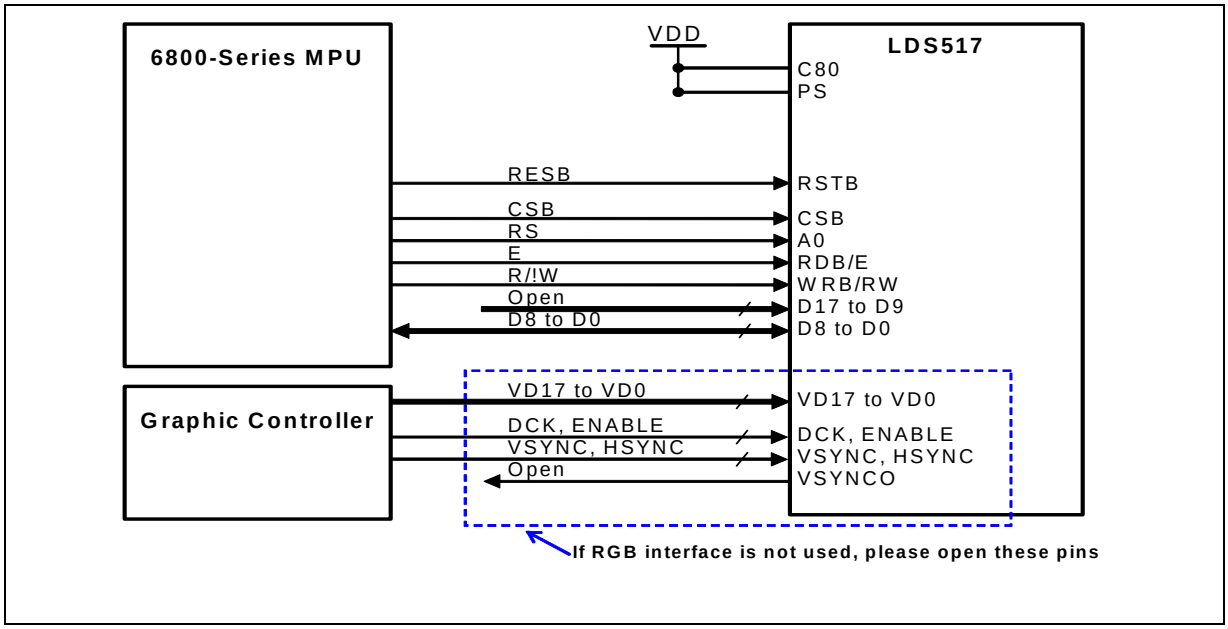
Interfacing with 8-bit 68-series

Interfacing with 80-series MPU 9-Bit Bus (PS="H", C80 = "L", IFMODE[2:0] = "LHL")



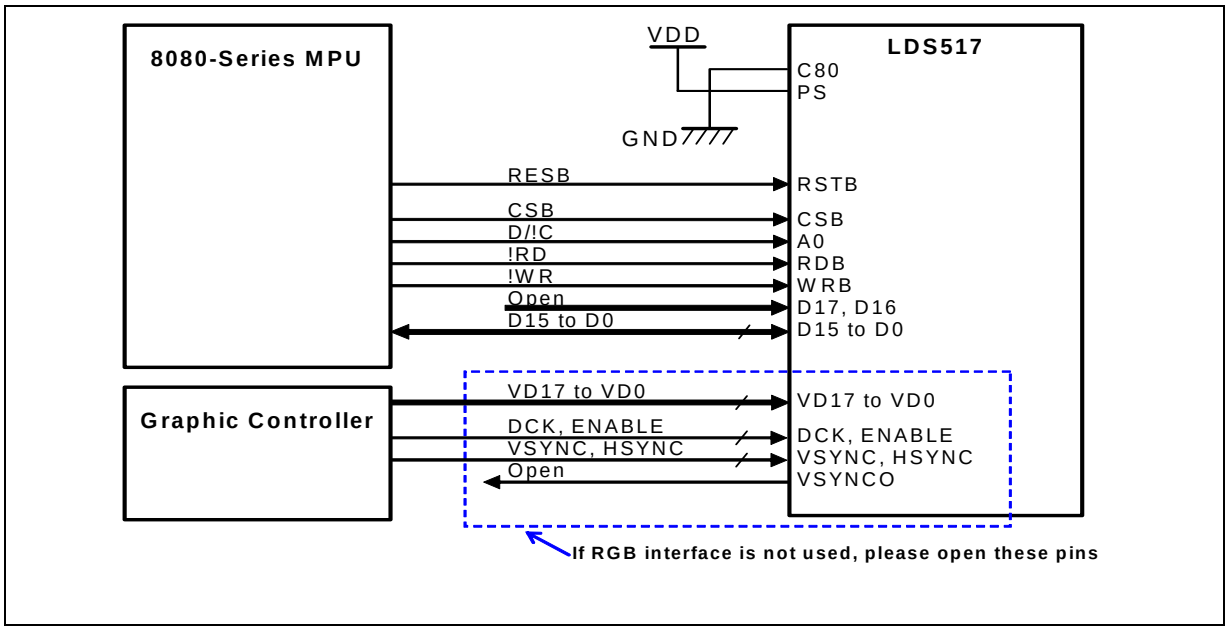
Interfacing with 9-bit 80-series

Interfacing with 68-series MPU 9-Bit Bus (PS="H", C80 = "H", IFMODE[2:0] = "LHL")



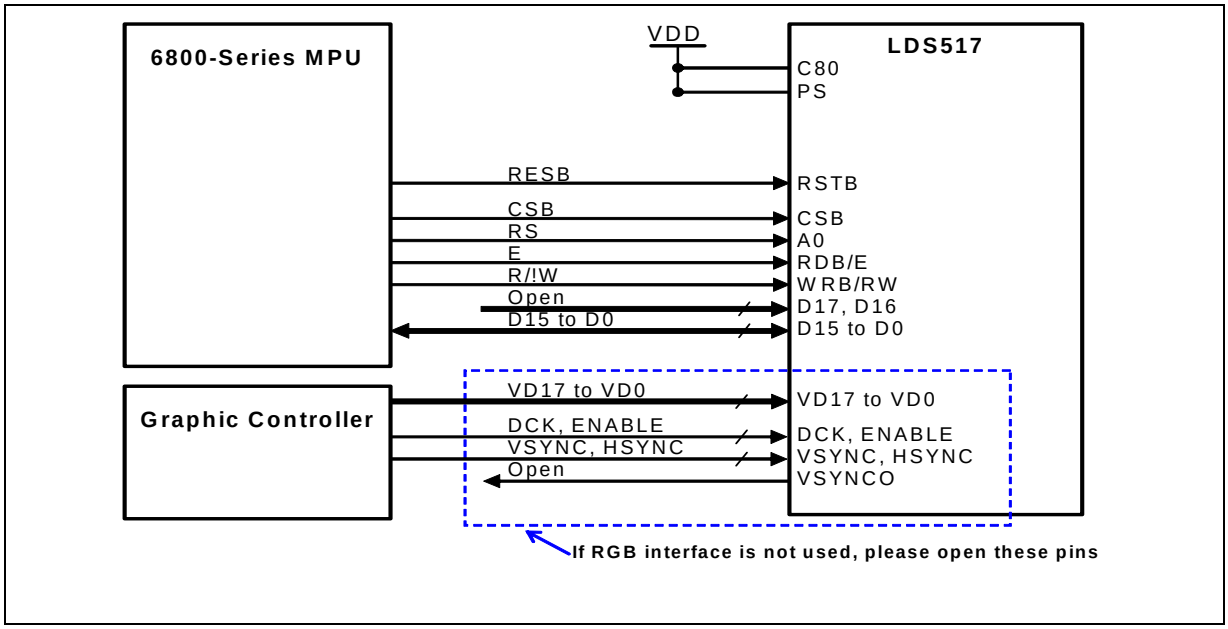
Interfacing with 9-bit 68-series

Interfacing with 80-series MPU 16-Bit Bus (PS="H", C80 = "L", IFMODE[2:0] = "LHH")



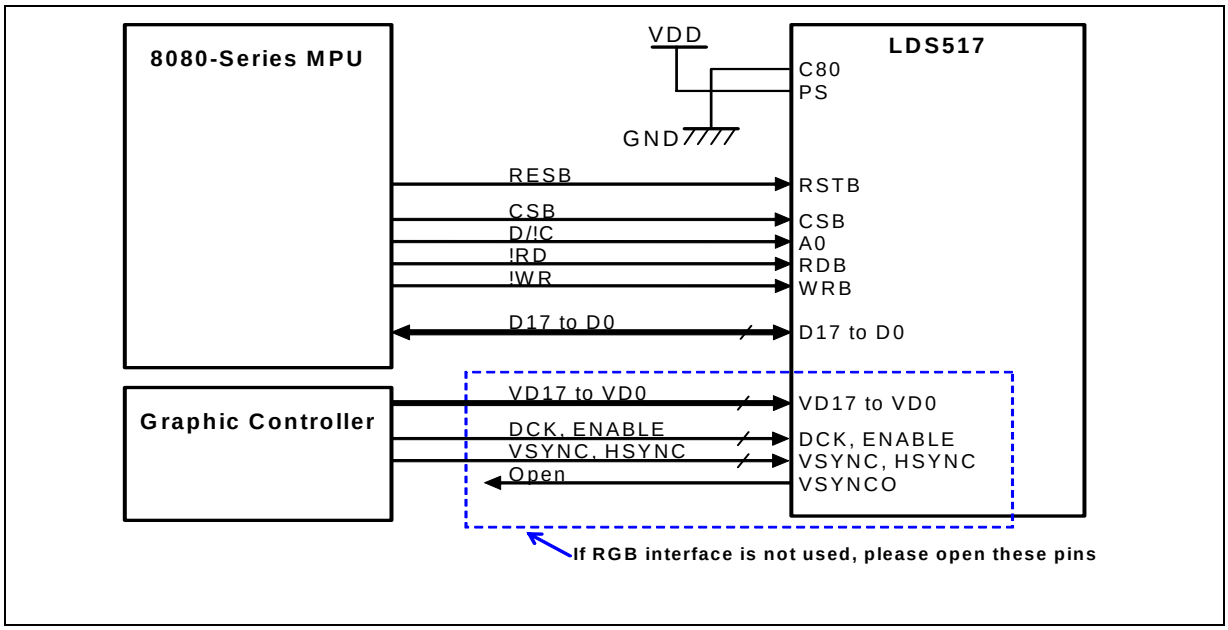
Interfacing with 16-bit 80-series

Interfacing with 68-series MPU 16-Bit Bus (PS="H", C80 = "H", IFMODE[2:0] = "LHH")



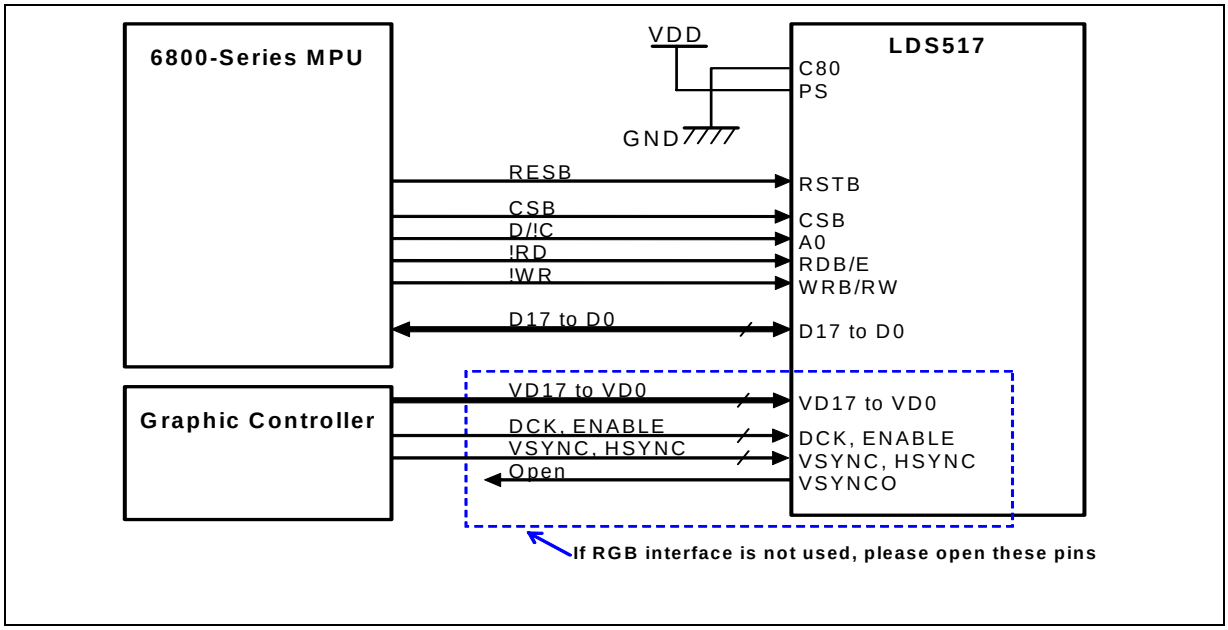
Interfacing with 16-bit 68-series

Interfacing with 80-series MPU 18-Bit Bus (PS="H", C80 = "L", IFMODE[2:0] = "HLL")



Interfacing with 18-bit 80-series

Interfacing with 68-series MPU 18-Bit Bus (PS="H", C80 = "H", IFMODE[2:0] = "HLL")



Interfacing with 18-bit 68-series

Connections with EL Panel