```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity DAC is
port(
      clk_in: in std_logic;
      ce_in: in std_logic;
      data_in : in std_logic_vector(11 downto 0);

      clk_in_2: in std_logic;
      ce_in_2: in std_logic;
      data_in_2 : in std_logic_vector(11 downto 0);

      PD : out std_logic;
      REFSELECT : out std_logic;
      DATA : out std_logic_vector(11 downto 0);

      DAC_CLK : out std_logic;
      DAC_CLK2 : out std_logic);
end DAC;

architecture Behavioral of DAC is

begin
   PD <= '0';
   REFSELECT <= '0';
   CLOCK_OUT_DATA_TO_P160 :  process (clk_in)
      begin
            if rising_edge(clk_in) then

                  if ce_in_2 = '1' then
                    if ce_in = '1' then
                              DATA(10 downto 0)<= data_in(10 downto 0);
                              DATA(11) <= NOT(data_in(11));
                              DAC_CLK <= '1';
                              DAC_CLK2 <= '0';
                              else
                              DAC_CLK <= '0';
                              DAC_CLK2 <= '1';
                     end if;
                   end if;

               end if;
          end process;

end Behavioral;
```