Version	1
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Date	2008/10/31

Product Specification

TFT LCD PANEL

Model : LMT-102-2WL-R51

10.2” SVGA (800xRGBx600)
200 nits Brightness
LED BACK LIGHT
With 5 wire resistor type touch screen

Approval

Issue by	R & D	QA	ME	Approve by

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Record of Revision

Version	Revise Date	Page	Content
1	2008/10/31	-	First edition V1

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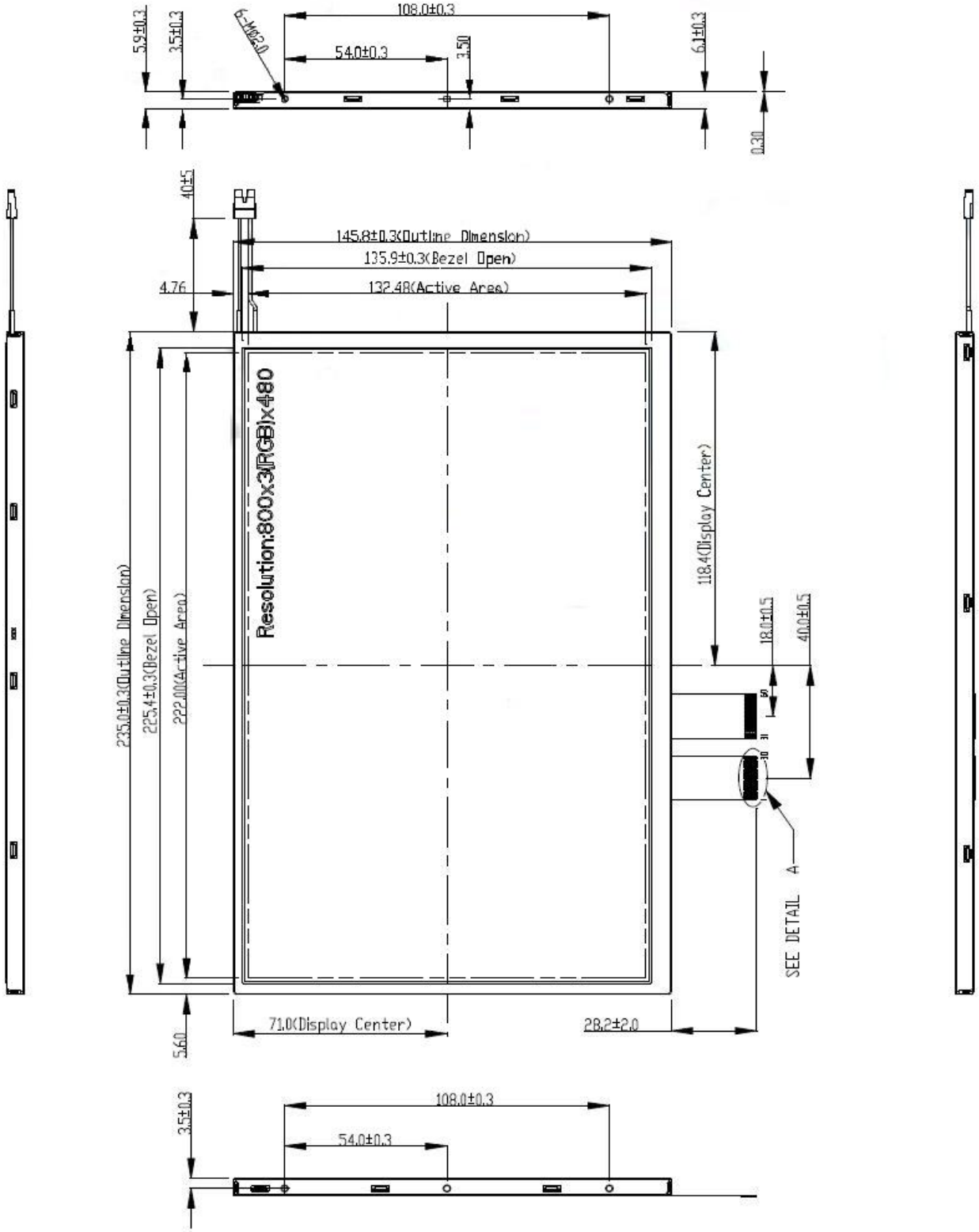
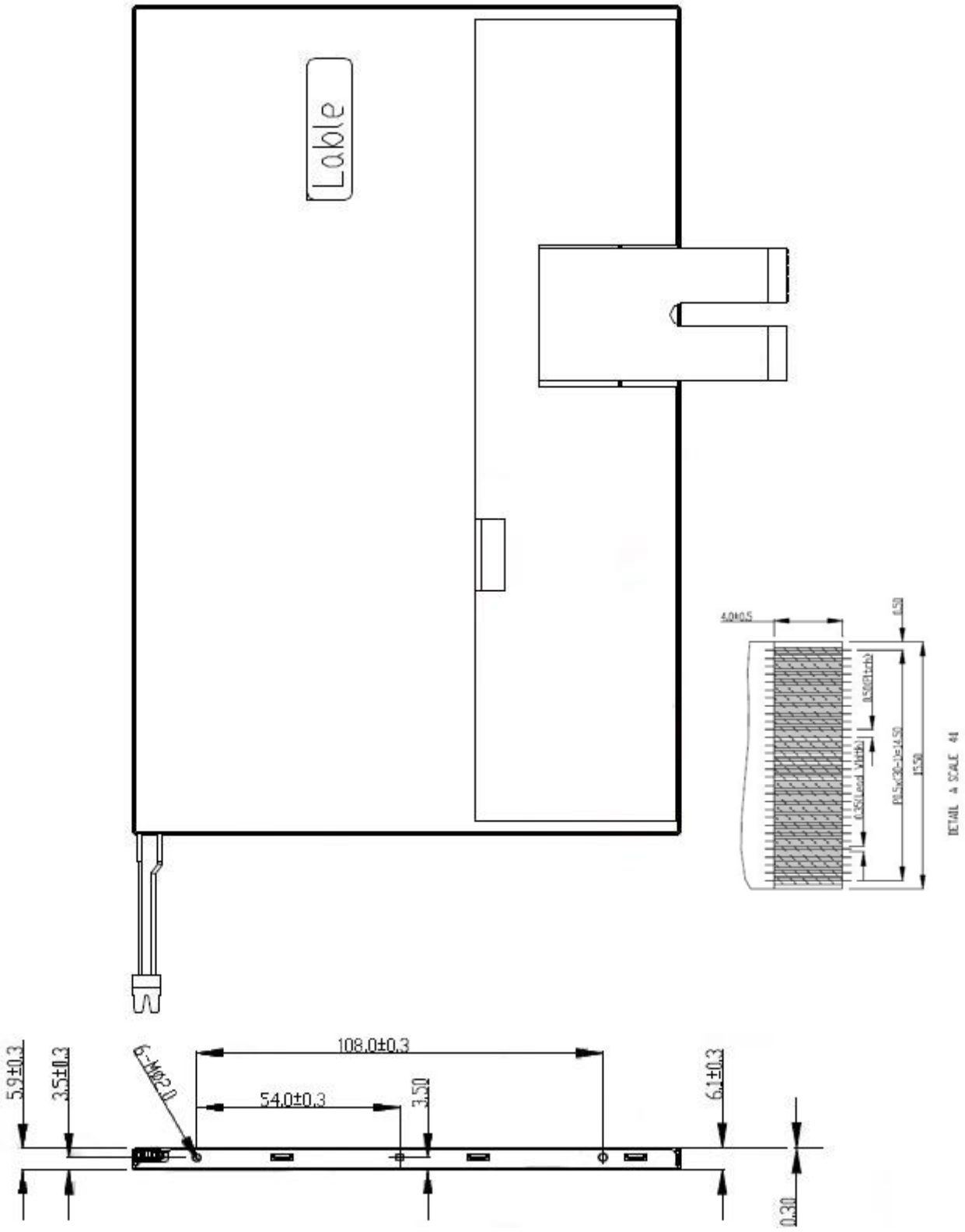
1. General Specification

Screen Size	10.2 inch
Aspect Ratio	16:9
Driver element	a-Si TFT active matrix
Input Interface	TTL, 6 bit digital RGB
Number of Pixels	800(H) x RGB x 480(V)
Pixel Pitch (mm)	0.0925(W) x 0.276(H)mm
Active Area (mm)	222(H) x 132.48(V)
Outline Dimension	235mm(W) x 145.8mm(H) x 6.1mm (D)
Display Mode	Normally White, Transmissive
Surface treatment	Anti-Glare
Back Light power consumption	2.57W (TYP.)
Panel power consumption	250 mW (TYP.)
Operation Temp.(℃)	-30 ~ +85
Storage Temp. (℃)	-40 ~ 95
View Angle (Up/Down/Left/Right)	45/65/65/65
Brightness (cd/m2)	200
Contrast Ratio	300
Response Time (msec)	35
Supply Voltage (VDC)	3.3 VDC for LCD

2. LCD Dimensions UNIT: mm




Lable
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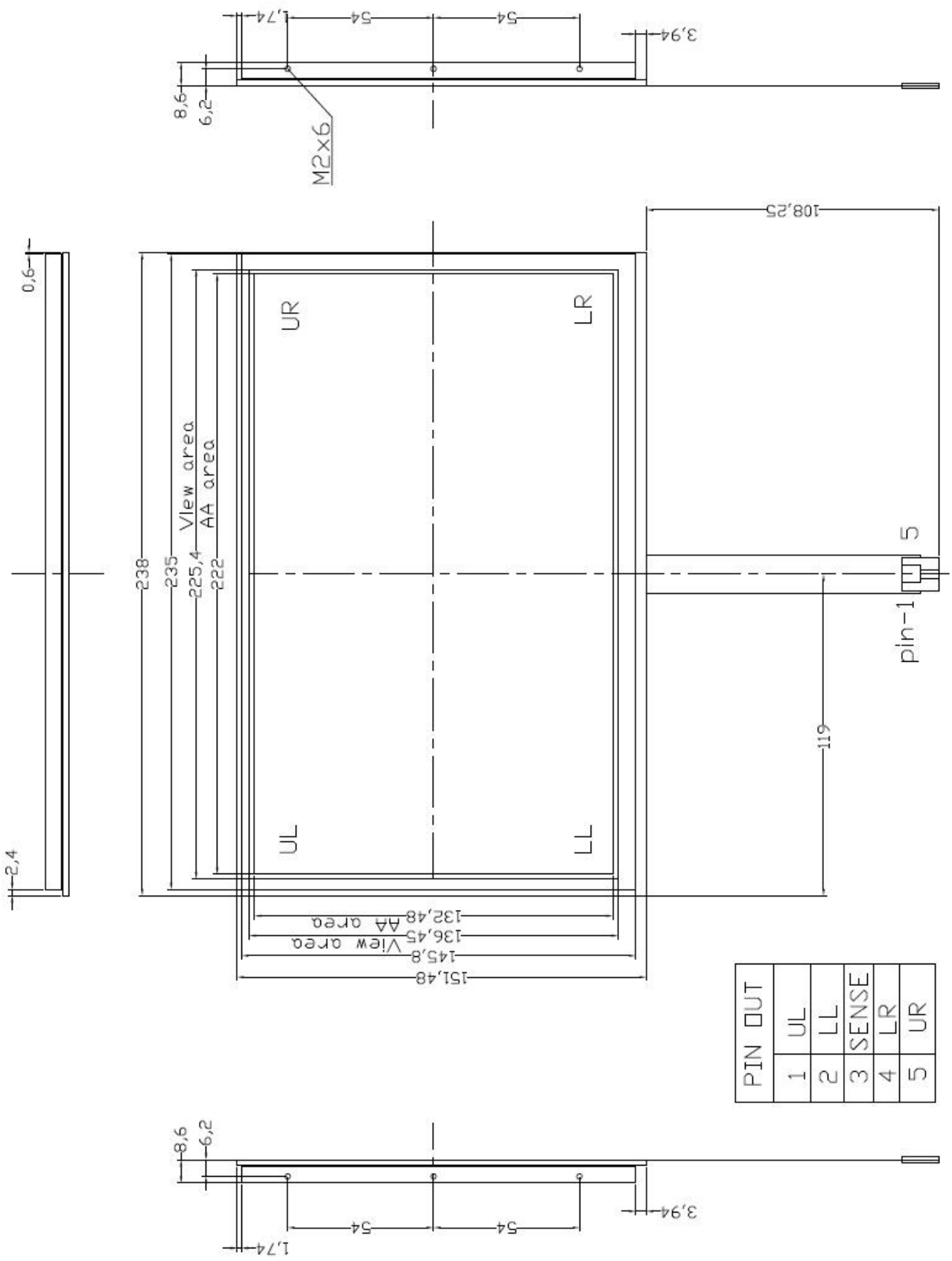
3.50
5.9±0.3
3.5±0.3
6-M2.0
6.1±0.3
0.30


1,74
54
54
3,94
8,6
6,2
M2x6
108,25
0,6
UR
LR
238
235
225,4
222
View area
AA area
5
pin-1
119
UL
LL
2,4
132,48
AA area
136,45
View area
145,8
151,48
PIN OUT
1 UL
2 LL
3 SENSE
4 LR
5 UR
8,6
6,2
3,94
54
54
1,74

3. Absolute Maximum Rating

ITEM	SYMBOL	VALUES		UNIT	REMARK
		MIN.	MAX.		
Power Voltage	Vcc	-03.	5	V	
	AV_{DD}	-0.5	12	V	
	V_{GH}	-0.3	18	V	
	V_{GL}	-15	0.3	V	
	V_{GH}-V_{GL}	-	33	V	
Input Signal Voltage	V1~V7	0.4 AV_{DD}	$AV_{DD-0.1}$	V	Note 1
	V8~V14	-0.3	0.6AV_{DD}	V	
Operation TEMP.	T_{OP}	-30	85	℃	
Storage TEMP.	T_{ST}	-30	85	℃	

Note 1: AV_{DD}-0.1≧V1≧V2≧V3≧V4≧V5≧V6≧V7≧V8≧V9≧V10≧V11≧V12≧V13≧V14≧AVSS+0.1

4. Electrical Characteristics

ITEM	SYMBOL	VALUES			UNIT	REMARK
		MIN.	TYP.	MAX.		
Power Voltage	Vcc	3.0	3.3	3.6	V	
	AV_{DD}	9.0	9.2	9.4	V	
	V_{GH}	14.3	15	15.7	V	
	V_{GL}	-10.5	-10	-9.5	V	
Input Signal Voltage	V_{COM}	3.5	3.7	3.9	V	(V1+V14)/2=4.5V
	V1~V7	0.4 AV_{DD}	-	$AV_{DD-0.1}$	V	
	V8~V14	-0.1	-	0.6AV_{DD}	V	
Input Logic HI Voltage	V_{IH}	0.7	-	Vcc	V	
Input Logic HI Voltage	V_{IL}	0	-	0.3 Vcc	V	
Operation TEMP.	T_{OP}	-30	-	85	℃	
Storage TEMP.	T_{ST}	-30	-	85	℃	

Note: Be sure to apply GND, V_{CC} and V_{GL}, to the LCD first, and then apply V_{GH}.

5. Interface Connection

Connector type: 30 pin / 0.5mm pitch, x 2 pcs, upper contact,

PIN NO	SYMBOL	I/O	DESCRIPTION	Remark
1.	POL	I	Polarity selection	
2.	STVD	I/O	Vertical start pulse input when U/D = H	Note 1
3.	OEV	I	Output enable	
4.	CKV	I	Vertical clock	
5.	STVU	I/O	Vertical start pulse input when U/D = L	Note 1
	GND	P	Power Ground	
7.	EDGSL	I	Select rising edge or falling edge	
8	V_{CC}	P	Power Supply for Digital Circuit.	
9.	V9	I	Gamma voltage level 9	
10.	VGL	P	Gate OFF Voltage	
11	V2	I	Gamma voltage level 2	
12.	VGH	I	Gate ON Voltage	
13	V6	I	Gamma voltage level 6	
14	U/D		Up down selection	Note 1,2.
15	VCOM	I	Common Voltage	
16	GND	P	Power Ground	
17	AVDD	P	Power supply for analog circuit	
18	V14	I	Gamma voltage level 14	
19	V11	I	Gamma voltage level 11	
20	V8	I	Gamma voltage level 8	
21	V5	I	Gamma voltage level 5	
22	V3	I	Gamma voltage level 3	
23	GND	P	Power Ground	
24	R5	I	Red Data 5 (MSB)	
25	R4	I	Red Data 4	
26	R3	I	Red Data 3	
27	R2	I	Red Data 2	
28	R1	I	Red Data 1	
29	R0	I	Red Data 0(LSB)	
30	GND	P	Power Ground	

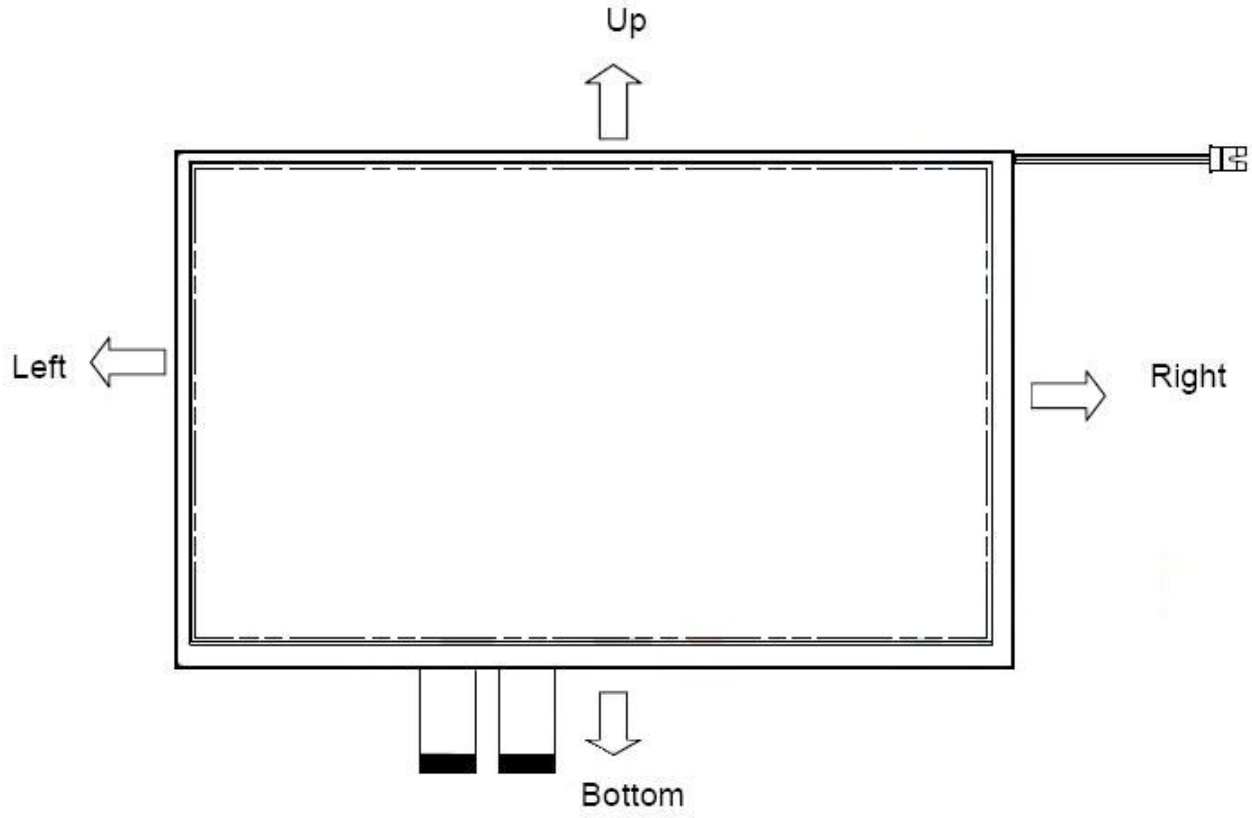
31	GND	P	Power Ground	
32	G5	I	Green Data 5 (MSB)	
33	G4	I	Green Data 4	
34	G3	I	Green Data 3	
35	G2	I	Green Data 2	
36	G1	I	Green Data 1	
37	G0	I	Green Data 0 (LSB)	
38	STHL	I/O	Horizontal start pulse input when R/L = L	Note 1
39	REV	I	Control signal are inverted or not	
40	GND	P	Power Ground	
41	DCLK	I	Sample clock	
42	VCC	P	Power supply for digital circuit	
43	STHR	I/O	Horizontal start pulse input when R/L = L	Note 1
44	LD	I	Latches the polarity of output and switches the new data to outputs	
45	B5	I	Blue Data 5 (MSB)	
46	B4	I	Blue Data 4	
47	B3	I	Blue Data 3	
48	B2	I	Blue Data 2	
49	B1	I	Blue Data 1	
50	B0	I	Blue Data 0 (LSB)	
51	R/L	I	Right / Left selection	Note 1,2.
52	V1	I	Gamma voltage level 1	
53	V4	I	Gamma voltage level 4	
54	V7	I	Gamma voltage level 7	
55	V10	I	Gamma voltage level 10	
56	V12	I	Gamma voltage level 12	
57	V13	I	Gamma voltage level 13	
58	AVDD	P	Power supply for analog circuit	
59	GND	P	Power Ground	
60	VCOM	I	Common Voltage	

I: Input, O: Output. P: Power.

Note 1: Selection of scanning mode

Setting of scan control input		IN/OUT state for start pulse				Scanning direction
U/D	R/L	STVD	STVU	STHR	STHL	
GND	Vcc	O	I	O	I	Up to down, Left to right
Vcc	GND	I	O	I	O	Down to up, right to left
GND	GND	O	I	I	O	Up to down, right to left
Vcc	Vcc	I	O	O	I	Down to up, left to right

Note 2: Definition of scanning direction.
Refer to the figure as below:



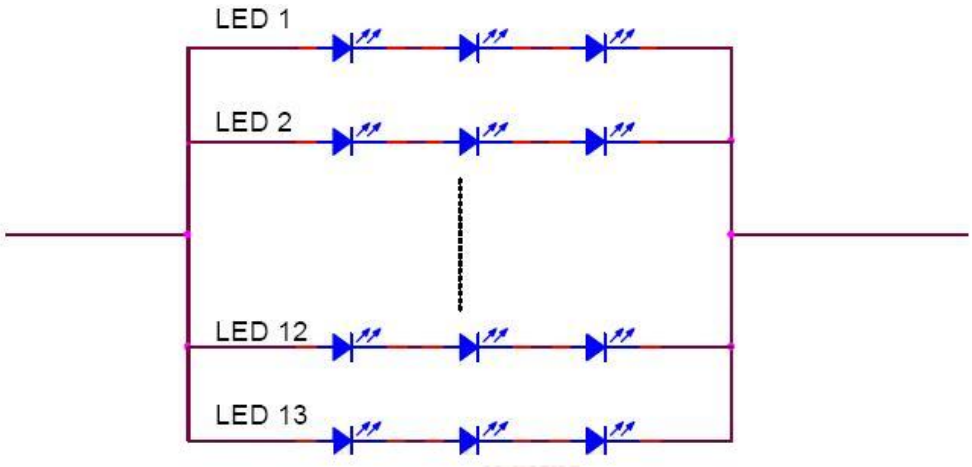
6. LED Driving Condition.

The LED Back Light system is connected by a connector BHSR-02VS-1 manufactured by JST or EQ.

Pin No.	Symbol	I/O	Function	Remark
1	HI	P	Power supply for backlight unit (High voltage)	Pink
2	GND	P	Ground for backlight unit	White

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
LED Voltage	VL	-	9.9	10.5	V	Note 1
LED Current	IL	-	20	-	mA	Note 1
LED Life time	-	20,000	-	-	Hr	Note 2

Note 1: The LED driving condition is defined for each LED module (3 LED in Serial)



Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at the ambient temperature 25 ℃ and IL=20mA

Note 3: The LED Supply voltage is defined by the quantity of LED at Ta=25℃ and IL=20mA. In the case of 3 pcs LED in serial, VL=3.3V x 3 = 9.9V

7. Optical Characteristics:

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR≥10)	θ_L	Φ=180°(9 o'clock)	55	65	-	degree	
	θ_R	Φ=0°(3 o'clock)	55	65	-		
	θ_T	Φ=90°(12 o'clock)	35	45	-		
	θ_B	Φ=270°(6 o'clock)	55	65	-		
Response time	T_{ON}	Normal θ=Φ=0°	-	15	30	msec	
	T_{OFF}		-	20	40	msec	
Contrast ratio	CR		250	300	-	-	
Color chromaticity	W_X		0.25	0.31	0.35	-	
	W_Y		0.28	0.33	0.38	-	
Luminance	L			200	-	cd/m^2	
Luminance uniformity	Y_U		70	75	-	-	

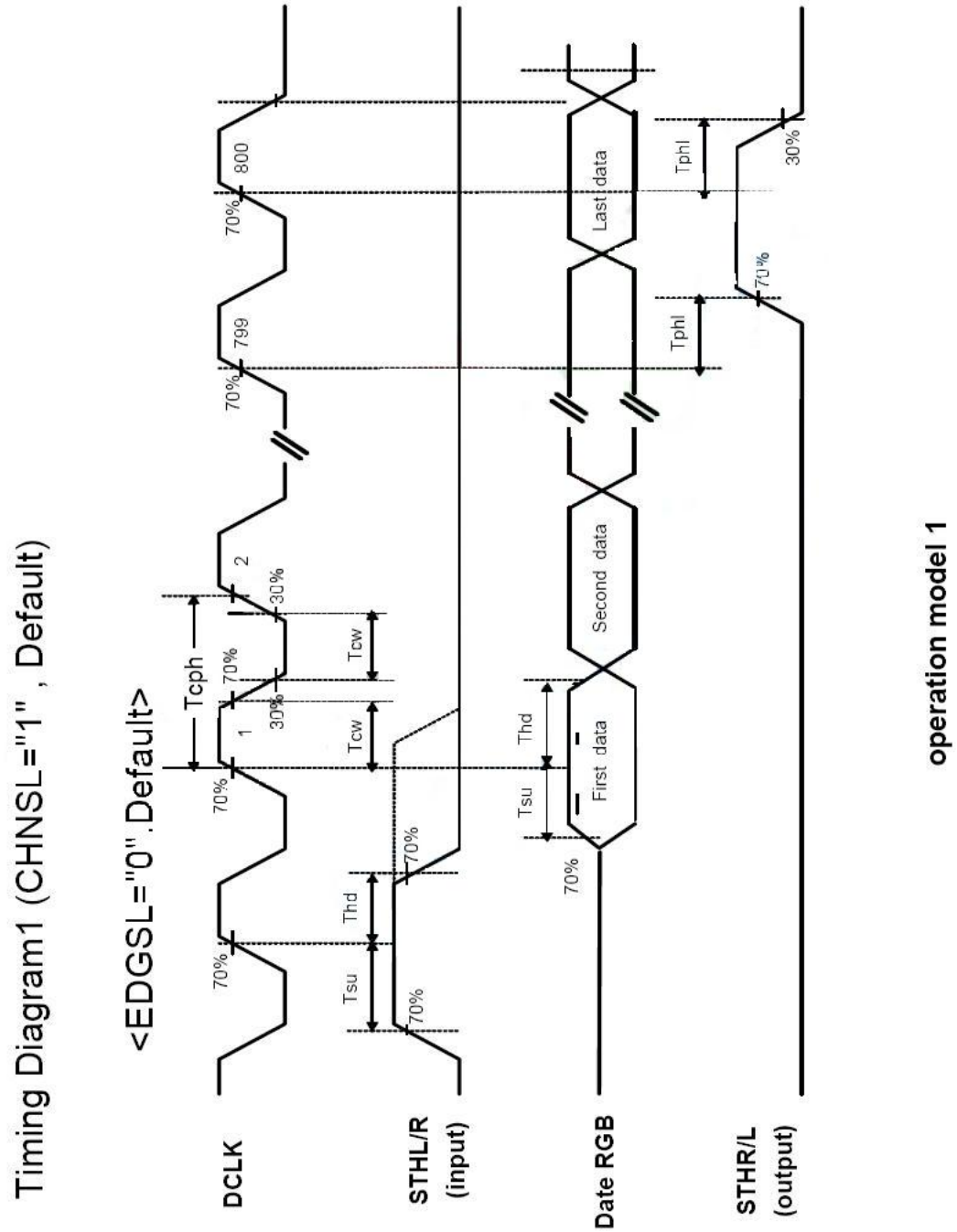
8. Timing:

8.2. Timing Condition

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DCLK frequency	F_{dclk}	-	40	45	MHz	
DCLK cycle	T_{cph}	22	25	-	ns	
DCLK pulse width	T_{cw}	8	-	-	ns	
Data set-up time	T_{su}	4	-	-	ns	
Data hold time	T_{hd}	2	-	-	ns	
Time that the last data to LD	T_{ld}	1	-	-	Tcph	
Pulse width of LD	T_{wld}	2	-	-	Tcph	
Time that LD to STHL/R	T_{lds}	5	-	-	Tcph	
POL set-up time	T_{psu}	6	-	-	ns	
POL hold time	T_{phd}	6	-	-	ns	
CKV frequency	F_{vclk}	-	-	200	KHz	
CKV rise time	T_{rck}	-	-	100	ns	
CKV falling time	T_{fck}	-	-	100	ns	
CKV pulse width	P_{WCLK}	500	-	-	ns	
Horizontal display timing range	T_{dh}	-	800	-	Tcph	
Horizontal timing range	T_{h}	-	1056	-	Tcph	
STVU/D setup time	T_{suv}	200	-	-	ns	
STVU/D hold time	T_{hdv}	300	-	-	ns	
STVU/D delay time	T_{dt}	-	-	500	ns	
Driver output delay time	T_{do}	-	-	900	ns	

Output rise time	T_{tlh}	-	500	1000	ns	
Output falling time	T_{thl}	-	400	800	ns	
OEV pulse width	T_{wcl}	1	-	-	us	
OEV to Driver output delay time	T_{oe}	-	-	900	ns	
Horizontal lines per field	T_v	512	525	610	Tdh	
Vertical display timing range	T_{vd}	-	480	-	Tdh	

8.2. Timing Diagram



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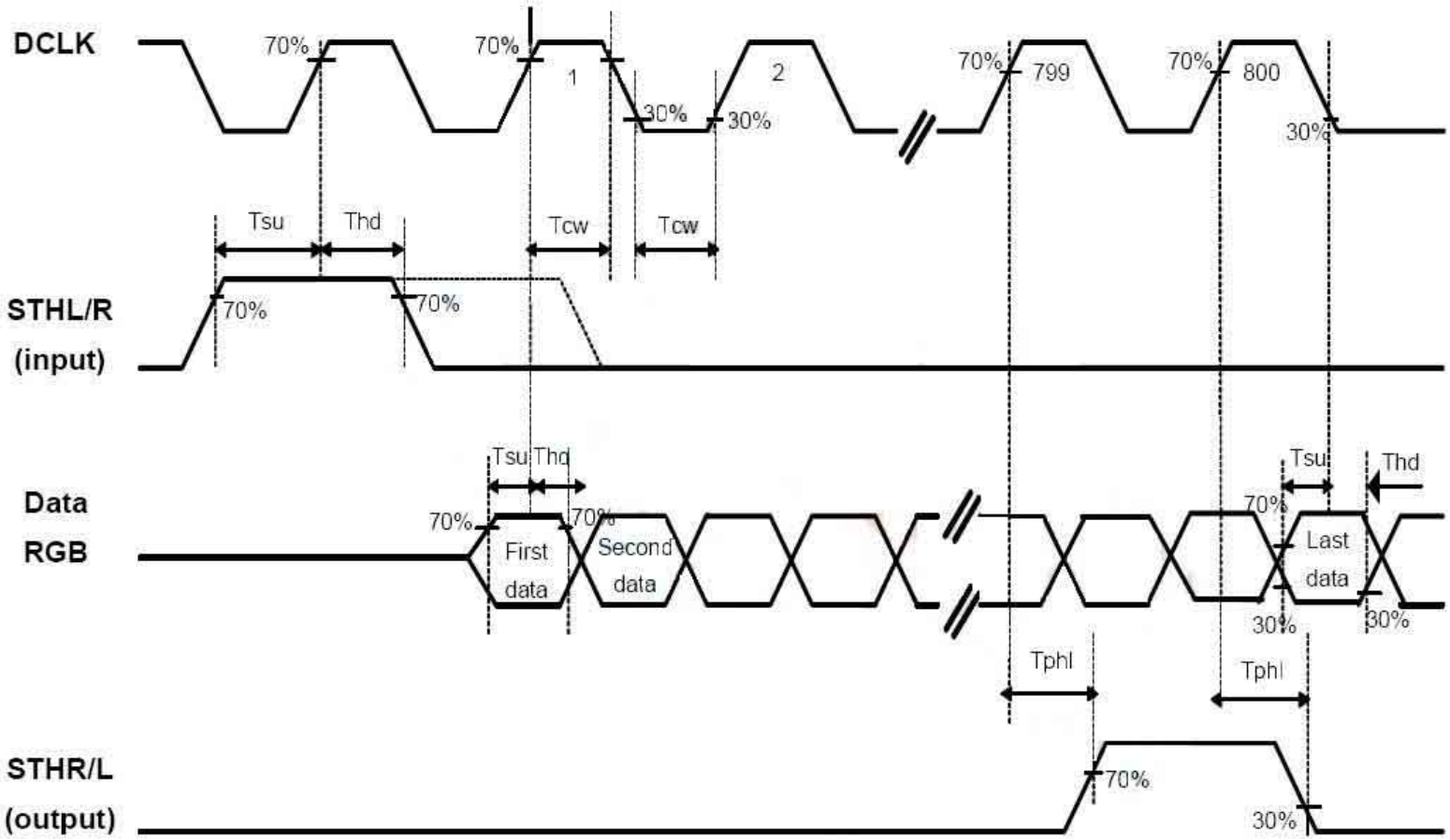
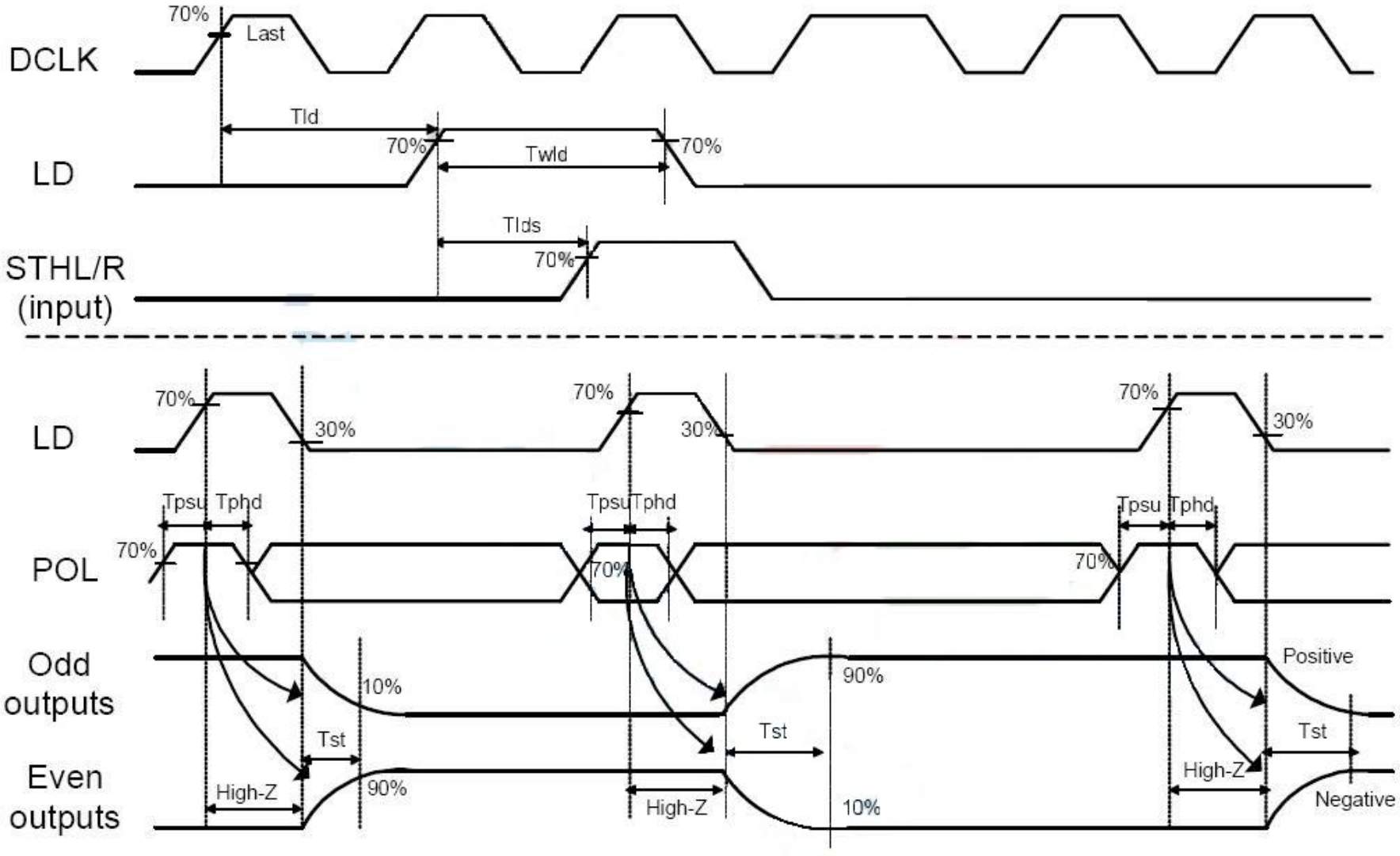
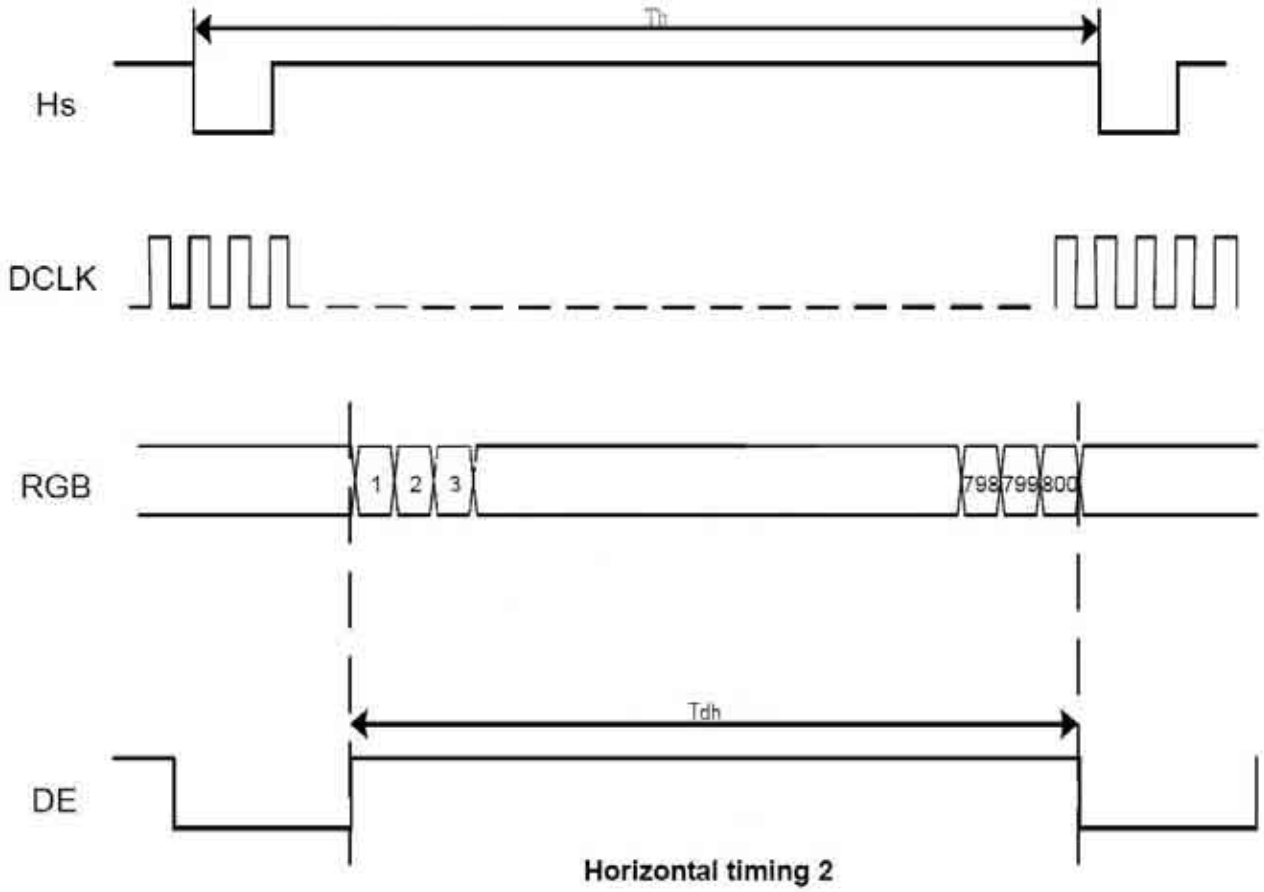


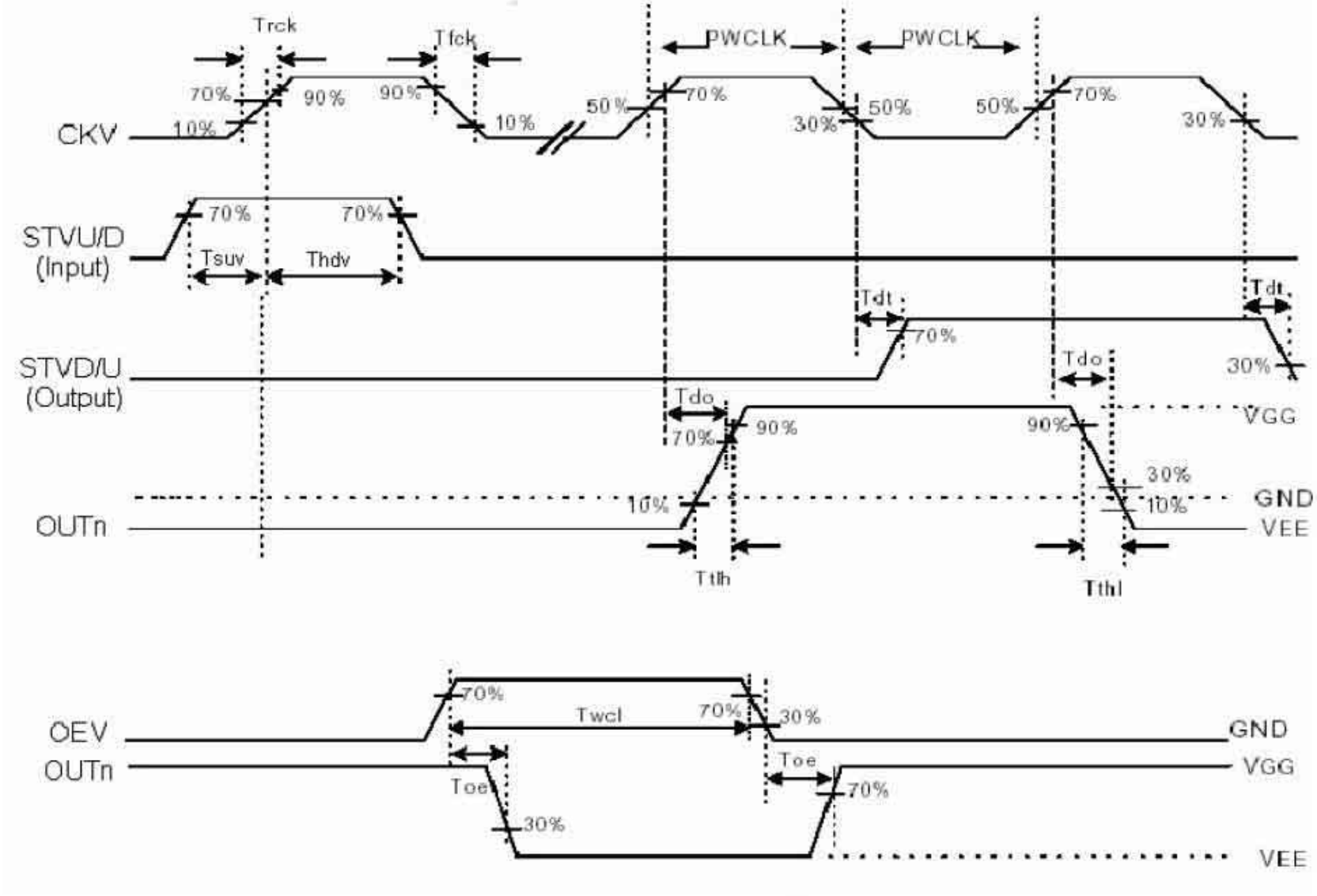
operation model 2

Timing Diagram 2

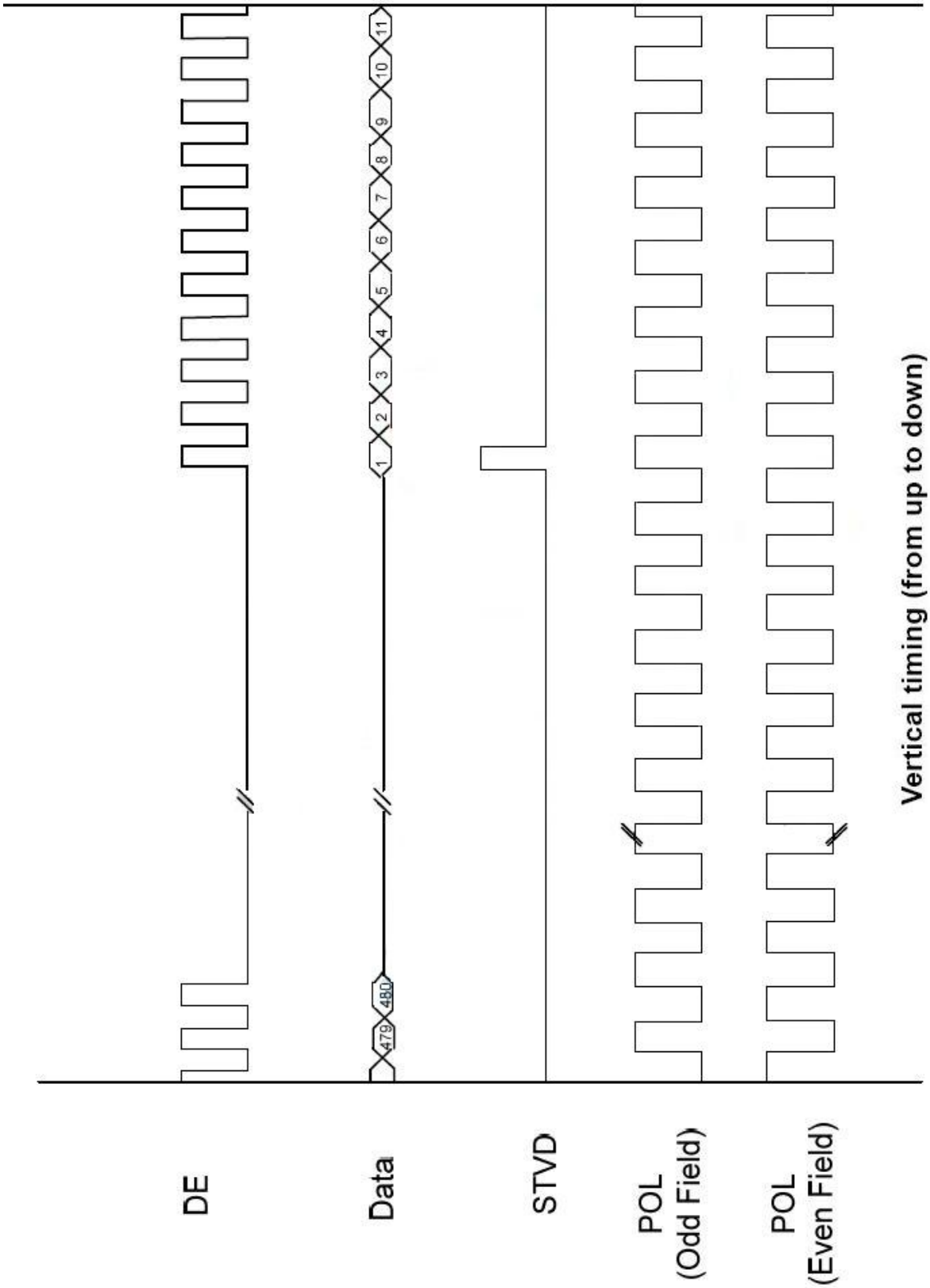




Horizontal timing 2



Vertical shift clock timing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Data
STVD
POL
(Odd Field)
POL
(Even Field)
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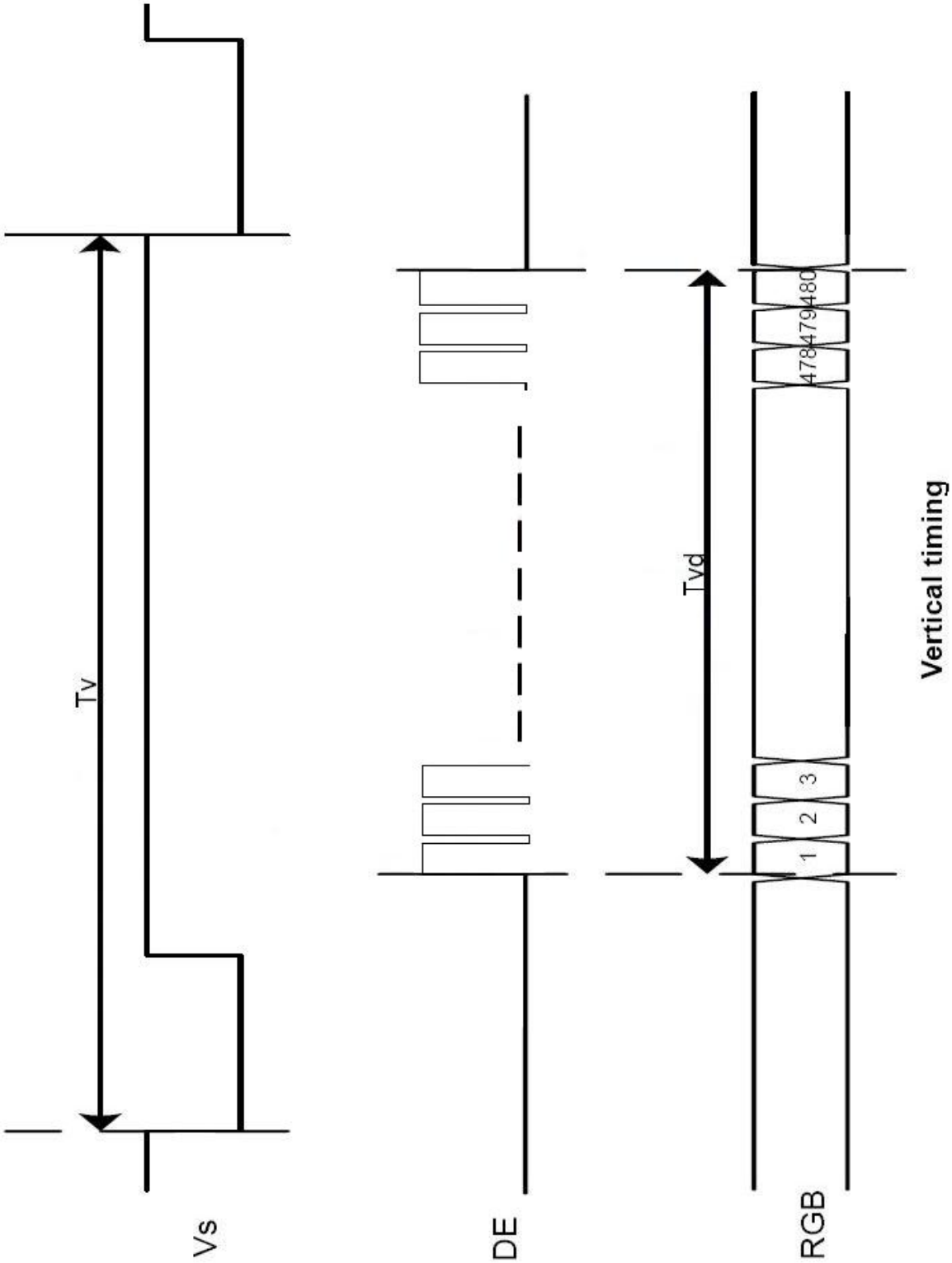
2
3
4
5
6
7
8
9
10
11
479
480
Vertical timing (from up to down)


Tv
Vs
DE
Tvd
1
2
3
478
479
480
RGB
Vertical timing