VTI TECHNOLOGIES

Doc.Nr. 8260800.08

Product Family Specification

SCP1000 Series
Absolute pressure sensor

SCP1000-D01
SCP1000-D11

Note: Reader is advised to notice that this Product Family Specification applies to SCP1000 having updated signal conditioning circuitry. This version can be recognized from the D01 or D11 marking on the top of the component (see image). If you are using old SCP1000 version (marked using P01 or P03), please use Product Family Specification rev. 0.06. Differences between the old and new SCP1000 version are described in Technical Note 59 (SCP1000 ASIC Update).

Product marking

Table of Contents

1 General Description

1.1 Introduction

SCP1000 is pressure sensor that measures absolute pressure. The sensor consists of a silicon bulk micro machined sensing element chip and a signal conditioning ASIC. The pressure sensor element and the ASIC are mounted inside a plastic pre-moulded package and wire bonded to appropriate contacts. The round shaped sensor component has 18 SMD solderable contacts. SCP1000 block diagram is presented in Figure 1 below.

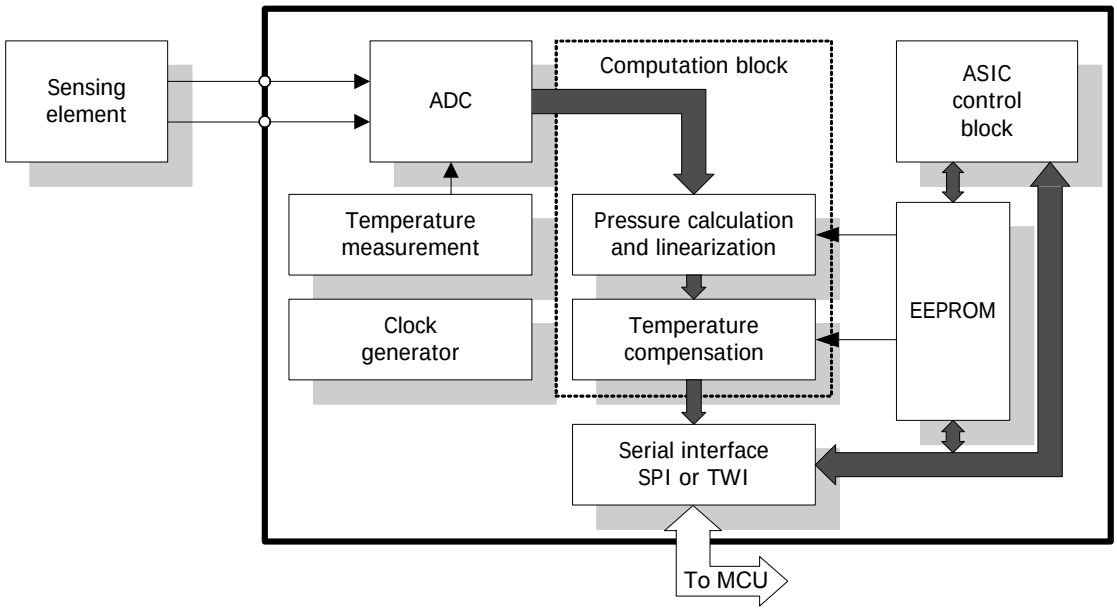


Figure 1. SCP1000 system level block diagram.

1.2 Functional Description

The SCP1000 performs almost complete data processing on-chip. The pressure and temperature output data are calibrated and compensated internally. The only operations over the output data required to obtain the pressure in [Pa] and the temperature in [°C] is single multiplication with constants, see more details in section 2.2.3.

1.2.1 Sensing element

The sensing element is manufactured using the proprietary bulk 3D-MEMS process of VTI enabling robust, stable, low noise and low power capacitive sensors.

Absolute pressure sensor element consists of a silicon wafer that is locally thinned to form a pressure sensitive diaphragm. The diaphragm acts as a movable plate of the capacitive sensor. The stationary plate is a thin film metal deposited on a second, glass coated silicon wafer. The wafers are joined by anodic bonding so that a hermetically enclosed space is formed between them. The diaphragm deflects due to the pressure difference between the exterior of the sensor and the internal vacuum reference chamber.

1.2.2 Interface IC

The communication between the SCP1000 and its host micro-controller (µC) is based on a serial interface, an interrupt line and specialized pins used to trigger special functions. The serial interface allows registers' read and write operations and the interrupt line signals events, which require host intervention. Two different serial interfaces are available: SPI and TWI (TWI is very similar to I^2C bus). The appropriate communication interface is pre-programmed in the factory. The register access protocol is independent on the selected interface.

1.2.3 Factory calibration

All sensors are factory calibrated. Some of the calibration parameters are: sensitivity to pressure, offset, temperature sensitivity and temperature compensation. Calibration parameters will be read automatically from the internal non-volatile during the start-up of the sensor.

1.2.4 Supported features

SCP1000 different versions and supported features are presented in Table 1 below.

Table 1. SCP1000 versions.

Features	SCP1000-D01	SCP1000-D11
Supply voltage	2.4 V – 3.3 V	2.4 V – 3.3 V
Measuring range	30 kPa – 120kPa	30 kPa – 120kPa
Resolution [1]	1.5 Pa	1.5 Pa
Interface	SPI max 500 kHz	TWI max 400 kHz
Temperature output	Yes	Yes
Clock	Internal	Internal
Marking on top of component	D01	D11

[1] typical value in high resolution measurement mode

1.2.5 Operation

The SCP1000 pressure sensor has 4 measurement modes plus standby and power down mode. In all measurement modes, the pressure output word-length is 19 bits and the temperature output word-length is 14 bits.

1.2.5.1 High resolution measurement

In the high-resolution measurement mode the pressure is measured continuously with the highest resolution and the output data refresh rate is typically 1.8 Hz.

1.2.5.2 High speed measurement

In the high speed measurement mode the measurements are performed continuously as well and the conversion time is shortened at the cost of output resolution. This allows for an increase of the output data refresh rate up approximately 9 Hz.

1.2.5.3 Ultra low power measurement

In the ultra low power measurement mode the device performs periodic measurements with the lowest resolution (15 bits) and switches to standby mode between the measurements. In this mode the updated pressure data is available approximately once per second.

1.2.5.4 Low power measurement with external trigger

In the low power measurement mode the device stays in standby mode and is ready to perform single measurement using the selected resolution, 15 bits or 17 bits. After the measurement is complete and the output data is refreshed, the sensor switches back to standby mode. Average current consumption in low power mode depends on measurement resolution and trigger frequency.

1.2.5.5 Temperature output

Temperature information is available in every measurement mode for each pressure measurement.

2 Start-up, Operation Modes, HW functions and Clock

2.1 Start-up

The SCP1000 initialization sequence described in this section (and in Figure 2) is performed each time the sensor is:

- powered up,
- waking up from power down mode
- waking up after reset.

During the start-up the power supplies must stabilize in to specified range before configuration and calibration data can be loaded from the non-volatile memory to volatile registers. The start-up sequence is divided into 3 phases described below in Figure 2.

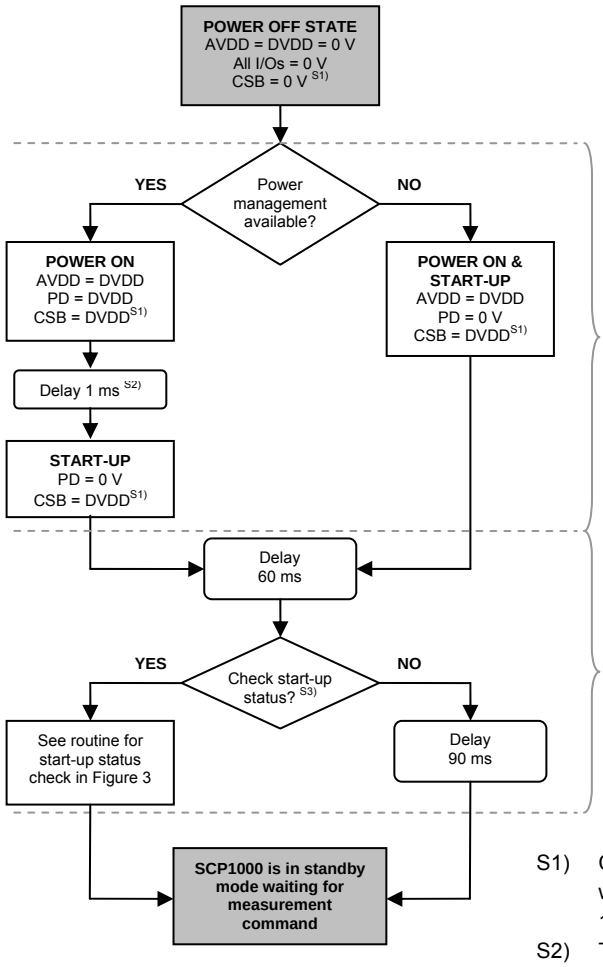


Figure 2. SCP1000 start-up sequence.

S1) Concerns SCP1000-D01 products. CSB is tied to AVDD with SCP1000-D11 (TWI-bus) products (refer to Table 19 in section 7.2).

S2) The delay immediately after powering the system is needed in order to let the power supply and the voltage over the filter capacitors to stabilize. If it is needed this delay time can be increased.

S3) Status check is optional, see section 2.1.2.

2.1.1 Power down-pin (PD) during start-up (Phase 1)

SCP1000 has an external power down (PD) pin. In case the system has power management capabilities, it is recommended that during power up the PD pin is tied to DVDD – this way the sensor is forced to remain in power down mode during the stabilization of the power supplies. After approximately 1ms (or longer depending on the power supply stabilization time) the PD pin can be switched to DVSS allowing the sensor to start the power up and the initialization procedure to begin.

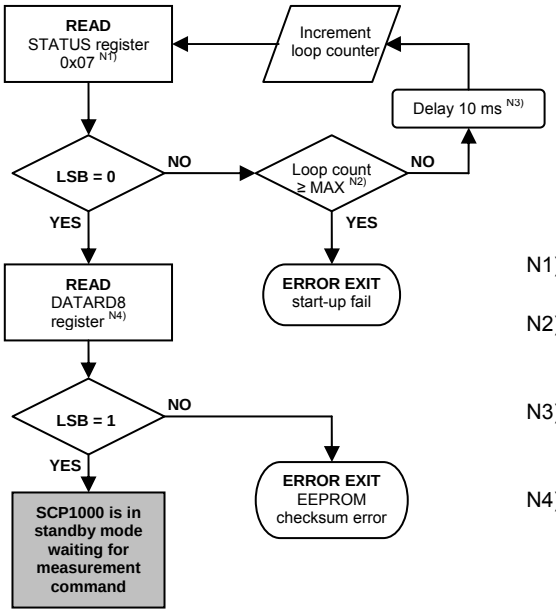
In case the system does not have power management capability the PD pin can be tied to DVSS.

2.1.2 SCP1000 initialization during start-up (Phase 2)

A 60 ms delay after the start-up (Phase 1 in Figure 2) is recommended. After the delay initialization will be finished and all configuration registers are loaded with their default values. During the 60 ms start-up delay there should not be any interface activity attempts.

Start-up status check is optional and can be replaced with 90 ms delay, see Figure 2.

The start-up status check includes EEPROM checksum error result check. The routine is described in Figure 3 and in sections 2.1.2.1 and 2.1.2.2 below.



N1) See the status register details in section 3.2. LSB = '0' means that start-up procedure is finished.

N2) The maximum number of retries (MAX loop count) depends entirely on the system design. The recommended value is 6.

N3) The recommended loop delay time can be changed depending on the system design. The recommended default value is 10 ms.

N4) DATARD8 register has address 0x1F when using SPI interface (SCP1000-D01) and 0x7F when using TWI interface (SCP1000-D11). If the content of DATARD8 is 0x01, the EEPROM checksum is correct.

Figure 3. Routine for start-up status check (optional).

2.1.2.1 SCP1000 initialization status check (optional)

The STATUS register 0x07 (see Figure 3) can be read to verify that start-up procedure is finished. If the STARTUP bit (LSB) of the STATUS register (0X07) is '0', the start-up procedure is finished successfully. If the STARTUP bit of the STATUS register is '1', the start-up procedure is still running.

If the start-up procedure is still running, it is advised to re-check the STATUS register after a delay. A recommend delay is 10ms. If the start-up procedure is not finished after the additional delay, the re-check procedure can be started again (see Figure 3). In order to avoid infinite loop in case of sensor malfunction it is advisable to limit the maximum number of cycles. Recommended value is 6 cycles when using 10 ms additional delay. If the start-up procedure is not finished successfully after the maximum number of STATUS register re-check cycles has expired, the start-up procedure has failed.

2.1.2.2 SCP1000 checksum error check (optional)

The DATARD8 register (address 0x1F when using SPI interface or 0x7F when using TWI interface) can be read in order to check the EEPROM checksum error (see Figure 3). If the content of DATARD8 is 0x00, EEPROM checksum calculation indicated an error and the start-up procedure is failed. Correct EEPROM checksum calculation result is indicated by content of 0x01 in DATARD8.

2.2 Measurement Modes

SCP1000 pressure sensor measurement modes are presented in Table 2 below. In three of the measurement modes SCP1000 samples pressure and temperature continuously. In low power mode SCP1000 measures pressure and temperature once after the measurement is triggered.

Table 2. SCP1000 measurement modes.

Measurement mode	Activation code	Resolution	Measurement type
High resolution	0x0A	17 bits	Continuous
High speed	0x09	15 bits	Continuous
Ultra low power	0x0B	15 bits	Continuous
Low power	0x0C or TRIG pin	17 bits or 15 bits	Triggered

2.2.1 Measurement modes timing and real time constraints

2.2.1.1 Continuous measurement modes

In continuous measurement mode the output data is refreshed after each measurement and the availability of the updated pressure and temperature data is signaled through the assertion of the DRDY pin and a DRDY bit is set to '1' in the STATUS register.

In Figure 4 is presented the timing diagram in the continuous measurement modes.

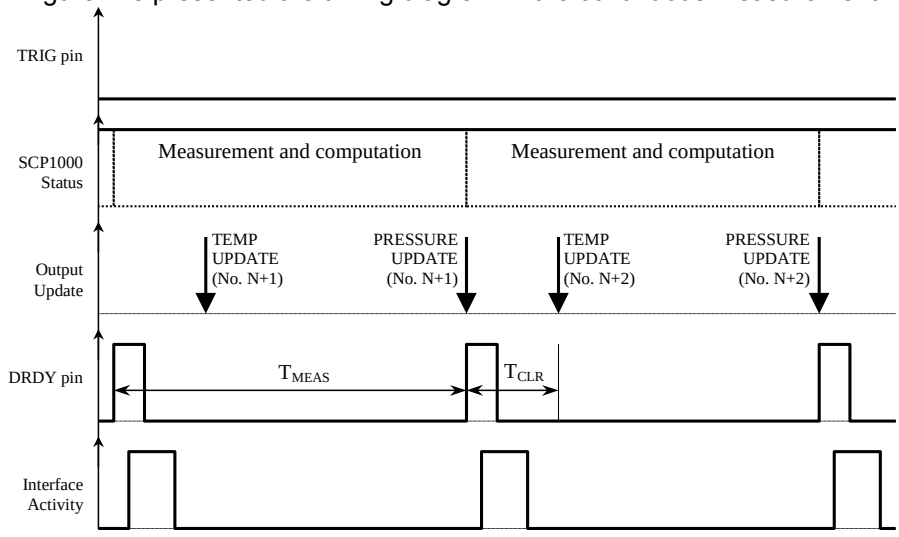


Figure 4. Timing diagram in continuous measurement mode.

In order to clear the DRDY signal, the host processor has to read the pressure output data. The temperature output data is updated before the pressure output data, thus the time to service the DRDY (T_{CLR} in Figure 4) is shorter than the measurement and computation time (T_{MEAS} in Figure 4).

In the case that the temperature data is not needed, the time for servicing the DRDY interrupt can be extended. In any case, the DRDY interrupt must be serviced (the pressure data reading has to be completed) before the next pressure data update.

If, for some reason, the real time requirement is not met, the output data will be overwritten and an RTERR error bit is set to '1' in the STATUS register. In order to clear the error status, the host processor has to read the output pressure data (this data can be invalid). Once the error has been cleared, normal operation can be continued.

2.2.1.2 Triggered (low power) measurement mode

In triggered measurement mode (low power) SCP1000 stays in standby mode until measurement is externally triggered, see section for more 2.2.4.4 details. The availability of updated pressure and temperature data is signaled as in continuous measurement modes (through the assertion of the DRDY pin and a DRDY bit is set to '1' in the STATUS register).

In Figure 5 is presented the timing diagram in the low power measurement mode (triggered).

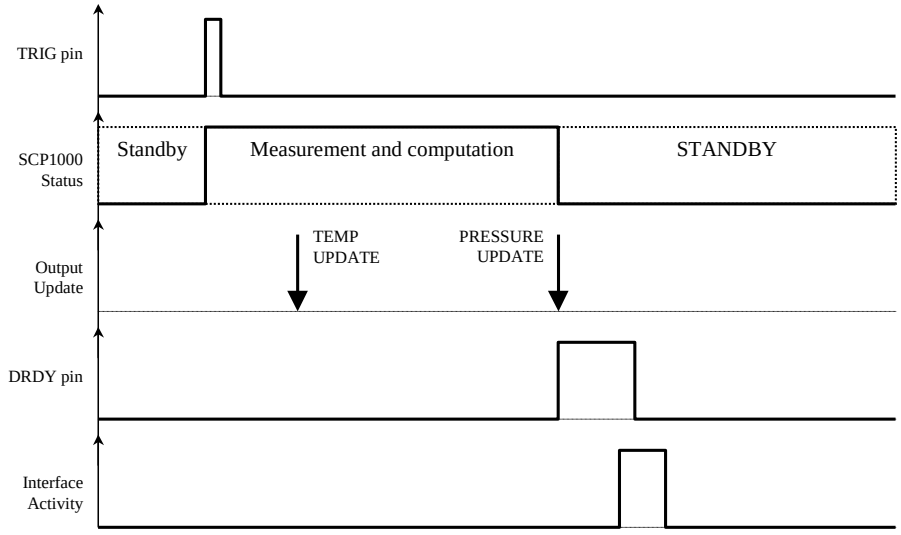


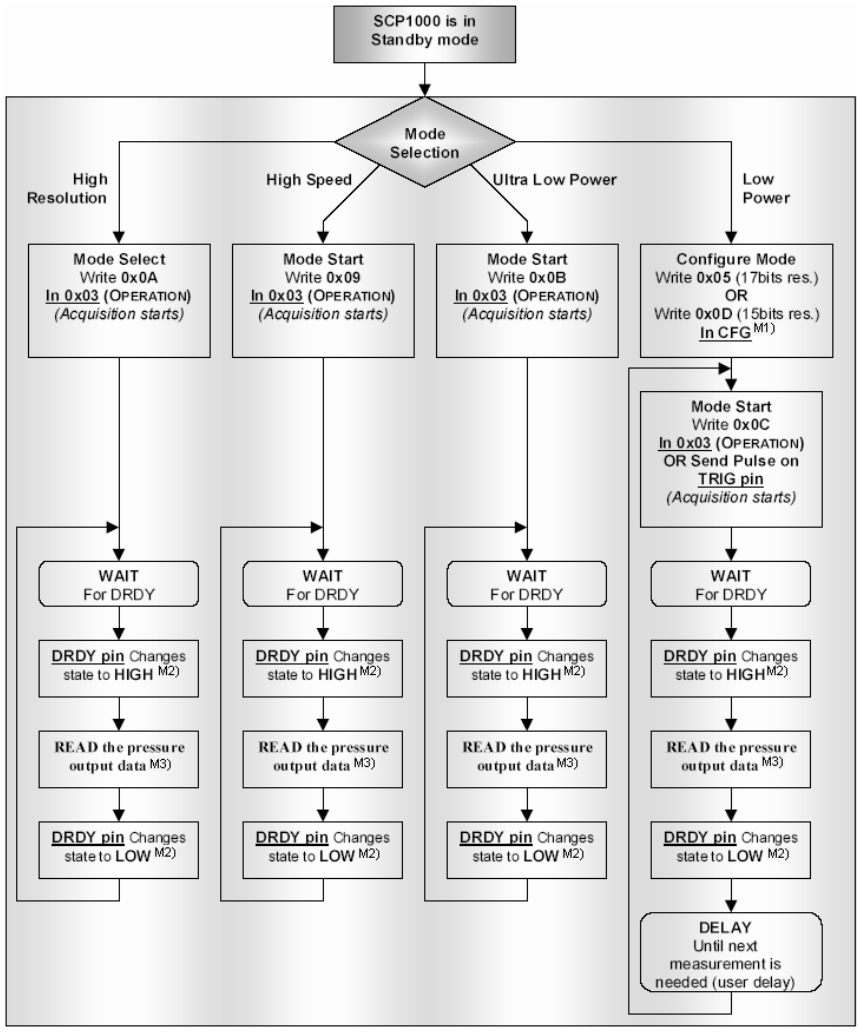
Figure 5. Timing diagram in triggered measurement mode.

See section 2.2.1.1 for details of clearing the DRDY signal and avoiding real time error.

The DRDY interrupt request has to be cleared before the next trigger signal is applied (rising edge at TRIG pin Figure 5).

2.2.2 Measurement mode selection

The selection and activation of the measurement mode is done by writing the corresponding mode activation code (see Table 2) in to OPERATION register, see section 3.2 for register details. The measurement mode selection and activation is illustrated in Figure 6 below.



M1) For details for low power mode resolution please refer to section 2.2.1.2.

M2) For details for DRDY signal please see Figure 4, Figure 5 and section 2.3.

M3) See section 2.2.3 for more details of reading the pressure and temperature

Figure 6. SCP1000 measurement mode selection.

2.2.2.1 Switching between measurement modes

In order to switch between the measurement modes, it is necessary first to stop the active mode before activating the new one by writing 0x00 in to OPERATION register. This will instruct SCP1000 to cancel the current operation (SCP1000 enters in to standby mode). After writing 0x00 to OPERATION register and before new measurement mode is activated there should be a 50 ms delay. Instead of the 50 ms delay, OPSTATUS register can be read. If OPSTATUS bit in OPSTATUS register is '0', new measurement mode can be activated as described in section 2.2.2 above (see Figure 6).

In order to avoid a real time error, it is strongly recommended to verify that the DRDY signal is low (no new data) before activating new mode. If DRDY is high it is necessary to read the output data before activating new measurement mode.

2.2.3 Reading the pressure and temperature

After the DRDY pin has signaled the availability of new measurement data, it is recommended that the output data is read immediately in the following order:

- read the TEMPOUT register (temperature data in bits [13:0] – in case the temperature data is not needed this step can be omitted).
- read the DATARD8 register (bits [2:0] contain the MSB of the pressure data)
- read the DATARD16 register (contains the 16 LSB of the pressure data)

For more details of pressure data bit level description, see section 3.2 (Table 12). Pressure data is presented in integer format. When operating within the nominal operation range (30…120 kPa) the output of the SCP1000 changes between 120000 and 480000. The output is converted from decimal format to [Pa] as follows:

Equation 1

$$Pres[Pa] = \frac{Pres[dec]}{4} = 0.25 \cdot Pres[dec],$$

where *Pres[dec]* is pressure read from SCP1000 in decimal format.

See section 3.1 (Table 13) for details more of temperature data bit level description. Temperature data is presented in 2's complement format and is converted from decimal format to [°C] as follows:

Equation 2

$$Temp[°C] = \frac{Temp[dec]}{20} = 0.05 \cdot Temp[dec]$$

where *Temp[dec]* is temperature read from SCP1000 in decimal format.

2.2.3.1 Examples of temperature conversion to [°C]

In case the sign bit is zero, '0' (see Table 3), the TEMPOUT binary value is converted to decimal value and then to [°C] as follows:

Table 3. An example TEMPOUT bit pattern of a positive temperature data.

	An example TEMPOUT bit pattern for positive temperature															
Bit#	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
~[°C]			s	204.8	102.4	51.2	25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1	0.05
Data bit #	x	x	s	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
TEMPOUT, raw data			0	0	0	0	1	0	0	0	1	0	1	1	1	0

s = sign bit
x = not used bit

The example binary value presented in Table 3 can be converted normally to decimal value because the sign bit is zero:

bin '00 0010 0010 1110' → dec '558'
→ conversion to [°C]: 558/20 = 27,9 °C

In case the sign bit is one, '1' (see Table 4), the TEMPOUT binary value is converted to decimal value and then to [°C] as follows (notice 2's complement format):

Table 4. An example TEMPOUT bit pattern of a negative temperature data.

	An example TEMPOUT bit pattern for negative temperature															
Bit#	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
~[°C]			s	204.8	102.4	51.2	25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1	0.05
Data bit #	x	x	s	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
TEMPOUT, raw data			1	1	1	1	1	1	1	0	0	1	0	1	0	0
TEMPOUT, inverted data			0	0	0	0	0	0	0	1	1	0	1	0	1	1
Add '1' (one LSB) to inverted TEMPOUT data																+1
Absolute value for TEMPOUT data			0	0	0	0	0	0	0	1	1	0	1	1	0	0

s = sign bit
x = not used bit

The raw TEMPOUT data (bin '11 1111 1001 0100') is not converted to decimal value because the sign bit is '1'. The bit pattern is first inverted (bin '00 0000 0110 1011') and then 1 LSB is added to the inverted bit pattern. The resulting bit pattern is presented in the last row of Table 4 (Absolute value for TEMPOUT data), which is converted normally to decimal value:

bin '00 0000 0110 1100' → dec '108' → dec '-108' (because sign bit is '1')
→ conversion to [°C]: -108/20 = -5,4 °C

2.2.4 Measurement mode details

In this section all measurement modes are described in detail.

2.2.4.1 High resolution measurement mode

In high resolution measurement mode pressure and temperature are measured continuously with the highest resolution. High resolution mode is activated by writing 0x0A in to OPERATION register. Once the mode has been started the only interface activity required is periodic reading of the output pressure and temperature registers (in applications where the temperature is not needed the output temperature reading can be omitted), see section 2.2.1.1.

SCP1000 operation parameters in high resolution measurement mode are presented in Table 5 below.

Table 5. SCP1000 operation parameters in high resolution mode.

Symbol	Parameter	Min	Typ	Max	Unit
V_{dd}	Supply voltage (AVDD & DVDD)	2.4	2.7	3.3	V
I_{dd}	Average supply current		25		µA
P_{res}	Pressure measurement resolution		17		bits
T_{res}	Temperature measurement resolution	–	14	–	bits
PWL	Pressure data output word-length	–	19	–	bits
TWL	Temperature data output word-length	–	14	–	bits
T_{meas}	Measurement and computation time		500		ms
F_{meas}	Output data refresh rate	1.6	1.8	2.0	Hz
T_{clr}	Maximum time for servicing the DRDY interrupt		55		ms

2.2.4.2 High speed measurement mode

In high speed measurement mode pressure and temperature are measured continuously the conversion time is shortened at the cost of output resolution. This allows an increased output refresh rate of approximately 9 Hz.

SCP1000 operation parameters in high speed measurement mode are presented in Table 6 below.

Table 6. SCP1000 operation parameters in high speed mode.

Symbol	Parameter	Min	Typ	Max	Unit
V_{dd}	Supply voltage (AVDD & DVDD)	2.4	2.7	3.3	V
I_{dd}	Average supply current		25		µA
P_{res}	Pressure measurement resolution		15		bits
T_{res}	Temperature measurement resolution	–	14	–	bits
PWL	Pressure data output word-length	–	19	–	bits
TWL	Temperature data output word-length	–	14	–	bits
T_{meas}	Measurement and computation time		140		ms
F_{meas}	Output data refresh rate	7.9	9	10.2	Hz
T_{clr}	Maximum time for servicing the DRDY interrupt		25		ms

2.2.4.3 Ultra low power measurement mode

In ultra low power measurement mode the device performs measurements continuously with the lowest resolution (15 bits) and switches to standby mode between measurements. In this mode the updated pressure data is available approximately once per second. The average current consumption is in the range of 3.5 µA.

SCP1000 operation parameters in ultra low power measurement mode are presented in Table 7 below.

Table 7. SCP1000 operation parameters in ultra low power mode.

Symbol	Parameter	Min	Typ	Max	Unit
V_{dd}	Supply voltage (AVDD & DVDD)	2.4	2.7	3.3	V
I_{dd}	Average supply current		3.5		µA
P_{res}	Pressure measurement resolution		15		bits
T_{res}	Temperature measurement resolution	–	14	–	bits
PWL	Pressure data output word-length	–	19	–	bits
TWL	Temperature data output word-length	–	14	–	bits
F_{meas}	Output data refresh rate		1		Hz
T_{clr}	Maximum time for servicing the DRDY interrupt		500		ms

2.2.4.4 Low power measurement mode

In low power measurement mode SCP1000 stays in standby mode until measurement is externally triggered. The measurement is triggered with rising edge of TRIG pin or by writing 0x0C to OPERATION register. Low power measurement can be triggered after start-up and power down. If some other measurement mode is activated, see section 2.2.2.1 for details of switching between measurement modes.

The default measurement resolution for low power mode is 17 bits. Resolution can be configured to 15 bit or 17 bit mode through indirect CFG register (see section 3.3). The CFG register contents are presented in Table 8 below.

Table 8. Recommended CFG register contents.

Resolution	CFG register content
17 bits (default)	0x05
15 bits	0x0D

SCP1000 operation parameters in low power measurement mode are presented in Table 9 below.

Table 9. SCP1000 operation parameters in low power mode.

Symbol	Parameter	Min	Typ		Max	Unit
			15 bits	17 bits		
V_{dd}	Supply voltage (AVDD & DVDD)	2.4	2.7		3.3	V
I_{dd}	Average supply current	1	Depends on resolution and trigger frequency		25	µA
P_{res}	Pressure measurement resolution		15	17		bits
T_{res}	Temperature measurement resolution	–	14		–	bits
PWL	Pressure data output word-length	–	19		–	bits
TWL	Temperature data output word-length	–	14		–	bits
T_{meas}	Measurement and computation time		140	500		ms
F_{trig}	Maximum trigger frequency		9	1.8		Hz
T_{clr}	Maximum time for servicing the DRDY interrupt	Before the next TRIG signal				-

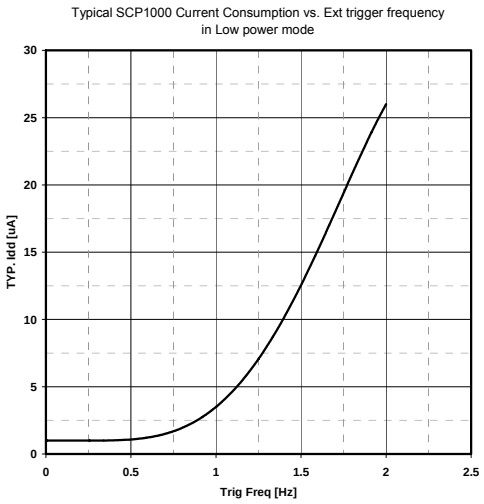


Figure 7. Typical current consumption in low power mode with 17 bit resolution.

2.3 Over Pressure

When operating within the nominal operation range (30…120 kPa) the output of the SCP1000 changes between 120000 and 480000. In major over pressure situations (over 131 kPa), a sudden drop of the output reading can be observed, since the SCP1000 pressure output is not limited.

2.4 DRDY – data ready pin

Availability of updated pressure and temperature data is signaled through the assertion of the DRDY pin. DRDY is cleared after the DATARD16 register is read, see section 2.2.1 for more detailed information.

2.5 TRIG – trigger pin

TRIG pin is used to trig the measurement in low power measurement mode (external trigger). The µC has to actively drive the signal in high and low states. In applications where the TRIG signal is not used it has be connected to DVSS. See section 2.2.4.4 for more detailed information.

2.6 Power Down Mode and PD Pin

In order to decrease further the current consumption in cases where there are long time intervals between the measurements, SCP1000 has a built in power down mode, which can be activated through the PD pin. SCP1000 will stay in power down mode as long as the PD signal is high. In power down mode every digital output pin of SCP1000 tristates.

After PD signal changes back to low, SCP1000 powers up, performs initialization and is ready to operate. Start-up sequence has to be executed always after power down mode, see section 2.1 for more detailed information.

The advantage of using power down mode instead of switching off the supply is that during wake-up from power down there is no need to recharge the filter capacitors on AVDD and DVDD lines. The µC has to actively drive the signal in high and low states. In applications where the PD signal is not used it has to be connected to DVSS.

The current consumption of SCP1000 in power down mode is typically 0.2 µA.

2.7 Standby Mode

SCP1000 is in standby mode after start-up, when OPERATION register content is 0x00 and in ultra low power measurement mode between the measurements. The average current consumption is in the range of 1 µA.

2.8 Reset

SCP1000 ASIC software can be reseted by writing 0x01 in to RSTR register. After reset the RSTR register content is set to 0x00 and the default values are loaded from EEPROM. The start-up sequence should be followed from section 2.1.2 onwards after reset.

2.9 Clock

The SCP1000 pressure sensor is operated with internal clock, so external clock signal is not needed.

3 Addressing Space

SCP1000 register contents and bit definitions are described in more detail in next sections. All registers are read and written through the serial host interface.

3.1 Register Description

SCP1000 register types:

- direct access registers,
- indirect access registers and
- EEPROM registers.

Table 10. List of SCP1000 direct and indirect access registers and EEPROM registers.

Address		Name	Description	Mode (R, W, RW)	Register access	Width[bits]
SPI	TWI					
0x00		REVID	ASIC revision number	R	Direct	8
0x01		DATAWR	Indirect register access data	RW	Direct	8
0x02		ADDPTR	Indirect register access pointer	RW	Direct	8
0x03		OPERATION	Operation register	RW	Direct	8
0x04		OPSTATUS	Operation status	R	Direct	8
0x06		RSTR	ASIC software reset	W	Direct	8
0x07		STATUS	ASIC top-level status	R	Direct	8
0x1F	0x7F	DATARD8	Pressure output data (MSB) or 8 bit data read from EEPROM	R	Direct	8
0x20	0x80	DATARD16	Pressure output data (LSB) or 8-bit data read from indirect register	R	Direct	16
0x21	0x81	TEMPOUT	14-bit temperature output data	R	Direct	16
0x00		CFG	Configuration register	RW	Indirect	8
0x05		TWIADD	TWI address	W	Indirect	8
0x29		USERDATA1	User data	RW	EEPROM	8
0x2A		USERDATA2	User data	RW	EEPROM	8
0x2B		USERDATA3	User data	RW	EEPROM	8
0x2C		USERDATA4	User data	RW	EEPROM	8

Register address in hex format.
RW – Read / Write register, R – Read only register.

3.2 Direct Access Registers

SCP1000 direct access register contents and bit definitions are described in this section. Direct access registers can be accessed directly through the serial interface.

Address: **0x00**
Register name: **REVID**, ASIC revision number

Bits	Mode	Initial Value	Name	Description
7:0	R	03h	REVID	ASIC revision number

Address: **0x01**
Register name: **DATAWR**, indirect register data

Bits	Mode	Initial Value	Name	Description
7:0	WR	00h	DATA	Indirect access data

Address: **0x02**
Register name: **ADDPTR**, indirect register address (address pointer)

Bits	Mode	Initial Value	Name	Description
7:0	WR	00h	ADDR	Indirect register address

Address: **0x03**
Register name: **OPERATION**, operation register

Bits	Mode	Initial Value	Name	Description
7:0	WR	00h	OPERATION	See operation description in Table 11.

Table 11. Description for register contents in OPERATION register.

Operation	Description
0x00	No operation / cancel current operation (standby mode). Default value after start-up, power down mode and reset.
0x01	Read indirect access register pointed by ADDPTR. Register contents is available in DATARD16 in bits [7:0].
0x02	Write DATAWR contents in to the indirect access register pointed by ADDPTR.
0x05	Read EEPROM register pointed by ADDPTR. Register contents is available in DATARD8 in bits [7:0].
0x06	Write DATAWR contents in to the EEPROM register pointed by ADDPTR.
0x07	Perform INIT sequence: INIT values are downloaded from the EEPROM to the processing unit. After the INIT sequence is over the INIT status is present at DATARD8: - DATARD8 = 0x01 → success - DATARD8 = 0x00 → fail – checksum error
0x09	High speed acquisition mode start (continuous measurement). Use operation 0x00 to stop the continuous acquisition
0x0A	High resolution acquisition mode start (continuous measurement). Use operation 0x00 to stop the continuous acquisition
0x0B	Ultra low power acquisition mode start (continuous measurement). Use operation 0x00 to stop the continuous acquisition
0x0C	Low power acquisition start (perform single temperature and pressure measurement, equivalent to external TRIG pin)
0x0F	ASIC self test. After the self test is over the result is present at DATARD8: - DATARD8 = 0x01 → self test successful - DATARD8 = 0x00 → self test failed
Others	Reserved

Address: **0x04**
Register name: **OPSTATUS**, operation status

Bits	Mode	Initial Value	Name	Description
7:1				Reserved
0	R	0	OPSTATUS	Operation status 0 – operation finished, results are available 1 – operation running

Address: **0x06**
Register name: **RSTR**, ASIC software reset

Bits	Mode	Initial Value	Name	Description
7:0	W	0x00	RSTR	ASIC software reset 0x00 – do not reset 0x01 – reset ASIC software (see section 2.8 for more details), other combinations are reserved.

Address: **0x07**
Register name: **STATUS**, ASIC top-level status

Bits	Mode	Initial Value	Name	Description
7				Reserved
6	R	0	EXT TRIGGED	Status due external trigger 0 – externally triggered acquisition is finished 1 – externally triggered acquisition is running
5	R	0	DRDY	Data ready (same behavior as DRDY-pin) 0 – no new results are available 1 – new results are available
4	R	0	RTERR	Real time error 0 – no real time error 1 – real time error (interrupt has not been serviced in time, cleared by DATARD16 read operation)
3:1				Reserved
0	R	0	STARTUP	Start-up status 0 – start-up procedure is finished 1 – start-up procedure is running

SPI address: **0x1F**
TWI address: **0x7F**
Register name: **DATARD8**, pressure data MSB or 8 bit data read from EEPROM

Bits	Mode	Initial Value	Name	Description
7:3				Reserved
2:0	R	000	PRES_MSB	Pressure data MSB (3 bits)
7:0	R	00h	DATA	8 bit data from EEPROM register

If EEPROM register is read the content of the DATARD8 register is the EEPROM register content. Otherwise pressure data MSB (bits [2:0]) can be read from DATARD8.

SPI address: **0x20**
TWI address: **0x80**
Register name: **DATARD16**, pressure data LSB or 8 bit data read from indirect register

Bits	Mode	Initial Value	Name	Description
15:0	R	0000h	PRES_LSB	Pressure data LSB (16 bits)
15:8				Reserved
7:0	R	00h	DATA	8 bit data from indirect register

If indirect register is read the content of the DATARD16 register is the indirect register content (bits [7:0]). Otherwise pressure data LSB (bits [15:0]) can be read from DATARD16.

Bit level description for pressure data from registers DATARD8 and DATARD16 is presented in Table 12 below. Pressure information is presented in integer format. See section 2.2.3 (Equation 1) for more detailed information of converting the pressure data in to Pascal, [Pa].

Table 12. Bit level description of pressure data.

	DATARD8			DATARD16														
Bit#	B2	B1	B0	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
~[Pa]	64K	32K	16K	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	0.5	0.25
Data bit #	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

SPI address: **0x21**
TWI address: **0x81**
Register name: **TEMPOUT**, temperature in 2's complement format

Bits	Mode	Initial Value	Name	Description
15:14				Reserved
13:0	R	0000h	TEMP	Temperature output data

Bit level description for temperature data from register TEMPOUT is presented in Table 13 below. See section 2.2.3 (Equation 2) for more detailed information of converting the temperature data in to [°C].

Table 13. Bit level description of1 temperature data.

	TEMPOUT															
Bit#	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
~[°C]			s	204.8	102.4	51.2	25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1	0.05
Data bit #	x	x	s	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

s = sign bit
x = not used bit

3.3 Indirect Access Registers

SCP1000 indirect access register contents and bit definitions are described in this section. Indirect access registers can be accessed through the serial interface using the OPERATION, DATAWR, ADDPTR and DATARD16 registers (see section 3.3.1).

Address: **0x00**
Register name: **CFG**, configuration register

Bits	Mode	Initial Value	Name	Description, INDIRECT ACCESS
7:0	RW	0x05		Low power mode resolution selection: 0x05 – high resolution selected (17 bits) 0x0D – low resolution selected (15 bits) other combinations are reserved.

Address: **0x05**
Register name: **TWIADD**, TWI device address

Bits	Mode	Initial Value	Name	Description, INDIRECT ACCESS
7:0	W	11h	TWIADD	TWI device address

3.3.1 Example of indirect access register write and read operations

Example of indirect access register WRITE operation (write 0x0D to indirect register CFG, 0x00):

- Write 0x00 in direct register ADDPTR (0x02)
- Write 0x0D in direct register DATAWR (0x01)
- Write 0x02 in direct register OPERATION (0x03)
- Wait 50 ms

Example of indirect access register READ operation (read indirect register CFG, 0x00):

- Write 0x00 in direct register ADDPTR (0x02)
- Write 0x01 in direct register OPERATION (0x03)
- Wait 5 ms
- Read direct register DATARD16 (0x20 for SPI, 0x80 for TWI), bits [15:8] should be treated as zeros, the register content is in bits [7:0], see section 3.2 for further information.

3.4 EEPROM memory

SCP1000 has internal non-volatile memory for calibration and configuration data. Memory content will be programmed during production. Initial configuration is loaded during sensor start-up.

EEPROM register contents and bit definitions are described in this section. User has access to 4 EEPROM registers. EEPROM registers can be accessed through the serial interface using the OPERATION, DATAWR, ADDPTR and DATARD8 registers (see sections 3.4.1 and 3.4.2).

Address: **0x29**
Register name: **USERDATA1**, user accessible EEPROM register

Bits	Mode	Initial Value	Name	Description
7:0	RW	00h	USERDATA1	User accessible EEPROM register

Address: **0x2A**
Register name: **USERDATA2**, user accessible EEPROM register

Bits	Mode	Initial Value	Name	Description
7:0	RW	00h	USERDATA2	User accessible EEPROM register

Address: **0x2B**
Register name: **USERDATA3**, user accessible EEPROM register

Bits	Mode	Initial Value	Name	Description
7:0	RW	00h	USERDATA3	User accessible EEPROM register

Address: **0x2C**
Register name: **USERDATA4**, user accessible EEPROM register

Bits	Mode	Initial Value	Name	Description
7:0	RW	00h	USERDATA4	User accessible EEPROM register

3.4.1 EEPROM writing

Please note that in order to guarantee reliable EEPROM writing operation it is very critical to follow the requirements below. The minimum value for supply voltage at +25 °C temperature is 3.0 V during EEPROM register write operation. The peak current consumption is also significantly higher than in normal operation (~2 mA for 15 ms period per byte).

Example of WRITE operation to EEPROM register 0x29 (write 0xAA to EEPROM register 0x29):

- Write 0x29 in direct register ADDPTR (0x02)
- Write 0xAA in direct register DATAWR (0x01)
- Write 0x06 in direct register OPERATION (0x03)
- Wait 50 ms

3.4.2 EEPROM reading

The EEPROM can be read with nominal supply voltage, but the peak current consumption is significantly higher than in normal operation (~1.5 mA for 20 µs period per byte).

Example of READ operation from EEPROM register 0x29 (read EEPROM register 0x29):

- Write 0x29 in direct register ADDPTR (0x02)
- Write 0x05 in direct register OPERATION (0x03)
- Wait 15 ms (minimum wait value)
- Read direct register DATARD8 (0x1F for SPI, 0x7F for TWI), the register content is in bits [7:0], see section 3.2 for further information.

4 Serial Interfaces

Communication between SCP1000 sensor and master controller is based on serial data transfer and dedicated interrupt line (DRDY-pin). Depending on operation mode an external trigger pin (TRIG) can also be used in serial interfacing. Two different serial interfaces are available for SCP1000 sensor: SPI and TWI (very similar to I^2C). However, only one interface per product is enabled by pre-programming in the factory. SCP1000 acts as a slave on both SPI and TWI bus.

4.1 SPI Interface

The SPI interface is a full duplex 4 wire serial interface. The connection between the µC and SCP1000 is done using MOSI, MISO, SCK and CSB. CSB selects the chip on multi-chip SPI bus, SCK is the serial data clock, MOSI is the data line from master to slave (Master Out Slave In) and MISO is data line from slave to master (Master In Slave Out). SCP1000 is configured to SPI slave mode (see Figure 8).

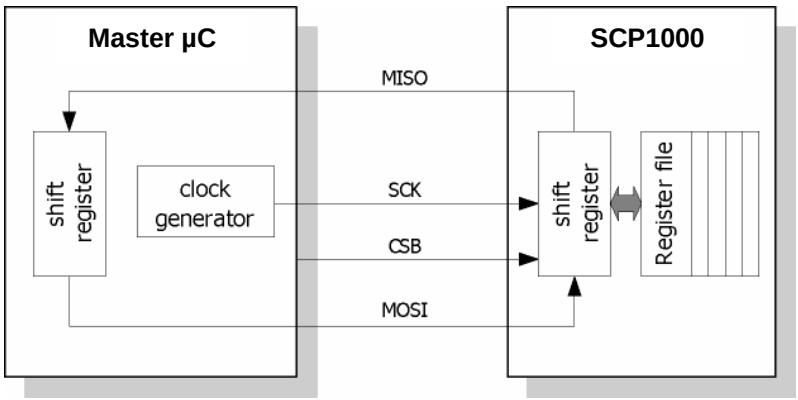


Figure 8. SPI master slave configuration.

4.1.1 SPI frame format

The SCP1000 SPI frame format is presented in Figure 9 below.

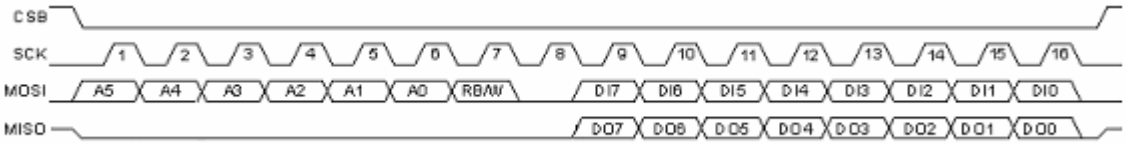


Figure 9. SPI frame format for two 8 bit words.

Each SPI communication frame contains two or three 8 bit words: the first word defines the register address (6 bits wide, bits [A5:A0] in Figure 9) followed by the type of access ('0' = Read or '1' = Write) and one zero bit (bit 0, LSB). The following word(s) contain the data being read or written. The MSB of the words are sent first. Bits from MOSI line are sampled in on the rising edge of SCK and bits to MISO line are latched out on falling edge of SCK.

The CSB line must stay low during the entire frame accesses, i.e. between the bytes. If the CSB line state changes to high, the access is terminated. The CSB has to be pulled up after each communication frame.

4.1.2 Examples of SPI communication

Examples SPI communication (8 and 16 bit read / write operations) are presented in Figure 10 below.

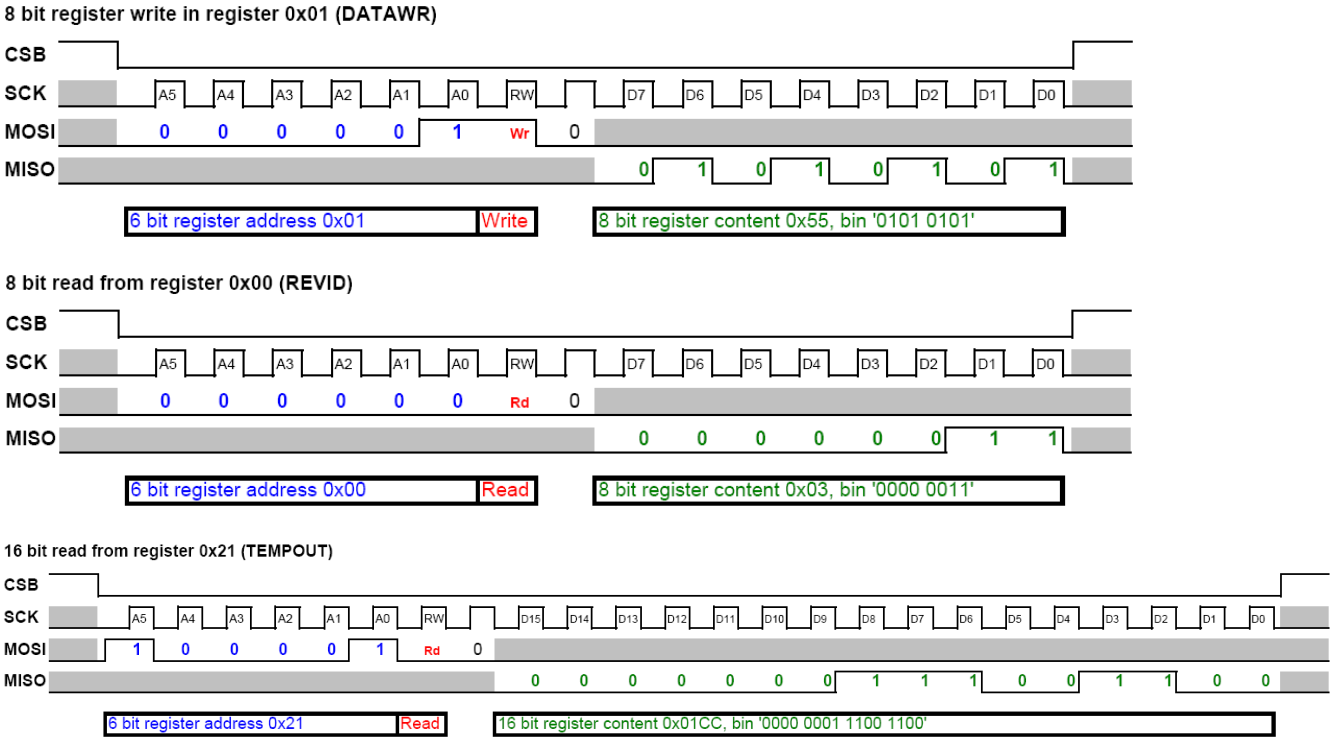


Figure 10. SPI communication examples.

4.2 TWI Interface

TWI is a 2-wire half-duplex serial interface. It consists of one master device and one or more slave devices. The master is defined as a micro controller providing the serial clock (SCL), and the slave as any integrated circuit receiving the SCL clock from the master. The SCP1000 sensor always operates as a slave device in master-slave operation mode. When in SPI interface a hardware addressing is used (slaves have dedicated CSB signals), the TWI interface uses a software based addressing (slave devices have dedicated bit patterns as addresses). Seven bit device addressing is used with SCP1000. The default TWI device address for SCP1000 is 0x11, b'001 0001' (pre-programmed during SCP1000 production).

The two wires in TWI bus are:

- SCL, serial clock and
- SDA, bi-directional data line.

The SCL pin of SCP1000 is an input pin (SCP1000 never controls the SCL line). Data is transferred in and out of the sensor through the bi-directional SDA pin. SDA has an open-drain output, so an external pull-up resistor to DVDD is required (see Figure 11). The minimum value for SDA pull-up resistor is 2 kΩ.

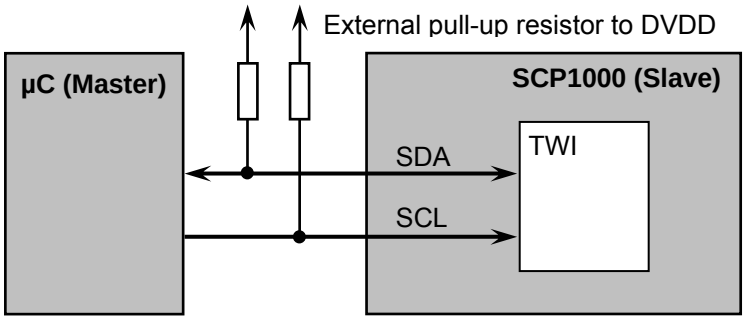
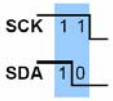


Figure 11. TWI master slave configuration.

External pull-up resistor from SCL to DVDD is not needed if master drives SCL actively to high and low states. There is no de-bouncing is implemented in the SCP1000 digital I/O pads, so the signals on SDA and SCL must be clean.

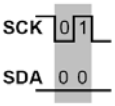
4.2.1 TWI frame format

TWI transactions are based on a byte-long transfers separated by acknowledgements. Bits from SDA line are sampled in on the rising edge of SCL and bits to SDA line are latched out on falling edge of SCL. Master starts and stops the communication by sending start and stop bits. After start bit master sends device TWI device address. The communication continues with predefined frame format. General patterns of TWI frame format are described below.



START BIT (µC → SCP1000)
The start bit is a high to low transition on SDA, while SCL is high. When the master issues a start bit, it takes the control of the bus.

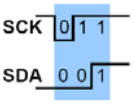
SLAVE DEVICE ADDRESS (µC → SCP1000)
Master sends a 7 bit slave device address, bits [7:1], MSB first. SCP1000 device address is 0x11, b'001 0001' by default. The LSB (bit 0) indicates the type of access ('1' = Read or '0' = Write).



ACKNOWLEDGE BIT
The transmitter of the acknowledge bit must tie the SDA line to low to perform an acknowledgement. The receiver of the acknowledge bit must release the SDA line because at this time, it is not the master of the TWI bus. The receiver then checks the acknowledge bit by reading a '0' on SDA.

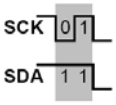
REGISTER ADDRESS (µC → SCP1000)
Master sends register address to SCP1000 MSB first.

REGISTER DATA (SCP1000 → µC)
The SCP1000 registers can be 8 or 16 bits wide. An 8 bit write is performed by sending MSB first. A 16 bits write is performed by sending two bytes (MSB first). After each byte, the slave sends an acknowledgement bit.



STOP BIT (µC → SCP1000)
The stop bit is a low to high transition on SDA, while SCL is high. The master, who has generated the stop bit, sets the bus free.

REPEATED START (µC → SCP1000)
A repeated start is a start signal generated by a master, which has already taken the control of the TWI bus. It is used by the master to initiate a transfer with a new slave, or with the same slave, in the other communication mode (transmit or receive mode), without releasing the bus.



NOT ACKNOWLEGDE BIT:
If the receiver of the acknowledge bit reads a '1' on SDA line during an acknowledge clock pulse, that means transmitter did not acknowledge. The master uses the not acknowledge bit to terminate a read action.

4.2.1.1 TWI write sequence

8 bit TWI write sequence is presented in Figure 13 and described below:

1. **START BIT** (to initiate a transmission, the master sends a start bit)
2. **SLAVE DEVICE ADDRESS** (slave device address with WRITE access → LSB = '0')
3. **SLAVE ACKNOWLEDGEMENT** (having identified device address as its own, slave acknowledges by sending an acknowledge bit)
4. **REGISTER ADDRESS** (the 8 bit address of the register to be written, MSB first)
5. **SLAVE ACKNOWLEDGEMENT** (the slave sends an acknowledgement bit)
6. **REGISTER DATA** (master sends the data to be written to the addressed register)
7. **SLAVE ACKNOWLEDGEMENT** (after receiving the byte, the slave sends an acknowledgement bit)
8. **STOP BIT** (master sets the bus free)

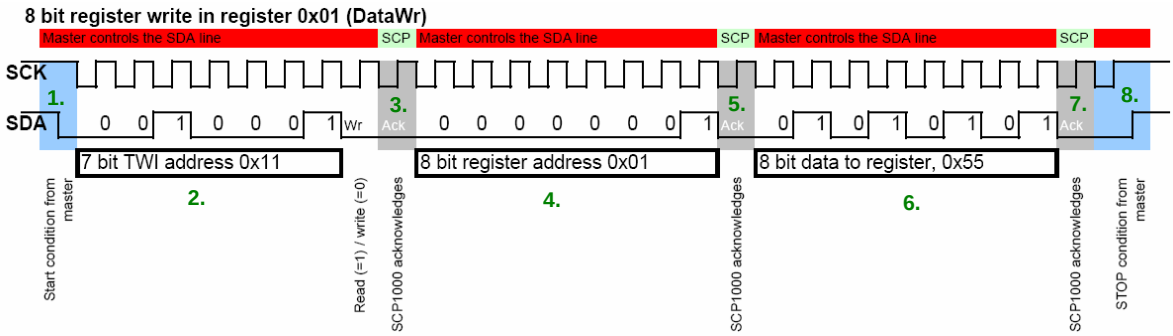


Figure 13. TWI frame format for 8 bit write operation (numbers from 1 to 8 refer to list above).

4.2.1.2 8 bit TWI read sequence

8 bit TWI read sequence is presented in Figure 14 and described below:

9. **START BIT** (to initiate a transmission, the master sends a start bit)
10. **SLAVE DEVICE ADDRESS** (slave device address with WRITE access → LSB = '0')
11. **SLAVE ACKNOWLEDGEMENT** (having identified device address as its own, slave acknowledges by sending an acknowledge bit)
12. **REGISTER ADDRESS** (the 8 bit address of the register to be read, MSB first)
13. **SLAVE ACKNOWLEDGEMENT** (the slave sends an acknowledgement bit)
14. **REPEATED START** (from master)
15. **SLAVE DEVICE ADDRESS** (slave device address with READ access → LSB = '1')
16. **SLAVE ACKNOWLEDGEMENT** (the slave acknowledges)
17. **REGISTER DATA** (the master continues sending the SCK pulses as slave sends the defined register content to SDA line)
18. **MASTER NOT ACKNOWLEDGE** (master terminates the data transfer by sending not acknowledge bit)
19. **STOP BIT** (master sets the bus free)

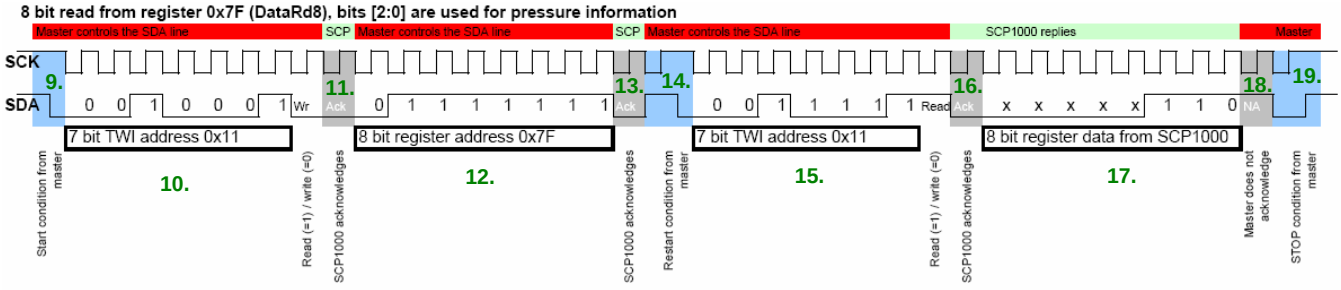


Figure 14. TWI frame format for 8 bit read operation (numbers from 9 to 19 refer to list

4.2.1.3 16 bit TWI read sequence

16 bit TWI read sequence is presented in Figure 15 and described below:

20. **START BIT** (to initiate a transmission, the master sends a start bit)
21. **SLAVE DEVICE ADDRESS** (slave device address with WRITE access → LSB = '0')
22. **SLAVE ACKNOWLEDGEMENT** (having identified device address as its own, slave acknowledges by sending an acknowledge bit)
23. **REGISTER ADDRESS** (the 8 bit address of the register to be read, MSB first)
24. **SLAVE ACKNOWLEDGEMENT** (the slave sends an acknowledgement bit)
25. **REPEATED START** (from master)
26. **SLAVE DEVICE ADDRESS** (slave device address with READ access → LSB = '1')
27. **SLAVE ACKNOWLEDGEMENT** (the slave acknowledges)
28. **MSB BYTE OF REGISTER DATA** (the master continues sending the SCK pulses as slave sends the defined register MSB content to SDA line)
29. **MASTER ACKNOWLEDGEMENT** (the master acknowledges after it has received the first 8 bit byte of register content)
30. **LSB BYTE OF REGISTER DATA** (the master continues sending the SCK pulses as slave sends the defined register LSB content to SDA line)
31. **MASTER NOT ACKNOWLEDGE** (master terminates the data transfer by sending not acknowledge bit)
32. **STOP BIT** (master sets the bus free)

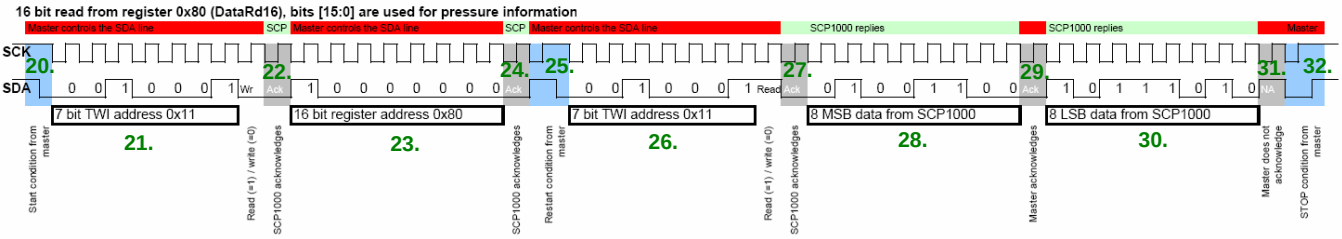


Figure 15. TWI frame format for 16 bit read operation (numbers from 20 to 32 refer to list above).

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

The absolute maximum ratings of SCP1000 are presented in Table 14 below.

Table 14. Absolute maximum ratings of SCP1000.

Parameter	Value	Unit
Supply voltage (V_{dd})	-0.3 to +3.6	V
Voltage at input / output pins[1]	-0.3 to (V_{dd} + 0.3)	V
ESD (Human body model)	±2.0	kV
Storage temperature	-30 … +85	°C
Proof pressure	2.0	MPa
Ultrasonic cleaning	Not allowed	

[1]Referred to DVDD

5.2 Power Supply

The analog and digital supply voltage levels (AVDD and DVDD) should always be equal.

5.3 Digital I/O Specification

5.3.1 Digital I/O characteristics

SCP1000 has no pull-up/down resistors in any pins.

Table 15. Characteristics of digital I/O pins.

	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input: CSB, MOSI, SCK/SCL, TRIG, PD							
1	Input high voltage		V_{IH}	0.7*DVDD			V
2	Input low voltage		V_{IL}			0.3*DVDD	V
3	Hysteresis		V_{HYST}	0.1*DVDD			V
4	Absolute maximum value of input peak current		$\|I_{in}\|$			1	µA
5	Input capacitance		C_{in}		1.6		pF
6	TRIG pulse width	Figure 16	T_{wtrig}	200			ns
Output terminal: MISO/SDA, DRDY							
7	Output high voltage	$\|I_{out}\|$ = 1 mA	V_{OH}	0.8*DVDD		DVDD	V
8	Output low voltage	$\|I_{out}\|$ = 1 mA	V_{OL}	0		0.2*DVDD	V
9	Absolute value of output current		$\|I_{out}\|$			1	mA
10	Load capacitance		C_{out}			50	pF

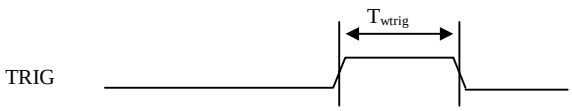


Figure 16. TRIG pulse timing.

5.3.2 SPI AC characteristics

The AC characteristics of the SPI interface are defined below in Figure 17 and Table 16. All the timing parameters are relative to 10% (falling edge) and 90% (rising edge) of signal maximum level.

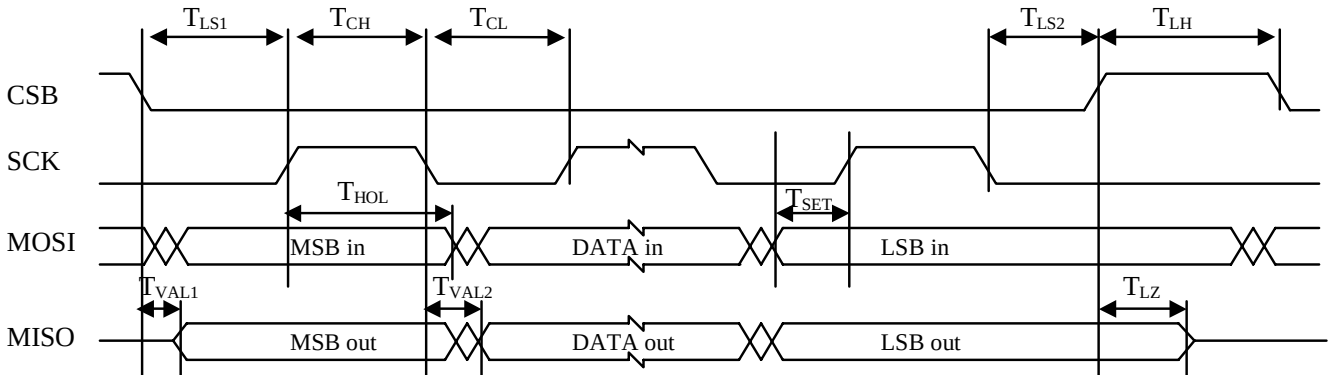


Figure 17. Timing diagram for SPI communication.

Table 16. AC characteristics of SPI communication.

	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Terminal CSB, SCK							
1	Time from CSB to SCK		T_{LS1}	100			ns
2	Time from SCK to CSB		T_{LS2}	100			ns
Terminal SCK							
3	SCK low time		T_{CL}	100			ns
4	SCK high time		T_{CH}	100			ns
5	SCK Frequency		Fsck			1	MHz
Terminal MOSI, SCK							
6	Time from MOSI to SCK. Data setup time		T_{SET}	20			ns
7	Time from SCK to MOSI. Data hold time		T_{HOL}	20			ns
Terminal MISO, CSB							
8	Time from CSB to stable MISO	Load capacitance at MISO < 20 pF	T_{VAL1}		100		ns
9	Time from CSB to high impedance state of MISO	Load capacitance at MISO < 20 pF	T_{LZ}		100		ns
Terminal MISO, SCK							
10	Time from SCK to stable MISO	Load capacitance at MISO < 20 pF	T_{VAL2}		50		ns
Terminal MOSI, CSB							
11	Time between SPI cycles, CSB at high level		T_{LH}	100			ns

5.3.3 TWI AC characteristics

The AC characteristics of the TWI interface are defined below in and. All the timing parameters are relative to 10% (falling edge) and 90% (rising edge) of signal maximum level.

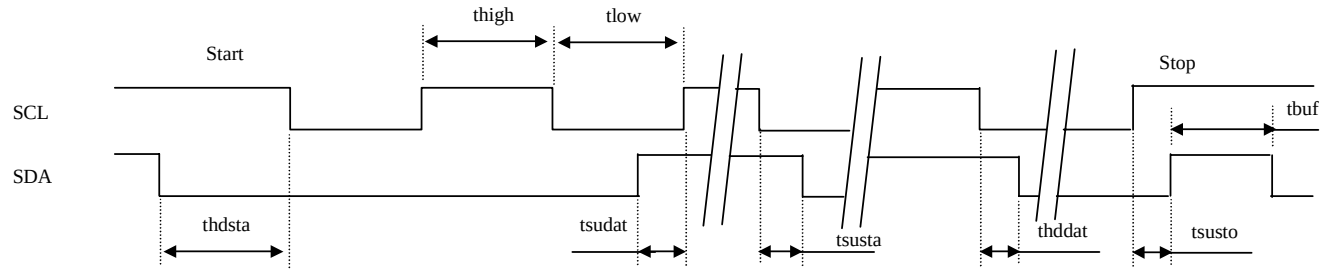


Figure 18. Timing diagram for TWI communication.

Table 17 AC characteristics of TWI communication.

	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
1	Hold time start condition		T_{hdsta}	600			ns
2	SCL frequency		F_{scl}			400	kHz
3	SCL high		T_{high}	1300			ns
4	SCL low		T_{low}	600			ns
5	Setup time for repeated start		T_{susta}	600			ns
6	Time from SCL to SDA: data hold time		T_{hddat}	300			ns
7	Time from SDA to SCL: data setup		T_{sudat}	100			ns
8	Time from SCL to SDA: data hold		T_{susto}	600			ns
9	Bus free time between a START and a STOP		T_{buf}	1300			ns

6 Package Characteristics

6.1 Dimensions

SCP1000 package dimensions are presented in Figure 19 below (dimensions in [mm]).

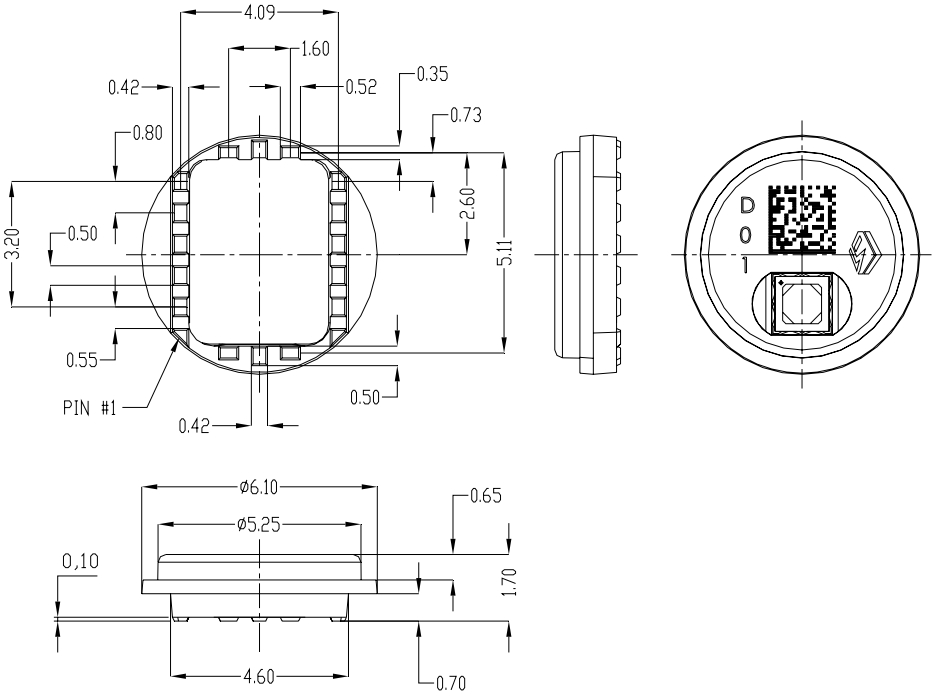


Figure 19. SCP1000 package dimensions.

7 Application Information

7.1 Pin Description

SCP1000 pin numbers are presented in Figure 20 below and pin descriptions in Table 18. Dummy pads in Figure 20 must be soldered also.

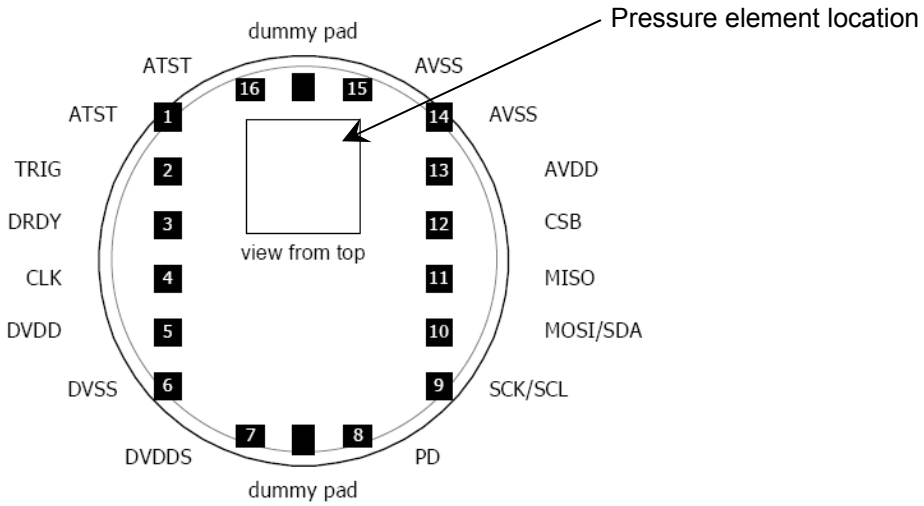


Figure 20. SCP1000 pin numbers.

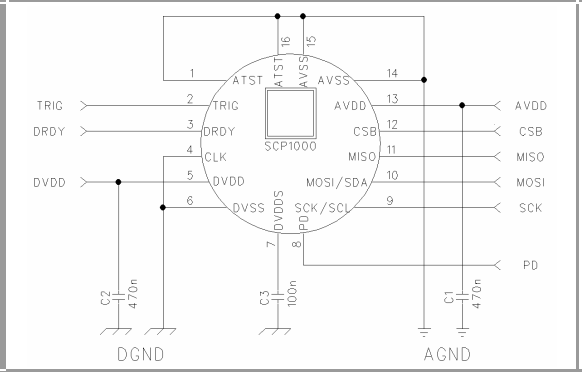
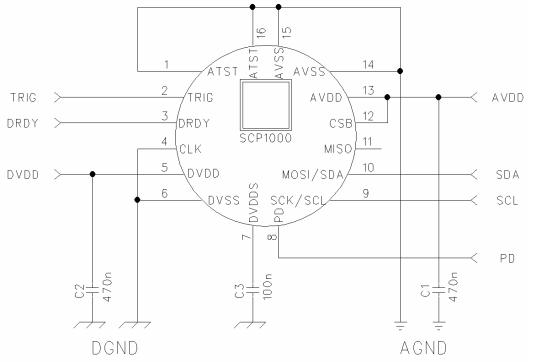
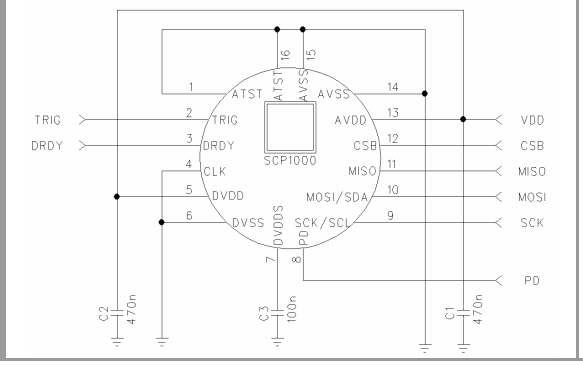
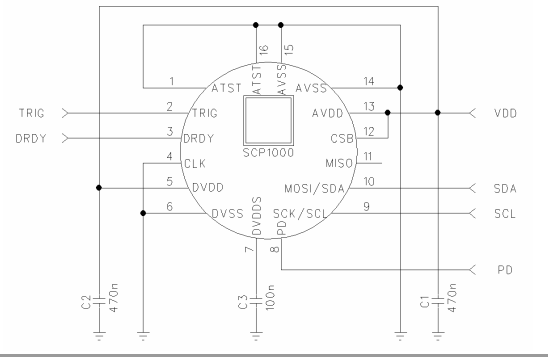
Table 18. SCP1000 pin description.

Pin #	Name	SCP1000-D01 (SPI)	SCP1000-D11 (TWI)
1	ATST	Connect to analog ground	Connect to analog ground
2	TRIG	Trigger input, connect to GND if not used	Trigger input, connect to GND if not used
3	DRDY	Interrupt signal (data ready)	Interrupt signal (data ready)
4	CLK	Connect to digital ground	Connect to digital ground
5	DVDD	Digital supply voltage	Digital supply voltage
6	DVSS	Digital ground	Digital ground
7	DVDDS	Digital supply voltage filter	Digital supply voltage filter
8	PD	Power down, connect to GND if not used	Power down, connect to GND if not used
9	SCK/SCL	SPI clock input, SCK	TWI serial clock input, SCL
10	MOSI/SDA	SPI data input, MOSI	TWI data input/output, SDA
11	MISO	SPI data output	Not connected
12	CSB	SPI chip select	Connect to analog supply voltage
13	AVDD	Analog supply voltage	Analog supply voltage
14	AVSS	Analog ground	Analog ground
15	AVSS	Analog ground	Analog ground
16	ATST	Connect to analog ground	Connect to analog ground

7.2 Recommended Circuit Diagrams

In order to achieve high performance and low noise level it is recommended both AVDD and DVDD have their own supply voltage regulators and analog ground plane is separated from digital ground plane near SCP1000. If high performance is not needed, DVDD and AVDD can be supplied from one regulator. Recommended circuit diagrams for SCP1000 are presented in Table 19 below.

Table 19. SCP1000 recommended circuit diagrams.

	SPI interface	TWI interface
High performance		
Simplified (single supply)		

In case PD or TRIG pins are not used, in order to decrease the number of connections, they can be connected to GND, this way the minimum number of connections can be as low as 5 (VDD, GND, SDA, SCL, DRDY).

Table 20. Recommended capacitor values for SCP1000 circuit diagrams presented in Table 19.

Capacitor	High performance circuit diagrams	Minimum requirements for simplified circuit diagrams
C1	470 nF	Minimum 200 nF
C2	470 nF	100 nF
C3	100 nF	10 nF

7.3 Recommended PWB Layout

General PWB layout recommendations for SCP1000 products (refer to Table 21):

1. Locate the ceramic SMD filtering capacitors right next to SCP1000 package.
2. Use plane for GND connection.
3. Connect the plane under SCP1000 to AGND.
4. Minimize the power supply/ground loops.

Recommended PWB pad layout for SCP1000 is presented in Figure 21 below (dimensions in [mm], tolerances ±0.05 mm).

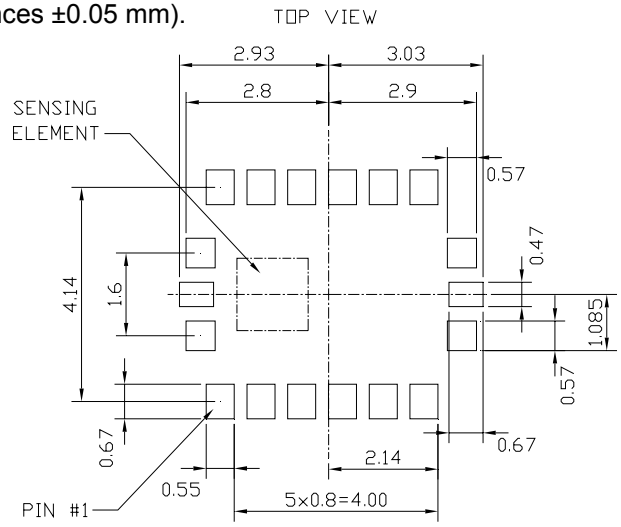
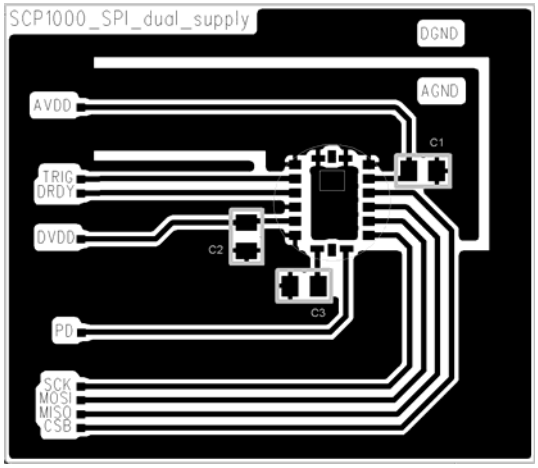
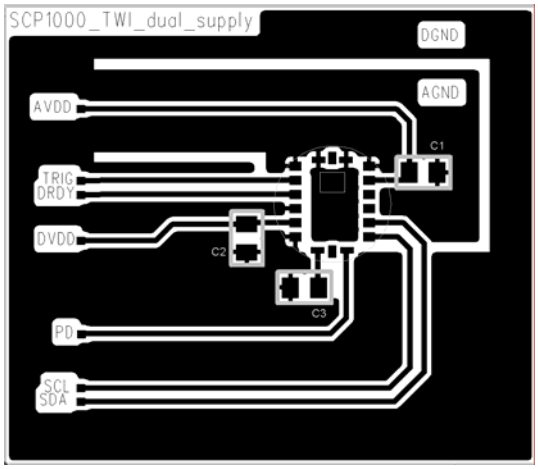
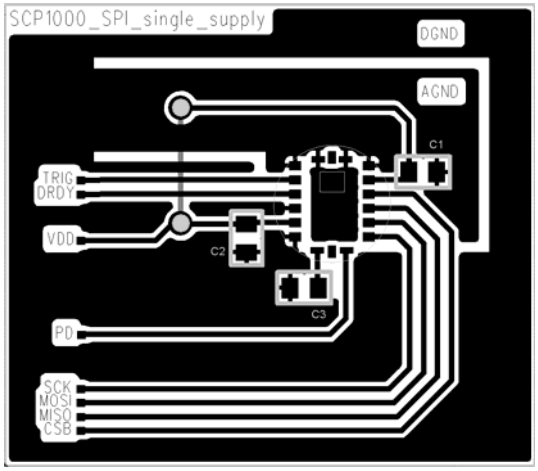
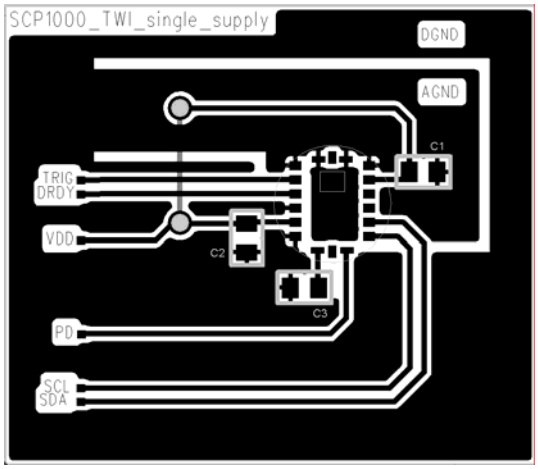


Figure 21. Recommended PWB pad layout for SCP1000.

Recommended PWB layout for SCP1000 with SPI and TWI interfaces is presented in Table 21 below (circuit diagram presented in Table 19 above).

Table 21. SCP1000 recommended PWB layouts (not in real size, for reference only).

	SPI interface	TWI interface
High performance		
Simplified (single supply)		

7.4 Assembly instructions

The Moisture Sensitivity Level (MSL) of the SCP1000 component is 3 according to the IPC/JEDEC J-STD-020C. Please refer to the document "TN51 SCP1000 Assembly Instructions" for more detailed information of SCP1000 assembly.

7.5 Tape and reel specifications

Please refer to the document "TN51 SCP1000 Assembly Instructions" for tape and reel specifications.

7.6 Example flex print design

The electric connections between the SCP1000 sensor and electronics of an application can be carried out by using a flex print. An example flex print design for SCP1000 is presented in Figure 22 and Figure 23 below. These flex print designs are designed by following the recommended circuit diagrams and PWB layouts presented in sections 7.2 and 7.3).

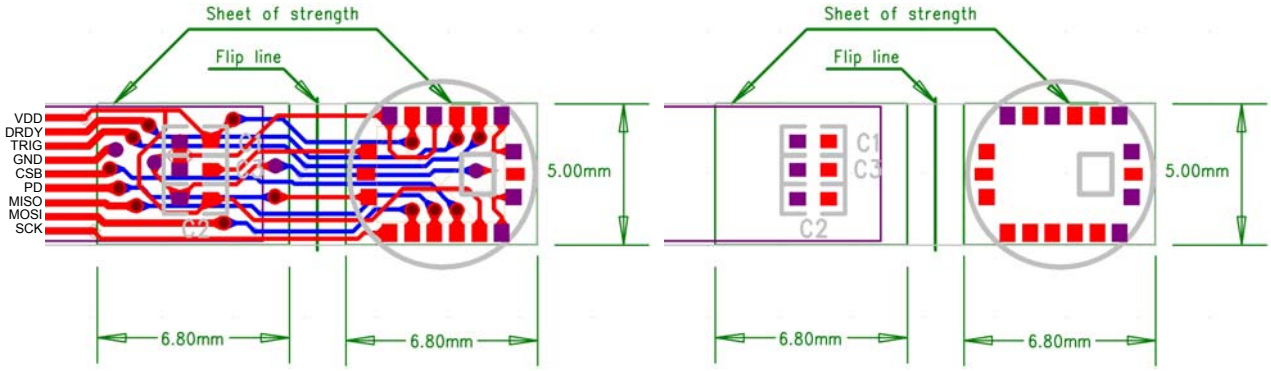


Figure 22. An example flex print design for SCP1000 with SPI connection (with and without leads).

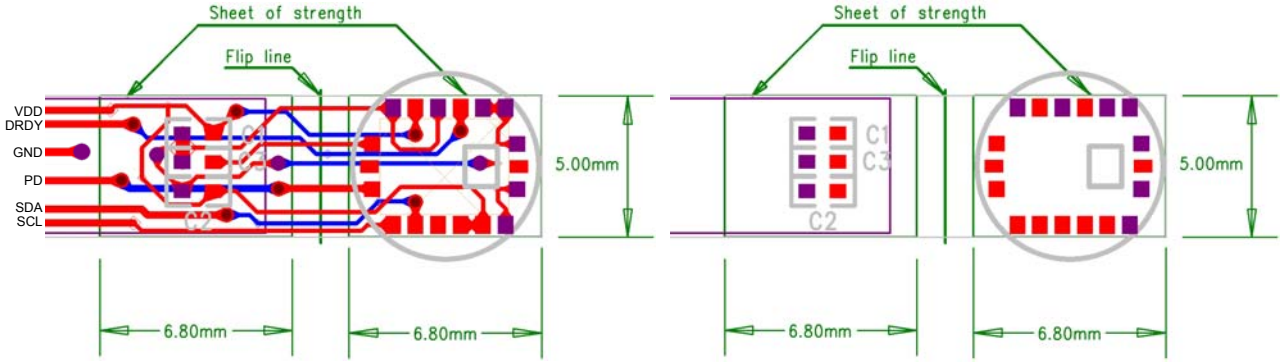


Figure 23. An example flex print design for SCP1000 with TWI connection (with and without leads).

Note the location of the filtering capacitors C1, C2 and C3. The used capacitor values are presented in Table 20 (the high performance circuit values). The circuit diagrams for these flex print designs are the presented in Table 19 (the single supply circuits). The example flex print is designed with the min. 6 mils clearance and trace width. Vias are 0,3 mm and via pads are 0,55mm. The figures of both designs are from top view, the SCP1000 sensor is assembled in top side of the flex print (top layer red, bottom layer blue). GND is connected as a plane throughout the whole flex print from connector to SCP1000 sensor.

8 Document Revision History

Version	Date	Change Description
0.01	10.03.2006	This document replaces the following SCP1000 documents: - “SCP1000_operation_instructions”, - “TN34_SCP1000_SPI_and_I2C_Interfaces”, - “TN35_SCP1000-D01,D02 MISO Configurations” and - “TN45_SCP1000_start_up_sequence”
0.02	27.04.2006	Package characteristics / dimensions update Recommended PWB layout update
0.03	22.05.2006	Figure17 SCP1000 package dimensions picture update Solder Instructions text update Figure 19 Recommended PWB pad layout picture update Changing the name of the document
0.04	04.07.2006	Updated: - Section "3.4.1 EEPROM writing " - Section "5 Electrical characteristics" - Section "6.2 Solder instructions" renamed to "7.4 Assembly instructions", - Section "7.5 Tape and reel specifications" added - Minor language corrections Contact information
0.05	30.08.2006	Minor updates in SCP1000 operation parameters, examples for temperature conversion to [°C] added (section 2.2.3.1).
0.06	14.11.2006	Minor updates in SCP1000 data refresh rates.
0.07	14.11.2006	Updated for C-version asic: - Section "2.1 Start-up" - Section "2.3 Over Pressure Detection" (removed) - Section "2.6 Power down mode" - Section "3.1 Register description" - Section "4.1 SPI Interface" - Section "7.6 Example flex print design" added
0.08	30.10.2007	Gel pockets added to SCP1000 package

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