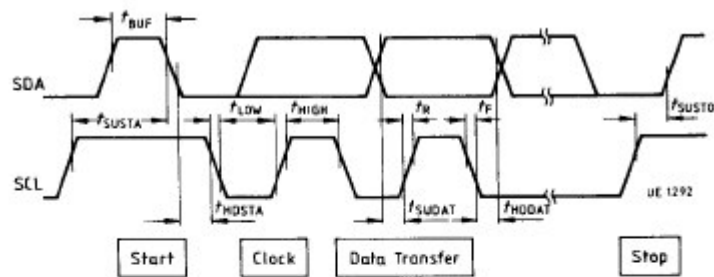


Expander TDA6200, MC44130 (TY45018, MC44130P, TY45013, MC44131P) zu TDA9852H

I²C-Daten des TDA6200



f_{SUSTA}	Set-up time (start)
f_{HDSTA}	Hold time (start)
f_{HIGH}	Pulse width (clock)
f_{LOW}	Pulse width (clock)
f_{SUDAT}	Set-up time (data transfer)
f_{HDDAT}	Hold time (data transfer)
f_{SUSTO}	Set-up time (stop)
f_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

The listed times are referenced to the V_H and V_{IL} values.

Software

The following data format is used:

1) Chip Address

MSB								LSB	
1	0	0	0	0	0	0	0	R/W	ack.
MSB will be transmitted first									
R/W = 0 IC in the receiving mode									

2) Data Bytes with Sub-Addresses

a) Volume

MSB								LSB	
1	0	V05	V04	V03	V02	V01	V00		(left) +
1	0	V15	V14	V13	V12	V11	V10		(right)
The two bytes are always transmitted in successive order									
$V \times 5 = \text{MSB}$									
$V \times 0 = \text{LSB}$									
1	0	0	0	0	0	0	0		min. volume
1	0	1	1	1	1	1	1		max. volume

b) Tone

MSB								LSB	
1	1	X	HV	H3	H2	H1	H0		+
1	1	X	TV	T3	T2	T1	T0		
The two bytes are always transmitted in successive order									
HV or TV are sign bits									
H3 or T3 = MSB									
H0 or T0 = LSB									
1	1	X	0	1	1	1	1		min. treble or bass
1	1	X	X	0	0	0	0		linear treble or bass
1	1	X	1	1	1	1	1		max. treble or bass

Software

c) AF set byte

MSB								LSB
0	0	M1	M2	Ch1/2	RK	Phys	Q-S/Bw	
M1	= 1	Muting for AF output						
M1	= 0	AF ON						
M2	= 1	Compulsory mono (via 4 level line)						
M2	= 0	Standard operation for identification signal decoder						
Ch1/2	= 0	During dual audio mode, channel 1 at AF output						
Ch1/2	= 1	During dual audio mode, channel 2 at AF output (only active with dual audio via 4 level line or during SCART playback and Kbit = 1)						
RK	= 1	Space sound ON; TV operating mode: Quasi-stereo during mono and dual audio or stereo basewidth expansion during stereo transmission – automatic switch-over via 4 level line SCART playback mode: stereo basewidth expansion ON						
RK	= 0	Stereo basewidth expansion and quasi-stereo OFF						
Phys	= 1	Physiological volume control ON						
Phys	= 0	Physiological volume control OFF						
Q-S/Bw	= 1	TV operating mode: Quasi-stereo and stereo basewidth expansion ON SCART playback mode: stereo basewidth expansion ON						
Q-S/Bw	= 0	Quasi-stereo and stereo basewidth expansion OFF						

d) SCART set byte

MSB								LSB
0	1	SC	Sch	Ch	X	X	X	
SC	= 1	SCART playback mode; SCART input connected with AF output						
SC	= 0	Standard operation						
Sch	= 1	Switching output ON (open collector)						
Sch	= 0	Switching output OFF (output can e.g. be used for switch-over from recording to playback mode in the video section)						
Ch	= 1	Playback of SCART dual transmission; channel selection via Ch1/2 bit for AF output						
Ch	= 0	AF output operates in stereo mode. Playback of SCART stereo (mono) transmission.						

Note:

The AF section is automatically controlled by the 4 level line. Compulsory mono M2 is given priority. After Power-ON-Reset all latches are set at 0 (volume min., tone linear, . . .); only the function Q-S/Bw is set at 1.

Software

3) Transmission Mode

requires new chip addressing with R/W bit = 1.

MSB						LSB	
St	D	X	X	X	X	X	X
St	D						
1	1	Decoder recognizes mono					
0	1	Decoder recognizes stereo					
1	0	Decoder recognizes dual					
0	0	Does not occur (internally suppressed)					

The transmission function is not required for the operation of the IC. Instead this function is used to inform the μC about the status of the identification signal decoder to enable additional functions.

LED Driver

TV operating mode:

4 level line	Ch1/2 bit	LED 1	LED 2
Mono	X	OFF	OFF
Stereo	X	ON	ON
Dual	0	ON	OFF
Dual	1	OFF	ON

SCART playback mode:

SC bit	Ch bit	Ch 1/2 bit	LED 1	LED 2
1	0	X	ON	ON
1	1	0	ON	OFF
1	1	1	OFF	ON

I²C-Daten des MC44130

All tests used the circuit in Figure 2. The following conditions are assumed, unless stated otherwise.

- 1% accuracy resistors; resonator Murata CSB437F2 ($f_s=427\text{ kHz}$, $f_p=464\text{ kHz}$, Cstat at 1 kHz = 630 pF, $R_s=30\ \Omega$); $V_{DD}=12\text{ V}$, $T_A=25^\circ\text{C}$.
- V_a amplitude is 500 mV rms, V_a frequency is 1 kHz, V_r amplitude is 400 mV pp, V_r frequency is 1 kHz, V_p frequency is 54.6875 kHz with or without amplitude modulation.
- Values for subaddress, data and read bits are stated as hexadecimal.
- Treble/Bass: flat = subaddress 05 data 88.
- Volumes HP & LS : Maximum = subaddress 01, 02, 03, 04 data 00.
- K1, K2 Set-up: Mid range = subaddress 00, 07 data 20.
- Demute, matrix option 00, no special effects = subaddress 06 data 00.
- When switches are not mentioned, they are considered to be OFF.
- Pin 22 is not connected or is connected to Pin 20.

IDENTIFICATION (See figures 3,4,5)

Read status byte code 01 → AM modulation frequency = 117 Hz
 code 10 → AM modulation frequency = 274 Hz

VOLUME CONTROLS

Left and right outputs may be balanced at any level to within half the step size by independent control of left/right attenuators.

HEADPHONE (See figures 6 and 7)

For these volume control tests, left and right channels are at the same setting. Subaddress 06 data 01, S2 = 4.

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Step size from step 0 to step 25 (understood as decimal values)	HPSS	5, 15, 16	Subaddr. 03,04 Data n → Vout(n) Subaddr. 03,04 Data n+1 → Vout(n+1) $HPSS = 120 \log (Vout(n)/Vout(n+1))$	0	2.5	4.0	dB
Depth from step 0 to step 25	HPDP	5, 15, 16	Subaddr. 03,04 Data 00 → Vout(00) Subaddr. 03,04 Data 19 → Vout(19) $HPDP = 120 \log (Vout(0)/Vout(19))$	55	60	70	dB
Depth at step 30	HPDP	5, 15, 16	Subaddr. 03,04 Data 1E → Vout(1E) $HPDP = 120 \log (Vout(0)/Vout(1E))$	60			dB

LOUDSPEAKER (see figures 8 and 9)

For these volume control tests, left and right channels are at the same setting. Subaddress 06 data 01, S2 = 5.

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Step size from step 0 to step 50 (understood as decimal values)	LSSS	6, 17, 18	Subaddr. 01,02 Data n → Vout(n) Subaddr. 01,02 Data n+1 → Vout(n+1) $LSSS = 120 \log (Vout(n)/Vout(n+1))$	0	1.25	2.5	dB
Depth from step 0 to step 50	LSDL	6, 17, 18	Subaddr. 01,02 Data 32 → Vout(32) $LSDL = 120 \log (Vout(0)/Vout(32))$	55	60	70	dB
Depth at step 62	LSDL	6, 17, 18	Subaddr. 01,02 Data 3E → Vout(3E) $LSDL = 120 \log (Vout(0)/Vout(3E))$	65			dB

K1, K2 SET-UP CONTROL (see figures 10 and 11)

S2=2, S3=ON, S4=ON; Vout is measured on pins 7 and 8 for K1 and K2, respectively.

This set-up control may also be used to equalise gains in dual language mode.

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Control range	SUD	2,3,7, 8	Subaddr. 06, data: 05 Subaddr. 00, 07, data: 3E, Vout(3E) Subaddr. 00, 07, data: 00, Vout(00) $SUD = 120 \log (Vout(3E)/Vout(00))$	3.5	4.5	5.5	dB
Step size K2	SSK2	2,3, 8	Subaddr. 06, data: 05 Subaddr. 07, data: 00 ... 3F	0	0.1	0.2	dB
Step size K1	SSK1	2,3, 7	Subaddr. 06, data: 05 Subaddr. 00, data: 00, 02 ... 3E	0	0.2	0.4	dB
Stereo separation set-up at K1/K2 mid.	SUSM	2,3,7, 8	Subaddr. 06, data: 00 Subaddr. 00, 07, data: 20 VoutL on pin 7, VoutR on pin 8 $SUSM = 120 \log (VoutL(20)/VoutR(20))$	20	40	–	dB
Stereo separation set-up optimized	SUSO	2,3,7, 8	Subaddr. 06, data: 00 Subaddr. 00, data: 20 Subaddr. 07, data: n $SUSO = 120 \log (VoutL(n)/VoutR(20))$	40	50	–	dB

DE-EMPHASIS

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
De-emphasis	DMP	2,3,7 8	Vp=50 mV rms, S1=ON, S2=1,2, S4=ON, S5=ON. Subaddr. 06, data: 05, Vout measured on pin 7,8. DMP= $20 \log (V_{out}(200\text{Hz}) / V_{out}(10\text{kHz}))$	9.8	10.3*	10.8	dB

* Corresponding to 50µs time constant (+/-7%; 46.5µs, 53.5µs)

TREBLE/BASS (See figures 12 and 13)

Subaddress 06, Data = 01, S2 = 5. Flat condition definition = Subaddress 05, data = 88 → Voutf

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Flat condition variation	BSSL		From 100Hz to 10kHz			2	dB
Treble & bass range Range at 100 Hz	BRH	17,18	BRH= $20 \log (V_{out}(8\text{E}) / V_{out} f) \rightarrow \text{max bass}$	+13	+16	+19	dB
	BRL	17,18	BRL= $20 \log (V_{out}(8\text{I}) / V_{out} f) \rightarrow \text{min bass}$	-19	-16	-13	dB
Range at 10 kHz	TRH	17,18	TRH= $20 \log (V_{out}(E8) / V_{out} f) \rightarrow \text{max Treble}$	+13	+16	+19	dB
	TRL	17,18	TRL= $20 \log (V_{out}(I8) / V_{out} f) \rightarrow \text{min Treble}$	-19	-16	-13	dB
Maximum deviation at 1 kHz related to flat condition	DEV		Treble and bass min...max	-4		4	dB
Step size	STZ		Except for the 2 first and 2 last steps	0	-	4	dB

SPECIAL EFFECTS S2 = 4**PSEUDO-STEREO**

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Frequency for 180° phase shift	FREO	5, 17, 18	Subaddr. 06 data 22 Input frequency Va for phase shift of 180° between Vout on pin 17,18 respectively.	1.2	1.25	1.4	kHz
Amplitude	PSA	5,18	Subaddr. 06 Data 02 : VoutN Subaddr. 06 Data 22 : VoutPS PSA=20 log (VoutPS/VoutN)		0.1	0.6	dB
	VARI		For frequencies up to 15 kHz			3.0	dB

Extra-wide

Subaddr. 06 Data 00

*Fva=300Hz
-S2=4 output pin 17 : V300NL
-S2=5 output pin 18 : V300NR
*Fva=1kHz
-S2=4 output pin 17 : VoutNL
-S2=5 output pin 18 : VoutNR

Subaddr. 06 Data 10

*Fva=300 Hz
-S2=4 output pin 18 : VhpLR
-S2=5 output pin 17 : VhpRL
*Fva=1 kHz
-S2=4 output pin 17 : VoutLL
-S2=4 output pin 18 : VoutLR
-S2=5 output pin 17 : VoutRL
-S2=5 output pin 18 : VoutRR

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Direct Gain left	LLA	5,6 17,18	$LLA = (V_{outLL} / V_{outNL}) \times 100$	110	120	130	%
Direct Gain Right	RRB	5,6	$RRB = (V_{outRR} / V_{outNR}) \times 100$	110	120	130	%
Left to Right CC	LRC	5,6 17,18	$LRC = (V_{outNR} \times V_{outLR}) / (V_{outNL} \times V_{outRR}) \times 100$	48	54	60	%
Right to Left CC	RLD	5,6 17,18	$RLD = (V_{outNL} \times V_{outRL}) / (V_{outNR} \times V_{outLL}) \times 100$	48	54	60	%
High Pass filter	HLPR	5,6 17,18	$HLPR = 20 \log((V_{outLR} \times V_{300NL}) / (V_{outNL} \times V_{hpLR}))$	2.8	3.2	3.6	dB
High Pass filter	HPRL	5,6 17,18	$HPRL = 20 \log((V_{outRL} \times V_{300NR}) / (V_{outNR} \times V_{hpRL}))$	2.8	3.2	3.6	dB

Extra-wide and pseudo-stereo

Fva = 1kHz; Subaddr. 06 Data 00, S2=4, output on pin 17:VspNL,
S2=5, output on pin 18:VspNR
Subaddr. 06 Data 30, S2=4, output on pin 17 : VspLL
and output on pin 18 : VspLR
S2=5, output on pin 17 : VspRL
and output on pin 18 : VspRR

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Left to Right CC	LRBT	5,6,17,18	$LRBT = 100(V_{spNR} \times V_{spLR}) / (V_{spNL} \times V_{spRR})$	32	37	42	%
Right to Left CC	RLBT	5,6,17,18	$RLBT = 100(V_{spNL} \times V_{spRL}) / (V_{spNR} \times V_{spLL})$	32	37	42	%

Insertion gain/loss

LIO is defined by $LIO = 20 \log (V_{out}/V_{in})$. For matrix options 00 to 04, S2=2,4,5 and S3=ON, S4=ON.
For matrix options 05 to 0F, S2=1,2,4,5, S4=ON. For matrix options 47 to 4F, S2=3,4,5. See also Table 1.

Characteristics	Symbol	Pin	Input	Output	Min	Typ	Max	Units
Insertion Gain/Loss	LIO	2,3	K1/K2 (*)	Matrix options=03, 04,05,06,08.				
		11,12		HIFI	-1		3	dB
		17,18		LS	-3		1	dB
		15,16		HP	-3		1	dB
				Matrix options = 07, 0F				
		11,12		HIFI	-2		2	dB
		17,18		LS	-5		-1	dB
		15,16		HP	-4		0	dB
				All matrix options (00 to 0F)				
		7,8		SCART	-1		3	dB
		4	AM MONO					
		11,12		HIFI (matrix option=47,4F)	-4		0	dB
		17,18		LS (matrix option=47,4F)	-7		-3	dB
		15,16		HP (matrix option=47,4F)	-6		-2	dB
		7,8		SCART (matrix option=47,4C,4D,4E,4F)	-3		+1	dB
		5,6	SCART					
		11,12		HIFI (matrix option = 00,01,02,08,09,0A,0C,0D,0E,4C,4D,4E).	-3		+1	dB
		17,18		LS (matrix option = 00,01,02,08,09,0A,0C,0D,0E,4C,4D,4E).	-6		-1	dB
		15,16		HP (matrix option = 00,01,02,08,09,0A,0C,0D,0E,4C,4D,4E).	-6		-1	dB

CROSS TALK

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Cross talk	XTLK	2,3,4 5,6,7,8 11,12 15,16 17,18	S2=1,2,3,4,5; S4=ON, S5=ON. For all switching matrix options : XTLK= 120 log (Vout/Vall)	60	-	-	dB

DISTORTION

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Distortion	DIST	2,3 4 5,6 7,8 11,12 15,16 17,18	For all selected matrix options, DIST is defined for each output by : DIST=100 X (Vharm/Vtot) where Vtot is measured on the output corresponding to the selected input (see S2 and the switching matrix table 1) with a low pass filter at 15 kHz and Vharm is measured on the same output with a high Q band pass filter from 2 kHz to 15 kHz.		0.2 0.4 *	0.5	% %

* Depending on matrix option

GLITCH

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Glitch on outputs when changing volume control	GLU	7,8,11, 12,15, 16,17, 18	S5=ON, use a first order RC high pass filter with a frequency cut-off of about 10 Hz as per Figure 5. For the first four steps : For the next four steps : For the remaining steps :	- - -	- - -	5 3 1	mV pp mV pp mV pp
DC level change when changing matrix option		7,8,11, 12,15, 16,17, 18		-	-	100	mV

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Units
Analog Ground Polarisation *	VAGD	1,13	Vpin20-Vdd=12V Vpin14-Vpin20-Vpin26-Vss=0V Pin 1 and Pin 13 have to be connected together.	6	6	7	V
Input Output Polarisation *	VPOL	2,3,4 5,6 7,8 11,12 15,16 17,18	Force VAGD = Vdd/2 on pin 1 and pin 13 and measure VPOL(n) on each input and output pin.	5	6	7	V
Input and Output Impedance *	IKR IR ORS ORA	2,3 4,5,6 7,8 11,12 15,16 17,18	Force pins 1 and 13 to VAGD = Vdd/2 Force tested pin to VPOL(n) -0,1 V and measure the source current K(n) : IKR(n) = 0,1/K(n) IR(n) = 0,1/K(n) ORS(n)=0,1/K(n) except for matrix 03 and 05. ORA(n)=0,1/K(n)	25 150		1 200 200 200	kΩ kΩ kΩ Ω Ω Ω
Noise	NKST NKDM NLMS NOMS NVCT	7,8 11,12 15,16 17,18	S6=ON, Bandwidth 20Hz-15 kHz Matrix option Stereo Input K1 or K2 Matrix option Dual or Mono or Nicam stereo Input K1 or K2 Output LS Input Mono or SCART Output SCART & Input Mono or Output HiFi/HP & Inputs Mono/SCART Output LS volctrl step 24 Output HP volctrl step 12	- - - - - -	160 120 90 60 5	- - - - -	μV rms μV rms μV rms μV rms μV rms
PSRR Power Supply Rejection	PSRR	15,16, 17,18, 28	S6=ON, Vout measured on each output PSRR = 20 log (Vout/Vr) - For LS outputs - For other outputs	-10 -30	-12 -40		dB dB

* This test measurement is done directly on the device without any external wiring and hardware, apart from a short circuit between pins 1 and 13

Note: output drive capability, when using the application circuit of Figure 16, is 1Vpp on 10 kΩ for all outputs.

NICAM Transmission

If NICAM transmission occurs, the decoder and de-emphasis are switched off, and the NICAM decoded signals are directly routed to the switching matrix.

Switching Matrix (see Table 1)

This selects the received and decoded mono, stereo, dual sound signals, or SCART inputs and switches them to one or more of the outputs. Selection is achieved by means of the IIC Bus interface.

For driving VCRs and HiFi sets, the signal is routed directly to the respective outputs. Input from a SCART can be routed to loudspeakers and/or headphones, while another SCART can record the broadcast in progress. (Caution: input from a SCART cannot be routed to the SCART outputs.)

A list of possible input/output combinations is shown in Table 1. Figure 15 shows the different routes from the inputs to the outputs.

Table 1. SWITCHING MATRIX

SELECTION CODE b e f g h	HEXA CODE Note 4	Input				Ident Code	Output				Note
		MONO	K1	K2	SCART L R		LS L R	HP L R	SCART L R		
0 0000	00	—			L° R°	01	L° R°	L° R°	L R	2	
0 0001	01	—			1° 2°	01	2° 2°	1° 1°	L R		
0 0010	02	—	(L+R) 2	R	1° 2°	01	1° 1°	2° 2°	L R		
0 0011	03	—			—	01	L R	L R	M* M*		
0 0100	04	—			—	01	L R	L R	L R		
0 0101	05	—	1	2	—	10	2 2	1 1	1 2	3	
0 0110	06	—	1	2	—	10	1 1	2 2	1 2		
0 0111	07	—	1	—	—	10	1 1	1 1	1 1		
0 1000	08	—	1	2	L° R°	10	L° R°	L° R°	1 2		
0 1001	09	—	1	2	1° 2°	10	2° 2°	1° 1°	1 2		
0 1010	0A	—	1	2	1° 2°	10	1° 1°	2° 2°	1 2		
0 1011	0B	—	1	2	—	10	2 2	1 1	2 2		
0 1100	0C	—	M	—	L° R°	00	L° R°	L° R°	M M	1	
0 1101	0D	—	M	—	1° 2°	00	2° 2°	1° 1°	M M	1	
0 1110	0E	—	M	—	1° 2°	00	1° 1°	2° 2°	M M	1	
0 1111	0F	—	M	—	—	00	M M	M M	M M	3	
1 0111	47	Mn	—	—	—	—	Mn Mn	Mn Mn	Mn Mn	3	
1 1100	4C	Mn	—	—	L° R°	—	L° R°	L° R°	Mn Mn		
1 1101	4D	Mn	—	—	1° 2°	—	2° 2°	1° 1°	Mn Mn		
1 1110	4E	Mn	—	—	1° 2°	—	1° 1°	2° 2°	Mn Mn		
1 1111	4F	Mn	—	—	—	—	Mn Mn	Mn Mn	Mn Mn	3	

BUS CONTROL

The Stereotone I.C. is digitally controlled by using the MOTOROLA two wire serial bus (IIC compatible). A simple description is given in appendix A, with emphasis on the word structure. The MOTOROLA Bus electrical specification is given in Figure 19.

Details of the Stereotone Bus operation are as follows:

- The chip address is 1 000 000 Y, where Y is read/write bit (R/W).
- There are 8 subaddresses available to control volumes, treble-bass, set-up and decoder-de-emphasis switching, and to select switching matrix options
- Two flag bits representing the actual sound mode can be read by the master.

Table 2 shows function subaddresses and data definitions. Some communication protocols to be used follow.

Table 2: STEREOTONE M-Bus Protocol (Note: X = Don't care)

Function	Subaddress	Data
Level Set-up K1 Decoder & Deemphasis switch	XXXXX000	(Note 1)
Level Set-up K2	XXXXX111	XX000000<= gain => XX111111
Volume, left speaker	XXXXX001	XX000000<= volume =>XX111111 (Note 2)
Volume, right speaker	XXXXX010	XX000000<= volume =>XX111111 (Note 2)
Volume, left headphone	XXXXX011	XX000000<= volume =>XX111111 (Note 2)
Volume, right headphone	XXXXX100	XX000000<= volume =>XX111111 (Note 2)
Treble/Bass	XXXXX101	0001XXXX<= treble =>1110XXXX XXXXX001<= bass =>XXXX1110 Flat response 10001000
Selection matrix + Special Effects	XXXXX110	Mute 1 : 1XXXXXXX Not muted 1: 0XXXXXXX
Special Effects		XX00XXXX No special effect XX10XXXX Pseudo stereo XX01XXXX Extra-wide stereo XX11XXXX Both effects
Matrix Select		XbXXefgh (See Table 1)

Note 1: Level set-up K1 + decoder & de-emphasis data XX12345Y, a 6-bit word.

The word XX00000Y corresponds to minimum gain (0.707x).

The word XX10000Y corresponds to midrange gain (1.0x)

The word XX11111Y corresponds to maximum gain (1.414x)

IMPORTANT: bit Y = 0 switches ON decoder & de-emphasis; bit Y = 1 switches it OFF.

Note 2: Performance is guaranteed only between:

XX000000 and XX110010 for LS

XX000000 and XXX11001 for HP

See also Figures 16 to 19.

Communication Protocols

-Write one Byte

STA	Chip Address 0	Ack (See Note 3)	Sub-address 	Ack	Data 	Ack	STO STA
-----	--------------------------	---------------------	-----------------	-----	----------	-----	------------

Note 3: The acknowledge flag is composed of one bit, and is generated by the MC44130, which pulls down the data line during one clock pulse (see Appendix A).

-Write N Bytes

STA	Chip addr. 0	Ack	Sub-addr. 	Ack	Data 1 	Ack	Sub-addr. 	Ack	Data 2 	Ack	STO STA
-----	------------------------	-----	---------------	-----	------------	-----	---------------	-----	------------	-----	------------

Ack. for byte n

- Read Status Byte

STA	Chip addr. 	Ack	Data In 	STO STA
-----	----------------	-----	-------------	------------

X Y

With X Y
0 0 MONO
0 1 STEREO
1 0 DUAL LANGUAGE