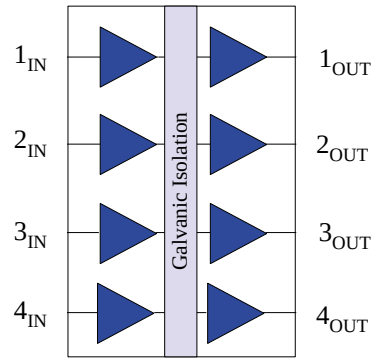
NVE CORPORATION

IL715/6/7 *IsoLoop*®

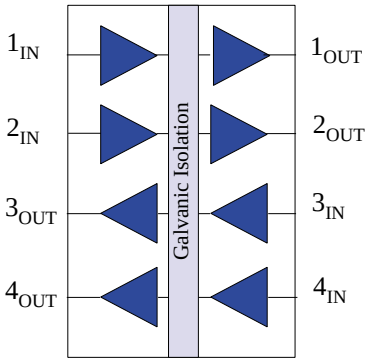
Four Channel Digital Isolators

Functional Diagram

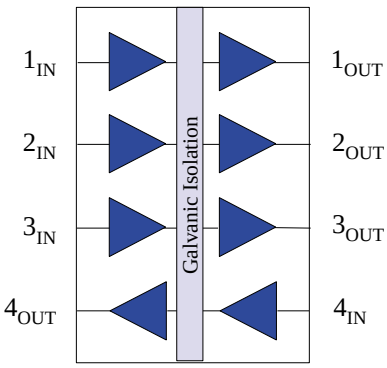
IL715



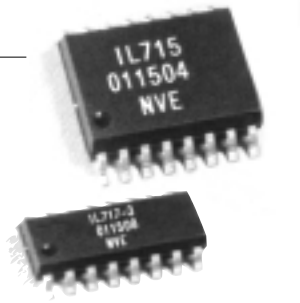
IL716



IL717



Features



- +5 and 3.3V CMOS Compatible
- 2500 V_{RMS} Isolation (1 min)
- 2 ns Typical Pulse Width Distortion
- 10 ns Typical Propagation Delay
- 2 ns Channel to Channel Skew
- 30 kV/µs Typical Transient Immunity
- 100 MBd Data Rate
- 0.3" and 0.15" 16–Pin SOIC Packages
- UL1577 Approved (File # E207481)
- IEC 61010-1 Approved (Report # 607057)

Applications

- Isolated Data Transmission
- Isolated ADCs and DACs
- Isolated RS485 and RS422
- Parallel Bus Isolation
- Computer Peripheral Interface Isolation
- Logic Level Shifting

Description

The IL715, IL716 and IL717 series of 4–channel digital isolators provide the designer with the most compact isolated logic devices yet available. These isolators are packaged in three options: IL715 with four unidirectional channels, IL716 with two channels in one direction and two channels in the opposite direction, and the IL717 with three channels in one direction and one channel in the other direction. All these devices are fabricated with patented* *IsoLoop*® technology giving them excellent transient immunity specifications. The symmetric magnetic coupling barrier gives these isolators a propagation delay of only 10 ns and a pulse width distortion of 2 ns. Devices are 100% high voltage tested to guarantee barrier integrity.

The IL715, IL716 and IL717 have a 100 MBaud data rate which is independent of direction. They are available in 0.3" and 0.15" 16–pin SOIC packages and are specified over the temperature range –40ºC to +100ºC.

Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	175	°C
Ambient Operating Temperature(1)	T_A	-55	125	°C
Supply Voltage	V_{DD1}, V_{DD2}	-0.5	7	Volts
Input Voltage	V_I	-0.5	V_{DD1}+0.5	Volts
Output Voltage	V_O	-0.5	V_{DD2}+0.5	Volts
Output Current Drive Channel	I_O		10	mAmps
Lead Solder Temperature (10s)			260	°C
ESD	2kV Human Body Model			

Insulation Specifications

Parameter	Symbol	Min	Typ.	Max.	Units	Test Condition
Barrier Impedance				$>10^{14}\|\|7$		Ω ‖ pF
Creepage Distance (External)		8.077 (0.3" SOIC) 4.026 (0.15" SOIC)			mm	
Leakage Current			0.2		µAmps	240 V_{RMS}
Capacitance (Input-Output)(5)	C_{I-O}		4.0		pF	f= 1MHz

Recommended Operating Conditions

Parameters	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	-40	100	°C
Supply Voltage	V_{DD1},V_{DD2}	3.0	5.5	Volts
Logic High Input Voltage	V_{IH}	2.4	V_{DD}	Volts
Logic Low Input Voltage	V_{IL}	0	0.8	Volts
Input Signal Rise and Fall Times	t_{IR},t_{IF}		1	µsec

IEC61010-1

TUV Certificate Numbers: B 01 07 44230 003
Classification as Table 1.

Model	Pollution Degree	Material Group	Max Working Voltage	Package Type	
				16–SOIC (0.3")	*16–SOIC (0.15")*
IL715, IL716, IL717	II	III	300 VRMS	✓	
IL715-3, IL716-6, IL717-3	II	III	150 VRMS		✓

UL 1577

Component Recognition program. File # E207481
Rated 2500Vrms for 1min.

Ordering Information

Model	Package Type	
	16-SOIC (0.3")	*16-SOIC (0.15")**
IL715	(no mark)	-3
IL716	(no mark)	-3
IL717	(no mark)	-3

* UL & IEC approval is pending for the 16-SOIC (0.15") parts.

Example: **IL715** is packaged as a *16-SOIC (0.3")*
IL716-3 is packaged as a *16-SOIC (0.15")*

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Electrical Specifications

Electrical Specifications are T_{min} to T_{max} .

Parameter	Symbol	3.3 Volt Specifiations			5Volt Specifications			Units	Test Conditions
DC Specifications		**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**		
Input Quiescent Supply Current									
IL715	I_{DD1}		17	27		22	40	µA	
IL716	I_{DD1}		2.4	3.3		4	5	mA	
IL717	I_{DD1}		1.5	1.7		2.2	2.5	mA	
Output Quiescent Supply Current									
IL715	I_{DD2}		4.8	7		8	10	mA	
IL716	I_{DD2}		2.4	3.3		4	5	mA	
IL717	I_{DD2}		2	5.3		7	8	mA	
Logic Input Current	I_I	-10		10	-10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD}-0.1 0.8*V_{DD}	V_{DD} V_{DD}-0.5		V_{DD}-0.1 0.8*V_{DD}	V_{DD} V_{DD}-0.5		V	I_O =-20 µA, V_I =V_{IH} I_O = -4 mA, V_I =V_{IH}
Logic Low Output Voltage	V_{OL}		0 0.5	0.1 0.8		0 0.5	0.1 0.8	V	I_O = 20 µA, V_I =V_{IL} I_O = 4 mA, V_I =V_{IL}
Switching Parameters									
Maximum Data Rate		100	110		100	110		MBd	C_L = 15 pF
Minimum Pulse Width	PW	10			10			ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18		10	15	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18		10	15	ns	C_L = 15 pF
Pulse Width Distortion[2] | tPHL- tPLH |	PWD		2	3		2	3	ns	C_L = 15 pF
Propagation Delay Skew[3]	t_{PSK}		4	6		4	6	ns	C_L = 15 pF
Output Rise Time (10-90%)	t_R		2	4		1	3	ns	C_L = 15 pF
Output Fall Time (10-90%)	t_F		2	4		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)[4]	|CMH| |CML|	20	30		20	30		kV/µs	Vcm =300V
Channel to Channel Skew	t_{CSK}		2	3		2	3	ns	C_L = 15 pF

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

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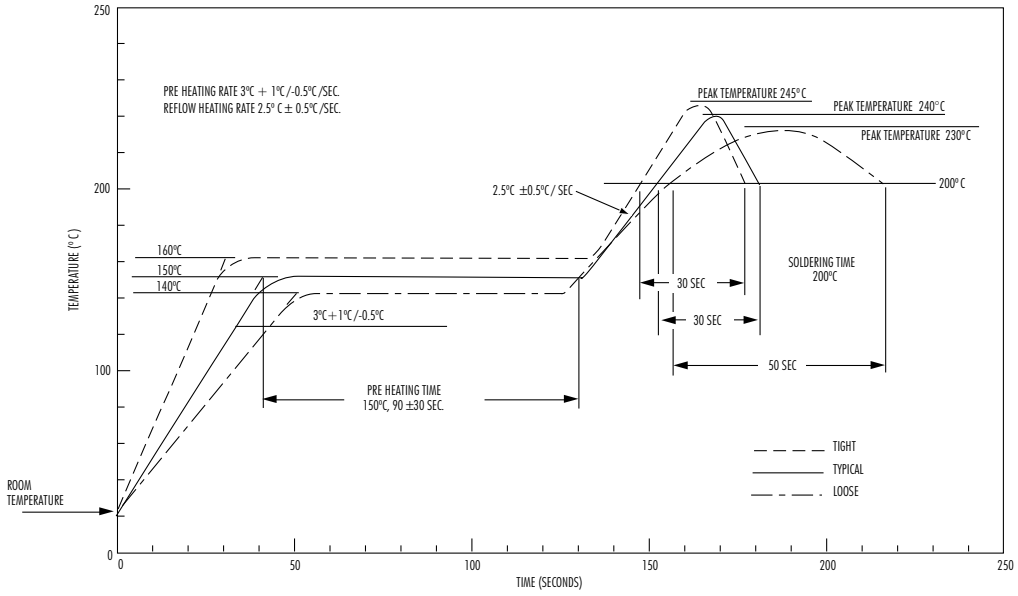
Notes:

1. Absolute Maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $| t_{PHL} - t_{PLH} |$. %PWD is equal to the PWD divided by the pulse width.
3. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at 25°C.
4. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1–8 shorted and pins 9–16 shorted.

IR Soldering Profile



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Application Notes:

Power Consumption

Isoloop® devices achieve their low power consumption from the manner by which they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5ns wide, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers whose power consumption is heavily dependent on its on-state and frequency.

The approximate power supply current per channel for *Isoloop*® is: $\mathbf{I(input) = 40 \cdot \frac{f}{fmax} \cdot \frac{1}{4}\ mA}$

where **f= operating frequency**

fmax= 50 MHz

Power Supply Decoupling

Both power supplies to these devices should be decoupled with good quality 47 nF ceramic capacitors. For data rates in excess of 10MBd, use of ground planes for both GND1 and GND2 is highly recommended. Capacitors should be located as close as possible to the device.

Signal Status on Start-up and Shut Down

To minimize power dissipation, the input signals to the IL715, IL716 and IL717 are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider the inclusion of an initialization signal in his start-up circuit.

Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are *pulse width distortion* and *propagation delay skew*.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in ns. It may also be expressed as a percentage:

$$PWD\% = \frac{\text{Maximum Pulse Width Distortion (ns)}}{\text{Signal Pulse Width (ns)}} \times 100\%$$

e.g. for the **IL717** @ 12.5 Mb

$$PWD\% = \frac{3\text{ ns}}{80\text{ ns}} \times 100\% = \mathbf{3.75\%}$$

This figure is almost ***3x*** better than for any available optocoupler with the same temperature range, and ***2x*** better than any optocoupler regardless of published temperature range. The *IsoLoop*® range of isolators including the IL717 surpasses the 10% maximum PWD recommended by PROFIBUS, and will run at almost 35 Mb before reaching the 10% limit.

Propagation delay skew is the difference in time taken for two or more channels to propagate their signals. This becomes significant when clocking is involved since it is undesirable for the clock pulse to arrive before the data has settled. A short propagation delay skew is therefore critical, especially in high data rate parallel systems, to establish and maintain accuracy and repeatability. The *IsoLoop*® range of isolators all have a maximum propagation delay skew of 6 ns, which is ***5x*** better than any optocoupler. The maximum channel to channel skew in the IL717, IL716, and IL715 isolators is only 3 ns which is ***10x*** better than any optocoupler.

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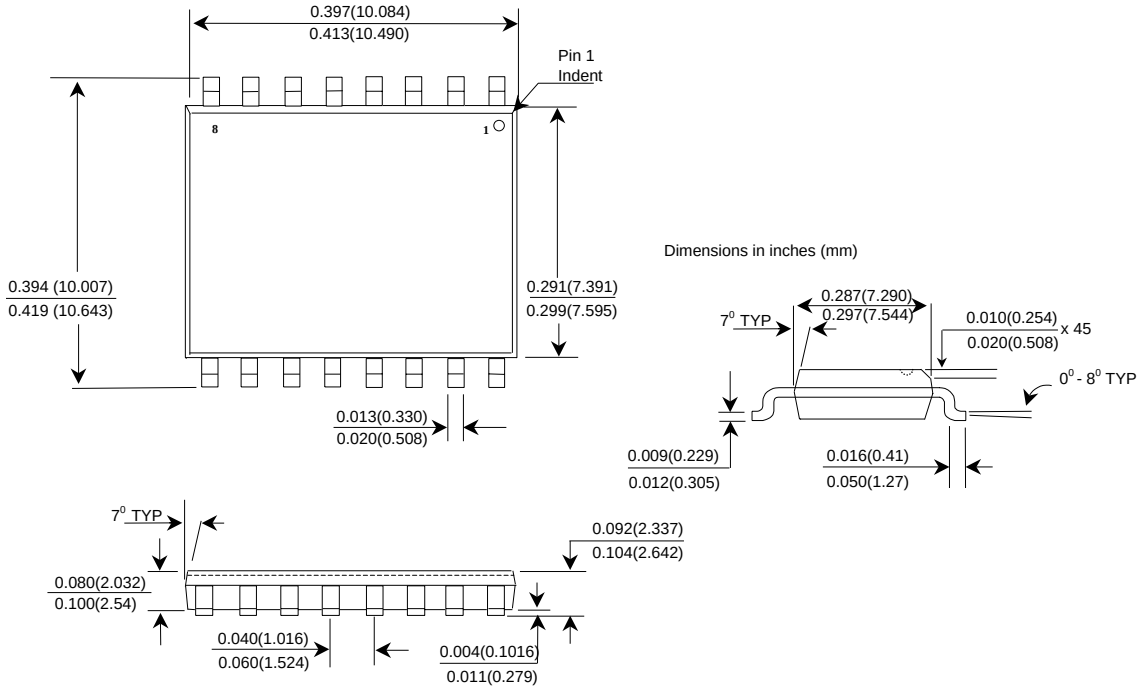
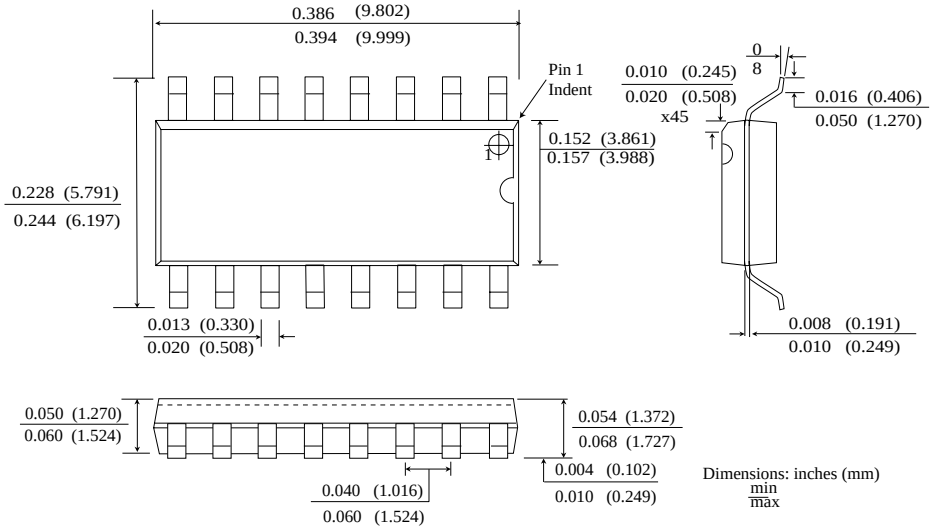
0.3” SOIC-16 Package



0.15” SOIC-16 Package



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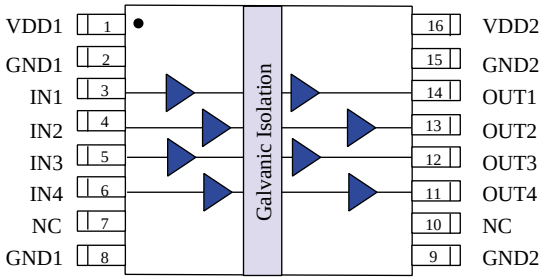
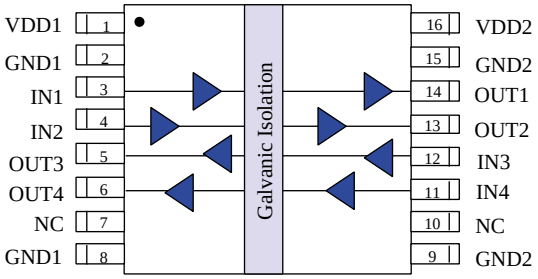
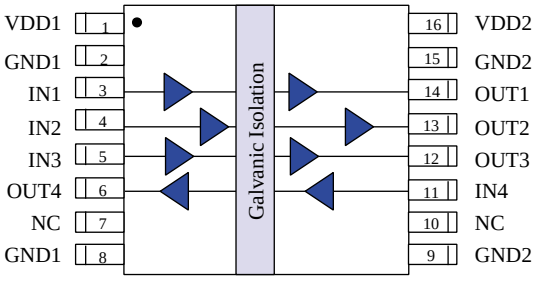
Pin Configurations IL715, IL716, IL717



IL715



IL716



IL717

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