2.7–5.5V Serial Infrared Transceiver Module Family (SIR, 115.2 kbit/s)

Features

- Compliant to IrDA 1.2 (up to 115.2 kbit/s)
- Wide Operating Voltage Range (2.7 to 5.5 V)
- Low Power Consumption (1.3 mA Supply Current)
- Power Sleep Mode Through V_{CC1}/SD Pin (5 nA Sleep Current)
- Long Range (up to 3.0 m at 115.2 kbit/s)
- Three Surface Mount Package Options
  - Universal (9.7 x 4.7 x 4.0 mm)
  - Side View (13.0x5.95x5.3mm)
  - Top View (13.0x7.6x5.95mm)
- BabyFace (Universal) Package Capable of Surface Mount Solderability to Side- and Top-View Orientation
- Directly Interfaces with Various Super I/O and Controller Devices and TEMIC's TOIM3000 and TOIM3232 I/Os
- Few External Components Required
- Backward Compatible to All TEMIC SIR Infrared Transceivers
- Built–in EMI Protection – No External Shielding Necessary

Applications

- Notebook Computers, Desktop PCs, Palmtop Computers (Win CE, Palm PC), PDAs
- Digital Still and Video Cameras
- Printers, Fax Machines, Photocopiers, Screen Projectors
- Telecommunication Products (Cellular Phones, Pagers)
- Internet TV Boxes, Video conferencing systems
- External Infrared Adapters (Dongles)
- Medical and Industrial Data Collection Devices

Description

The TFDU4100, TFDS4500, and TFDT4500 are a family of low-power infrared transceiver modules compliant to the IrDA 1.2 standard for serial infrared (SIR) data communication, supporting IrDA speeds up to 115.2 kbit/s. Integrated within the transceiver modules are a photo PIN diode, infrared emitter (IRED), and a low-power analog control IC to provide a total front–end solution in a single package. TEMIC's SIR transceivers are available in three package options, including our BabyFace package (TFDU4100), the smallest SIR transceiver available on the market. This wide selection provides flexibility for a variety of applications and space constraints.

The transceivers are capable of directly interfacing with a wide variety of I/O chips which perform the pulse-width modulation/demodulation function, including TEMIC's TOIM3000 and TOIM3232. At a minimum, a current-limiting resistor in series with the infrared emitter and a Vcc bypass capacitor are the only external components required to implement a complete solution.

Package Options

TFDU4100
Baby Face (Universal)

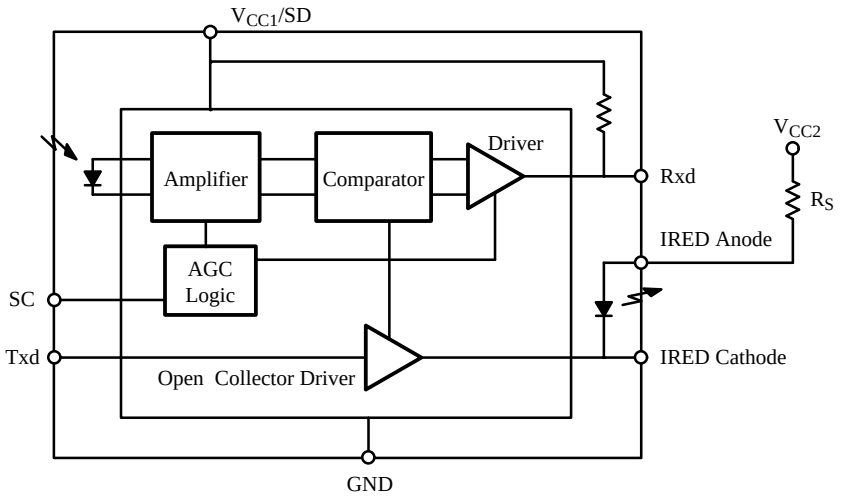
TFDS4500
Side View

TFDT4500
Top View

This product is currently in devleopment. Inquiries regarding the status of this product should be directed to TEMIC Marketing.

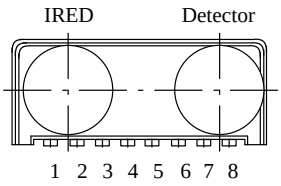
Pre-Release Information

Functional Block Diagram

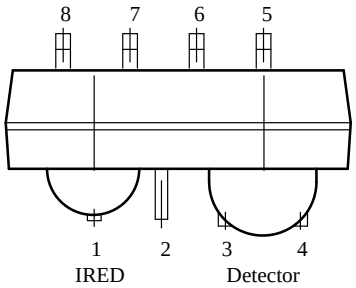


Pin Assignment and Description

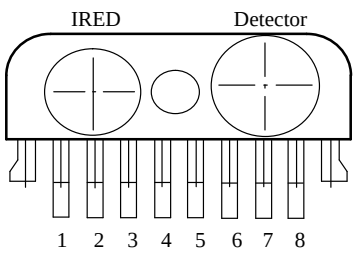
Pin Number		Function	Description	I/O	Active
" U ", " T " Option	" S " Option				
1	8	IRED Anode	IRED anode, should be externally connected to V_{CC2} through a current control resistor		
2	1	IRED Cathode	IRED cathode, internally connected to driver transistor		
3	7	Txd	Transmit Data Input	I	HIGH
4	2	Rxd	Received Data Output, push–pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull–up or pull–down resistor is required (20 kΩ resistor internal to device). Pin is inactive during transmission.	O	LOW
5	6	NC	Do not connect		
6	3	V_{CC1}/ SD	Supply Voltage/Shutdown (see "Shutdown" on page 6)		
7	5	SC	Sensitivity control	I	HIGH
8	4	GND	Ground		



"U" Option
BabyFace (Universal)



"S" Option
Side View



"T" Option
Top View

Ordering Information

Part Number	Qty/ Reel	Description
TFDU4100–TR3	1000 pcs	Oriented in carrier tape for side view surface mounting
TFDU4100–TT3	1000 pcs	Oriented in carrier tape for top view surface mounting
TFDS4500–TR3	750 pcs	
TFDT4500–TR3	750 pcs	

Absolute Maximum Ratings

Parameter	Symbol	Test Conditions[a]	Min[b]	Typ[c]	Max[b]	Unit
Supply Voltage Range	V_{CC1}		– 0.5		6	V
Voltage Range of IRED Drive Output	V_{CC2}	IRED anode pin, T_{xd} LOW	– 0.5		6	
Input Currents[d]					10	mA
Output Sink Current					25	
Power Dissipation[e]	P_D				200	mW
Junction Temperature	T_J				125	°C
Ambient Temperature Range (Operating)	T_{amb}		–25		85	
Storage Temperature Range	T_{stg}		–25		85	
Soldering Temperature		t = 20 s		215	240	
Average IRED Current	I_{IRED} (DC)				100	mA
Repetitive Pulsed IRED Current	I_{IRED} (RP)	t < 90µs, t_{on}<20%			500	
IRED Anode Voltage at Current Output	V_{IREDA}		– 0.5		6	V
Transmitter Data Input Voltage	V_{Txd}		– 0.5		V_{cc} + 0.5	
Receiver Data Output Voltage	V_{Rxd}		– 0.5		V_{cc} + 0.5	
Virtual Source Size[f]	d		2.5	2.8		mm
Maximum Intensity for Class 1 Operation of IEC 825 or EN60825[g]		EN60825, 1997			400	mW/sr

Notes
a. Reference point GND pin unless otherwise noted.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. All pins except IRED cathode pin and IRED anode pin.
e. See Derating Curve
f. Method: (1-1/e) encircled energy.
g. Worst case IrDA SIR pulse pattern.

Electrical Characteristics

Parameter	Symbol	Test Conditions[a]	Min[b]	Typ[c]	Max[b]	Unit
Transceiver						
Supply Voltage	V_{CC1}	Receive Mode	2.7		5.5	V
Supply Voltage	V_{CC1}	Transmit Mode, R_2 = 51 Ω	2.0		5.5	
Supply Current, V_{CC1} Pin (Receive Mode)	I_S	V_{CC1}= 5.5V		1.3	2.5	mA
		V_{CC1}= 2.7V		1.0	1.5	
Supply Current, V_{CC1} Pin (avg) (Transmit Mode) [d]	I_S	V_{CC1}= 5.5V		5.0	5.5	
		V_{CC1}= 2.7V		3.5	4.5	
Leakage Current of IR Emitter, IRED Anode Pin	I_S	V_{CC1}= OFF, T_{xd} = LOW, V_{CC2} = 6V, T = 25°– 85° C		0.005	0.5	µA
Transceiver Power On Settling Time	I_S			50		µs

Optoelectronic Characteristics

Parameter	Symbol	Test Conditions[a]	Min[b]	Typ[c]	Max[b]	Unit
Receiver						
Min Detection Threshold Irradiance[e]	E_{emin}	α = ±15°, SIR Mode, SC = LOW		20	35	mW/m²
		α = ±15°, SIR Mode, SC = LOW, V_{CC1} = 2.7V			35	
Min Detection Threshold Irradiance[d]	E_{emin}	α = ±15°, SIR Mode, SC = HIGH	6	10	15	
Max Detection Threshold Irradiance[d]	E_{emax}	α = ± 90°, SIR Mode, V_{CC1} = 5V	3.3	5		kW/m²
		α = ± 90°, SIR Mode, V_{CC1} = 3V	8	15		
Logic Low Receiver Input Irradiance	$E_{emax\ (low)}$	SC = HIGH or LOW			4	mW/m²
Rxd Output Voltage	V_{OL}	Active, C = 15 pF, R = 2.2 kΩ		0.5	0.8	V
	V_{OH}	Non–active, C = 15 pF, R = 2.2 kΩ	V_{CC}–0.5			
Output Current		V_{OL} < 0.8V		4		mA
Rise Time	t_r	C = 15 pF, R = 2.2 kΩ	20		1400	ns
Fall Time	t_f	C = 15 pF, R = 2.2 kΩ	20		200	
Rxd Pulse Width of Output Signal	P_w	115.2 kbit/s mode	1.41		8	µs
Jitter[f]	t_j	Over a period of 10 bit, 115.2 kbit/s			2	
Latency	t_L			100	500	µs

Notes
a. T_{amb} = 25°C, V_{CC} = 2.7 – 5.5 V unless otherwise noted.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. I_{IRED} (peak) = 210 mA (At IRED Anode pin)
e. BER = 10^{-8} (IrDA specification).
f. Leading edge of output signal.

Optoelectronic Characteristics (Cont'd)

Parameter	Symbol	Test Conditions[a]	Min[b]	Typ[c]	Max[b]	Unit
Transmitter						
IRED Operating Current[d]	I_D	Current limiting resistor is series to IRED: R_1 = 8.2 Ω, V_{CC2} = 5V		0.3	0.4	A
Logic Low Transmitter Input Voltage	V_{IL} (T_{xd})		0		0.8	V
Logic High Transmitter Input Voltage	V_{IH} (T_{xd})		2.4		V_{CC1}+0.5	
Output Radiant Intensity[e]	I_{eH}	Current limiting resistor in series to IRED: R_1 = 8.2Ω @ V_{CC2} = 5V, α = ±15°	45	140	200	mW/sr
Output Radiant Intensity	I_{eL}	Logic Low Level			0.04	mW/sr
Angle of Half Intensity	α			±24		°
Peak Wavelength of Emission	λ_P		880		900	nm
Halfwidth of Emission Spectrum				60		
Optical Rise Time, Fall Time	t_R, t_F	115.2 kHz square wave signal, duty cycle 1:1		200	600	ns
Optical Overshoot					25	%
Rising Edge Peak–to–Peak Jitter	t_j	Over a period of 10 bits, independent of information content			0.2	µs

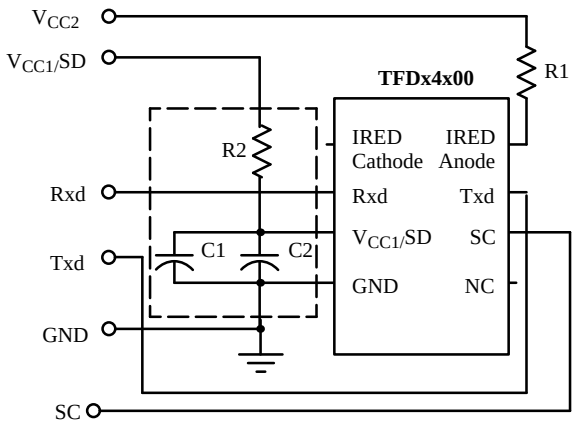
Notes
a. T_{amb} = 25°C, V_{CC} = 2.7 – 5.5 V unless otherwise noted.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. IRED Operating Current can be adjusted by variation of R_1
e. In agreement with IEC 825 eye safety limit

Recommended Circuit Diagram

The only required components for designing an IrDA 1.2 compatible design using TEMIC SIR transceivers are a current limiting resistor to the IRED. However, depending on the entire system design and board layout, additional components may be required (see Figure 1).

It is recommended that the capacitors C1 and C2 are positioned as near as possible to the transceiver power supply pins, as in the proposed layout in Figure 1. A tantalum capacitor should be used for C1, while a ceramic capacitor should be used for C2 to suppress RF noise. Also, when connecting the described circuit to the power supply, low impedance wiring should be used.

R1 is used for controlling the current through the IR emitter. For increasing the output power of the IRED, the value of the resistor should be reduced. Similarly, to reduce the output power of the IRED, the value of the resistor should be increased. For typical values of R1 see Fig 2. For IrDA compliant operation, a current control resistor of 8–12 Ω is recommended. The upper drive current limitation is dependent on the duty cycle and is given by the absolute maximum ratings on the data sheet and the eye safety limitations given by IEC825–1.



Note: Outlined components are optional depending on quality of power supply.

Figure 1. Recommended Application Circuit

R2, C1 and C2 are optional and dependent on the quality of the supply voltage V_{CC1} and injected noise. An

unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver.

Table 1. Recommended Application Circuit Components

Component	Recommended Value
C1	100 nF, Ceramic (use 470 nF for less stable power supplies)
C2	1 µF, Tantalum
R1	8.2 Ω, 0.25 W (recommend using two 0.125 W resistors in parallel)
R2	22 – 47 Ω, 0.125 W

The sensitivity control (SC) pin allows the minimum detection irradiance threshold of the transceiver to be lowered when set to a logic HIGH. Lowering the irradiance threshold increases the sensitivity to infrared signals and increases transmission range up to 3 meters. However, setting the SC pin to logic HIGH also makes the transceiver more susceptible to transmission errors due to an increased sensitivity to fluorescent light distrubances. It is recommended to set the SC pin to logic LOW or left open if the increased range is not required or if the system will be operating in bright ambient light.

The guide pins on the side-view and top-view packages are internally connected to ground but should not be connected to the system ground to avoid ground loops. They should be used for mechanical purposes only and should be left floating.

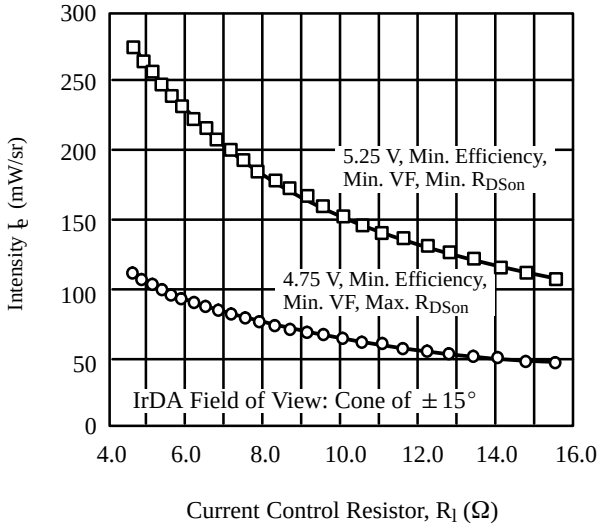


Figure 2. I_e vs R_l

Shutdown

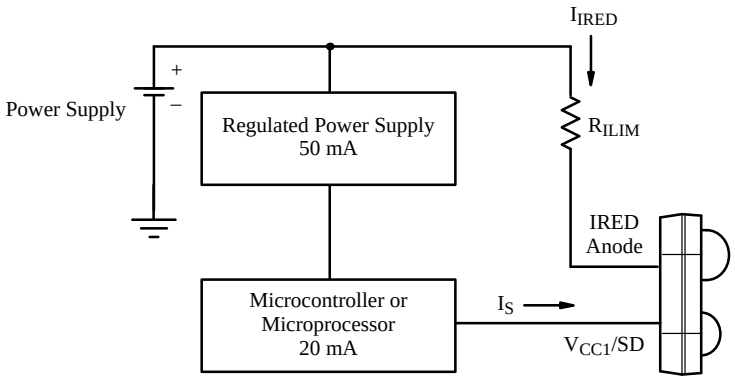
The internal switch for the IRED in TEMIC SIR transceivers is designed to be operated like an open collector driver. Thus, the V_{CC2} source can be an unregulated power supply while only a well regulated power source with a supply current of 1.3 mA connected to V_{CC1}/SD is needed to provide power to the remainder of the transceiver circuitry in receive mode. In transmit mode, this current is slightly higher (approxiamately 4 mA average at 3V supply current) and the voltage is not required to be kept as stable as in receive mode. A voltage drop of V_{CC1} is acceptable down to about 2.2V when buffering the voltage directly from the V_{CC1} pin to GND by a 470 nF ceramic capacitor (C1) and a 51 Ω serial resistor (R2) is used (see figure 1).

This configuration minimizes the influence of high current surges from the IRED on the internal analog control circuitry of the transceiver and the application circuit. Also, board space and cost savings can be achieved by eliminating the additional linear regulator normally needed for the IRED's high current requirements.

The transceiver can be very efficiently shutdown by keeping the IRED connected to the power supply V_{CC2} but switching off V_{CC1}/SD. The power source to V_{CC1}/SD can be provided directly from a microcontroller (see Figure 3). In shutdown, current loss is realized only as leakage current through the current limiting resistor to the IRED (typically, 5 nA). The settling time after switching V_{CC1}/SD on again is approxiamately 50 µs. TEMIC's TOIM3232 interface circuit is designed for this shutdown feature. The V_{cc}_SD, S0 or S1 outputs on the TOIM3232 can be used to power the transceiver with the necessary supply current.

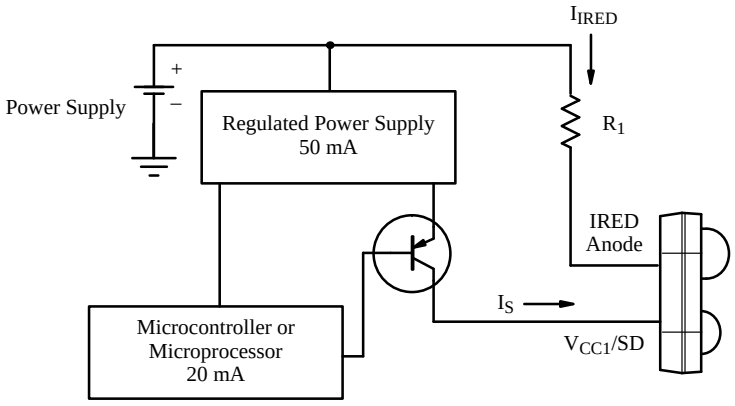
If the microcontroller or the microprocessor is unable to drive the 1.3-mA supply current required by the transceiver, a low-cost SOT-23 pnp transistor can be used to switch voltage on and off from the regulated power supply (see figure 4). The additional component cost is minimal and saves the system designer additional power supply costs.

Shutdown (Cont'd)



TFDU4100 (Note: Typical Values Listed)
Receive Mode
@5 V: I_{IRED} = 300 mA, I_S = 1.3 mA
@2.7 V: I_{IRED} = 300 mA, I_S = 1.0 mA
Transmit Mode
@5 V: I_{IRED} = 300 mA, I_S = 5 mA (Avg.)
@2.7 V: I_{IRED} = 300 mA, I_S = 3.5 mA (Avg.)

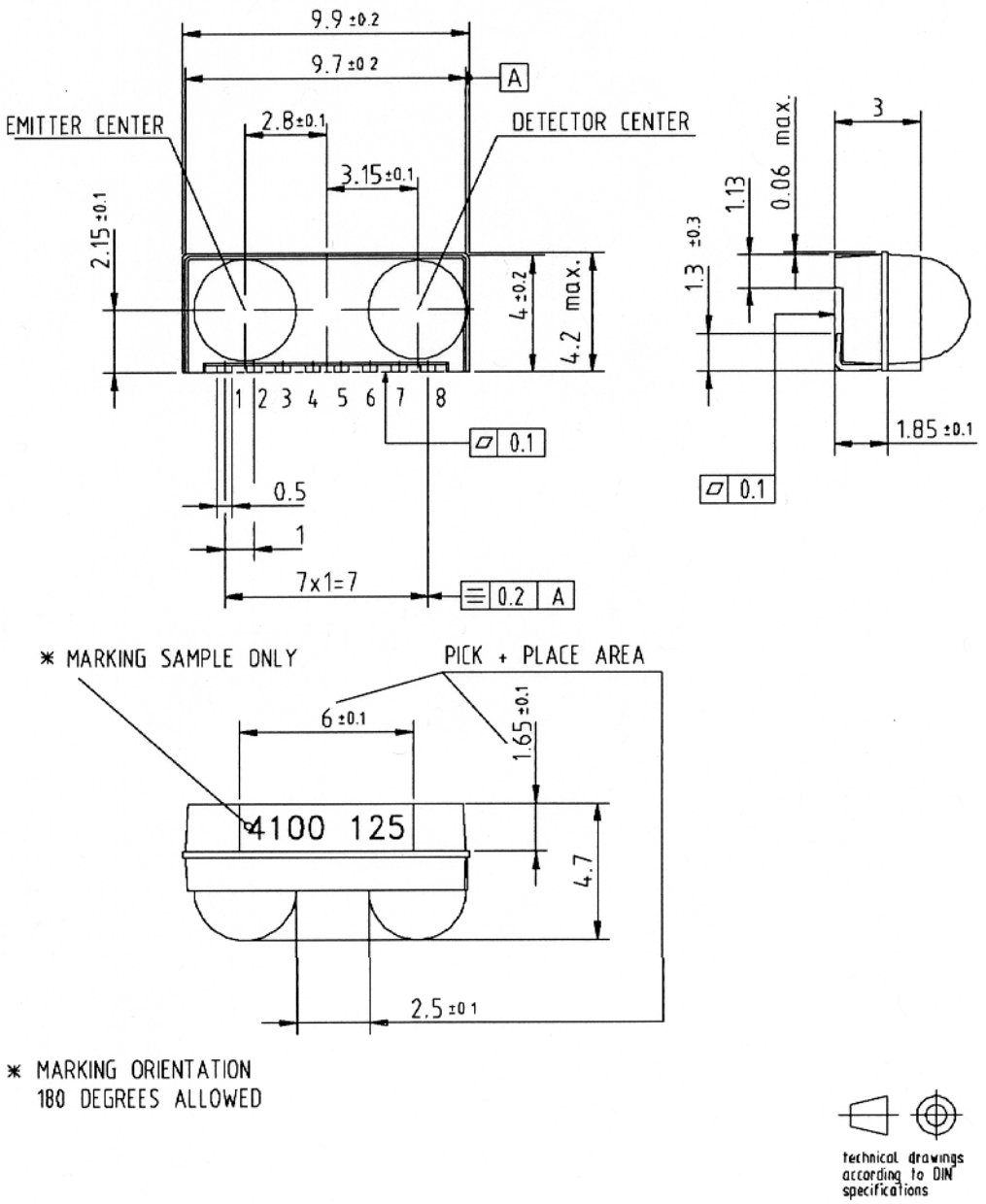
Figure 3.



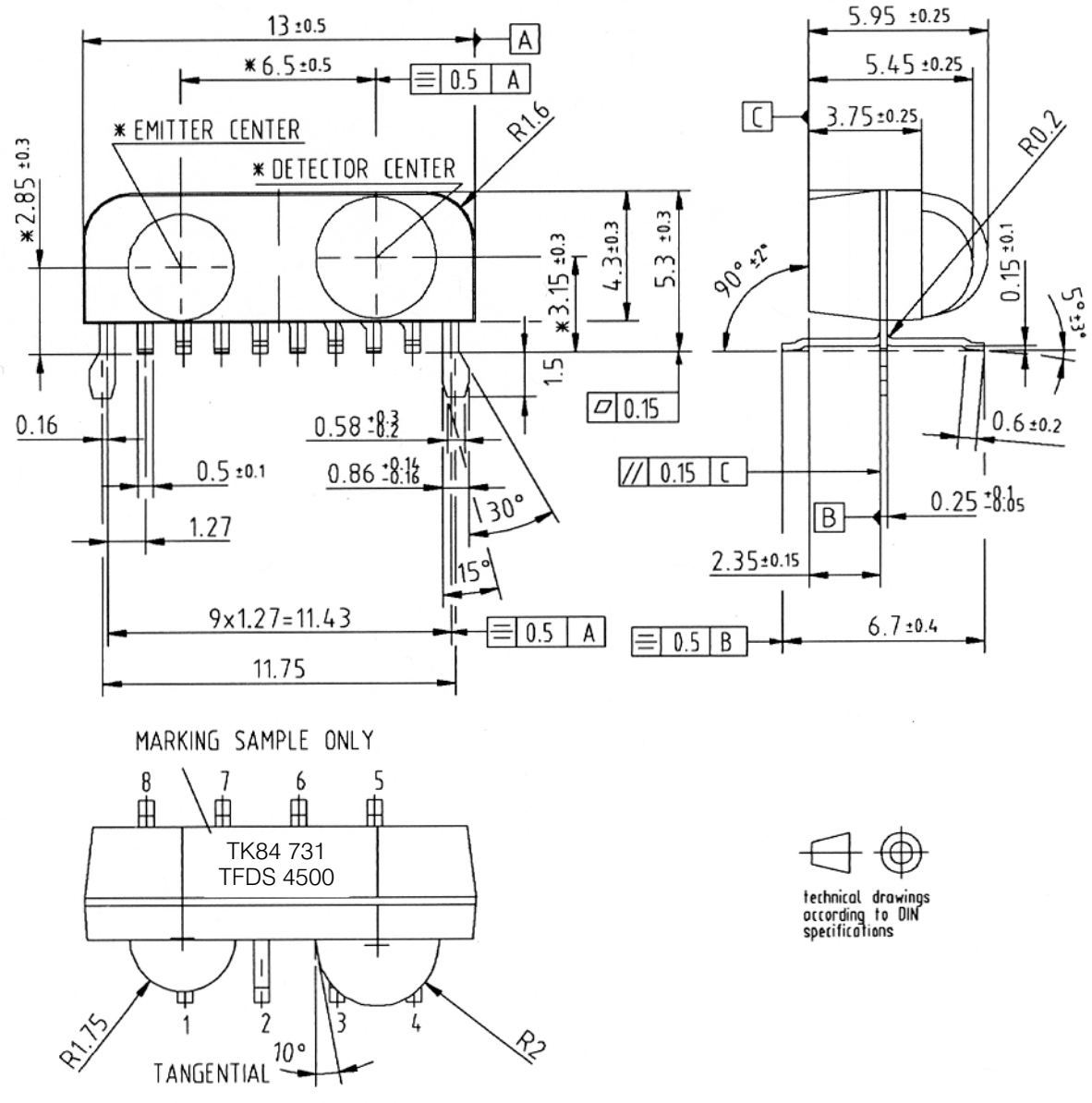
TFDU4100 (Note: Typical Values Listed)
Receive Mode
@5 V: I_{IRED} = 300 mA, I_S = 1.3 mA
@2.7 V: I_{IRED} = 300 mA, I_S = 1.0 mA
Transmit Mode
@5 V: I_{IRED} = 300 mA, I_S = 5 mA (Avg.)
@2.7 V: I_{IRED} = 300 mA, I_S = 3.5 mA (Avg.)

Figure 4.

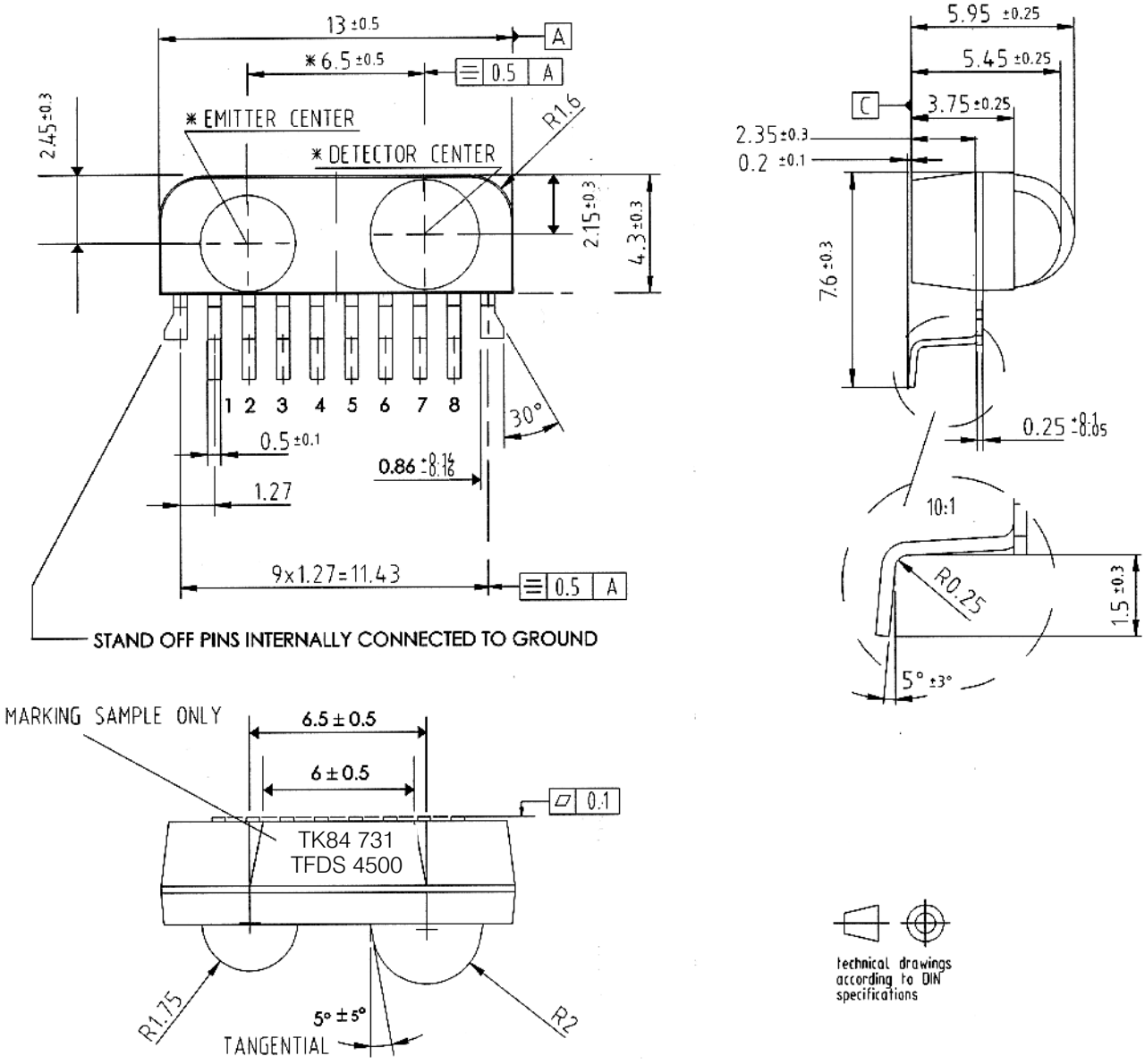
TFDU4100 – BabyFace (Universal) Package
Mechanical Dimensions



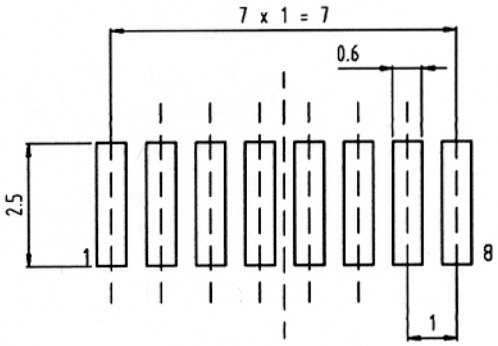
TFDS4500 – Side View Package
Mechanical Dimensions



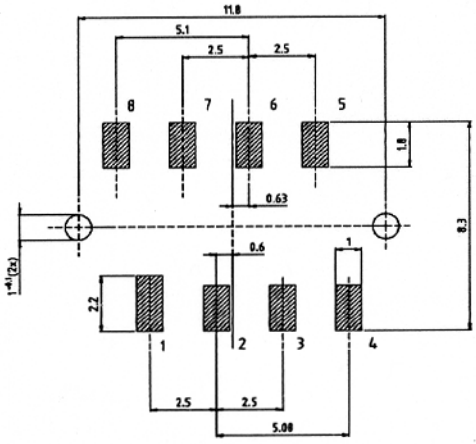
TFDT4500 – Top View Package
Mechanical Dimensions



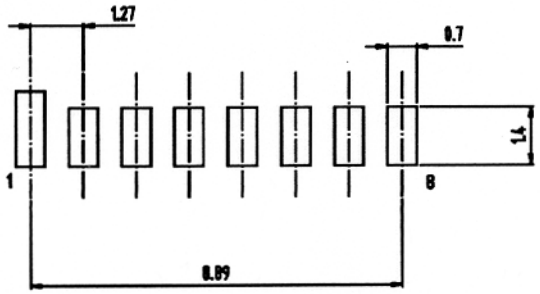
Recommended SMD Pad Layout[a]



TFDU4100 - BabyFace (Universal) Package



TFDS4500 - Side View Package

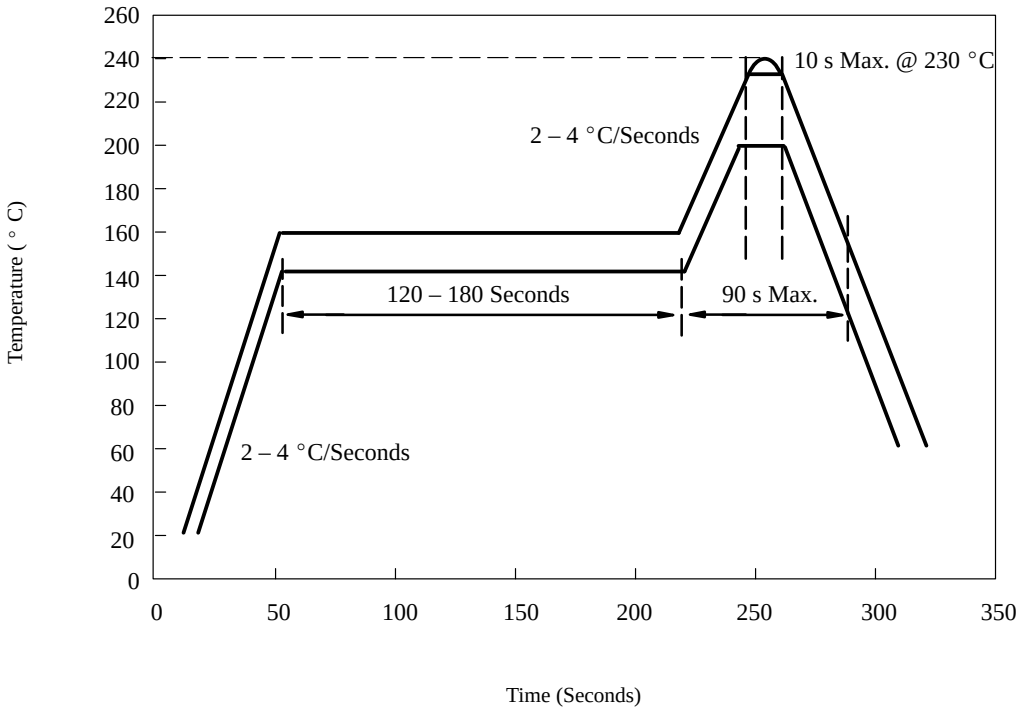


TFDT4500 - Top View Package

(note: leads of the device should be at least 0.3 mm within the ends of the pads. Pad 1 is longer to designate pin 1 connection to transciver)

a. The leads of the device should be soldered in the center position.

Recommended Solder Profile



Current Derating Curve