NOVATEK
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Data Sheet

NT7533

65 X 102 RAM-Map

STN LCD Controller/Driver

V1.0

Revision History

NT7533 Specification Revision History		
Version	**Content**	**Date**
1.0	Released	Mar. 2005

Features

■ 65 x 102 dot RAM-Map display LCD controller/driver
■ RAM capacity: 65 x 102 = 6,630 bits
■ Power supply voltage:
  - VDD1 = 1.8 ~ 3.5 V (for serial interface)
  - VDD1 = 2.0 ~ 3.5 V (for parallel interface)
  - VDD2 = 2.4 ~ 3.5 V (power for logic)
  - VDD3 = 2.4 ~ 3.5 V (power for high voltage generator)
  - VLCD = 4.5 ~ 11 V
■ On chip LCD driving voltage generator or selectable external power supply
■ Programmable 4, 3 and 2 times on chip DC-DC converter
■ Built-in voltage regulator to generate VLCD
■ Built-in voltage follower to generate intermediate LCD bias voltage
■ Built-in oscillator requires no external components
■ Programmable bias values (1/6~1/9) displayed on LCD
■ Partial display function (24-lines display)
■ High-speed 8-bit parallel interface for 8080 or 6800 series
■ Serial interface
■ 400KHz fast I^{2}C-bus interface
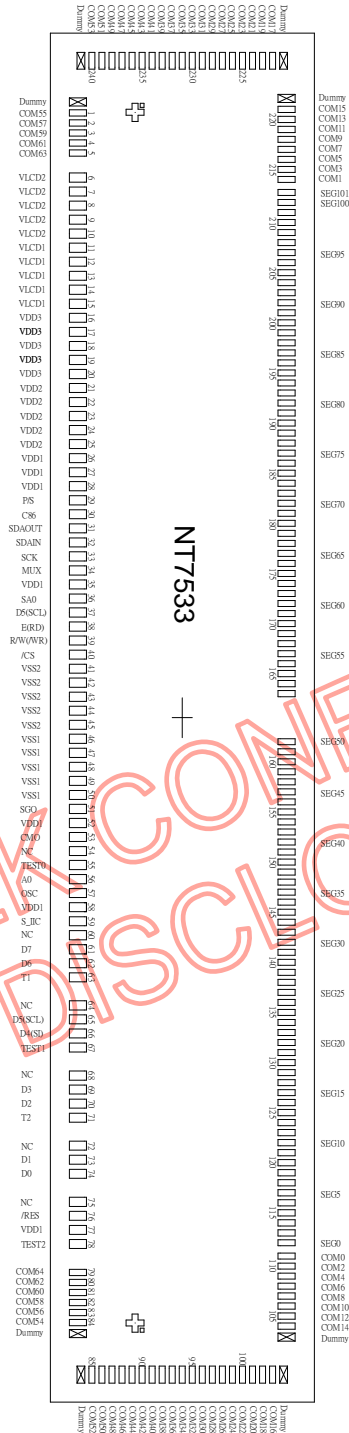■ Power save function
■ CMOS process

General Description

The NT7533 is a single-chip LCD controller/driver LSI for dot-matrix liquid crystal displays, which is connected to a microprocessor bus. It accepts display data through 8-bit parallel (8080 or 6800 series), serial or I^{2}C-bus directly sent from a microprocessor and stores it in an on-chip display RAM. It generates an LCD drive signal independent of a microprocessor clock.
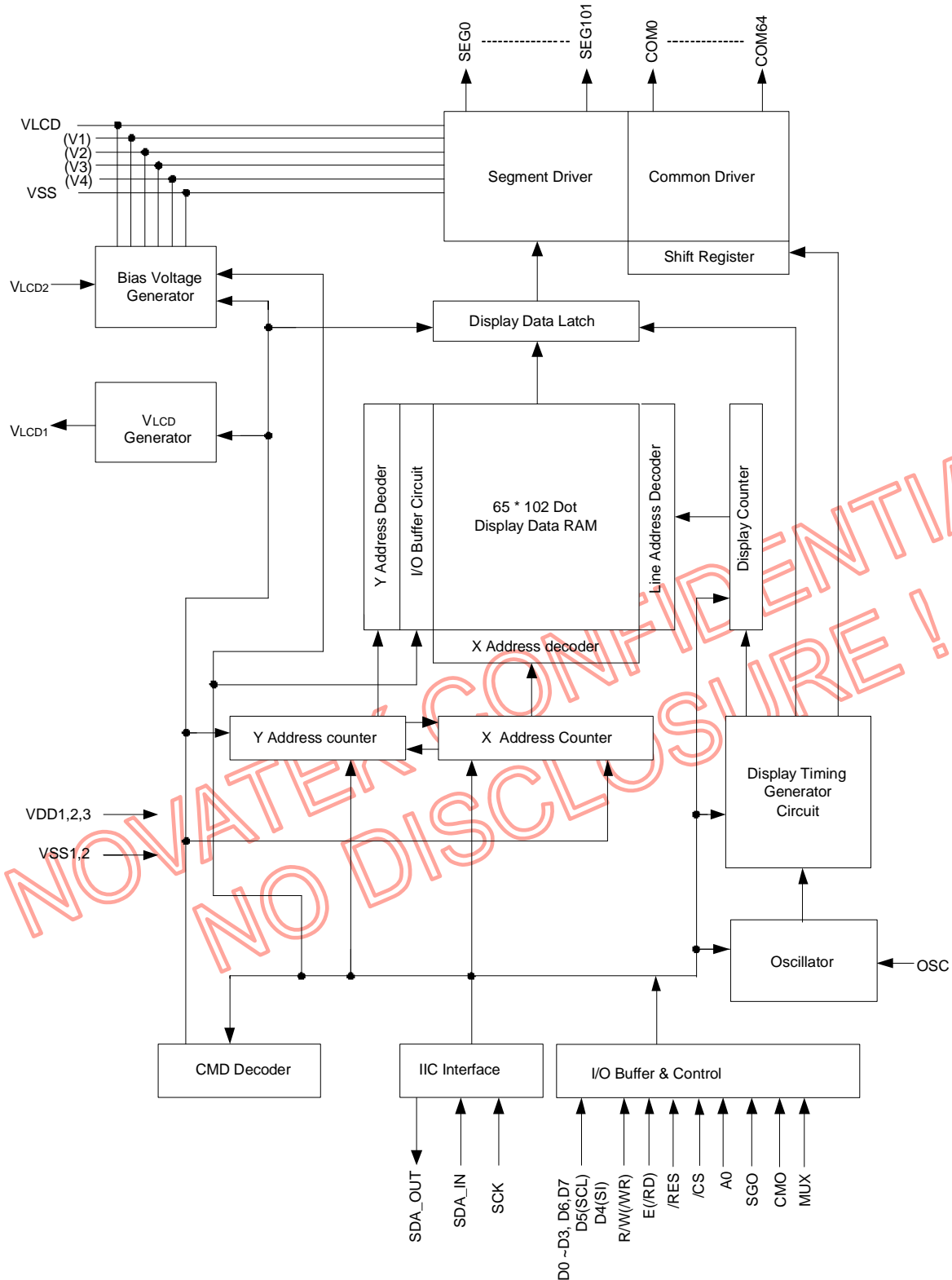
The set of the on-chip display RAM of 65 x 102 bits and every one-to-one correspondence between LCD panel pixel dots and on-chip RAM bits permits implementation of displays with a high degree of freedom.

The NT7533 contains 65 common output circuits and 102 segment output circuits. It can make 65 X 102 and 48 X 102 dot displays with pad option (MUX).

All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltage, resulting in a minimum of external components. No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement high-performance handy display system with minimum current consumption and the smallest LSI configuration.

Pad Configuration (Bumper face up)

NT7533

Left side pads (top to bottom):
Dummy, COM55, COM57, COM59, COM61, COM63, VLCD2, VLCD2, VLCD2, VLCD2, VLCD2, VLCD1, VLCD1, VLCD1, VLCD1, VLCD1, VDD3, **VDD3**, VDD3, **VDD3**, VDD3, VDD2, VDD2, VDD2, VDD2, VDD2, VDD1, VDD1, VDD1, P/S, C86, SDAOUT, SDAIN, SCK, MUX, VDD1, SA0, D5(SCL), E(RD), R/W(WR), /CS, VSS2, VSS2, VSS2, VSS2, VSS2, VSS1, VSS1, VSS1, VSS1, VSS1, SGO, VDD1, CMO, NC, TEST0, A0, OSC, VDD1, S_IIC, NC, D7, D6, T1, NC, D5(SCL), D4(SI), TEST1, NC, D3, D2, T2, NC, D1, D0, NC, /RES, VDD1, TEST2, COM64, COM62, COM60, COM58, COM56, COM54, Dummy

Right side pads (top to bottom):
Dummy, COM15, COM13, COM11, COM9, COM7, COM5, COM3, COM1, SEG101, SEG100, SEG95, SEG90, SEG85, SEG80, SEG75, SEG70, SEG65, SEG60, SEG55, SEG50, SEG45, SEG40, SEG35, SEG30, SEG25, SEG20, SEG15, SEG10, SEG5, SEG0, COM0, COM2, COM4, COM6, COM8, COM10, COM12, COM14, Dummy

Block Diagram

NT7533

Pad Descriptions

Power Supply

Pad No.	Designation	I/O	Description
26 – 28 35, 52, 58,77	VDD1	Supply	Pad 26 -28 are the power supply for Interface. These pads must be connected together. Pad 35, 52, 58 and 77 are used for pad option.
21 – 25	VDD2	Supply	Power supply for logic. These pads must be connected together.
16 – 20	VDD3	Supply	Power supply for analog. These pads must be connected together.
46 – 50	VSS1	Supply	Ground for logic
41 – 45	VSS2	Supply	Ground for HV-generator (analog)
11 – 15	VLCD1	O	VLCD output pad. If VLCD is generated internally, this pad must be connected with VLCD2.
6 – 10	VLCD2	I	This input used for the generation of the LCD bias levels.

Liquid Crystal Drive Pad

Pad No.	Designation	I/O	Description
112 – 213	SEG0 - SEG101	O	Segment signal outputs for LCD display. In the display off period or power-down mode, all pins output VSS2 level.
1 - 5 79 – 111 214 – 240	COM0 - COM63	O	Common signal outputs for LCD display. In the display off period or power-down mode, all pins output VSS2 level.

Configuration Pad

Pad No.	Designation	I/O	Description
51	SGO	I	This pad is used to determine the output number of Segment. When SGO = "H": there are 102 segment outputs (Seg0 ~ 101) When SGO = "L": there are 101 segment outputs (Seg0 ~ 100)
53	CMO	I	Instruction Set selection pad: When CMO = "H", use the Instruction Table 2. When CMO = "L", use the Instruction Table 1.
34	MUX	I	This pad is used to determine the duty ratio When MUX = "H", the Common output is 1/65 duty (COM0 ~ 64) When MUX = "L", the Common output is 1/48 duty (COM0 ~ 47)

System Bus Connection Pads

Pad No.	Designation	I/O	Description
29	P/S	I	Serial/Parallel selection pad: P/S = "H": parallel interface P/S = "L": serial interface When I²C interface is used (S_IIC = "H"), this pad must be connected to VDD1 or VSS1.
30	C86	I	Select MPU parallel interface mode: When P/S = "H"(parallel mode): C86 = "H": 6800 series MPU interface C86 = "L": 8080 series MPU interface When P/S = "L"(serial or IIC mode) : C86 should be connected to VDD1 or VSS1.
40	/CS	I	This is the chip select signal. When /CS = "L", then the chip select becomes active, and data/command I/O is enabled. Must be fixed to VDD1 or VSS1 when I²C interface is selected.
56	A0	I	A0 = "H": Indicates that D0 to D7 are Display data A0 = "L": Indicates that D0 to D7 are Control data If the IIC interface is selected, fix this pad to VDD or VSS level.
76	/RES	I	When /RES is set to "L", the settings are initialized. The minimum pulse width for a reset signal is 200 μ s.
39	R/W (/WR)	I	When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When connected with an 8080 MPU, it is active LOW. This pad is connected to the /WR signal of the 8080 MPU, and writes data at the low level. When the serial or I²C interface is selected, fix this pad to VDD1 or VSS1.
38	E (/RD)	I	When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable signal input of the 6800 series MPU. When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /RD signal and the NT7533 data bus is in an output status when this signal is LOW. When using a serial or I²C interface, this pad must be connected to VDD1 or VSS1.
37, 61, 62, 65, 66, 69, 70, 73, 74	D0 ~ D3, D6, D7 D4 (SI) D5 (SCL)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then D4 serves as the serial data input terminal (SI) and D5 serves as the serial clock input terminal (SCL). At that time, D0 to D3, D6 and D7 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.
59	S_IIC	I	This is the MPU interface switch terminal. S_IIC = "H": Use I²C interface. S_IIC = "L": Use 6800, 8080 parallel MPU interface or serial Interface.

Pad No.	Designation	I/O	Description
33	SCK	I	This pad is used to input the I^{2}C-bus clock signal. When use Serial or Parallel interface, this pad must be connected to VSS1.
32	SDAIN	I	This pad is the data input of I^{2}C -bus. When using Serial or Parallel interface, this pad must be connected to VSS1.
31	SDAOUT	O	This is the I^{2}C -bus acknowledge output. When using Serial or Parallel interface, this pad must be connected to VSS1.
36	SA0	I	To distinguish the different address of LCD driver on IIC-bus with the pad. When using serial or parallel interface, this pad must be connected to VSS1.
57	OSC	I/O	Oscillator. When the on-chip oscillator is used, this input must be connected to VDD1. An external clock signal, if used, is connected to this input.

Test Pad

Pad No.	Designation	I/O	Description
63, 71	T1, T2	T	Test pads. When NT7533 is used, T1 must be connected to VSS1 and T2 is left open.
55, 67, 78	TEST0, 1, 2	T	Test pad. TEST0, TEST1 must be connected to VSS1 and TEST2 be connected to VDD1 when NT7533 is used.
60, 64, 68, 72, 75	NC	T	Test pad. No connection for user.

Functional Descriptions

Microprocessor Interface

The NT7533 can transfer data via 8-bit bi-directional data bus (D7 to D0) or via serial data input (SI) or I^{2}C-bus. When high or low is selected for the parity of S_IIC pad and P/S pad, either 8-bit parallel data input or serial data or I^{2}C input can be selected as shown in Table 1. When serial (serial and I^{2}C bus) data input is selected, the RAM data cannot be read out.

Table 1

S_IIC	P/S	Type	/RES	/CS	A0	E(/RD)	R/W (/WR)	C86	D4	D5	D7, D6 D3 ~ D0	SDA (IN, OUT)	SCK
L	H	Parallel input	/RES	/CS	A0	E(/RD)	R/W (/WR)	C86	D4	D5	D7, D6 D3 ~ D0	-	-
L	L	Serial input	/RES	/CS	A0	(HZ)	(HZ)	-	SI	SCL	(HZ)	(HZ)	(HZ)
H	-	I^{2}C input	/RES	-	-	-	-	-	(HZ)	(HZ)	(HZ)	SDA	SCL

"-" Must always be high or low

Parallel Interface

When the NT7533 selects parallel input (P/S = "H" & S_IIC = "L"), the 8080 series microprocessor or 6800 series microprocessor can be selected by the C86 pad to be connected high or low as shown in Table 2.

Table 2

C86	Type	/RES	/CS	A0	E(/RD)	R/W(/RD)	D0 ~ D7
H	6800 microprocessor bus	/RES	/CS	A0	E	R/W	D0 ~ D7
L	8080 microprocessor bus	/RES	/CS	A0	/RD	/WR	D0 ~ D7

Data Bus Signals

The NT7533 identifies the data bus signal according to A0, E (/RD), R/W (/WR) signals as shown in Table 3.

Table 3

Common	6800 processor	8080 processor		Function
A0	R/W	/RD	/WR	
0	1	0	1	Reads status
0	0	1	0	Writes control data in internal register. (Command)
1	1	0	1	Read display data.
1	0	1	0	Write display data.

*A dummy read is required before the first actual display data read for parallel interface.

Serial Interface (P/S is low & S_IIC is low)

When the serial interface has been selected (P/S = Low, S_IIC= Low)then when the chip is in active state (/CS= "Low") the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.

The A0 input is used to determine whether the serial data input is display data, and when A0 = "L" then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.
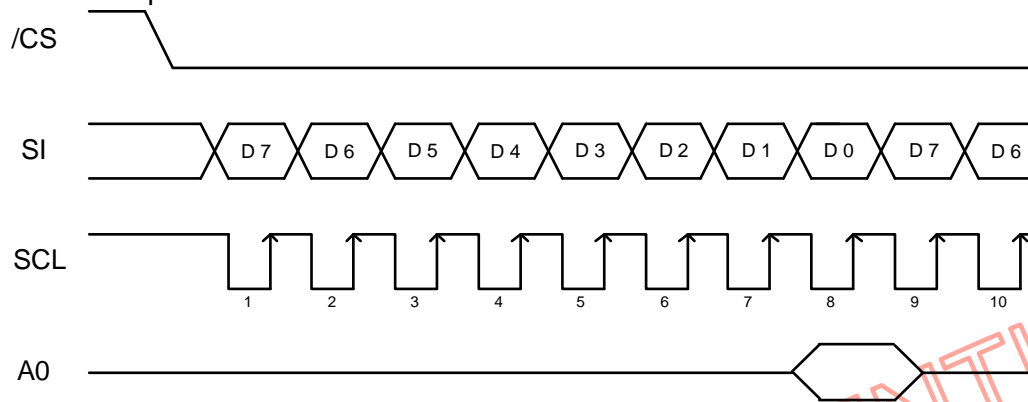
Fig. 1 Data Transfer of Serial interface

Note:

- When the chip is not active, the shift registers and the counter are reset to their initial states.
- Reading is not possible while in serial interface mode.
- Caution is required for the SCL signal when there are line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

I^{2}C-bus Interface

The NT7533 can transfer data via a standard I^{2}C-bus and uses slave mode only in communication. The command or RAM data can be written into the chip and the status can be read out of the chip.

Characteristics of the I^{2}C-bus

The I^{2}C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCK). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit Transfer (see Fig.2)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as a control signal.

Start and Stop conditions (see Fig.3)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

System configuration (see Fig.4)

• Transmitter: The device that sends the data to the bus.
• Receiver: The device that receives the data from the bus.
• Master: The device that initiates a transfer generates clock signals and terminates a transfer.
• Slave: The device addressed by a master.
• Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
• Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
• Synchronization: Procedure to synchronize the clock signals of two or more devices.

Acknowledge (see Fig.5)

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge signal after the reception of each byte. If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCK LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and release the clock line SCK. Also a master receiver must generate an acknowledge signal after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge signal related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge signal on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

Protocol

The NT7533 supports both data write and status read access. The R/W bit is part of the slave address. Before any data is transmitted on the I^{2}C-bus, the device, which should respond, is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the NT7533. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0 (VSS1) or 1 (VDD1). The I^{2}C-bus protocol is illustrated in Fig.5. The sequence is initiated with a START condition (S) from the I^{2}C-bus master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^{2}C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and A0 (note1), plus a data byte (see Fig.5). The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte is with a cleared Co-bit, only data bytes will follow. The state of the A0 bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended NT7533 device. If the A0 bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte.
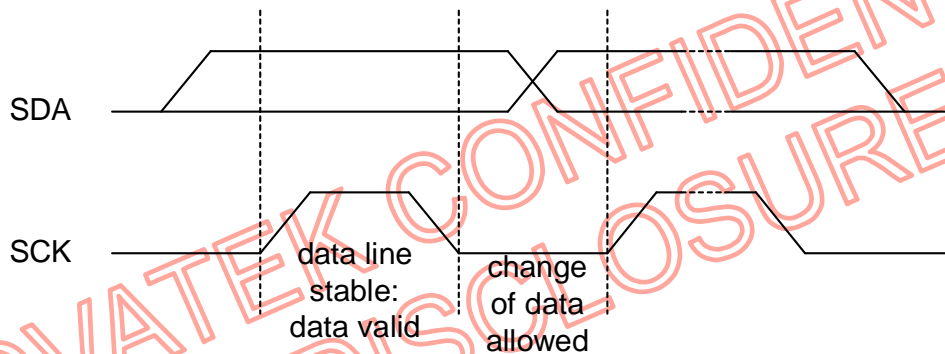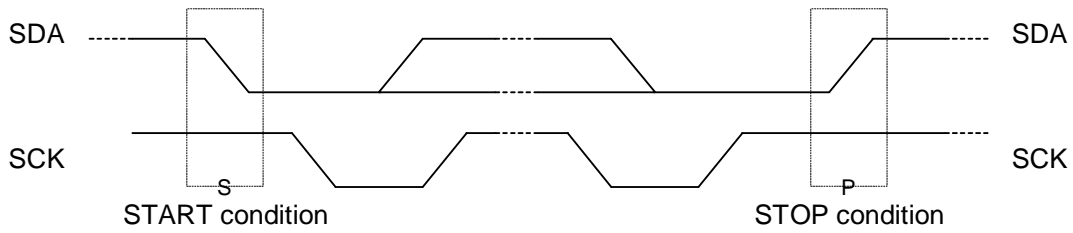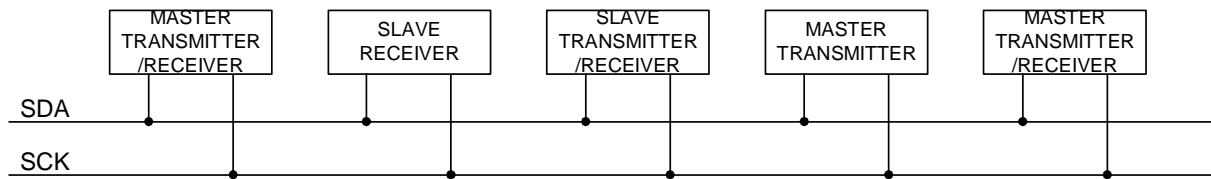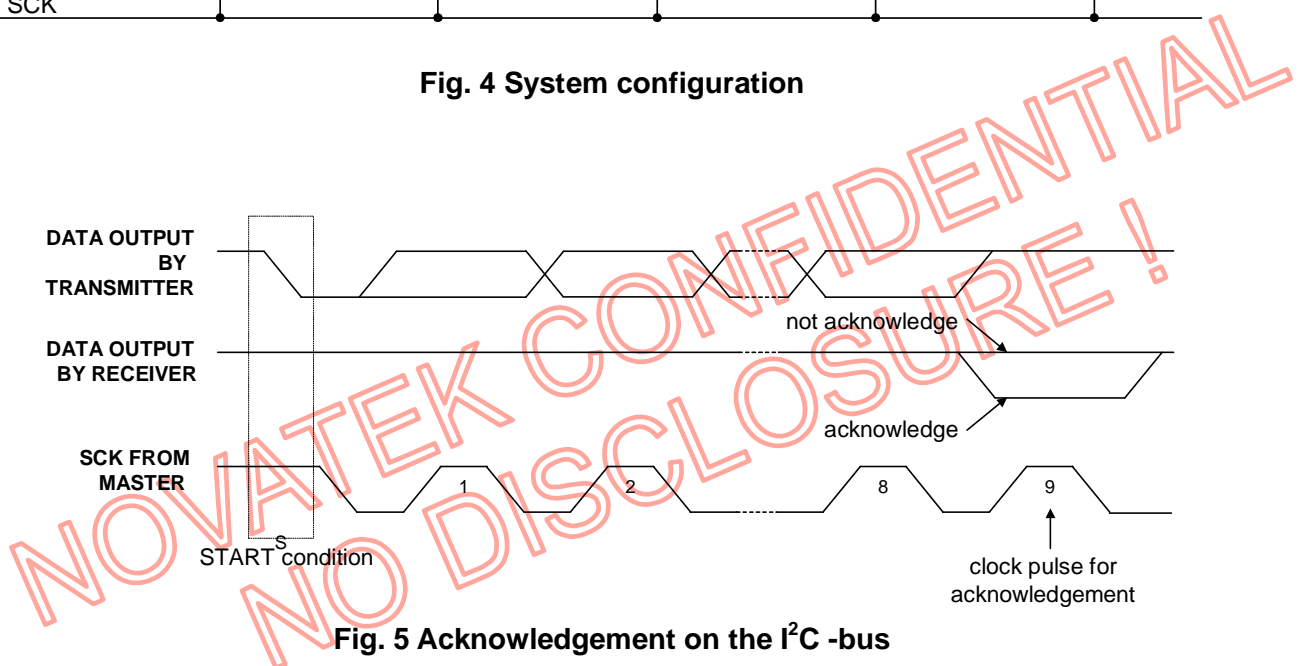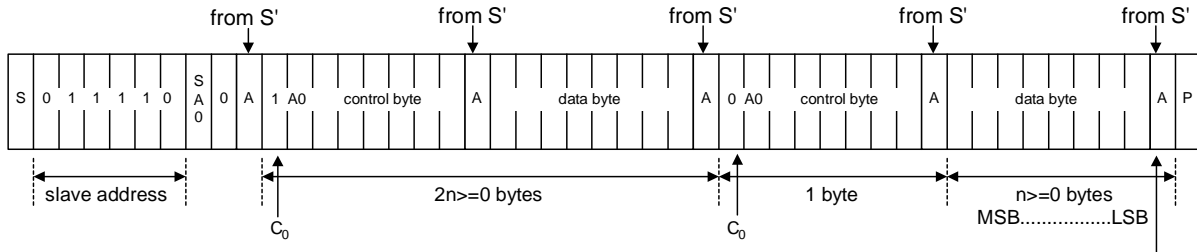

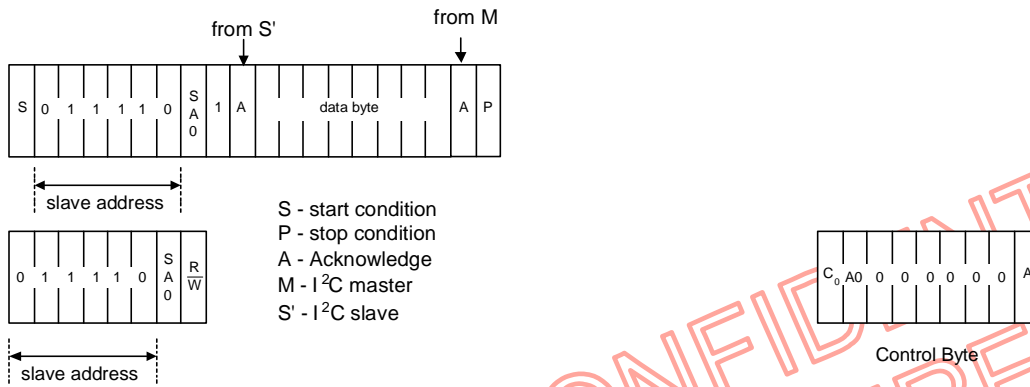**Fig. 2 Bit Transfer**

Fig. 3 Definition of start and stop conditions

Fig. 4 System configuration

Fig. 5 Acknowledgement on the I²C -bus

(i) Master transmits data to slave receiver; write mode

(ii) Master reads status from slave; read mode

S - start condition
P - stop condition
A - Acknowledge
M - I^{2}C master
S' - I^{2}C slave

Fig. 6 I^{2}C –bus Protocol

Note:

1. Co = "0" : The last control byte , only data bytes to follow，
   Co = "1" : Next two bytes are a data byte and another control byte；
2. A0 = "0" : The data byte is for command operation,
   A0 = "1" : The data byte is for RAM operation.

Chip Select Inputs

The NT7533 has a chip-select pad: /CS and it is active when it is low. D0 to D7 are high impedance and A0, E and R/W inputs are disabled.

When serial input interface is selected, the shift register and counter are reset.

Display Data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 65 (Y * 8 bit + 1)*102 dot structure. It is possible to access the desired bit by specifying the row address and the column address. Because, as is shown in Fig. 8, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the tie of display common direction, there are few constraints at the time of display data transfer when multiple NT7533 chips are used, thus and display structures can be created easily and with a high degree of freedom.

Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display.

Moreover, the NT7533 can store the display data in the opposite placement of a byte. There is a register DO can be set to determine the place of MSB.

When DO = 0, the MSB is on the top;
When DO = 1, the LSB is on the top (see Fig. 7).

DO = 0

Display data RAM   Display on LCD

DO = 1

Display data RAM   Display on LCD

Fig.7

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when OSC pad is connected to VDD1. An external clock signal, if used, is connected to the OSC pad.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of access to the display data RAM by the MPU. Consequently, even if the display data Ram is accessed asynchronously during the liquid crystal display, there is absolutely no adverse effects (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive waveform using a 2-frame alternating current drive method, as is shown in Fig. 10, for the liquid crystal drive circuit.

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. Common output mode select instruction specifies the scanning direction of the common output pads.

Table 4

Duty	Status	Common output pads		Remark
		COM [0-47]	**COM [48-63]**	
1/48	Normal	COM [0-47]	NC	MY=0
	Reverse	COM [47-0]	NC	MY=1
1/65	Normal	COM [0-64]		MY=0
	Reverse	COM [64-0]		MY=1

When the pad "Duty" is connected to "High", the NT7533 has 1/65 duty output, and 1/48 duty when this pad is connected to "Low". Changing the scan direction of Common is applicable to the NT7533.

When MY = 0, the scan direction is normal (COM0 ~ COM47/64);
When MY = 1, the scan direction is reversed (COM47/64 ~ COM0).

Segment Output Control Circuit

There are two types of segment output defaulted direction:
1. When CMO is connected to VSS1, the defaulted segment output is described as below:

    When MX = 0, the segment output direction is normal (Seg0 ~ Seg101);
    When MX = 1, the segment output direction is reversed (Seg101 ~ Seg0).

2. When CMO is connected to VDD1, the segment output direction is Seg101 ~ Seg0 (see Fig. 10, 11).

To change the relationship between RAM column address and segment driver is applicable. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during LCD module assembly. User can set the register "MX" to control the segment output.

CMO = 0;
1/48duty

Page Address (bin)	DO=0	DO=1		Line Address (hex)	Common Output MY=0	Common Output MY=1
	D7	D0		00	COM0	COM47
	D6	D1		01	COM1	COM46
	D5	D2		02	COM2	COM45
000	D4	D3		03	COM3	COM44
	D3	D4		04	COM4	COM43
	D2	D5		05	COM5	COM42
	D1	D6		06	COM6	COM41
	D0	D7		07	COM7	COM40
	D7	D0		08	COM8	COM39
	D6	D1		09	COM9	COM38
	D5	D2		0A	COM10	COM37
001	D4	D3		0B	COM11	COM36
	D3	D4		0C	COM12	COM35
	D2	D5		0D	COM13	COM34
	D1	D6		0E	COM14	COM33
	D0	D7		0F	COM15	COM32
	D7	D0		10	COM16	COM31
	D6	D1		11	COM17	COM30
	D5	D2		12	COM18	COM29
010	D4	D3		13	COM19	COM28
	D3	D4		14	COM20	COM27
	D2	D5		15	COM21	COM26
	D1	D6		16	COM22	COM25
	D0	D7		17	COM23	COM24
	D7	D0		18	COM24	COM23
	D6	D1		19	COM25	COM22
	D5	D2		1A	COM26	COM21
011	D4	D3		1B	COM27	COM20
	D3	D4		1C	COM28	COM19
	D2	D5		1D	COM29	COM18
	D1	D6		1E	COM30	COM17
	D0	D7		1F	COM31	COM16
	D7	D0		20	COM32	COM15
	D6	D1		21	COM33	COM14
	D5	D2		22	COM34	COM13
100	D4	D3		23	COM35	COM12
	D3	D4		24	COM36	COM11
	D2	D5		25	COM37	COM10
	D1	D6		26	COM38	COM9
	D0	D7		27	COM39	COM8
	D7	D0		28	COM40	COM7
	D6	D1		29	COM41	COM6
	D5	D2		2A	COM42	COM5
101	D4	D3		2B	COM43	COM4
	D3	D4		2C	COM44	COM3
	D2	D5		2D	COM45	COM2
	D1	D6		2E	COM46	COM1
	D0	D7		2F	COM47	COM0

Column Address	MX=0	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E		5B	5C	5D	5E	5F	60	61	62	63	64	65	(hex)
	MX=1	65	64	63	62	61	60	5F	5E	5D	5C	5B	5A	59	58	57		0A	09	08	07	06	05	04	03	02	01	00	
Segment Output		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14		91	92	93	94	95	96	97	92	99	100	101	

Fig. 8

CMO = 0;
1/65 duty

Fig. 9

**CMO = 1;
1/48duty**

Page Address (bin)		Line Address (hex)	Common Output
000	D7	00	COM0
	D6	01	COM1
	D5	02	COM2
	D4	03	COM3
	D3	04	COM4
	D2	05	COM5
	D1	06	COM6
	D0	07	COM7
001	D7	08	COM8
	D6	09	COM9
	D5	0A	COM10
	D4	0B	COM11
	D3	0C	COM12
	D2	0D	COM13
	D1	0E	COM14
	D0	0F	COM15
010	D7	10	COM16
	D6	11	COM17
	D5	12	COM18
	D4	13	COM19
	D3	14	COM20
	D2	15	COM21
	D1	16	COM22
	D0	17	COM23
011	D7	18	COM24
	D6	19	COM25
	D5	1A	COM26
	D4	1B	COM27
	D3	1C	COM28
	D2	1D	COM29
	D1	1E	COM30
	D0	1F	COM31
100	D7	20	COM32
	D6	21	COM33
	D5	22	COM34
	D4	23	COM35
	D3	24	COM36
	D2	25	COM37
	D1	26	COM38
	D0	27	COM39
101	D7	28	COM40
	D6	29	COM41
	D5	2A	COM42
	D4	2B	COM43
	D3	2C	COM44
	D2	2D	COM45
	D1	2E	COM46
	D0	2F	COM47

Column Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E		5B	5C	5D	5E	5F	60	61	62	63	64	65	(hex)
Segment Output	101	100	99	98	97	96	95	94	93	92	91	90	89	88	87		10	9	8	7	6	5	4	3	2	1	0	

Fig. 10

CMO = 1;
1/65 duty

Page Address (bin)	DO =0																																	Line Address (hex)	Common Output
	D7																																		00	COM0
	D6																																		01	COM1
	D5																																		02	COM2
0000	D4																																		03	COM3
	D3																																		04	COM4
	D2																																		05	COM5
	D1																																		06	COM6
	D0																																		07	COM7
	D7																																		08	COM8
	D6																																		09	COM9
	D5																																		0A	COM10
0001	D4																																		0B	COM11
	D3																																		0C	COM12
	D2																																		0D	COM13
	D1																																		0E	COM14
	D0																																		0F	COM15
	D7																																		10	COM16
	D6																																		11	COM17
	D5																																		12	COM18
0010	D4																																		13	COM19
	D3																																		14	COM20
	D2																																		15	COM21
	D1																																		16	COM22
	D0																																		17	COM23
	D7																																		30	COM48
	D6																																		31	COM49
	D5																																		32	COM50
0110	D4																																		33	COM51
	D3																																		34	COM52
	D2																																		35	COM53
	D1																																		36	COM54
	D0																																		37	COM55
	D7																																		38	COM56
	D6																																		39	COM57
	D5																																		3A	COM58
0111	D4																																		3B	COM59
	D3																																		3C	COM60
	D2																																		3D	COM61
	D1																																		3E	COM62
	D0																																		3F	COM63
1000	D7																																		40	COM64
Column Address		00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E						5B	5C	5D	5E	5F	60	61	62	63	64	65		(hex)	
Segment Output		101	100	99	98	97	96	95	96	94	93	92	91	90	89	88						10	9	8	7	6	5	4	3	2	1	0			

Fig. 11

Addressing

Data is downloaded in bytes into the RAM matrix of NT7533. The display RAM has a matrix of 65 by 102 bits. The columns are addressed by the address pointer. The address ranges are: X 0 to 101 (1100101), Y 0 to 8 (1000). Address outside these ranges are not allowed.

In vertical addressing mode (V=1) the Y address increments after each byte. After the last Y address (Y=7) Y wraps around to 0 and X increments to address the next column.

In horizontal addressing mode (V=0) the X address increments after each byte. After the last X address (X=1100101) X wraps around to 0 and Y increments to address the next row.

After the very last address (X=101, Y=8) the address pointers wrap around to address (X=0, Y=0).
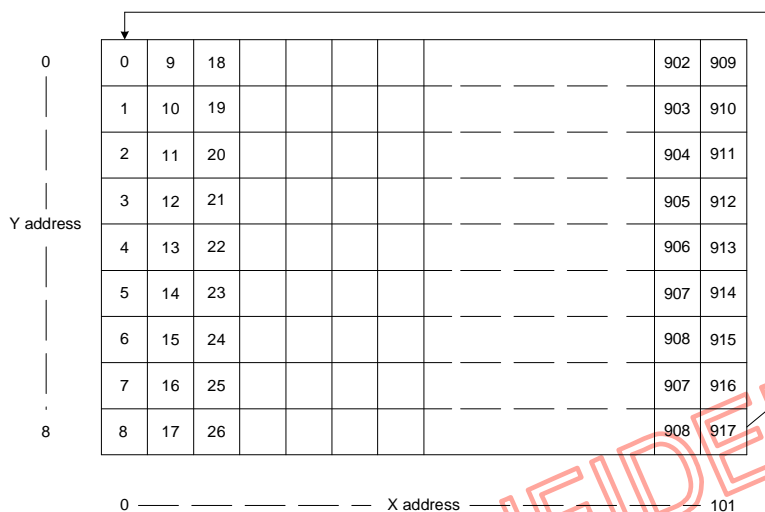
**Fig. 12   sequence of writing data bytes into RAM
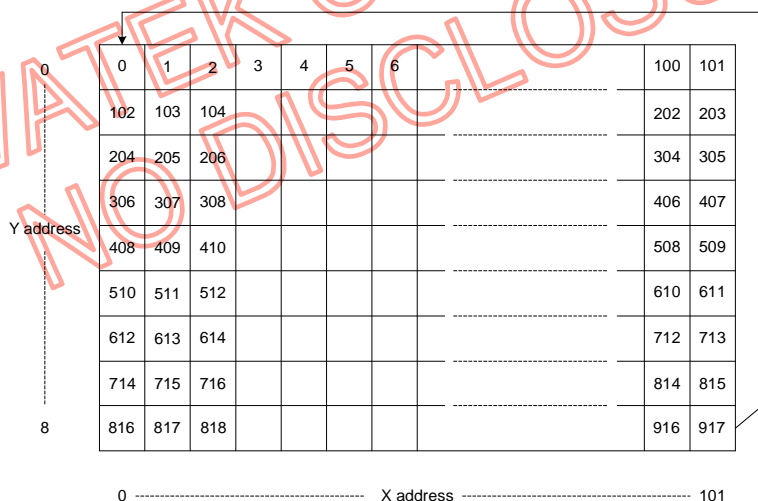With vertical addressing (V=1)**

**Fig. 13 sequence of writing data bytes into RAM
With horizontal addressing (V=0)**

LCD Power Supply

NT7533 has an internal voltage generator. When VLCD is generated on-chip the VLCD pads should be decoupled to VSS with a suitable capacitor. During 'display off' and 'power-down' the VLCD generator is also disabled. When the generator is switched off, an external voltage may be supplied at connected pads VLCD1. VLCD1 may be higher than VDD.

The NT7533 incorporates a software configuration voltage multiplier. After reset (/RES) the voltage multiplier is set to 2*VDD2. Other voltage multiplier factors are set via the command "Set HV-gen stages" shown on Instruction Table 1, 2 (page 29, 30).

LCD driving voltage VLCD Control

The optration voltege VLCD can be set by software and the generated voltage is dependent on the temperature. There are two overlapping VLCD renges are selectable via the command "HV-generator control". For the low (PRS = 0) range VA1 = 3.135V and for the high (PRS = 1) range VA2= 7.103V with steps equal to "α" in both ranges. "α" is set to 0 level of 127 possible levels by the electronic volume function depending on the data set in the 7-bit electronic volume register. The table shown below shows the value for α depending on the electronic volume register settings.The voltage at reference temperature can be calculated as:

$VLCD = (VAn + \alpha VB) + (T - TREF) * TC$
where VA1=3.135 (PRS=0), VA2=7.103V (PRS=1), α=0~127and VB=0.031V

The voltage at reference temperature can be calculated as:
$VLCD = (VAn + \alpha VB)$

The maximum voltage that can be generated depends on the VDD2 voltage and the display load current. Note that the voltage booster is turned off if electronic volume register VOP[6:0] are all set to zero.

Table 5

VOP6	VOP5	VOP4	VOP3	VOP2	VOP1	VOP0	α	VLCD
0	0	0	0	0	0	0	0	Minimum
0	0	0	0	0	0	1	1	:
0	0	0	0	0	1	0	2	:
			:					:
1	0	0	0	0	0	0	64	:
								:
1	1	1	1	1	1	0	126	:
1	1	1	1	1	1	1	127	Maximum
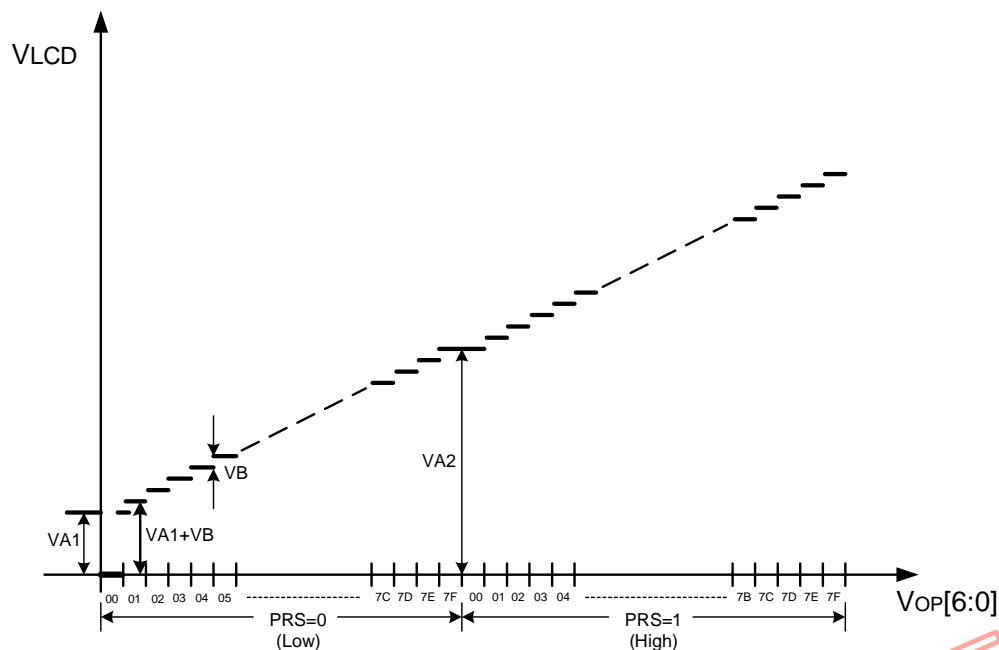
Fig. 14

The NT7533 has two types of command about setting the VLCD range and voltage pump stage. We can connect the CMO pad to "H" or "L" to set it.

When the CMO pad is connected to "H", we can set the VLCD range and voltage pump stage by writing the commands "0000010X" (H=0) and "000100XX" (H=0).
When the CMO pad is connected to "L", we can set the VLCD range and voltage pump stage by writing the commands "0001000X" (H=0) and "000010XX" (H=1).

Caution
As the programming range for the internally generated VLCD allows values above the max. allowed VLCD, the customer has to ensure while setting the VOP register and selecting the temperature compensation (TC), that under all conditions and including all tolerances the VLCD remains below 11.0V.

Temperature coefficient

Due to the temperature dependency of the liquid crystals viscosity the LCD controlling voltage VLCD must be increased with a lower temperature to maintain optimal contrast. There are 4 different temperature coefficients available in NT7533. The coefficients are selected by the two bits TC[1 : 0]. Table 11 shows the typical values of the different temperature coefficients. The coefficients are proportional to the programmed VLCD.

Default is TC1 and TC0 = 0. This selects the default temperature coefficient for the internally generated VLCD.

Table 6

TC1	TC0	Description
0	0	Temperature Coefficient 0 : -0.76E-3/℃
0	1	
1	0	Temperature Coefficient 1 : -1.05E-3/℃
1	1	
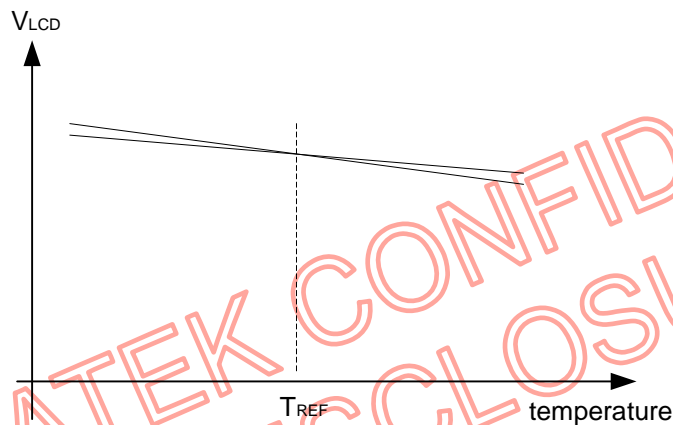
Figure 15

Segment output number

There are two types of the segment output number of NT7533. User can determine to use 101 segments outputs or 102 segment outputs by setting the status of SGO pad.

When SGO = "0", there are 101 segment outputs.
When SGO = "1", there are 102 segment outputs.

Reset Circuit

Immediately following power-on, all internal registers as well the RAM content are undefined. A /RES pulse must be applied. When reset occurs within the specified time, all internal registers are reset, however the RAM is still undefined.

Reset is accomplished by applying an external /RES pulse at /RES pad. /RES input must be<= 0.2*VDD1 when VDD1 reaches VDDmin (or higher) within a maximal time tVHRL after VDD goes high.

The state after reset is described as below:

- Normal X addressing (X = 0)
- Normal display (MY = 0)
- Power down mode (PD = 1)
- Horizontal addressing (V = 0)
- Normal instruction set (H = 0)
- Display blank (D = E = 0)
- Normal (65-lines) display (PDIS = 0)
- MSB is on the top of the RAM (DO = 0)
- Partial display line is 0 (L[6:0] = 00h)
- 2X voltage pump (S[1:0] = 00b)
- VLCD range is low (PRS = 0)
- Address counter X6 to X0 = 0; Y2 to Y0 = 0
- Temperature coefficient (TC1 to TC0 = 0)
- VLCD is equal to 0; the HV-generator is switched off (Vop6 to Vop0 = 0 and PRS = 0)
- After power-on, RAM data is undefined; the reset signal doesn't change the content of the RAM
- All LCD outputs at VSS (display off)

Bias value

The bias voltage levels are set in the ratio of R – R – nR – R – R giving a 1/(n+4) bias system. Different miltiplex rates require different factors n (see Table). This is programmed by BS[2:0]. For using 1/48 duty, the optimum Bias value n is given by

$$n = \sqrt{48} - 3 = 3.928 = 4$$

resulting in 1/8 bias.

Table 7

BS2	BS1	BS0	n	B (res. count)	Duty
0	1	0	5	9	1:65 / 1:65
0	1	1	4	8	1:48
1	0	0	3	7	1:40 / 1:34
1	0	1	2	6	1:24

Table 8

Symbol	Bias voltage for 1/N bias	Symbol	Bias voltage for 1/N bias
V0	V_{LCD}	V3	$2/N * V_{LCD}$
V1	$(N-1)/N * V_{LCD}$	V4	$1/N * V_{LCD}$
V2	$(N-2)/N * V_{LCD}$	Vss	Vss

Commands

The instruction format is divided into two modes: if A0 is set to "0" the current byte is interpreted as command byte. If A0 is set to "1" the following bytes are stored in the Display Data RAM. After every data byte the address counter is incremented automatically.

Every instruction can be sent in any order to the NT7533. A reset pulse with /RES interrupts the transmission. No data is written into the RAM. The registers are cleared.

1. Reset

   This command is used to reset the NT7533. After executing this command, the internal status is described as shown on page 25.
   *Note that the Reset command can be used only when CMO is connected to VSS1 (Low).

2. MX

   Changes the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during LCD module assembly.
   When MX = 0, the segment output is in normal direction
   When MX = 1, the segment output is in reverse direction
   *Note that the command is unavailable when CMO is connected to VDD1.

3. MY

   By setting the register MY, the scan direction of the COM output pad is selectable.
   When MY = 0, the scan direction of COM is normal (COM0 → COM64/47).
   When MY = 1, the scan direction of COM is reversed (COM64/47 → COM0).
   *Note that the command is unavailable when CMO is connected to VDD1.

4. PD

   The power-down mode is issued when the register PD = 1. The internal status in the power-down mode is as follows:
   ● All LCD outputs are at VSS (display off)
   ● Bias generator and VLCD generator off, VLCD can be disconnected
   ● Oscillator off (external clock possible)
   ● RAM contents not cleared; RAM data can be written0
   ● VLCD output is discharged to VSS in power-down mode

5. V

   When V = 0, the horizontal addressing is selected. The data is written into the RAM as shown in Fig. 13
   When V = 1, the vertical addressing is selected. The data is written into the RAM as shown in Fig.12

6. H

   When H = 0, the commands 'display control', 'set Y address' and 'set X address', 'set the PRS bit' and 'set Partial display' can be performed; when H = 1, the commands 'set Temperature', 'set the DO bit' and 'set Vop' can be performed.

7. Read Status

   This command can be used when Parallel interface is used (P/S is connected to VDD1).
   The status of registers PD, D, E, MX, MY & H can be read.

*Note that the command is unavailable when CMO is connected to VDD1.

8. PRS

    This bit is set to determine the range of VLCD.
    When PRS = 0, the VLCD output will be in the lower range.
    When PRS = 1, the VLCD output will be in the higher range. (see Fig. 14)

9. D, E

    These bits are used to select the display mode. See page 31 Instruction table.

10. Set HV-generator: S[1:0]

    The NT7533 incorporates a software configurable voltage multiplier. After reset, the voltage multiplier is set to 2*VDD2. Other voltage multiplier factors are set via the command 'Set HV-generator' (see Instruction table)

11. Set Partial display: PDIS

    The NT7533 can satisfy Partial display function by setting the PDIS bit.
    When PDIS = 0, NT7533 is in normal display mode.
    When PDIS = 1, NT7533 is in partial display mode (24-lines). We can write a two-byte command of 'Set partial display line' to set the start line of partial display area after setting this bit.
    *Note that the Partial display is available only when CMO is connected to VSS1 (Low).

12. Set Y address of RAM

    Y3 to Y0 defines the Y address vector of the display RAM. The range of Y is 0 to 8.

13. Set X address of RAM

    The X address points the segment output. The range of X is 0 to 101 (65h).

14. Temperature coefficient

    There are 4 different temperature coefficients are available in the NT7533 and the coefficients are selected by the two bits TC[1:0]. See Fig. 15

15. DO

    The bit DO is used to determine the order of every byte stored in RAM.
    When DO = 0, the MSB is on top.
    When DO = 1, the LSB is on top.
    *Note that the command is unavailable when CMO is connected to VDD1.

16. Set Vop

    The voltage at reference temperature can be calculated as VLCD (T=Tcut).
    The operating voltage VLCD can be adjusted by setting the electronic volume 'α'.
    See Fig. 14 and Table 5.

Instruction Table 1 (CMO = Low)

Instruction (H = 0 or 1)	A0	/RW	Code								Function & Remark
			D7	D6	D5	D4	D3	D2	D1	D0	
NOP	0	0	0	0	0	0	0	0	0	0	No operation
Reset	0	0	0	0	0	0	0	0	0	1	
Function Set	0	0	0	0	1	MX	MY	PD	V	H	Power down control (PD) Entry mode (V) Extended Instruction Set control (H)
Read Status	0	1	PD	-	-	D	E	MX	MY	DO	
Write Display Data	1	0	Write Data								Write data to display RAM

Instruction (H = 0)											Function & Remark
Set VLCD range (* 1.)	0	0	0	0	0	0	0	1	0	PRS	
Display Control	0	0	0	0	0	0	1	D	PDIS	E	
Set HV-gen. Stages	0	0	0	0	0	1	0	0	S1	S0	
Set Partial display line	0	0	0	0	0	1	1	0	0	0	Partial display command and set Start line of display area.
	0	0	0	L6	L5	L4	L3	L2	L1	L0	
Set Y address of RAM	0	0	0	1	0	0	Y3	Y2	Y1	Y0	Set the Y-address of RAM $0 \leqq Y \leqq 8$
Set X address of RAM	0	0	1	X6	X5	X4	X3	X2	X1	X0	Set the X-address of RAM $0 \leqq X \leqq 101$
Instruction (H = 1)											Function & Remark
Temperature Control	0	0	0	0	0	0	0	1	TC1	TC0	Set temperature coefficient (TCn)
Display configuration	0	0	0	0	0	0	1	DO	0	0	Determine the order of every byte stored in RAM
Bias system	0	0	0	0	0	1	0	BS2	BS1	BS0	Set the bias of LCD driving signal
Set V$_{OP}$	0	0	1	V$_{OP6}$	V$_{OP5}$	V$_{OP4}$	V$_{OP3}$	V$_{OP2}$	V$_{OP1}$	V$_{OP0}$	Set VLCD output voltage electronic volume register

Instruction Table 2(CMO = High)

Instruction (H = 0 or 1)	A0	/RW	Code								Function & Remark
			D7	D6	D5	D4	D3	D2	D1	D0	
NOP	0	0	0	0	0	0	0	0	0	0	No operation
Function Set	0	0	0	0	1	0	0	PD	V	H	Power down control (PD) Entry mode (V) Extended Instruction Set control (H)
Write Display Data	1	0	Write Data								Write data to display RAM

Instruction (H = 0)											Function & Remark
Set VLCD range (* 1.)	0	0	0	0	0	1	0	0	0	PRS	
Display Control	0	0	0	0	0	0	1	D	0	E	
Set Y address of RAM	0	0	0	1	0	0	Y3	Y2	Y1	Y0	Set the Y-address of RAM $0 \leq Y \leq 8$
Set X address of RAM	0	0	1	X6	X5	X4	X3	X2	X1	X0	Set the X-address of RAM $0 \leq X \leq 101$
Instruction (H = 1)											**Function & Remark**
Temperature Control	0	0	0	0	0	0	0	1	TC1	TC0	Set temperature coefficient (TCn)
HV-gen stages setting	0	0	0	0	0	0	1	0	S1	S0	Set the stage of Voltage Booster
Bias system	0	0	0	0	0	1	0	BS2	BS1	BS0	Set the bias of LCD driving signal
Set V_{OP}	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	Set VLCD output voltage electronic volume register

Bit	0	1
MX	Segment output direction is Normal	Segment output direction is Reversed
MY	Common output direction is Normal	Common output direction is Reversed
PD	Chip is normally active	Chip is in power down mode
V	Horizontal address	Vertical address
H	Use basic instruction set	Use extended instruction set
PRS	VLCD programming range: LOW	VLCD programming range: HIGH
PDIS	Normal display mode	Partial display mode
DO	The MSB is on the top	The LSB is on the top

D, E		
	00	Display blank
	01	All display on
	10	Normal display
	11	Display inversed

S [1:0]		
	00	2X charge pump; defaulted
	01	3X charge pump
	10	4X charge pump
	11	Not used

TC [1:0]		
	00	Temperature coefficient 0 (defaulted); -0.76E-3/℃ 0/℃
	10	Temperature coefficient 1; -1.05E-3/℃

BS [2:0]		
	010	1/9 bias
	011	1/8 bias
	100	1/7 bias
	101	1/6 bias

Absolute Maximum Rating*

DC Supply Voltage (VDD1, VDD2, VDD3).. -0.3V to +3.6V
DC Supply Voltage (VLCD)... -0.3V to +14.0V
Input Voltage .... -0.3V to VDD+0.3V
Operating Ambient Temperature ....-40°C to +85°C
Storage Temperature ....-55°C to +110°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics   (V_{SS}=0V, V_{DD1}=2.0~3.5V, $V_{DD2, 3}$=2.4~3.5V, Ta= -30 to 85℃ unless specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD1	Interface power supply voltage	1.8	-	3.5	V	Serial
		2.0	-	3.5		Parallel
VDD2, 3	Logic/analog circuit power supply voltage	2.4	-	3.5	V	
VLCD1, 2	LCD supply voltage range	4.5	-	11.0	V	
IDD1, 2	Operating current	-	40	60	µA	VDD1, VDD2 = 2.8V; No data access, TA = 27℃
IDD3	DC-DC power consumption	-	100	150	µA	4X boosting; VDD3 = 2.8V; built-in power supply on and VLCD = 8.5V, display on, all-on pattern; no data access and no load; TA = 27℃
		-	70	100		3X boosting; VDD3 = 2.8V; built-in power supply on and VLCD = 5.5V, display on, all-on pattern; no data access and no load; TA = 27℃
IPD	Power-down mode current consumption	-	-	1.0	µA	
VIH	Input high voltage	0.8*VDD		VDD	V	
VIL	Input low voltage	VSS		0.2*VDD	V	
VOH	Output high voltage	0.8*VDD		VDD	V	
VOL	Output low voltage	VSS		0.2*VDD	V	
ILI	Input leakage current	-1.0	-	1.0	µA	VI = VDD or VSS
IHZ	HZ leakage current	-3.0	-	3.0	µA	

DC Characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
RON	LCD driver on resistance	-	3	-	KΩ	
fOSC	Oscillation frequency	43.2	48	52.8	KHz	VDD = 2.85V; TA = 20 ~ 70℃
fFR	Frame frequency	66.5	73.8	81.2	Hz	

AC Characteristics (V$_{DD}$ = 2.4V ~ 3.5V, V$_{SS}$ = 0V, Ta = -40°C ~ +85°C, unless noted)
Reset signal
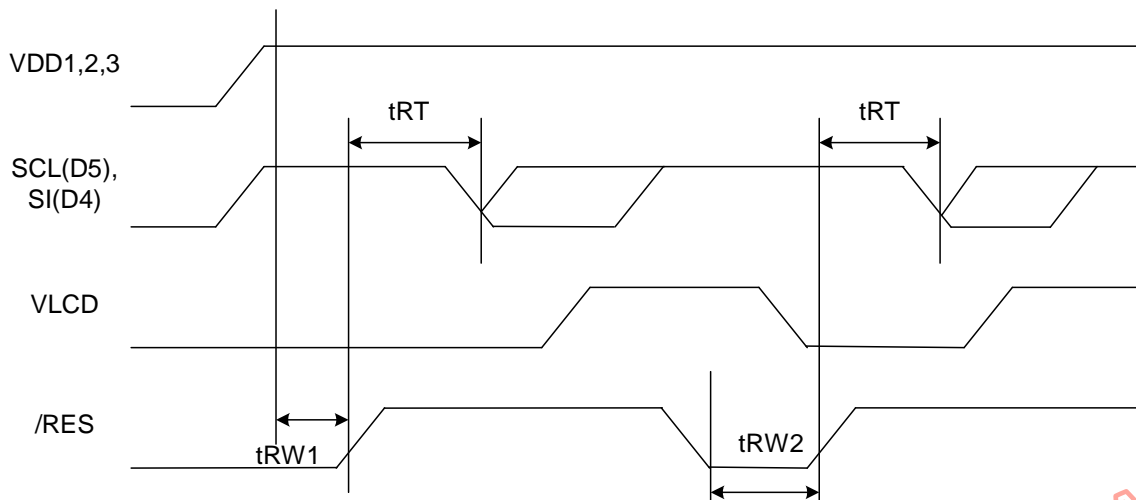
(VDD1 = 2.0 ~ 3.5V, VDD2 =2.4 ~ 3.5V, TA = -30 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tRW1	Reset pulse width 1	200			µs	
tRW2	Reset pulse width 2	100			µs	
tRT	Reset cancel	10			µs	

Parallel Interface

1. System buses Read/Write characteristics 1 (For the 8080 Series MPU)
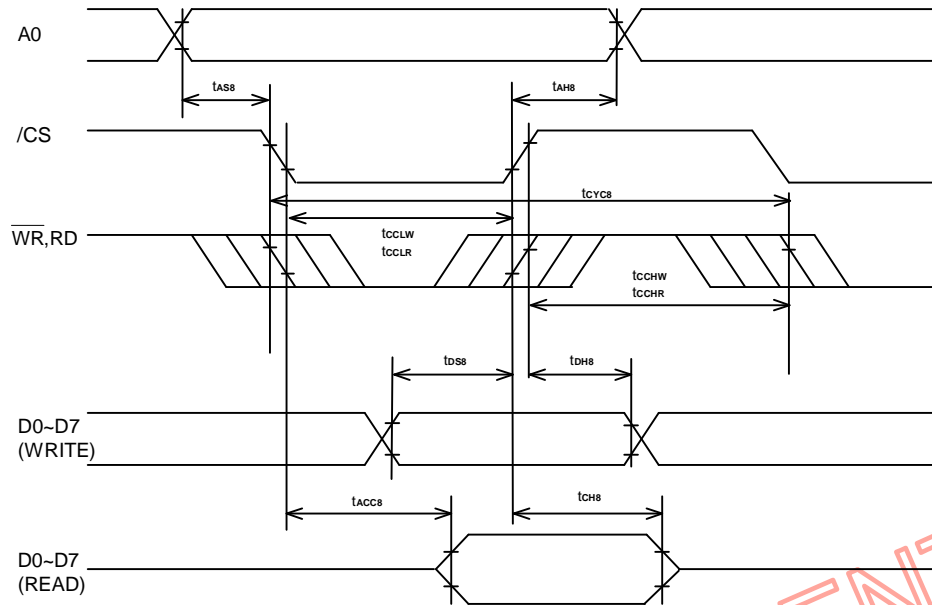
(VDD1 = 2.0 ~ 3.5V, VDD2 =2.4 ~ 3.5V, TA = -30 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tAH8	Address hold time	40	-	-	ns	
tAS8	Address setup time	40	-	-	ns	
tCYC8	System cycle time	1000	-	-	ns	
tCCLW	Control L pulse width (/WR)	200			ns	
tCCLR	Control L pulse width (/RD)	200			ns	
tCCHW	Control H pulse width (/WR)	200			ns	
tCCHR	Control H pulse width (/RD)	200	-	-	ns	
tDS8	Data setup time	160	-	-	ns	
tDH8	Data hold time	40	-	-	ns	
tACC8	/RD access time	-	-	250	ns	CL=15pF
tCH8	Output disable time	10	-	120	ns	CL=15pF

2. System Buses Read/Write Characteristics (for 6800 Series MPU)
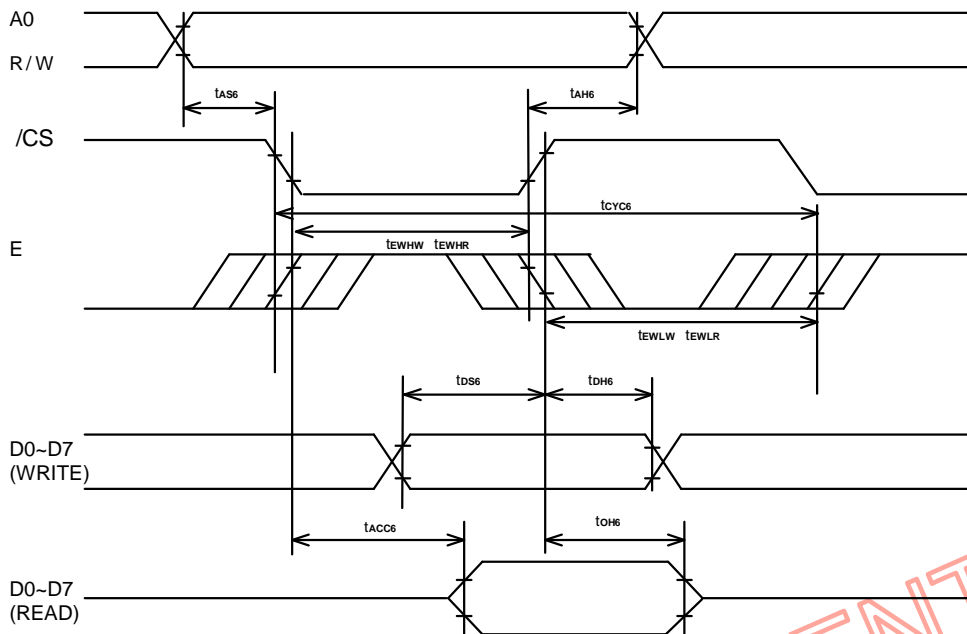
(VDD1 = 2.0 ~ 3.5V, VDD2 =2.4 ~ 3.5V, TA = -30 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tCYC6	System cycle time	1000	-	-	ns	
tAH6	Address hold time	40	-	-	ns	
tAS6	Address setup time	40	-	-	ns	
tDS6	Data setup time	160	-	-	ns	
tDH6	Data hold time	40	-	-	ns	
tACC6	Access time	-	-	250	ns	CL=15pF
tOH6	Output disable time	10	-	120	ns	CL=15pF
tEWHR	Enable H pulse width (/RD)	200	-	-	ns	
tEWHW	Enable H pulse width (/WR)	160	-	-	ns	
tEWLR	Enable L pulse width (/RD)	200	-	-	ns	
tEWLW	Enable pulse width (/WR)	160	-	-	ns	

Serial interface
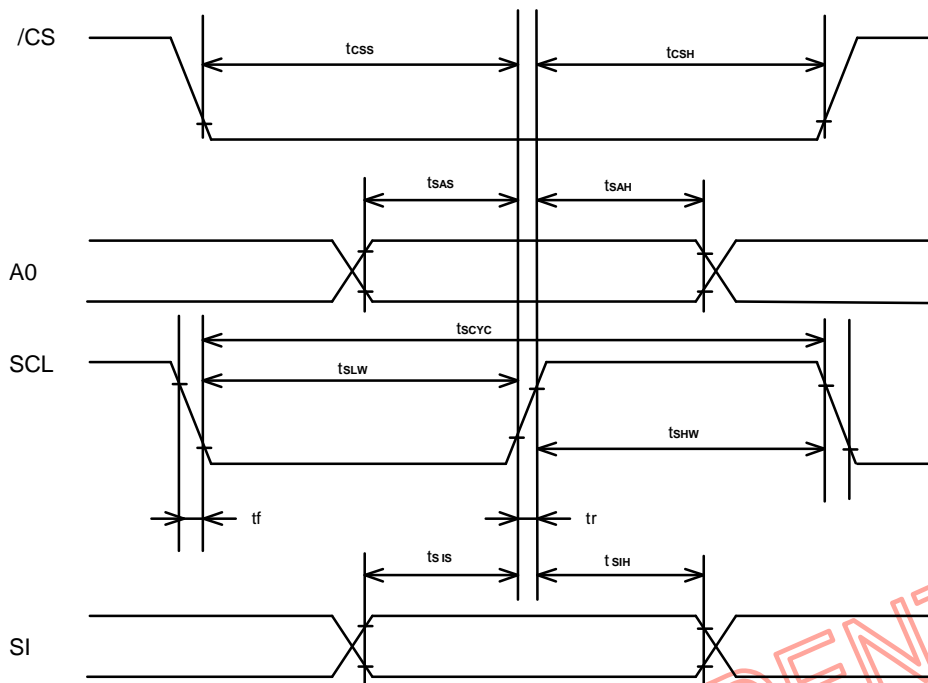
(VDD1 = 2.0V, VDD2 = 2.4 ~ 3.5V, T$_A$ = -30 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tCYC	SCL clock cycle time	150			ns	
tSWH	SCL pulse width high	60			ns	
tSWL	SCL pulse width low	60			ns	
tR	SCL pulse rise time			20	ns	Cload = 10pF
tCSS	/CS setup time	60			ns	
tCSH	/CS hold time	60			ns	
tSIS	SI setup time	60			ns	
tSIH	SI hold time	60			ns	

*1. Rise/fall time of the input signal is 15ns or less.
*2. Timing is specified at 20% of 80% or the signal waveform.

I²C-bus Interface timing
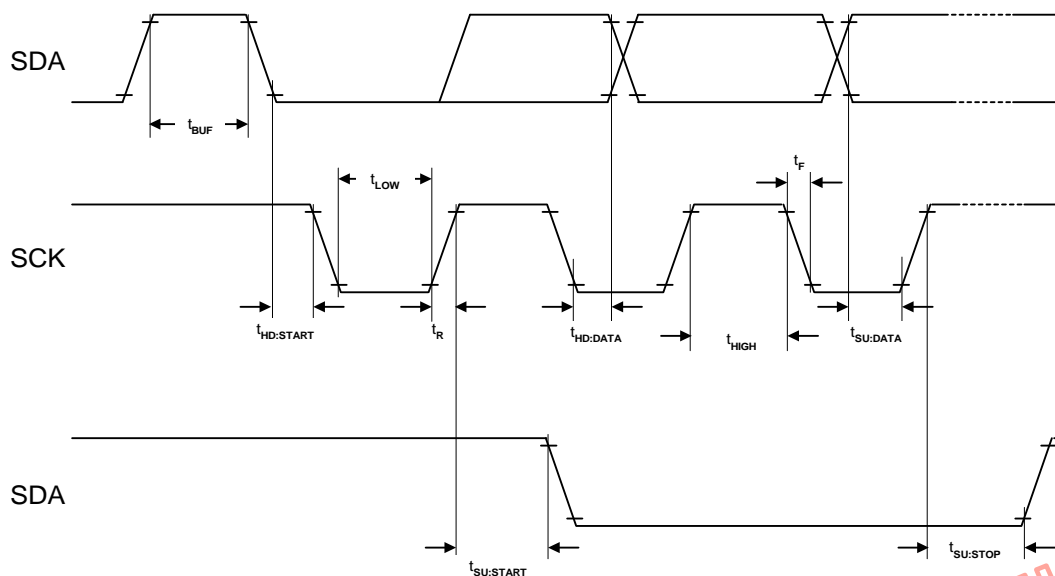
I²C-bus timing diagram

(VDD1 = 2.0 ~ 3.5V, VDD2=2.4 ~ 3.5V, TA = -30 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f$_{SCL}$	SCK clock frequency	DC	-	400	KHz	
t$_{LOW}$	SCK clock Low pulse width	1.3	-	-	µs	
t$_{HIGH}$	SCK clock High pulse width	0.6	-	-	µs	
t$_{SU:DATA}$	data setup time	100	-	-	µs	
t$_{HD:DATA}$	data hold time	0	-	0.9	µs	
t$_R$	SCK，SDA rise time	20+0.1C$_b$	-	300	ns	
t$_F$	SCK，SDA fall time	20+0.1C$_b$	-	300	ns	
C$_b$	Capacity load on each bus line	-	-	400	pF	
t$_{SU:START}$	Setup time for re-START	0.6	-	-	µs	
t$_{HD:START}$	START Hold time	0.6	-	-	µs	
t$_{SU:STOP}$	Setup time for STOP	0.6	-	-	µs	
t$_{BUF}$	Bus free times between STOP and START condition	1.3	-	-	µs	

Connections Between NT7533 and LCD Panel (Single Chip, 1/65Duty Configurations)

1. Type I (CMO=0; MX=1; MY=1)
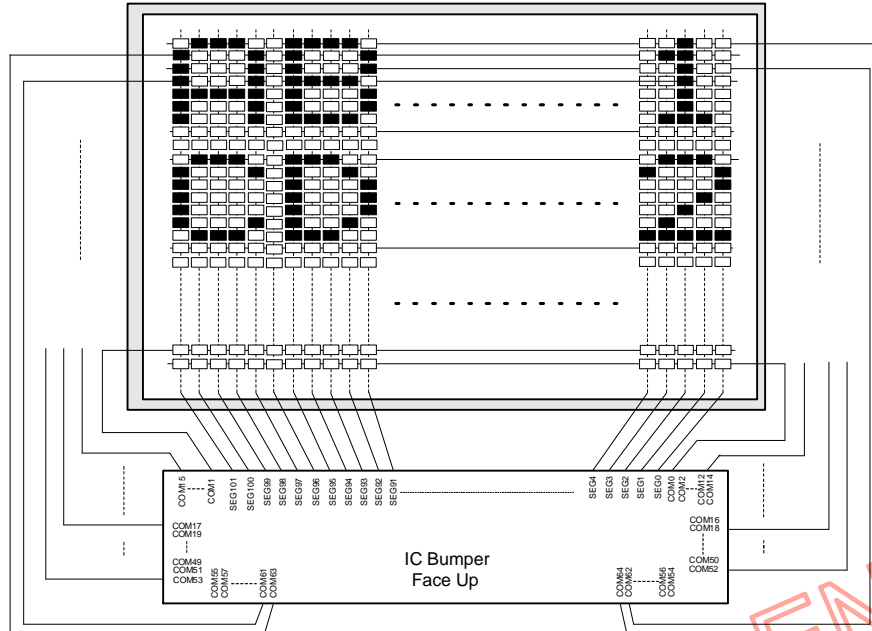
2. Type II (CMO=0; MX=0; MY=1)
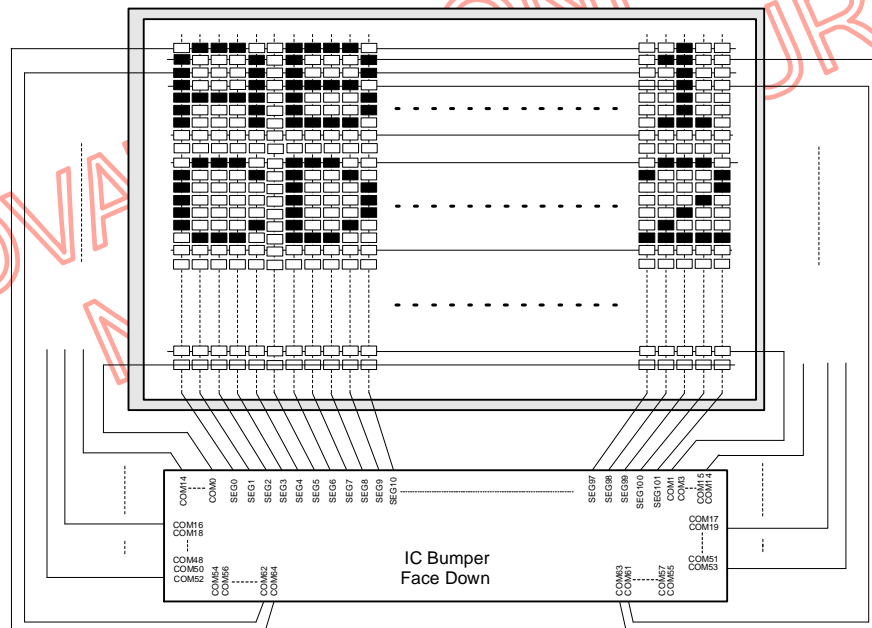
3. Type III (CMO=0; MX=0; MY=0)
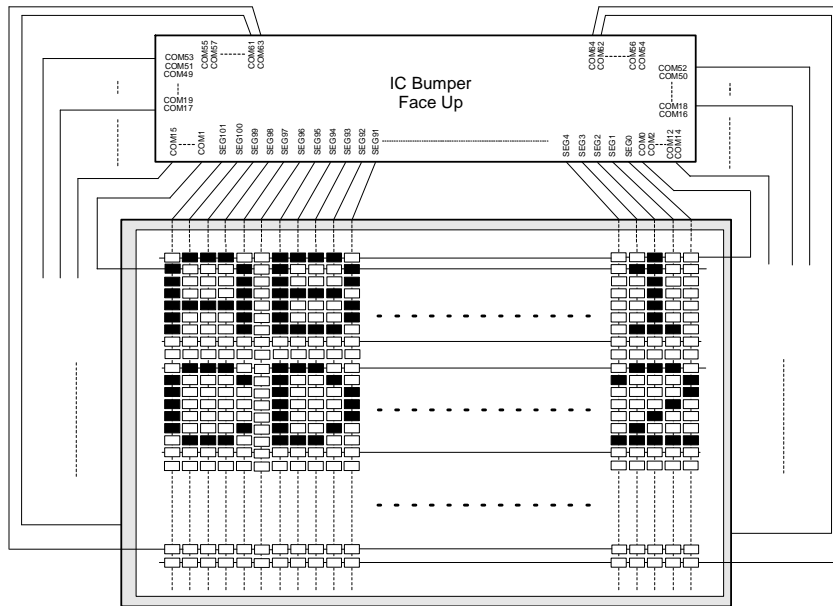
4. Type IV (CMO=0; MX=1; MY=0)
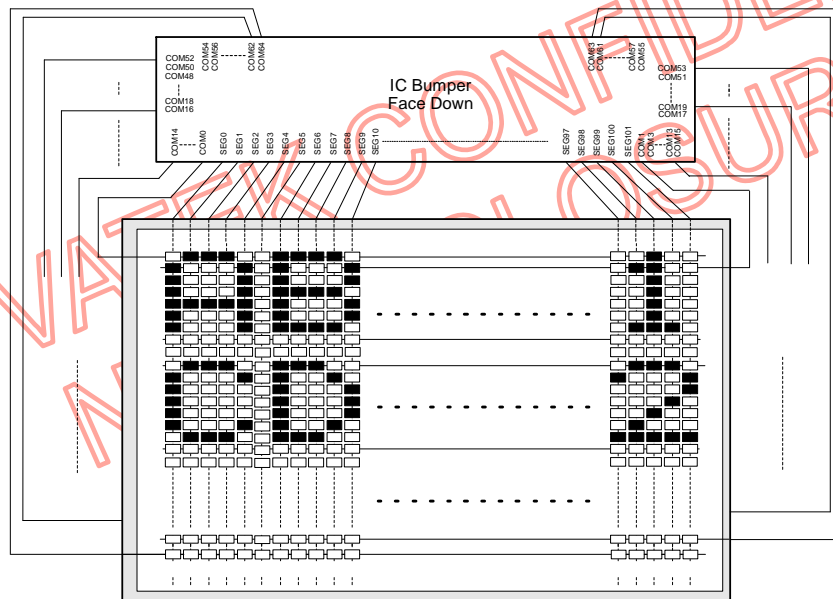
Pin connection to MPU
Parallel mode (6800 series MPU)
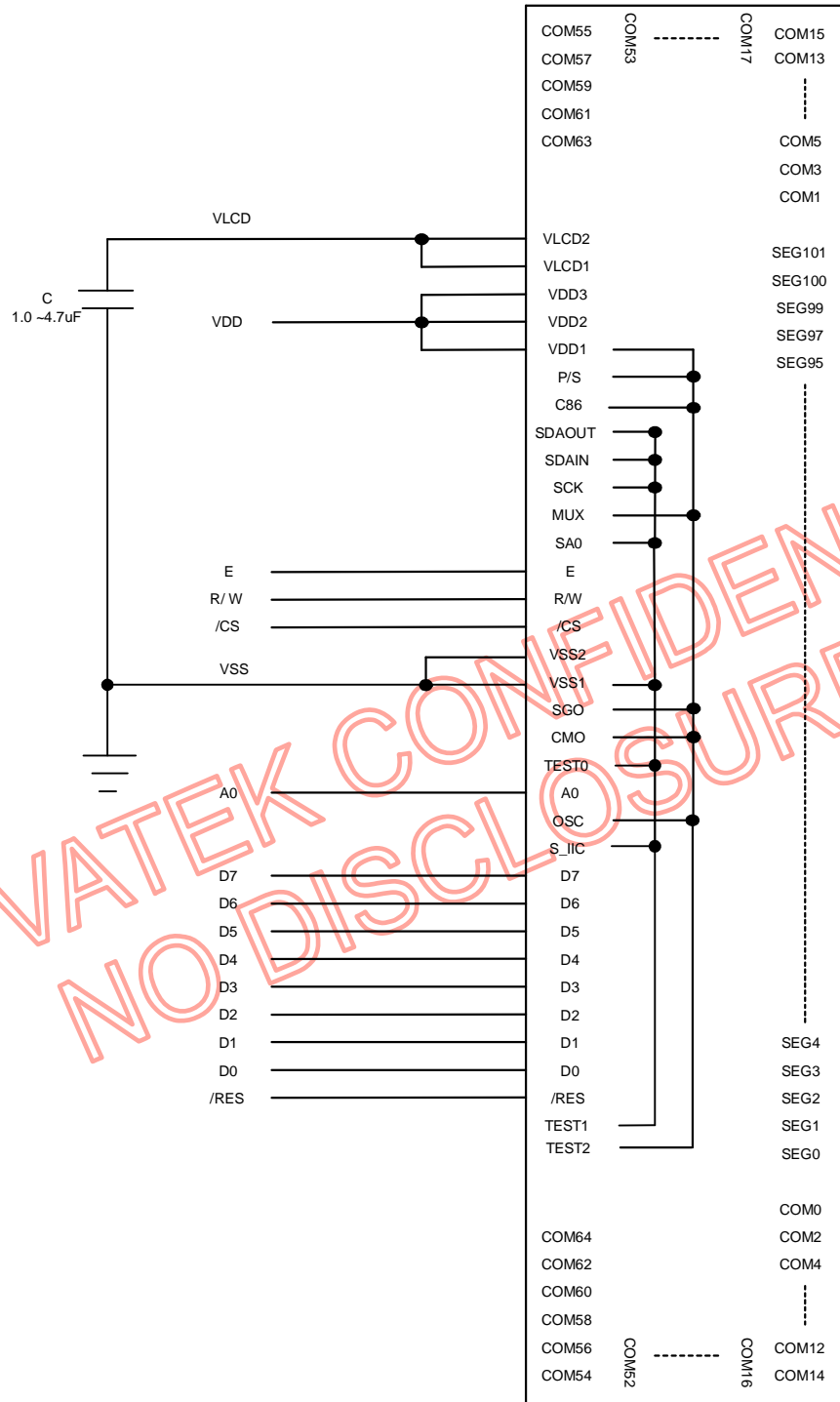
Parallel mode (8080 series MPU)

Serial mode
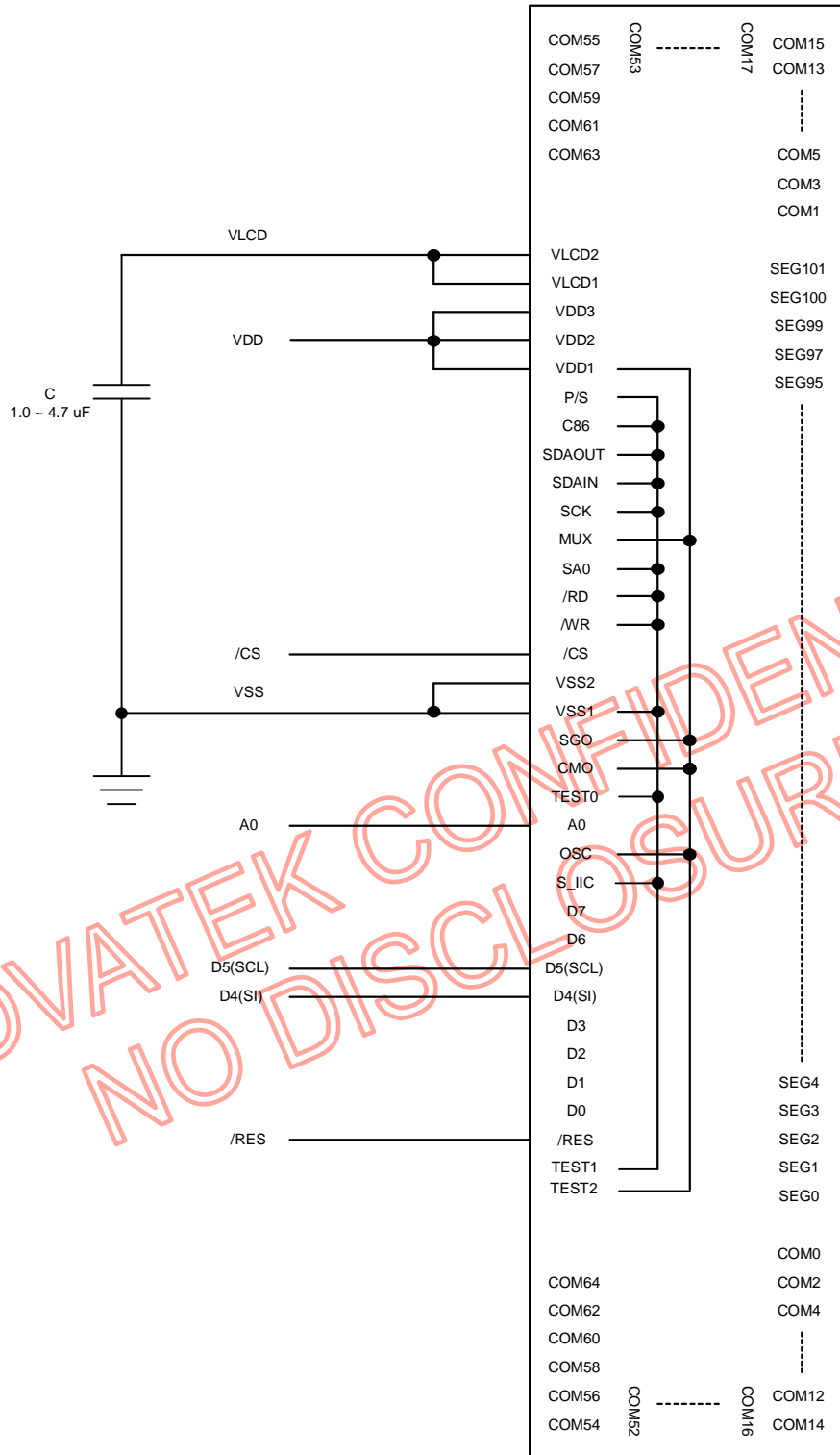
I²C Interface
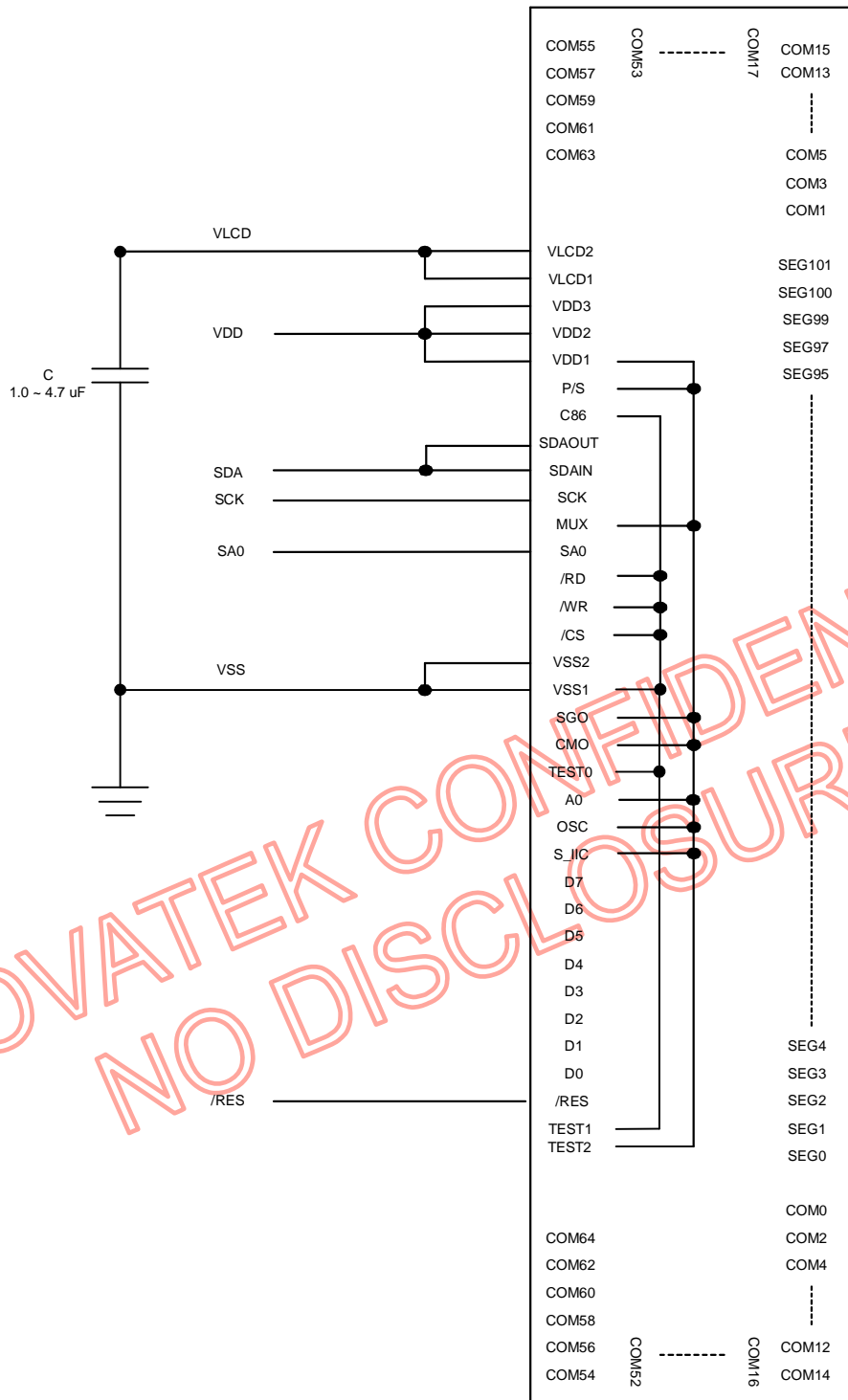
Pad Configuration
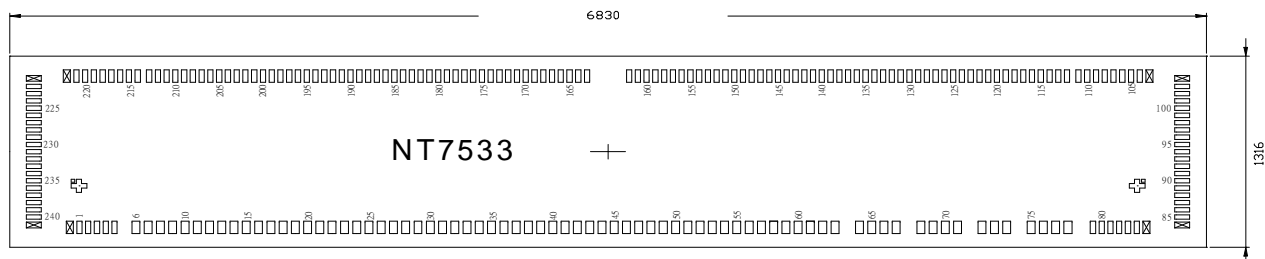
Bonding Diagram

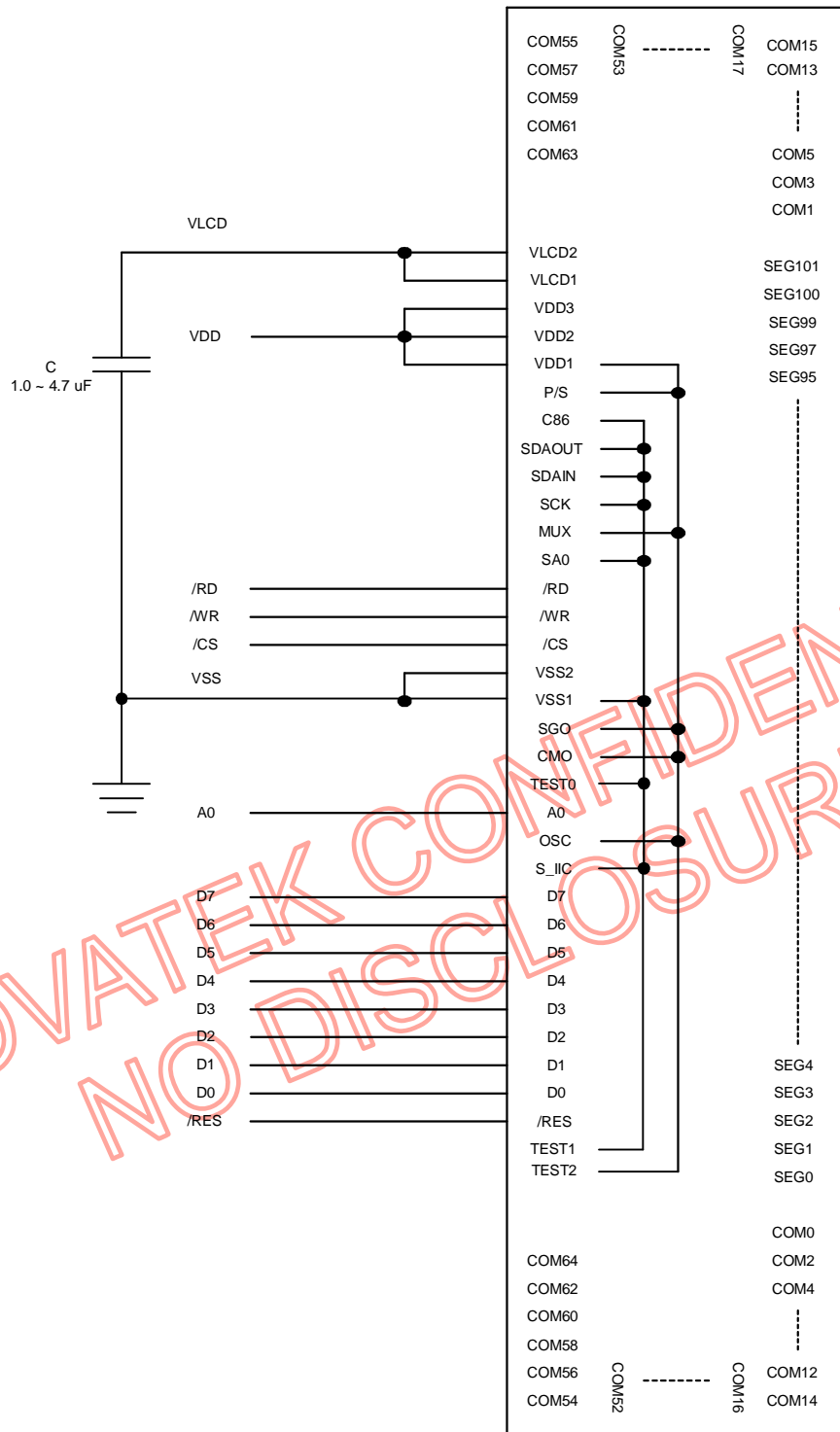| Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	COM55	-3017.5	-520.5	24	VDD2	-1435.0	-520.5
2	COM57	-2967.5	-520.5	25	VDD2	-1365.0	-520.5
3	COM59	-2917.5	-520.5	26	VDD1	-1295.0	-520.5
4	COM61	-2867.5	-520.5	27	VDD1	-1225.0	-520.5
5	COM63	-2817.5	-520.5	28	VDD1	-1155.0	-520.5
6	VLCD2	-2695.0	-520.5	29	P/S	-1085.0	-520.5
7	VLCD2	-2625.0	-520.5	30	C86	-1015.0	-520.5
8	VLCD2	-2555.0	-520.5	31	SDAOUT	-945.0	-520.5
9	VLCD2	-2485.0	-520.5	32	SDAIN	-875.0	-520.5
10	VLCD2	-2415.0	-520.5	33	SCK	-805.0	-520.5
11	VLCD1	-2345.0	-520.5	34	MUX	-735.0	-520.5
12	VLCD1	-2275.0	-520.5	35	VDD1	-665.0	-520.5
13	VLCD1	-2205.0	-520.5	36	SA0	-595.0	-520.5
14	VLCD1	-2135.0	-520.5	37	D5(SCL)	-525.0	-520.5
15	VLCD1	-2065.0	-520.5	38	E(/RD)	-455.0	-520.5
16	VDD3	-1995.0	-520.5	39	R/W(/WR)	-385.0	-520.5
17	VDD3	-1925.0	-520.5	40	/CS	-315.0	-520.5
18	VDD3	-1855.0	-520.5	41	VSS2	-245.0	-520.5
19	VDD3	-1785.0	-520.5	42	VSS2	-175.0	-520.5
20	VDD3	-1715.0	-520.5	43	VSS2	-105.0	-520.5
21	VDD2	-1645.0	-520.5	44	VSS2	-35.0	-520.5
22	VDD2	-1575.0	-520.5	45	VSS2	35.0	-520.5
23	VDD2	-1505.0	-520.5	46	VSS1	105.0	-520.5

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
47	VSS1	175.0	-520.5	77	VDD1	2555.0	-520.5
48	VSS1	245.0	-520.5	78	TEST2	2625.0	-520.5
49	VSS1	315.0	-520.5	79	COM64	2767.5	-520.5
50	VSS1	385.0	-520.5	80	COM62	2817.0	-520.5
51	SGO	455.0	-520.5	81	COM60	2867.5	-520.5
52	VDD1	525.0	-520.5	82	COM58	2917.0	-520.5
53	CMO	595.0	-520.5	83	COM56	2967.5	-520.5
54	NC	665.0	-520.5	84	COM54	3017.5	-520.5
55	TEST0	735.0	-520.5	85	COM52	3277.5	-450.0
56	A0	805.0	-520.5	86	COM50	3277.5	-400.0
57	OSC	875.0	-520.5	87	COM48	3277.5	-350.0
58	VDD1	945.0	-520.5	88	COM46	3277.5	-300.0
59	S_IIC	1015.0	-520.5	89	COM44	3277.5	-250.0
60	NC	1085.0	-520.5	90	COM42	3277.5	-200.0
61	D7	1155.0	-520.5	91	COM40	3277.5	-150.0
62	D6	1225.0	-520.5	92	COM38	3277.5	-100.0
63	T1	1295.0	-520.5	93	COM36	3277.5	-50.0
64	NC	1435.0	-520.5	94	COM34	3277.5	0.0
65	D5(SCL)	1505.0	-520.5	95	COM32	3277.5	50.0
66	D4(SI)	1575.0	-520.5	96	COM30	3277.5	100.0
67	TEST1	1645.0	-520.5	97	COM28	3277.5	150.0
68	NC	1785.0	-520.5	98	COM26	3277.5	200.0
69	D3	1855.0	-520.5	99	COM24	3277.5	250.0
70	D2	1925.0	-520.5	100	COM22	3277.5	300.0
71	T2	1995.0	-520.5	101	COM20	3277.5	350.0
72	NC	2135.0	-520.5	102	COM18	3277.5	400.0
73	D1	2205.0	-520.5	103	COM16	3277.5	450.0
74	D0	2275.0	-520.5	104	COM14	3035.0	520.5
75	NC	2415.0	-520.5	105	COM12	2985.0	520.5
76	/RES	2485.0	-520.5	106	COM10	2935.0	520.5

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
107	COM8	2885.0	520.5	137	SEG25	1370.0	520.5
108	COM6	2835.0	520.5	138	SEG26	1320.0	520.5
109	COM4	2785.0	520.5	139	SEG27	1270.0	520.5
110	COM2	2735.0	520.5	140	SEG28	1220.0	520.5
111	COM0	2685.0	520.5	141	SEG29	1170.0	520.5
112	SEG0	2620.0	520.5	142	SEG30	1120.0	520.5
113	SEG1	2570.0	520.5	143	SEG31	1070.0	520.5
114	SEG2	2520.0	520.5	144	SEG32	1020.0	520.5
115	SEG3	2470.0	520.5	145	SEG33	970.0	520.5
116	SEG4	2420.0	520.5	146	SEG34	920.0	520.5
117	SEG5	2370.0	520.5	147	SEG35	870.0	520.5
118	SEG6	2320.0	520.5	148	SEG36	820.0	520.5
119	SEG7	2270.0	520.5	149	SEG37	770.0	520.5
120	SEG8	2220.0	520.5	150	SEG38	720.0	520.5
121	SEG9	2170.0	520.5	151	SEG39	670.0	520.5
122	SEG10	2120.0	520.5	152	SEG40	620.0	520.5
123	SEG11	2070.0	520.5	153	SEG41	570.0	520.5
124	SEG12	2020.0	520.5	154	SEG42	520.0	520.5
125	SEG13	1970.0	520.5	155	SEG43	470.0	520.5
126	SEG14	1920.0	520.5	156	SEG44	420.0	520.5
127	SEG15	1870.0	520.5	157	SEG45	370.0	520.5
128	SEG16	1820.0	520.5	158	SEG46	320.0	520.5
129	SEG17	1770.0	520.5	159	SEG47	270.0	520.5
130	SEG18	1720.0	520.5	160	SEG48	220.0	520.5
131	SEG19	1670.0	520.5	161	SEG49	170.0	520.5
132	SEG20	1620.0	520.5	162	SEG50	120.0	520.5
133	SEG21	1570.0	520.5	163	SEG51	-120.0	520.5
134	SEG22	1520.0	520.5	164	SEG52	-170.0	520.5
135	SEG23	1470.0	520.5	165	SEG53	-220.0	520.5
136	SEG24	1420.0	520.5	166	SEG54	-270.0	520.5

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
167	SEG55	-320.0	520.5	197	SEG85	-1820.0	520.5
168	SEG56	-370.0	520.5	198	SEG86	-1870.0	520.5
169	SEG57	-420.0	520.5	199	SEG87	-1920.0	520.5
170	SEG58	-470.0	520.5	200	SEG88	-1970.0	520.5
171	SEG59	-520.0	520.5	201	SEG89	-2020.0	520.5
172	SEG60	-570.0	520.5	202	SEG90	-2070.0	520.5
173	SEG61	-620.0	520.5	203	SEG91	-2120.0	520.5
174	SEG62	-670.0	520.5	204	SEG92	-2170.0	520.5
175	SEG63	-720.0	520.5	205	SEG93	-2220.0	520.5
176	SEG64	-770.0	520.5	206	SEG94	-2270.0	520.5
177	SEG65	-820.0	520.5	207	SEG95	-2320.0	520.5
178	SEG66	-870.0	520.5	208	SEG96	-2370.0	520.5
179	SEG67	-920.0	520.5	209	SEG97	-2420.0	520.5
180	SEG68	-970.0	520.5	210	SEG98	-2470.0	520.5
181	SEG69	-1020.0	520.5	211	SEG99	-2520.0	520.5
182	SEG70	-1070.0	520.5	212	SEG100	-2570.0	520.5
183	SEG71	-1120.0	520.5	213	SEG101	-2620.0	520.5
184	SEG72	-1170.0	520.5	214	COM1	-2685.0	520.5
185	SEG73	-1220.0	520.5	215	COM3	-2735.0	520.5
186	SEG74	-1270.0	520.5	216	COM5	-2785.0	520.5
187	SEG75	-1320.0	520.5	217	COM7	-2835.0	520.5
188	SEG76	-1370.0	520.5	218	COM9	-2885.0	520.5
189	SEG77	-1420.0	520.5	219	COM11	-2935.0	520.5
190	SEG78	-1470.0	520.5	220	COM13	-2985.0	520.5
191	SEG79	-1520.0	520.5	221	COM15	-3035.0	520.5
192	SEG80	-1570.0	520.5	222	COM17	-3277.5	450.0
193	SEG81	-1620.0	520.5	223	COM19	-3277.5	400.0
194	SEG82	-1670.0	520.5	224	COM21	-3277.5	350.0
195	SEG83	-1720.0	520.5	225	COM23	-3277.5	300.0
196	SEG84	-1770.0	520.5	226	COM25	-3277.5	250.0

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
227	COM27	-3277.5	200.0	234	COM41	-3277.5	-150.0
228	COM29	-3277.5	150.0	235	COM43	-3277.5	-200.0
229	COM31	-3277.5	100.0	236	COM45	-3277.5	-250.0
230	COM33	-3277.5	50.0	237	COM47	-3277.5	-300.0
231	COM35	-3277.5	0.0	238	COM49	-3277.5	-350.0
232	COM37	-3277.5	-50.0	239	COM51	-3277.5	-400.0
233	COM39	-3277.5	-100.0	240	COM53	-3277.5	-450.0

DUMMY PAD

Designation	X	Y	Designation	X	Y
DUMMY0	-3072.5	-520.5	DUMMY4	3090.0	520.5
DUMMY1	3072.5	-520.5	DUMMY5	-3090.0	520.5
DUMMY2	3277.5	-505.0	DUMMY6	-3277.5	505.0
DUMMY3	3277.5	505.0	DUMMY7	-3277.5	-505.0

ALIGNMENT MARK

Designation	X	Y	Designation	X	Y
L-ALIGN	-3020.0	-235.0	R-ALIGN	3020.0	-235.0

Packaging Information
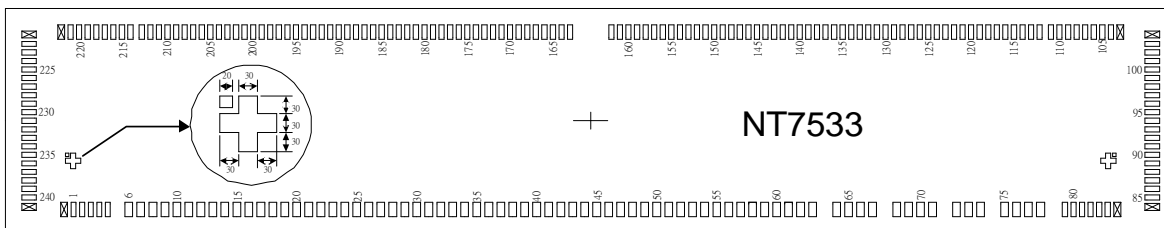
Item	Pad No.	Size	Unit
Chip size	-	6830 * 1316	μm * μm
Thickness	-	525	μm
Pad pitch	6 ~ 63 64 ~ 67 68 ~ 71 72 ~ 74 75 ~ 78	70	μm
	1 ~ 5 79 ~ 84 85 ~ 103 104 ~ 111 112 ~ 162 163 ~ 213 214 ~ 221 222 ~ 240	50	μm
	111 ~112 213 ~ 214	65	μm
	5 ~ 6	122.5	μm
	78 ~ 79	142.5	μm
	63 ~ 64 67 ~ 68 71 ~ 72 74 ~ 75	140	μm
	162 ~ 163	240	μm
	dummy 0 ~ pad 1 pad 84 ~ dummy 1 dummy2 ~ pad 85 pad 103 ~ dummy 3 dummy 4 ~ pad 104 pad 221 ~ dummy 5 dummy 6 ~ pad 222 pad 240 ~ dummy 7	55	μm
Bump size	6 ~ 78	45 * 85	μm * μm
	1 ~ 5 79 ~ 240	30 * 85	μm * μm
	dummy 0 ~ dummy 7	40 * 85	μm * μm
Bump height	all pads	15 ± 3	μm

Ordering Information

Part No.	Packages
NT7533H-BDT	Gold Bump on Chip Tray

Cautions

1. The contents of this document will be subjected to change without notice.
2. Precautions against light projection:

   Light has the effect of causing the electrons of semiconductor to move; so light projection may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB, COG, TCP and COF, etc.) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip.

   Observe the following instructions in using this product:

   a. During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.

   b. Test and inspect the product under an environment free of light source penetration.

   c. Confirm that all surfaces around the IC will not be exposed to a light source.