Preliminary

Ver 0.30

TFT LCD Specification

Model NO.: TD028STEB1

Customer Signature
Date

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Record of Reversion

Rev	Issued Date	Description
0.00	Sep, 1, 2004	New
0.10	Nov, 10, 2004	1.Modify 2.Weight: from TBD to 35(Max). 2.Modify 3-1.Gate Off Voltage from -5.2V ~ -5.8V to -5.5~-4.5V, Typ. from -5.5 to -5V 3.Modify 3-1 Digital Supply Power from2.7V ~ 3.0V to 2.5~3.0V, Typ. from 2.85V to 2.8V 4.Modify 5-1 Logic Supply Voltage: VDD1 & VDD2 MAX from 3.5V to 3V. 5.Modify 5-4 Driving touch panel: Resistor between terminals (XR-XL): MIN from 300Ω to 250Ω, MAX from 1000Ω to 950Ω 6. Add IC using statement in Page12: (1) If choice DC-DC disable --> need to add a schottky diode between VDD2 (Analog power supply) & VGH in customer's system-board. (2) If choice DC-DC enable --> don't need to add component in customer's system-board. 7.In Mechanical Drawing: Define Module label & Backlight label position & dimension
0.20	Dec, 13, 2004	1. 5.1 Driving TFT LCD Panel: Define VDD1, VDD2 & AVDD & VGH & VVEE Supply Current 2. 5.2 DC/DC Spec: Define VDD2 & AVDD & VGH & VVEE Input Current &Input ripple (Max) 3. Add Surface hardness value: MIN 3H in 5.4 Driving touch panel 4. Add application circuit diagram & Delete IC using statement in Page 12 5. Modify 8 Power ON/OFF sequence 6. Delete 9.1(1): NTSC 7. Modify 9.1(2): Chromaticity (TYP) & Remark of Chromaticity from Note 9-3 to 9-9 & Add Note 9-9 White chromaticity as back light on (Measure System B) 8. Modify 9.2(4): Testing Facility: Environmental illumination from =10Lux to = 1Lux
0.30	Feb, 15, 2005	1. Modify 5-1 Logic Supply Voltage: VDD1 & VDD2 MAX from 3V to 3.3V 2. Update 7.1 Display timing & 7.3 Setup / Hold timing 3. Add Note2: Maximum rising time of VDD1/VDD2 is 2ms in power on sequence of page18. 4. Update 9 Optical Characteristics 5. Update Mechanical Drawing: Update position of Module & Backlight label

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1. FEATURES

The 2.8 inch (real 2.83 inch) LCD module is the Transflective active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used and COG design are built on the panel. Highly integrated LCD module includes touch panel, backlight and TFT LCD panel with minimal external circuits and components required.

2. GENERAL SPECIFICATION

Item		Description	Unit
Display Size (Diagonal)		2.8 inch (real 2.83 inch)	-
Display Type		Transflective	-
Active Area (HxV)		43.2 X 57.6	mm
Number of Dots (HxV)		240 x RGB x 320	dot
Dot Pitch (HxV)		0.06 X 0.180	mm
Color Arrangement		RGB Stripe	-
Color Numbers		262,144 (18 bits)	-
Outline Dimension (HxVxT)		52.9X 71.7 X 4.2 (FPC excluded)	mm
Weight		35 (Max)	g
Power consumption	LCD Panel + System	23 (Typ)	mW
	Backlight	288 (Typ, I_F= 20mA)	

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3. INPUT/OUTPUT TERMINALS

3.1 TFT LCD module

Recommend connector: FH23-61S-0.3SHW, HIROSE

Pin	Symbol	I/O	Description	Remark
1	DE	IN	Data Enable Signal	
2	MCLK	IN	LCM Pixel Clock	
3	ENABLE	IN	IC Reset Signal	
4	TSP1	OUT	TSP Interface Signal Y2	
5	DVSS	IN	Digital Ground	
6	VCOM_I	IN	VCOM Input	
7	VCOM_I			
8	AVSS	IN	Analog Ground	
9	VVEE	IN	Gate Off Voltage, -5.5~-4.5V, Typ. -5V	
10	VVEE			
11	VGH	IN	Gate On Voltage, 9.5V ~ 10.5V, Typ. 10V	
12	VGH			
13	DVSS	IN	Digital Ground	
14	TSP2	OUT	TSP Interface Signal X2	
15	VCOM_H	OUT	Positive Power Output for VCOM	
16	VCOM_O	OUT	VCOM Output	
17	VCOM_O			
18	VCOM_L	OUT	Negative Power Output for VCOM	
19	AVSS	IN	Analog Ground	
20	DVDD	IN	Digital Supply Power, 2.5V~3.0V, Typ. 2.8V	
21	DVDD			
22	AVDD	IN	Analog Supply Power, 4.8V ~ 5.6V, Typ. 5.0V	
23	AVDD			
24	TSP3	OUT	TSP Interface Signal Y1	
25	DVSS	IN	Digital Ground	
26	IV6P	OUT	Negative Voltage Output Pad	
27	TSP4	OUT	TSP Interface Signal X1	
28	DVDD	IN	Digital Supply Power, 2.5~3.0V, Typ. 2.8V	
29	PD17	IN	R5 (Red MSB)	
30	PD16		R4	
31	PD15		R3	
32	PD14		R2	

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33	PD13		R1	
34	PD12	IN	R0 (Red LSB)	
35	PD11	IN	G5 (Green MSB)	
36	PD10		G4	
37	PD9		G3	
38	PD8		G2	
39	PD7		G1	
40	PD6		G0 (Green LSB)	
41	PD5	IN	B5 (Blue MSB)	
42	PD4		B4	
43	PD3		B3	
44	PD2		B2	
45	PD1		B1	
46	PD0	IN	B0 (Blue LSB)	
47	ISC	OUT	Capacitor Connection Pad	
48	DVSS(SCL)	IN	Digital Ground(Serial interface clock input)	
49	DVSS(SDA)	IN/OUT	Digital Ground(Serial interface data input/output)	
50	DVSS(CS)	IN	Digital Ground(Serial interface chip select input)	
51	DVSS	IN	Digital Ground	
52	HSYNC	IN	Horizontal SYNC Input	
53	DVSS	IN	Digital Ground(Display mode select)	
54	DVSS(CM)			
55	VS	OUT	Positive Power Output for Source Driver	
56	VSYNC	IN	Vertical SYNC Input	
57	MAIN_LED+	IN	LED Power (Anode)	
58	MAIN_LED+			
59	MAIN_LED-	OUT	LED Power (Cathode)	
60	MAIN_LED-			
61	DVSS	IN	Digital Ground	

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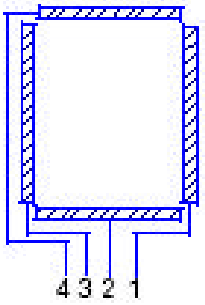
3.2 Touch panel Pin

Touch Panel Pin	Module Pin	Symbol	Description	Remark
1	27	X1	Touch Panel Right Side	
2	24	Y1	Touch Panel Lower Side	
3	14	X2	Touch Panel Left Side	
4	4	Y2	Touch Panel Upper Side	

Pin Assignment for Touch panel



Touch Panel Pin/Name		
Pin No	Assignment	Note
1	X1	Glass
2	Y1	Film
3	X2	Glass
4	Y2	Film

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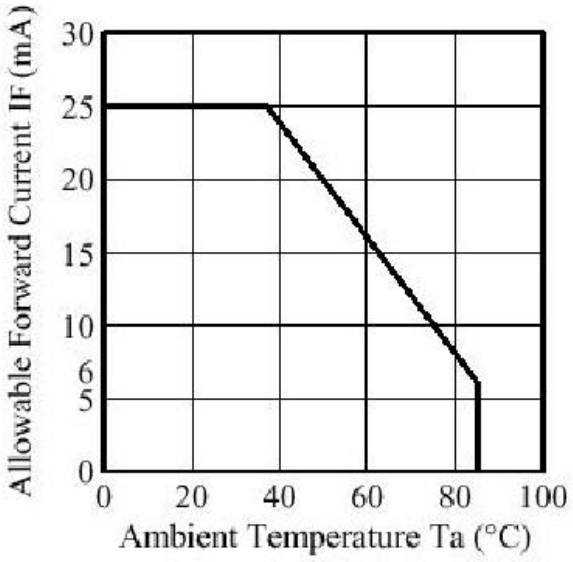
4.ABSOLUTE MAXIMUM RATINGS

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	VDD1, VDD2	-0.3	3.6	V	
	AVDD	-0.3	6.0	V	
Power Supply for H/V Driver	VGH	-0.3	19	V	
	VVEE	-0.3	19	V	
Touch Panel Operation Voltage	V_{Touch}	-	5	V	
Backlight LED forward Voltage	V_F	-	14.4	V	
Backlight LED reverse Voltage	V_R	-	20	V	
Backlight LED forward current (Ta=25℃)	I_F	-	25	mA	Note
Operating Temperature	Topr	-20	+60	℃	
Storage Temperature	Tstg	-30	+70	℃	

Note: Relation between maximum LED forward current and ambient temperature is showed as bellow.

■ Ambient Temperature vs.
Allowable Forward Current



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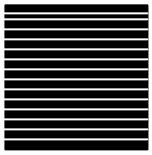
5.ELECTRICAL CHARACTERISTICS

5.1 Driving TFT LCD Panel

Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage		VDD1	1.6	2.8	3.3	V	
		VDD2	2.5	2.8	3.3	V	
		AVDD	4.8	5.0	5.6	V	
Power Supply for H/V Driver		VGH	9.5	10	10.5	V	
		VVEE	-5.5	-5.0	-4.5	V	
Data Input Voltage	High	VIH	0.8VDD1	-	VDD1	V	R[5:0], G[5:0], B[5:0], CLK DE
	Low	VIL	GND	-	0.2VDD1		
VDD1, VDD2 Supply Current		I_{VDD1}	--	0.7	1.7	mA	Note 1
AVDD Supply Current		I_{AVDD}	--	1.85	4.0	mA	Note 2
VGH Supply Current		I_{VDD}	--	0.07	0.3	mA	
VVEE Supply Current		I_{VEE}	--	0.05	0.5	mA	

Note 1: The typical supply current specification is measured at the line inversion test pattern (black and white interlacing horizontal lines as the diagram shown below)



Note 2: Gamma correction voltage is set to achieve the optimun at VCC5=5.0V. Use the voltage at level as close to 5.0V as possible.

5.2 DC/DC Spec

Ta=25℃

Item	Input voltage			Input Current	Input ripple (Max)	Remark
	MIN	TYP	MAX			
VDD2	2.5	2.8	3.0	0.05	--	
AVDD	4.8	5.0	5.6	1.85	50mV	Note 1
VGH	9.5	10.0	10.5	0.07	150mV	
VVEE	-5.5	-5.0	-4.5	0.05	--	

Note 1: VCC5 is analog voltage supply therefore use as less ripple as possible.

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5.3 Driving backlight Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	25	mA	LED/Part
LED Life Time	-	-	10000		Hr	I_F: 20mA
Forward Current Voltage	V_F	-	14.4	16	V	I_F: 20mA ,LED/Part

Note: Backtlight driving circuit is recommend as the fix current circuit.

5.4 Driving touch panel (Analog resistance type) Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Resistor between terminals (XR-XL)	Rx	250	650	950	Ω	
Resistor between terminals (YU-YL)	Ry	250	600	950	Ω	
Operation Voltage	V_{Touch}	-	5	-	V	DC
Line Linearity (X direction)	-	-	1.5	-	%	Note 1
Line Linearity (Y direction)	-	-	1.5	-	%	
Chattering	-	-	10	-	ms	
Surface Hardness	-	3	-	-	H	JIS K 5600
Minimum tension for detecting	-	-	-	80	g	
Insulation Resistance	Ri	20	-	-	MΩ	At DC 25V

Note 1. The minimum test force is 80 g.

6. BLOCK DIAGRAM

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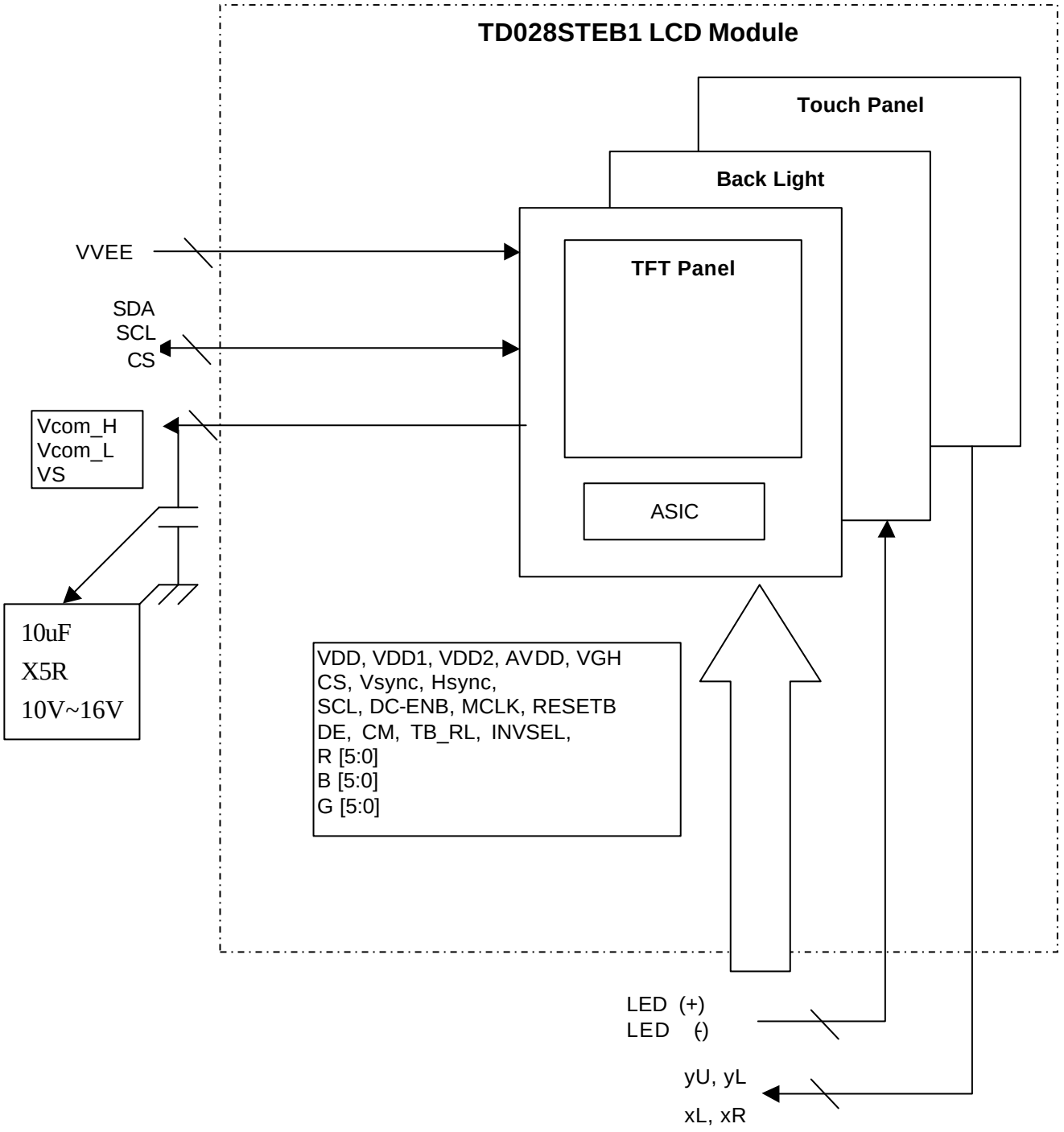

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Application Circuit Diagram

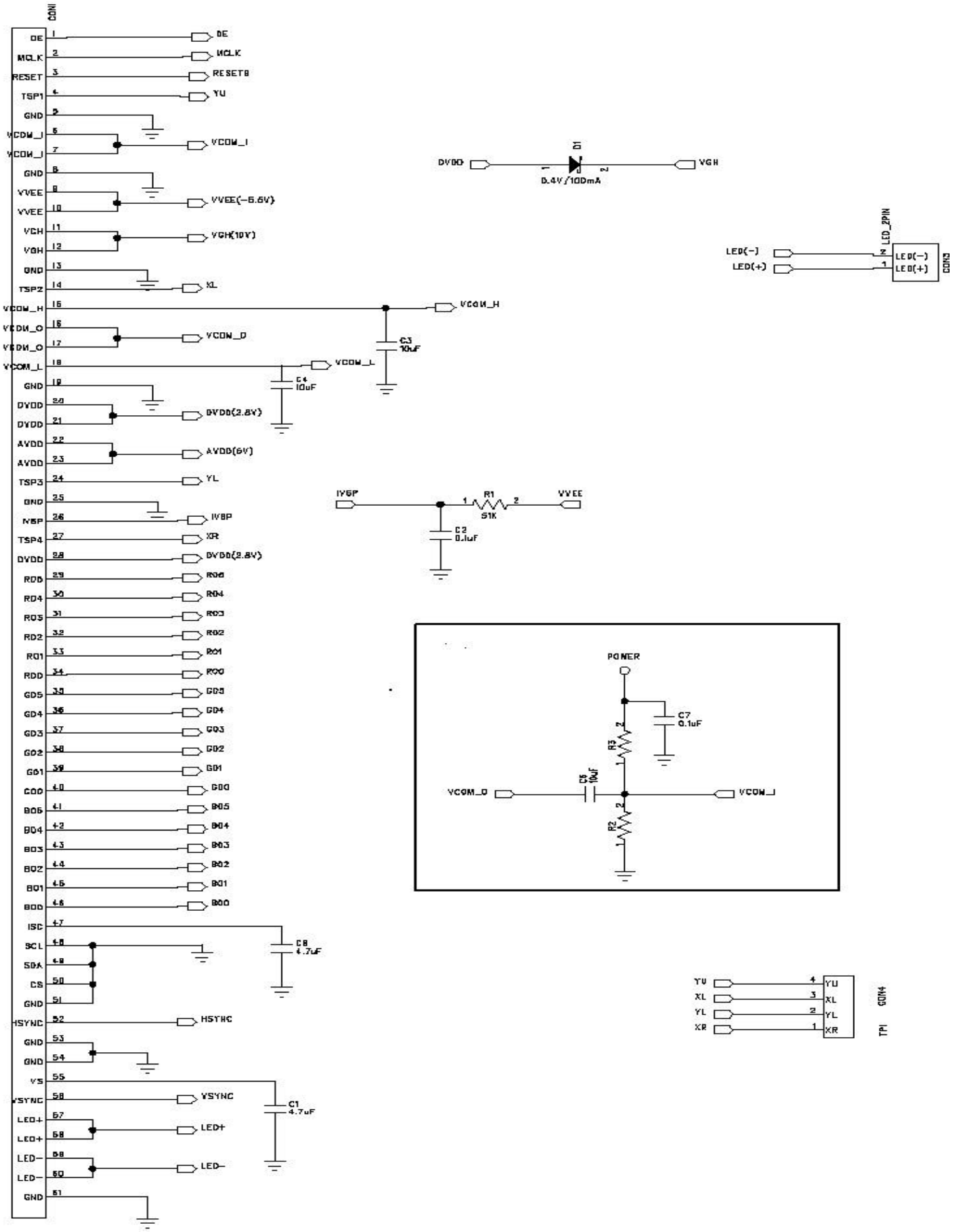

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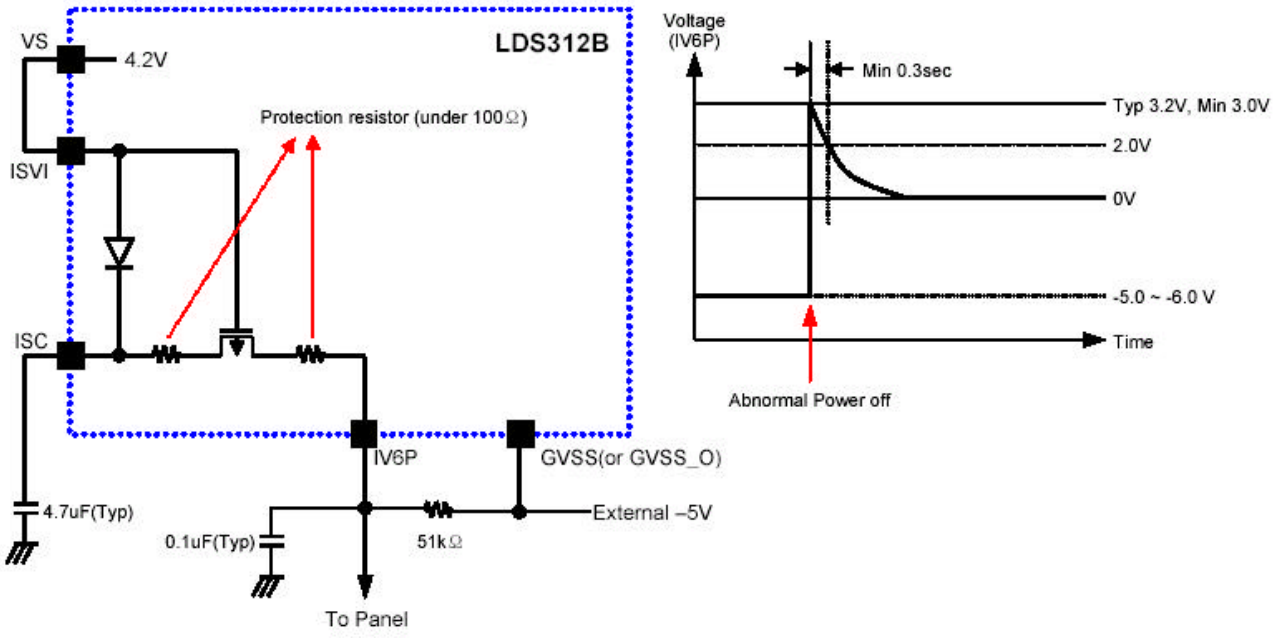
Image sticking circuit:

DC/DC disable model (DC_ENB=High)



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7. TIMING CHART

7.1 Display timing

Display Mode	Parameter	Symbol	Conditions	Ratings			Unit
				MIN	TYP	MAX	
Normal	Vertical cycle	VP	-	323	326	340	Line
	Vertical data start	VDS	VS+VBP	—	4	—	Line
	Vertical front porch	VFP	-	—	2	—	Line
	Vertical back portch	VBP		—	2	—	Line
	Vertical active area	VDISP	-	—	320	—	Line
	Horizontal cycle	HP	-	260	280	300	dot
	Horizontal front porch	HFP	-	—	10	—	dot
	Horizontal Sync Pulse width	HS	-	—	10	—	dot
	Horizontal Back porch	HBP		—	20	—	dot
	Horizontal Data start	HDS	HS+HBP	—	30	—	dot
	Horizontal active area	HDISP	-	—	240	—	dot
	Clock frequency	tclk	-	5.02	5.48	5.93	MHz
		fclk		199	183	169	nS

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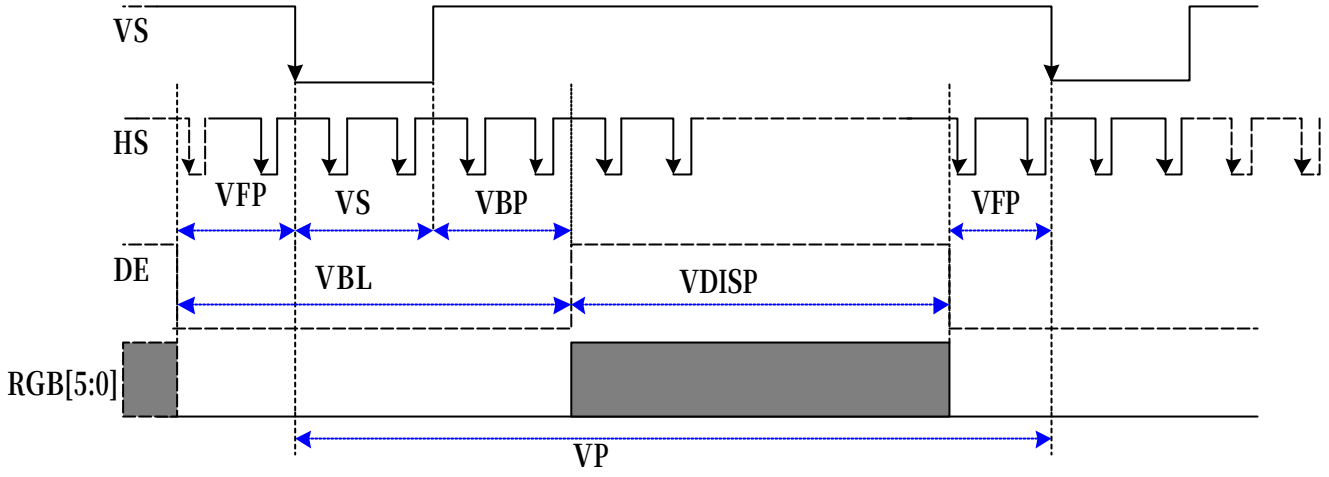
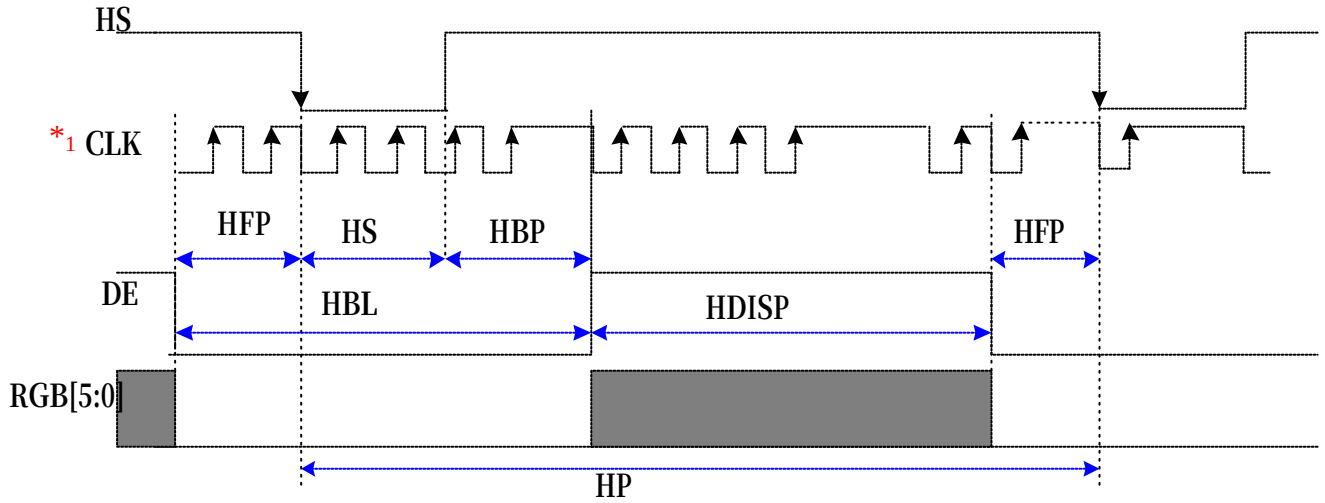
7.2 Input timing chart

＜Vertical Timing chart＞



＜Horizontal Timing chart＞



*1 The frequency of CLK should keep in the range as input timing chart determined whether in display or blanking region to ensure IC operating normally.

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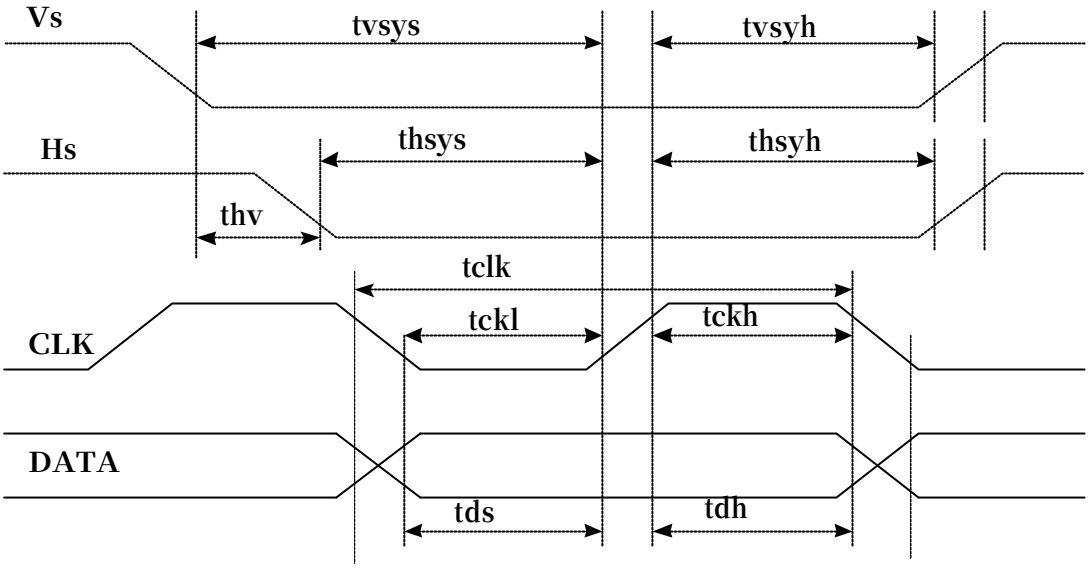
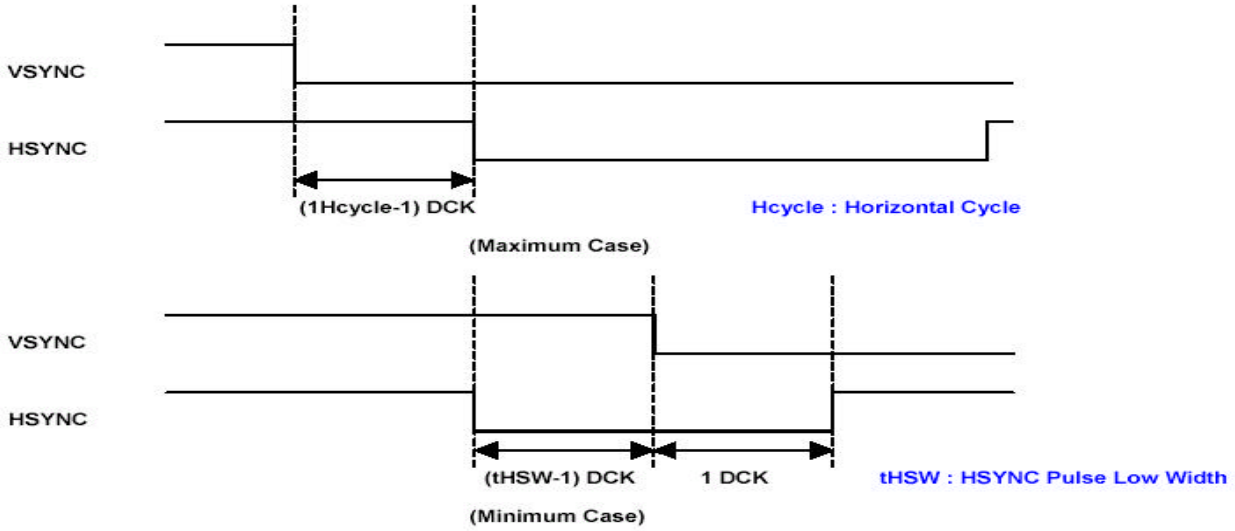
7.3 Setup / Hold Timing chart





Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Vertical Sync. Setup time	tvsys		20	-	-	ns
Vertical Sync. Hold time	tvsyh		20	-	-	ns
Horizontal Sync. Setup time	thsys		20	-	-	ns
Horizontal Sync. Hold time	thsyh		20	-	-	ns
Phase difference of Sync. Signal Falling edge(Note1)	thv	240x320	-(tVSW-1)	-	1Hcycle-1	clk
Clock “L” Period	tckl		75	-	-	%
Clock “H” Period	tckh		75	-	-	%
Data setup time	tds		20	-	--	ns
Data Hold time	tdh		20	-	-	ns

Note1: Thv range if it can't met our spec, just give up first Hsync. It can't impact any side effect.

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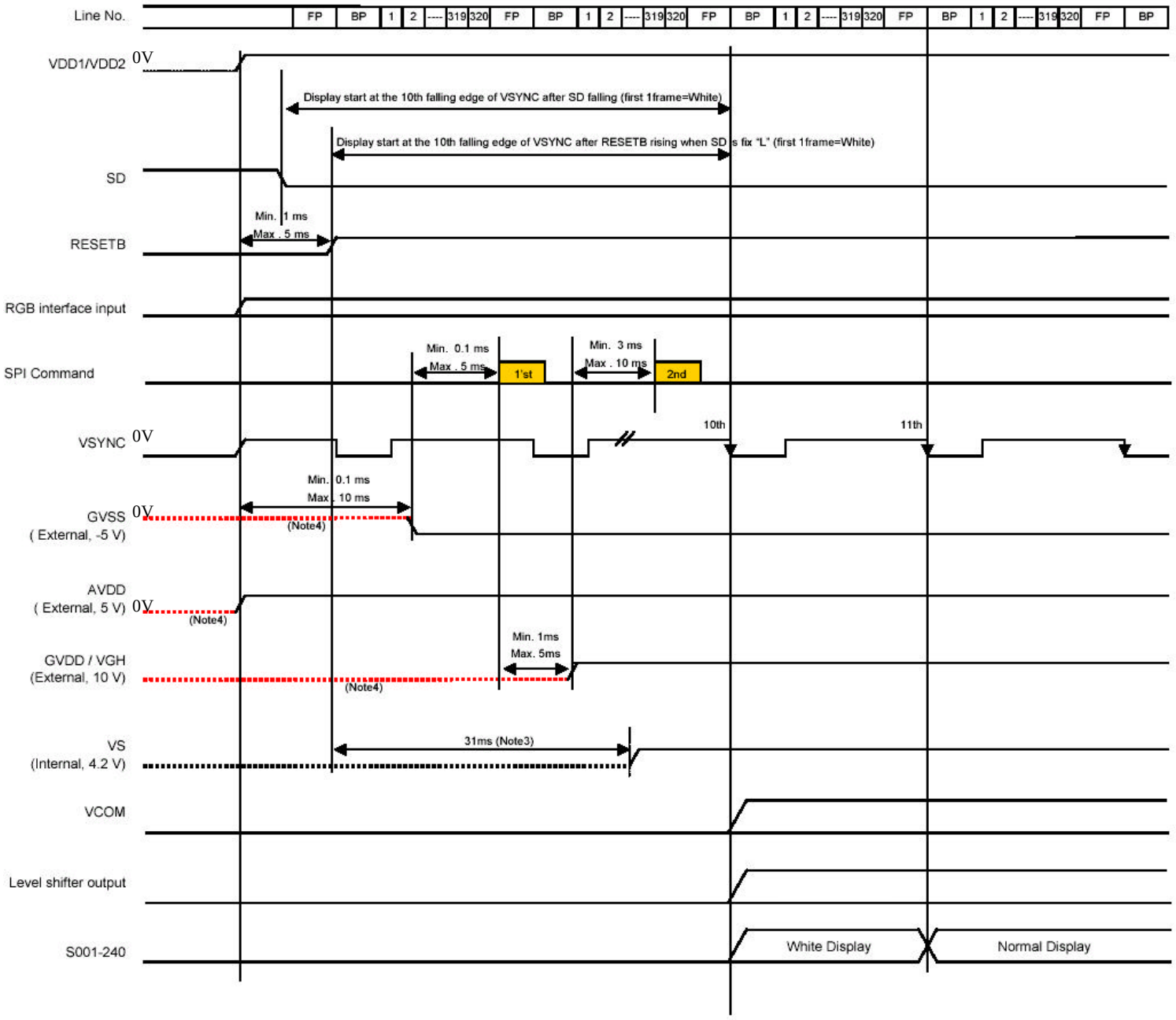
8. Power On/Off Sequence

1. Power On Sequence (with DC/DC supply outward & SD fixed at low)
   Power on sequence is controlled by SD or RESETB signal (fVSYNC=60Hz)



(Note1) RGB interface input – VSYNC/HSYNC/DCK/R5-0/G5-0/B5-0/DE/CM

(Note2) Level shifter output – CKH1/CKH2/CKH3/STV1/STV2/CKV1/CKV2/ENBV/CSV)

(Note3) Marked time is typical value (Typical values depend on the frequency of VSYNC)

(Note4) GVSS, AVDD and GVDD/VGH should be open before external power on

*(Note5) In order to prevent high current due to the latch-up in external power on sequence, shot-key diode should be connected between VGH and VDD2 as shown **External Component Application2** in page5. (Recommended spec of the shot-key diode: VF < 0.4V/100mA, VR > 15V)*

Note1: In some application, SD signal fixed at "low" level during power on. ASIC should produce white pattern when receiving10th S. And internal power regulator should function normally.

Note2: Maximum rising time of VDD1/VDD2 is 2ms.

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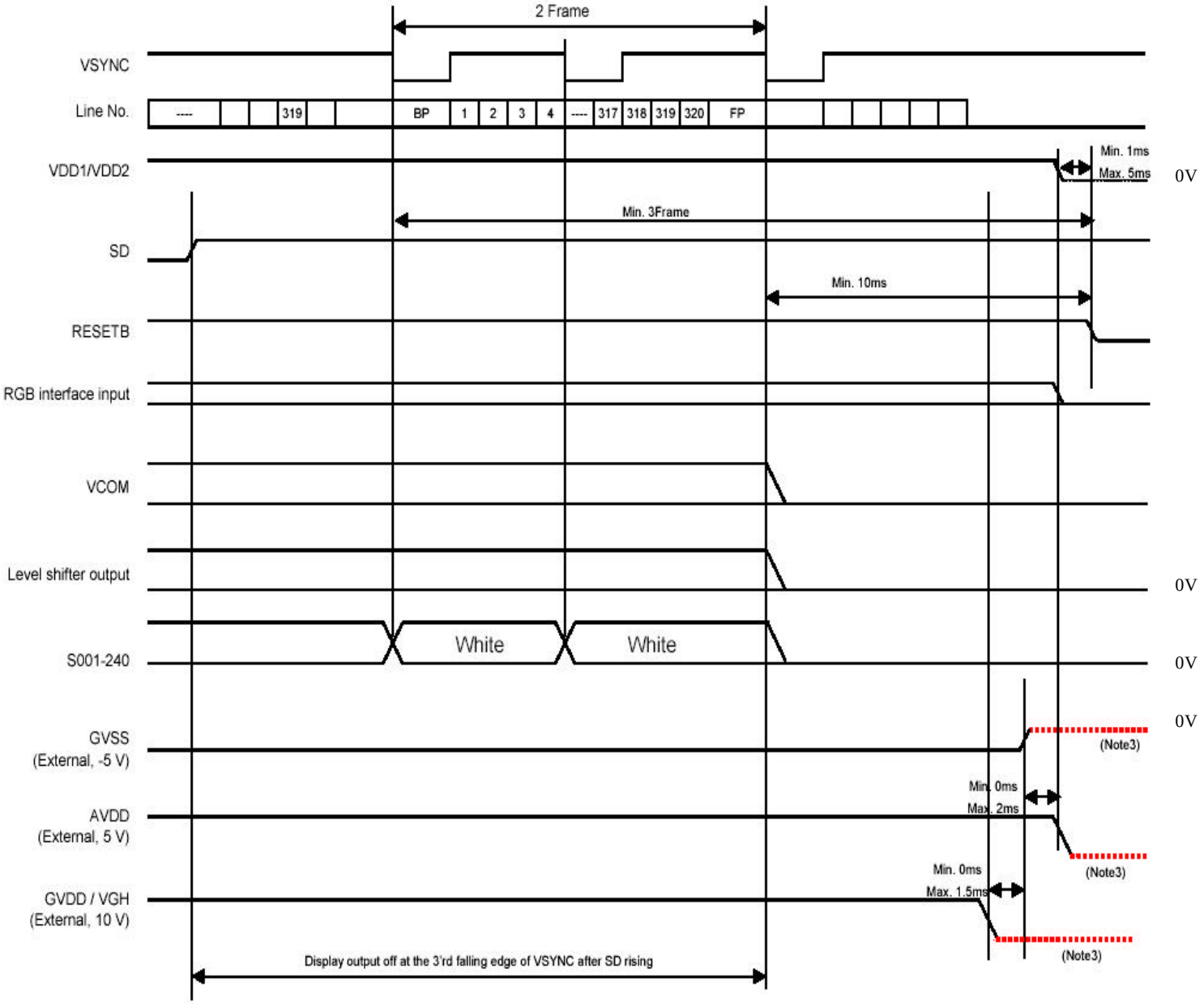
2. Power Off Sequence (with DC/DC supply outward & SD fixed at low)
   Power off sequence is controlled by SD signal



(Note1) RGB interface input – VSYNC/HSYNC/DCK/R5-0/G5-0/B5-0/DE/CM

(Note2) Level shifter output – CKH1/CKH2/CKH3/STV1/STV2/CKV1/CKV2/ENBV/CSV)

(Note3) GVSS, AVDD and GVDD/VGH should be open after external power off

*(Note5) In order to prevent high current due to the latch-up in external power on sequence, shot-key diode should be connected between VGH and VDD2 as shown **External Component Application2** in page5. (Recommended spec of the shot-key diode: VF < 0.4V/100mA, VR > 15V)*

Note: In some application, SD signal fixed at "low" level during power on. ASIC should produce white pattern when receiving10th S. And internal power regulator should function normally.

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9. Optical Characteristics

9.1 Optical Specification

(1) Back light Off / w Touch panel

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	T 11(R)		CR = 2	35	45	-	Degree	Note 9-1
	T 12(L)			25	35	-		
	T21(U)			35	45	-		
	T22(D)			35	45	-		
Chromaticity	White	x	Θ=0°	0.275	0.310	0.345	-	Note 9-3
		y		0.290	0.330	0.370	-	
Contrast Ratio	CR		Θ=0°	5:1	10:1	-	-	Note 9-2
Reflectivity	R		Θ=0°	5	10	-	%	Note 9-4

(2) Back Light On /w Touch panel

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	T 11(R)		CR = 10	40	45	-	Degree	Note 9-1
	T 12(L)			35	40	-		
	T21(U)			55	60	-		
	T22(D)			30	35	-		
Response Time	Tr+Tf		Θ=0°	-	35	50	ms	Note 9-5
Contrast Ratio	CR		Θ=0°	90:1	150:1	-	-	Note 9-6
Luminance	L		Θ=0° I_F=20mA	125	150	-	cd/m^2	Note 9-7
NTSC	-		-	40	45	-	%	Note 9-7
Uniformity	-		-	75	80	-	%	Note 9-8
Chromaticity	Red	x	Θ=0°	0.533	0.568	0.603	-	Note 9-9
		y		0.305	0.345	0.385		
	Green	x		0.265	0.300	0.335		
		y		0.529	0.569	0.609		
	Blue	x		0.111	0.146	0.181		
		y		0.093	0.133	0.173		
	White	x		0.260	0.295	0.330		
		y		0.283	0.323	0.363		

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9.2 Basic measure condition

(1) Driving voltage

VDD= 12.0V, VEE=-6.5V

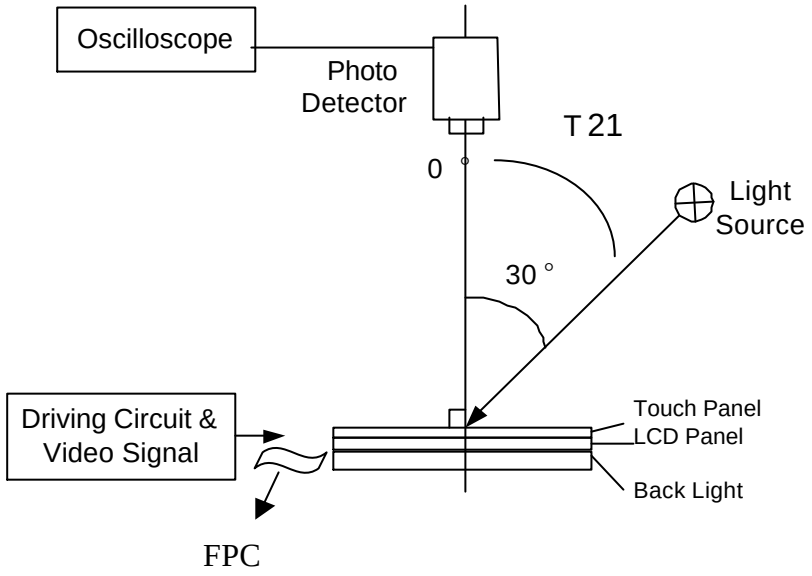
(2) Ambient temperature: Ta=25℃

(3) Testing point: measure in the display center point and the test angle Θ=0 °

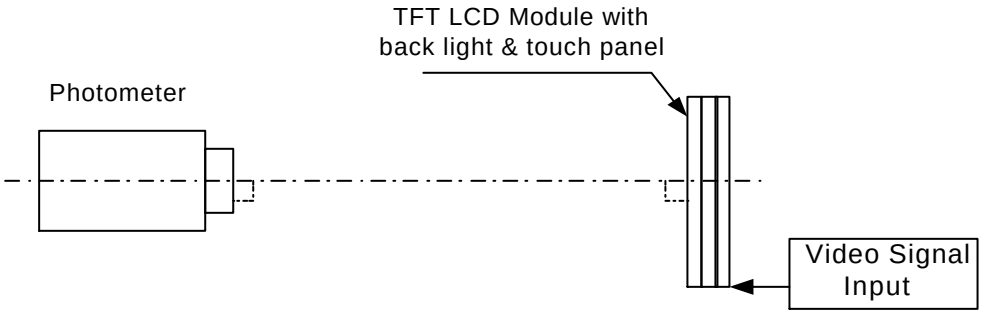
(4) Testing Facility

Environmental illumination: = 1 Lux

a. System A



b. System B



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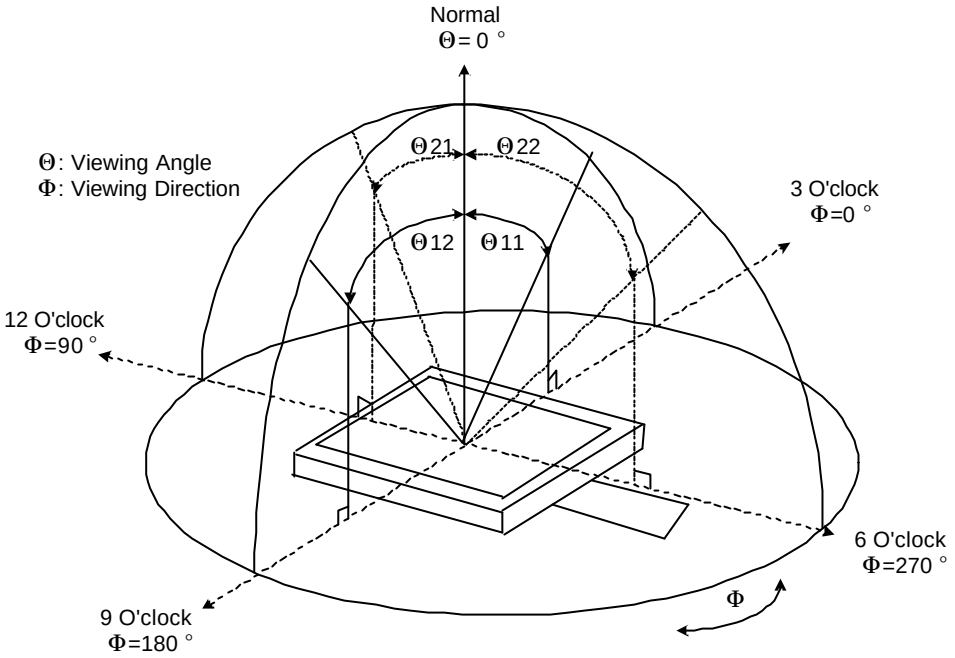
Note 9-1: Viewing angle diagrams (Measure System A)



Note 9-2: Contrast ratio in back light off (Measure System A)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 9-3: White chromaticity as back light off: (Measure System A)

Note 9-4: Reflectivity (R) (Measure System A)

In the measuring system B. calculate the reflectance by the following formula.

$$\text{Reflectivity(R)} = \frac{\text{Output from the white display panel}}{\text{Output from the reflectance standard}} \times \text{Reflectance factor of reflectance standard}$$

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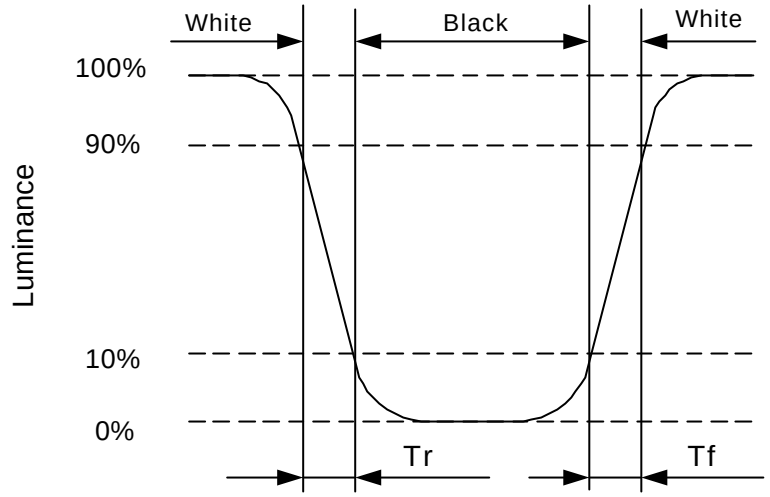
Note 9-5: Definition of response time: (Measure System B)



Note 9-6: Contrast Ratio in back light On (Measure System B)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

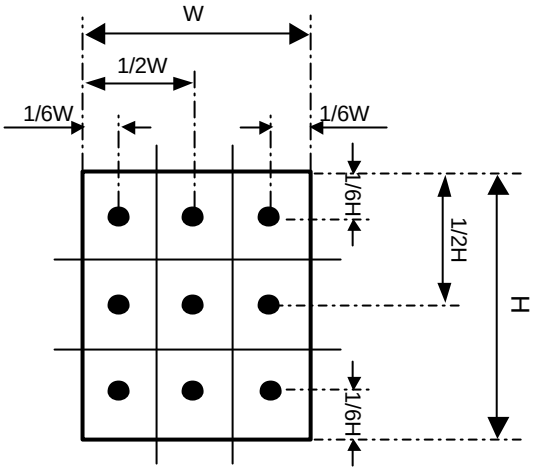
Note 9-7: Luminance: (Measure System B)

Test Point: Display Center

Note 9-8: Uniformity (Measure System B)

The luminance of 9 points as the black dot in the figure shown below are measured and the uniformity is defined as the formula:

$$\text{Uniformity} = \frac{\text{The minimum luminance among 9 points}}{\text{The maximum luminance among 9 points}}$$



Active Area (W x H)

Note 9-9: White chromaticity as back light on(Measure System B)

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10. Reliability

No	Test Item	Condition
1	High Temperature Operation	Ta=+60℃, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta= -20℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+70℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta= -30℃, 240hrs
6	Thermal Shock (non-operation)	-30℃ ← → 70℃, 50 cycles 30 min 30 min
7	Resistance to Static Electricity Discharge (non-operation)	C=200pF, R=0 Ω; Discharge: ±150V 3 times / Terminal
8	Surface Discharge (non-operation) (LCD surface)	C=150pF, R=330 Ω; Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel
9	Vibration (non-operation)	Frequency: 10~55Hz; Amplitude: 1.5mm Sweep Time: 11min Test Time: 2 hrs for each direction of X, Y, Z
10	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Three times
11	Pin Activation Test (Touch Panel)	Hit 1,000,000 times with a silicon rubber of R8 HS 60. Hitting Force: 250g Hitting Speed: 3 time/sec
12	Writing Friction Resistance Test (Touch Panel)	Pen: 0.8R Polyacetal stylus Load: 250g Speed: 3 Strokes/sec Stroke: 35mm 100000 times

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11. Handling Cautions

11.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

(1) In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connects wrist to the earth and the conducting shoes to the earth necessary is.

(2) The machine and working table for the panel should have ESD protection strategy.

(3) In handling the panel, ionized airflow decreases the charge in the environment is necessary.

(4) In the process of assemble the module, shield case should connect to the ground.

11.2 Environment

(1) Working environment of the panel should be in the clean room.

(2) Because touch panel has protective film on the surface, please remove the protection film slowly with ionized air to prevent the electrostatic discharge.

11.3 Touch panel

(1) The front touch panel is vulnerable to heavy weight, so any input must be done by special stylus or by a finger. Do not put any heavy stuff on it.

(2) When any dust or stain is observed on a film surface, clean it using a glass lens cleaner for something similar.

11.4 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface or condensation as panel power on will corrode panel electrode.

(4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

(5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible

11.5 Design notes on touch panel

(1) Explanation of each boundary of touch panel

「१.Boundary of Double-sided adhesive

a. Electrically detectable within this zone.

When holding the touch panel by housing, it needs to be held at outside of this zone.

b. Film is supported by double-sided adhesive tape.

「२.Viewing area

a. Cosmetic inspection to be done for this area.

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This area is set as inside of boundary of double-sided adhesive with tolerance.

「ㅅ.Boundary of transparent insulation

a. Purpose is to "Help" to secure insulation.

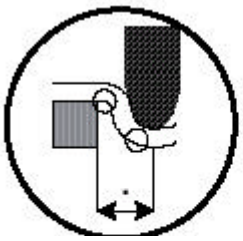
b. Electrical insulation on this area is not guaranteed.

c. We do recommend not to hold this area by something like housing or gasket.

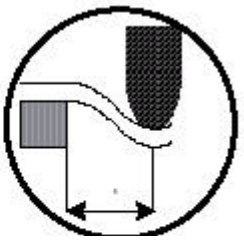
「ㅈ.Active area

a. This area is where the performance is guaranteed.

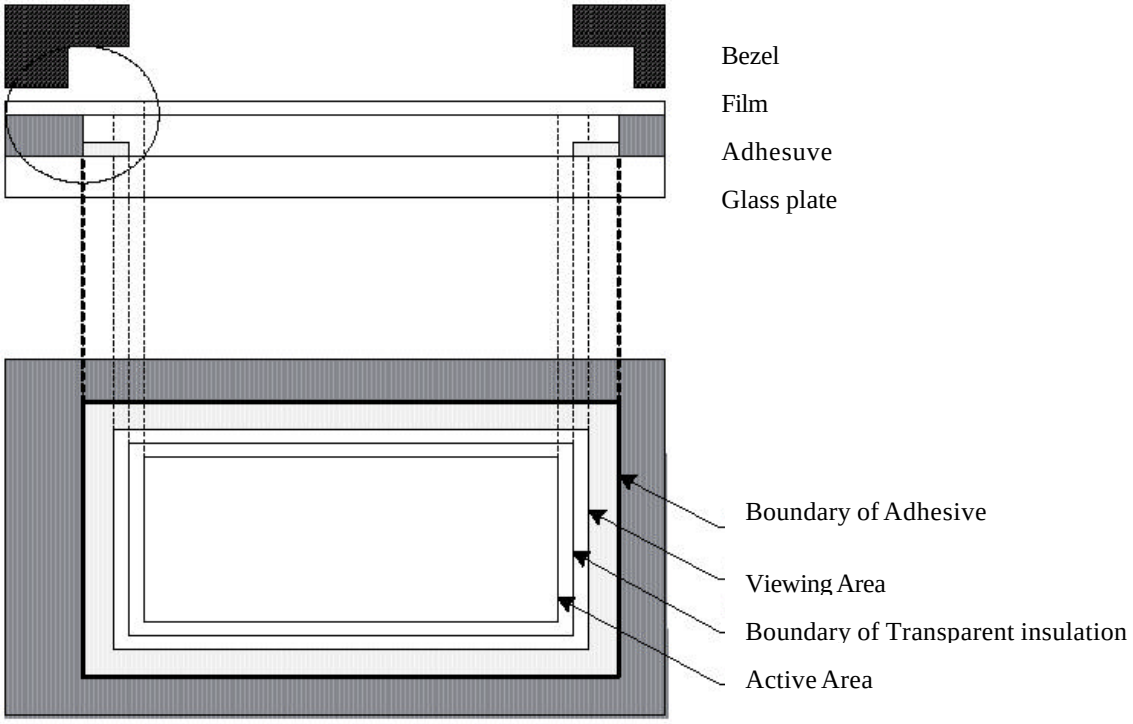
This area set as 2.3mm inside from the boundary area of double-sided adhesive tape since its neighboring area is less durable to writing friction.



There is some possibility to damage ITO



No Damage to ITO



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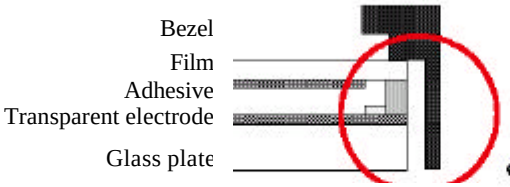
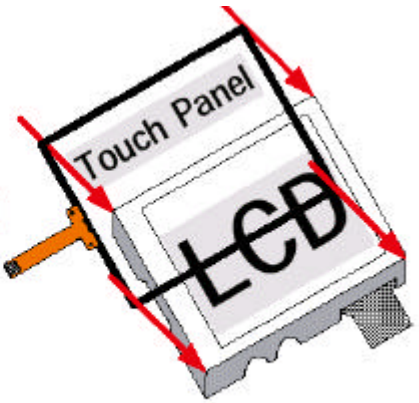
(2) Housing and touch panel

a. Please have clearance between the side of touch panel and any conductive material such as metal frame (Drawing.1). Transparent electrode exists on glass of touch panel from end to end.

b. It is recommended to fix a touch panel on the LCD module chassis rather than the touch panel housing. Clinging at conductive material and side of touch panel might cause the malfunction.



Drawing 1



Drawing 2

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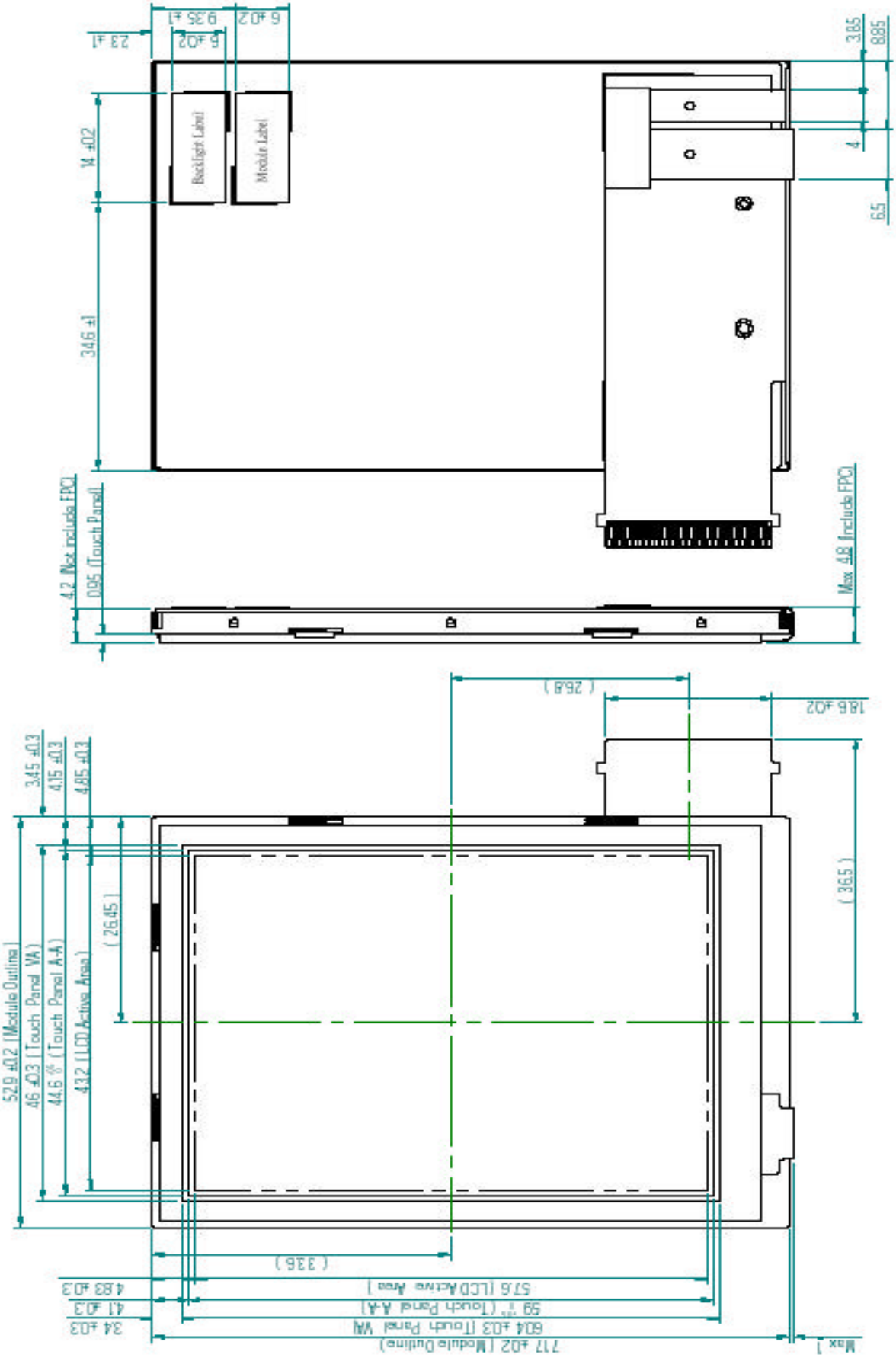
12. Mechanical Drawing



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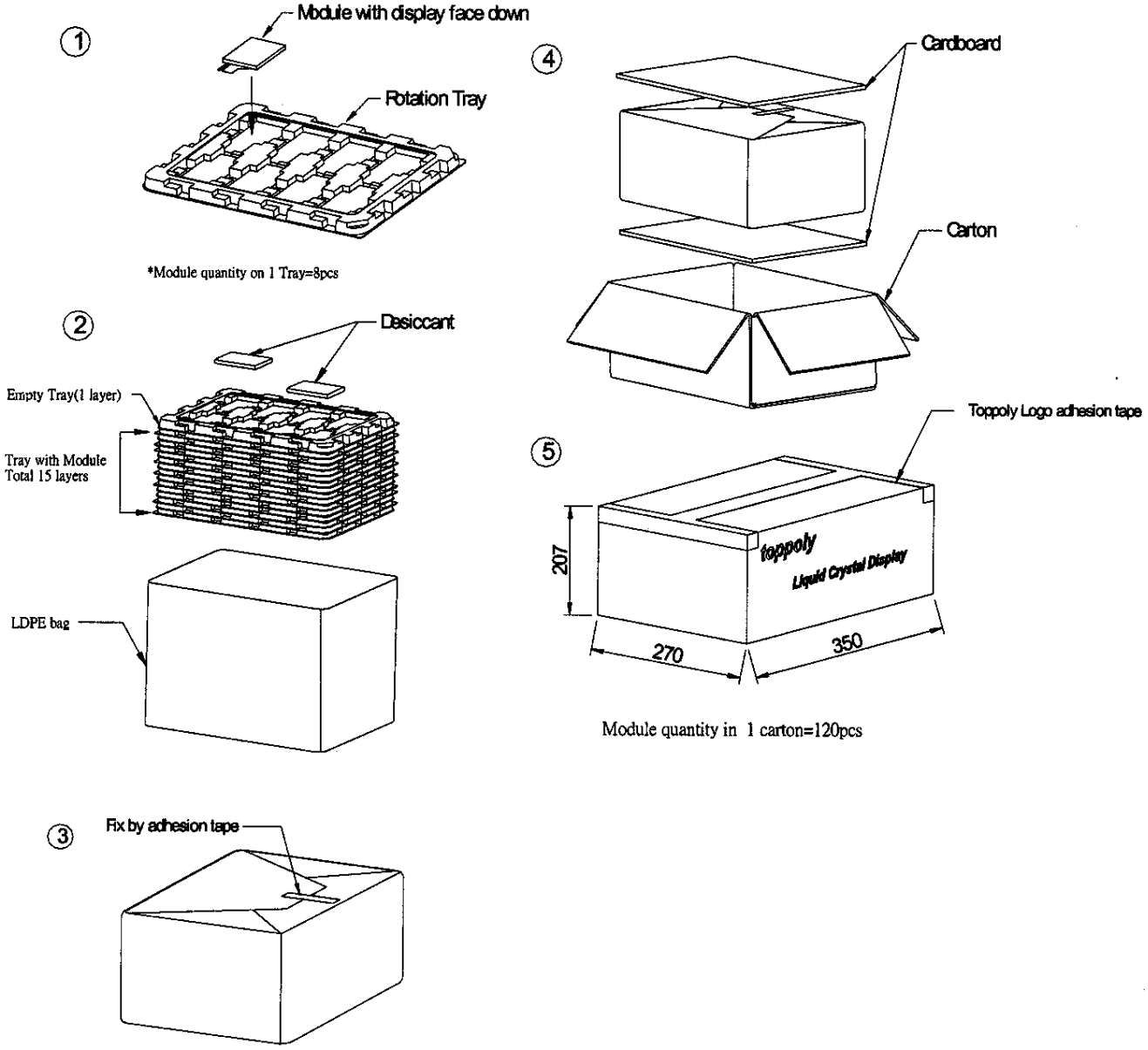
13. Packing Drawing



TD028STEB1 Module Delivery Packing Instruction:

(1) Module packed into tray cavity with panel face down.

(2) Tray stacking with 15 layers and with 1 empty tray above the stacking tray unit.
Then put 2pcs desiccant above the empty tray.

(3) Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4) Put 1pcs cardboard inside the carton bottom, and pack the finished package into the carton.
Then put 1pcs cardboard above the packing finished good.

(5) Carton sealing with adhesive tape.

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