LIBRARY ieee;  
USE ieee.std\_logic\_1164.ALL;  
USE ieee.std\_logic\_arith.ALL;  
USE IEEE.std\_logic\_unsigned.ALL;  
----------------------------------------------------------  
ENTITY test\_1 IS  
    PORT(  
        clk                : in    std\_logic;  
        reset\_n            : in    std\_logic;  
        button\_1        : in    std\_logic;  
        button\_2        : in    std\_logic;  
        button\_3        : in    std\_logic;  
        LED\_1            : out    std\_logic;  
        LED\_2            : out    std\_logic;  
        LED\_3            : out    std\_logic;  
        clk\_out         : out    std\_logic  
        );  
END test\_1;  
----------------------------------------------------------  
architecture beh of test\_1 is  
signal    test\_sig\_1         :   std\_logic;  
signal   count           :   std\_logic\_vector(0 downto (25000000/2)-1 );  
signal   clk\_temp        :   std\_logic;  
  
----------------------------------------------------------  
begin  
    LED\_1 <= button\_1;  
    LED\_2 <= button\_2;  
    LED\_3 <= button\_3;  
    process(clk,clk\_temp,reset\_n)  
    begin  
        if clk'event and clk = '1' then  
------------------------------------------------  
         if (reset\_n = '1') then  
         clk\_temp <='0';  
         count <= (others =>'0') ;-- setze alle bit auf null  
          else  
          count <= count + 1;  
          if count = "10111110101111000010000000" then   
          clk\_temp <= not clk\_temp;  
          count <= (others=>'0');  
          end if;  
          end if;  
         --  x"17D7840"  
------------------------------------------------  
        end if

    end process;  
      
end beh;  
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