Å

SMLS851-JANUARY 1993

- Organization . . . $64K \times 8$ or $32K \times 16$.
- Single 5-V Power Supply
- **JEDEC Approved Pin Assignment** • (STD 21-C)
- **Industry Standard 28-Pin Plastic and** Ceramic Dual-In-Line Package, 32-Lead **Plastic and Ceramic Chip Carrier**
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

V _{CC} ± 5%	V _{CC} ± 10%	
'87C510-100		100 ns
'87PC510-100		100 ns
'87C510-120	'87C510-12	120 ns
'87PC510-120	'87PC510-12	120 ns
'87C510-150	'87C510-15	150 ns
'87PC510-150	'87PC510-15	150 ns
'87C510-200	'87C510-20	200 ns
'87PC510-200	'87PC510-20	200 ns

- 8-Bit or 16-Bit Output For Use in **Microprocessor Based Systems**
- **On Chip Latches for Address and Data**
- No Interface Needed to Most **Microcontrollers**
- **TI Proprietary Novel Features**
 - ON BOARD Programming
 - GLUE-LESS BUS INTERFACE™
 - FRIENDLY WRITE INTERFACE™
- Very High-Speed SNAP! Pulse • Programming
- 2 Byte or 1 Word Programming •
- **Power-Saving CMOS Technology** .
- . **3-State Output Buffers**
- 400-mV Minimum DC Noise Immunity With Standard TTL Loads
- Latchup Immunity of 250 mA on All Input • and Output Pins
- **Differentiated Chip Enables:**
 - E1 for Fast Access,

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

- E2 for Low Power Consumption
- Low Power Dissipation (V_{CC} = 5.5 V)
 - Active . . . 165 mW Worst Case
 - Economy ... 55 mW (CMOS-Input Levels)
 - Power Down 1.1 mW (CMOS-Input Levels)
- **PEP4 Version Available With 168-Hour Burn-In and Choices of Operating Temperature Ranges**

J AND N PACKAGES [†]										
	(TOP VIEW)									
1			1							
V _{PP} [1	28] V _{CC}							
E1[2	27	PGM							
G	3	26	BG							
E2	4	25	ALE							
NC	5	24] MODE							
AD0[6	23] A16							
AD8	7	22	AD15							
AD1	8	21	AD7							
AD9	9	20	AD14							
AD2	10	19	AD6							
D10	11	18	AD13							
AD3	12	17	AD5							
م 111 آ	13	16	AD12							
GND	14	15	AD4							
			۲							





[†] Packages are shown for pinout reference only.

[‡] Pin 1 and Pin 16 must be externally connected to ground.

PIN NOMENCLATURE							
AD15-AD0	Address/Data Inputs/Outputs						
E1, E2	Chip Enable Inputs						
G	Output Enable						
PGM	Program Enable						
ALE	Address Latch Enable						
BG	Byte Mode Select						
MODE	Bus Mode Select						
NC	No Internal Conections						
V _{CC}	5-V Power Supply						
GND	Ground						
V _{PP}	13-V Power Supply [§]						

§ Only in program mode, 5-V or open in read mode.



Copyright © 1992, Texas Instruments Incorporated

SMLS851-JANUARY 1993

description

The TMS87C510 series are 524 288-bit, ultraviolet-light erasable, electrically programmable read-only memories. The TMS87PC510 series are 524 288-bit, one time, electrically programmable read-only memories. Address and data are fully multiplexed on the same pins (AD0–AD15). This allows minimizing the number of interconnection lines between the memory and industry standard microprocessors with time multiplexed address and data bus.

A bus mode control pin (MODE) allows the memory to be directly interfaced to either any Intel-like multiplexed bus or to any Motorola-like multiplexed bus without need of glue logic (GLUE-LESS BUS INTERFACE[™]).

A byte mode control pin BG, in conjunction with AD0, allows the device to be used either as a byte wide (8 bit data input/output) or as a word wide (16 bit data input/output) memory. In particular no interface is required to 80C48/51, 80C88/98, 70C20/40/42, 68H05/11 8-bit families and 80C86/186, 80C96/196 16-bit families of microprocessors/microcontrollers.

The TMS87C510 and TMS87PC510 can be programmed using $V_{PP} = 13$ V, $V_{CC} = 5$ V (SNAP! Pulse programming algorithm) for a minimum programming time of 7 sec. and a maximum programming time of 70 sec. An internal voltage reference allows the memory to be programmed without changing the 5-V supply available at the P.C. board level. In this way the chip can be programmed without removing it from the board. This facility, not available on standard EPROMs, is called *ON BOARD* Programming.

Unlike any other EPROM, THE TMS87C510 and TMS87PC510 are internally provided with a write interface that allows the microprocessor to control programming of the memory by using short pulse signals at the beginning and at the end of each program operation (FRIENDLY WRITE INTERFACETM), this avoids keeping the \overrightarrow{PGM} line and the address and data lines steady throughout the program operation.

The TMS87C510 and TMS87PC510 are provided with two enable pins: active high E1 and active low $\overline{E2}$. The memory is enabled only when both enable pins are active. The availability of two enable pins increases flexibility in using this memory in systems where either the response speed, or low power consumption is a key concern. E1 allows the memory to respond quickly and therefore can be activated just before strobing data in or out whereas $\overline{E2}$ needs to be asserted earlier, but guarantees the lowest power consumption while inactive.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS87C510 EPROM is offered in both 28 pin dual in-line ceramic package (J suffix) and 32-lead chip-carrier ceramic package (FN suffix).

The TMS87PC510 OTP PROM is offered in both 28 pin dual in-line plastic package (N suffix) and 32-lead chip-carrier plastic package (FM suffix).

The TMS87C510 and TM87PC510 are offered with three choices of temperature ranges of 0°C to 70°C, -40°C to 85°C and -40°C to 110°C.

The TMS87C510 is also offered with 168-Hour Burn-in for all temperature ranges. (See table below).

EPROM AND OTP PROM	SUFFIC FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN			SUFFIX VS	FOR PEP4 168-HOU TEMPERATURE RA	JR BURN-IN ANGES
	0°C TO 70°C - 40°C TO 85°C - 40°C TO 110°		– 40°C TO 110°C	0°C TO 70°C	– 40°C TO 85°C	– 40°C TO 110°C
TMS87C510_xxx	JL/FNL	JE/FNE	JQ/FNQ	JL4/FNL4	JE4/FNE4	JQ4/FNQ4
TMS87PC510_xxx	NL/FML	NE/FME	NQ/FMQ			



SMLS851-JANUARY 1993

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming. All programming signals are TTL level. These devices are programmable using the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 5 V for a nominal programming time of seven seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

A key feature of this family of devices is the direct interfaceability to either of the two standard microprocessor control busses widely known as Intel-like and Motorola-like busses.

When the MODE pin is tied to V_{CC} , the TMS87C510 and TMS87PC510 are directly compatible with the Intel- mode bus scheme.



Figure 1. Intel-Mode Control Bus

When the MODE pin is tied to GND, the TMS87C510 and TMS87PC510 are directly compatible with the Motorola- mode bus scheme.







SMLS851-JANUARY 1993

operation

Intel-mode (MODE = V_{CC})

The ten device-level modes of operation are listed in the following table. The read mode requires a single 5 V supply. All inputs are TTL level except V_{PP} during programming is 13 V, MODE in all modes is 5 V and $\overline{E2}$ in signature mode is 12 V.

MODE			READ			W		CTAND	DOWER	
FORMAT	ADDR IN	READ DATA	OUTPUT DISABLE	SIGNATURE MODE	ADDR IN	PROGRAM DATA	PROGRAM VERIFY	PROGRAM INHIBIT	BY	DOWER
E1	Х	V _{IH}	V _{IL} or	VIH	Х	V _{IH}	VIH	V _{IL} or	VIL	Х
E2	VIL	V _{IL}	V _{IH} or	HV [†]	VIL	V _{IL}	V _{IL}	V _{IH}	VIL	V _{IH}
G	VIH	VIL	VIH	V _{IL}	VIH	VIH	V _{IL}	Х	Х	Х
PGM	VIH	V _{IH}	Х	VIH	VIH	V _{IL} §	VIH	Х	Х	Х
ALE	V _{IH}	V _{IL}	Х	V _{IL}	V _{IH}	V _{IL}	V _{IL}	Х	Х	Х
BG	AIN [‡]	Х	Х	Х	AIN	Х	Х	Х	Х	Х
V _{PP}	5 V or open	5 V or open	5 V or open	5 V or open	13 V	13 V	13 V	13 V	5 V or open	5 V or open
V _{CC}	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V
AD0	AIN [‡]	DOUT/Z [‡]	Z	MFG/DEV	AIN [‡]	DIN/X‡	DOUT/Z [‡]	Z	Z	Z
AD1-AD7	AIN	DOUT/Z‡	Z	CODE	AIN	DIN/X‡	DOUT/Z‡	Z	Z	Z
AD8-AD15	AIN	DOUT/Z [‡]	Z	00	AIN	DIN/X [‡]	DOUT/Z [‡]	Z	Z	Z
MODE	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V

X = Don't care input

Z = High impedance output

[†] High voltage = $12 V \pm 0.5 V$

[‡] See Input/Output Truth Table

§ Data loaded when asserted and

programmed when deasserted until dummy read is executed

INPUT/OUTPUT TRUTH TABLE							
BG AD0 D 15:8 D 7:0 WIDTH							
LOW	LOW	UPPER BYTE	LOWER BYTE	WORD			
LOW	HIGH	UPPER BYTE	X / HIGH-Z	BYTE			
HIGH	LOW	X / HIGH-Z	LOWER BYTE	BYTE			
HIGH	HIGH	X / HIGH-Z	UPPER BYTE	BYTE			

Below is the functional table for the MOTOROLA-mode. (MODE = GND).





SMLS851-JANUARY 1993

operation

Motorola-mode (MODE = GND)

The ten device-level modes of operation are listed in the in the following table. The read mode requires a single 5 V supply. All inputs are TTL level except V_{PP} during programming is 13 V, MODE in all modes is 0 V and $\overline{E2}$ in signature mode is 12 V.

MODE			READ			W	'RITE		OTAND	DOWED
FORMAT	ADDR IN	READ DATA	OUTPUT DISABLE	SIGNATURE MODE	ADDR IN	PROGRAM DATA	PROGRAM VERIFY	PROGRAM INHIBIT	BY	DOWER
E1	Х	V _{IH}	V _{IL} or	VIH	Х	V _{IH}	VIH	V _{IL} or	VIL	Х
E2	VIL	V _{IL}	V _{IH} or	HV [†]	VIL	V _{IL}	V _{IL}	V _{IH}	VIL	VIH
G	VIH	V _{IH}	VIH	VIH	VIL	V _{IH}	VIH	Х	Х	Х
PGM	VIH	V _{IH}	Х	VIH	VIL	VIL§	VIH	Х	Х	Х
ALE	V _{IH}	V _{IL}	Х	V _{IL}	V _{IH}	V _{IL}	V _{IL}	Х	Х	Х
BG	AIN [‡]	Х	Х	Х	AIN [‡]	Х	Х	Х	Х	Х
V _{PP}	5 V or open	5 V or open	5 V or open	5 V or open	13 V	13 V	13 V	13 V	5 V or open	5 V or open
V _{CC}	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V	5 V
AD0	AIN [‡]	DOUT/Z [‡]	Z	MFG/DEV	AIN [‡]	DIN/X [‡]	DOUT/Z [‡]	Z	Z	Z
AD1-AD7	AIN	DOUT/Z [‡]	Z	CODE	AIN	DIN/X‡	DOUT/Z [‡]	Z	Z	Z
AD8-AD15	AIN	DOUT/Z [‡]	Z	00	AIN	DIN/X [‡]	DOUT/Z [‡]	Z	Z	Z
MODE	0 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V

X = Don't care input

Z = High impedance output

[†] High voltage = $12 V \pm 0.5 V$

[‡] See Input/Output Truth Table

§ Data loaded when asserted and programmed when deasserted until dummy read is executed

	INPUT/OUTPUT TRUTH TABLE							
BG	AD0	D 15:8	D 7:0	WIDTH				
LOW	LOW	UPPER BYTE	LOWER BYTE	WORD				
LOW	HIGH	UPPER BYTE	X / HIGH-Z	BYTE				
HIGH	LOW	X / HIGH-Z	LOWER BYTE	BYTE				
HIGH	HIGH	X / HIGH-Z	UPPER BYTE	BYTE				

address latching

Multiplexing of address and data consists of issuing a set of valid values on address lines AD0–AD15, and signal BG, at the beginning of every memory access cycle along with a valid address strobe ALE.

The address values are latched onto a set of static registers internal to the memory by using the \overline{ALE} signal as transparent address latch enable. The described operation is called address latching. After this phase, lines AD0–AD15 are made available for data transfer.

Multiplexing of address and data on the same line implies that on the bus AD0–AD15 will be present at different times either information related to the address (indicated specifically with A0–A15 and generally with AIN) or information related to the data (indicated specifically with D0–D15 and generally with DIN or DOUT).

During the address latching phase it is not required to have both E1, $\overline{E2}$ chip enables active. In particular the access time is not affected by delays in the external decoding used to enable the memory chip with E1, if $\overline{E2}$ has been asserted since the beginning of the current memory access cycle or earlier (see economy mode).

During address latching the signals \overline{BG} and AD0 are latched and decoded to configure the memory chip input/output data width to be either a word (16 bit data), or a byte (8 bit data). (See input/output truth tables, pages 4, 5).



SMLS851-JANUARY 1993

Configurations are as follows:

- BG = low, AD0 = low: data width is a word. The lower byte (i.e., the even address byte, AD0 = 0) and the upper byte (the odd address byte, AD0 = 1) are simultaneously transferred on address/data lines with lower byte on lower half of address/data lines and upper byte on upper half of address/data lines.
- BG = low, AD0 = high: data width is a byte. The upper byte (the odd address byte AD0 = 1) is transferred on upper half of address/data lines.
- Cases with BG = high correspond to standard byte wide memory operation. Data is always transferred on the lower half of address/data lines. AD0 has the usual meaning of least significant bit of the byte address.

The address latch operation is the same in both read and write modes except for V_{PP} value.

output disable

When the outputs of two or more TMS87C510 or TMS87PC510 are connected in parallel on the same bus, the output of any particular device can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low-level is applied to the $\overline{E2}$ and \overline{G} pins and a high level is applied to $\overline{E1}$ pin. All other devices in the circuit should have their outputs disabled by applying a high level signal to either $\overline{E2}$ or \overline{G} pins or a low level to $\overline{E1}$ pin.

latchup immunity

Latchup immunity on the TMS87C510 and TMS87PC510 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, "*Design Considerations; Latchup Immunity of the HVCMOS EPROM Family*", available through TI Sales Offices.

power down and economy/standby modes

Active I_{CC} supply current can be reduced from 30 mA to 200 μ A for a high CMOS input on $\overline{E2}$ (power down mode) or to 10 mA for a low CMOS input on both E1, and $\overline{E2}$ (economy or standby mode). All other inputs are supposed to be steady CMOS level (for TTL input levels the power consumption is higher). In either mode, all outputs are in the high-impedance state.

erasure (TMS87C510)

Before programming, the TMS87C510 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity \times exposure time) is 15-W-s/cm². A typical 12-mW/cm², filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS87C510, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.



inititalizing (TMS87PC510)

The one-time programmable TMS87PC510 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS87C510 and TMS87PC510 PROM are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 3, which programs in a minimum time of seven seconds. Actual programming time will vary as a function of the programmer used.

The SNAP! Pulse programming algorithm uses internal pulse of $t_{pw} = 100 \ \mu s$ followed by a data verification to determine when the addressed location has been successfully programmed. Up to ten 100- μs pulses per location are provided before a failure is recognized.

The programming mode is achieved when $V_{PP} = 13 \text{ V}$, $V_{CC} = 5 \text{ V}$, $E1 = V_{IH}$, $E2 = V_{IL}$ and $\overline{G} = V_{IH}$ in Intel-mode ($\overline{PGM} = V_{IL}$ in Motorola-mode). Once addresses are latched and data are issued, \overline{PGM} is pulsed low (\overline{G} is pulsed high) for a minimum time of 50 nsec. Depending on the data transfer mode the memory is operating in (see input/output truth table, pages 4, 5) the data to be programmed is handled, before the actual program operation can start, in the way reported below.

- \overline{BG} = low, AD0 = low: data width is a word. Rising edge of \overline{PGM} (falling edge of \overline{G}) latches the 16 bit data into the internal 16 bit data register and an internal programming operation is started.
- BG = low, AD0 = high: data width is a byte. Rising edge of PGM (falling edge of G) latches the 8 bit data present on lines AD8–AD15 into the upper byte of the internal data register and an internal programming operation is started.
- BG = high, AD0 = high: data width is a byte. Rising edge of PGM (falling edge of G) latches the 8 bit data present on lines AD0–AD7 into the upper byte of the internal data register and an internal programming operation is started.
- BG = high, AD0 = high: data width is a byte. Rising edge of PGM (falling edge of G) latches the 8 bit data present on lines AD0–AD7 into the lower byte of the internal data register. After this data latch, another data latch operation must be executed for upper byte (BG = high, AD0 = high); the second PGM (G pulse) will latch the 8 bit data into the upper byte of the internal data register and will start the internal programming operation.

Two byte latching allows to reduce programming time since two bytes are programmed with only one internal programming operation. In case only one byte program operation is required, a dummy write of FF (Hex) into the other byte of the internal 16 bit data register must be done.

Once activated, the internal programming operation prevents the latched address from being modified by bus data transfer activity until programming is complete. However it is recommended not to reiterate write cycles to the memory since this may result in corruption of the data being programmed.

The internal programming operation enables the contents of the internal 16 bit data register to be permanently stored into the memory array at the desired location.

The internal programming operation is terminated (after 100 μ s min) when a dummy read is executed, with \overline{G} pulsed low (pulsed high) for a minimum time of 50 nsec, and the device is enabled.

This technique to generate the internal enable signal for program operation is called FRIENDLY WRITE[™] and allows the microprocessor to easily control program operation with the simplest interfacing possible.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{PP} = V_{CC}$ or open.



SMLS851-JANUARY 1993

ON BOARD Programming

Unlike a standard EPROM, the TMS87C510 and TMS87PC510 need not raise V_{CC} to 6.5 V since this voltage is generated internally when V_{PP} = 12.5 V. This provision is called ON BOARD Programming and simplifies the design of systems featuring in-field programming.

program inhibit

Programming may be inhibited by maintaining a high level input on E2 or PGM, or a low level input on E1.

program verify

Programmed bits may be verified with $V_{PP} = 13 \text{ V}$ when $\overline{G} = V_{IL}$, $E1 = V_{IH}$, $\overline{E2} = V_{IL}$ and $\overline{PGM} = V_{IH}$. This assures that adequate read margin is used to obtain the same data retention as standard devices.



SMLS851-JANUARY 1993



Figure 3. SNAP! Pulse Programming Flowchart



SMLS851-JANUARY 1993

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when $\overline{E2}$ is forced to 12 V (word width only is allowed). Two identifier bytes are accessed by different values of AD0. All other addresses must be helf low. The signature code for these devices is 97 B0. AD0 low selectes the manufacturere's code 97 (Hex), and AD0 high selects the device code B0 (Hex), as shown by the signature mode table below.

					PII	NS				
IDEN HFIER ¹	AD0	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MANUFACTURER CODE	VIL	1	0	0	1	0	1	1	1	97
DEVICE CODE	VIH	1	0	1	1	0	0	0	0	B0

[†] E1 = V_{IH}, \overline{G} pulsed low when readinig out, $\overline{E2}$ = HV, A1–A15 = V_{IL}, V_{PP} = V_{CC} or open.



SMLS851-JANUARY 1993

absolute maximum ratings over operating free-air temperature range (unless otherwis	se noted)‡
Supply voltage range, V _{CC} (see Note 1)	-0.6 V to 7 V
Supply voltage range, V _{PP}	0.6 V to 14 V
Input voltage range: All inputs except E2	to V_{CC} + 1 V
Ε2 0.	6 V to 13.5 V
Output voltage range, with respect to GND (see Note 1)	to V_{CC} + 1 V
Operating free-air temperature range ('87C510JL/FNL/FNL4 and	
'87PC510NL/FML)	-0°C to 70°C
Operating free-air temperature range ('87C510JE/FNE/JE4/FNE4 and	
'87PC510NE/FME)	10° C to 85°C
Operating free-air temperature range ('87C510JQ/FNQ/FQ4/FNQ4 and	
'87PC510NQ/FMQ))° C to 110°C
Storage temperature range	5°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		'87C5 '87C5 '87C5 '87C5 '87C5	10/PC51 10/PC51 10/PC51 10/PC51	0-100 0-120 0-150 0-200	'87C5 '87C5 '87C5	UNIT			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage (see No	te 2)	4.75	5	5.25	4.75	5	5.5	V
		Read Mode (see Note 3)	V _{CC} – 0.6	V _{CC}	V _{CC} + 0.6	V _{CC} – 0.6	V _{CC}	V _{CC} + 0.6	V
V _{PP}	Supply voltage	SNAP! Pulse Programming Algorithm	12.75	13	13.25	12.75	13	13.25	V
	High-level input voltage	TLL	2.0		V _{CC} + 0.5	2.0		V _{CC} + 0.5	
VIH		CMOS	V _{CC} – 0.2		V _{CC} + 0.5	V _{CC} – 0.2		V _{CC} + 0.5	V
v	Low-level input	TTL	– 0.5		0.8	- 0.5		0.8	V
VIL	voltage	CMOS	- 0.5		GND + 0.2	- 0.5		GND + 0.2	v
T _A	Operating free-air temperature	'87C510JL/FNL/FNL4 '87PC510NL/FML	0		70	0		70	°C
T _A	Operating free-air temperature	'87C510JE/FNE/FNE4 '87PC510NE/FME	- 40		85	- 40		85	°C
T _A	Operating free-air temperature	'87C510_JQ/FNQ/FNQ4 '87PC510_NQ/FMQ	- 40		110	- 40		110	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly or left open (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.



SMLS851-JANUARY 1993

electrical characteristics over full ranges of operating conditions

	PARAMET	ER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT			
v	l lieb level erderstræktere		I _{OH} = - 20 mA	V _{CC} – 0.2			V			
VOH	High-level output voltage		I _{OH} = – 2 mA	2.4			v			
	In the start strate strate		I _{OL} = 2.1 mA			0.4				
VOL	Low-level output voltage		I _{OL} = 20 μA			0.1	V			
II.	Input current (leakage)		V _I = 0 to 5.5 V			±1	μA			
IO	Output current (leakage)		$V_{O} = 0$ to V_{CC}			±1	μA			
I _{PP1}	V _{PP} supply current		$V_{PP} = V_{CC} = 5.5 V$			10	μA			
I _{PP2}	V _{PP} supply current (during	program pulse)	V _{PP} = 13 V			50	mA			
	V _{CC} supply current	urrent TTL-input level $\overline{E2} = V_{IH}, V_{CC} = 5 V, V_{PP}$ open				450				
ICC1	(power down)	CMOS-input level	$\overline{E2} = V_{CC} = 5.5 \text{ V}, \text{ V}_{PP} \text{ open}$			200	μA			
		TTL-input level	$E1 = \overline{E2} = V_{IL}, V_{CC} = 5 V, V_{PP} \text{ open}$			10				
I _{CC2}	V _{CC} supply current (economy)	CMOS-input level	$E1 = \overline{E2} = GND, V_{CC} = 5.5 V, V_{PP}$ open			10	mA			
I _{CC2}	V _{CC} supply current (active)		$ E1 = V_{IH}, \overline{E2} = V_{IL}, V_{CC} = 5.5 V \\ t_{cycle} = minimum cycle time†, \\ outputs open $			30	mA			

[†] Minimum cycle time = maximum address access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 \mbox{MHz}^{\ddagger}

	PARAMETER	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
Ci	Input capacitance	$V_I = 0, f = 1 MHz$		4	8	pF
CO	Output capacitance	V _O = 0, f = 1 MHz		6	10	pF

[‡] Capacitance measurements are made on a sample basis only.

 $^{\$}$ All typical values are at T_A = 25°C and nominall voltages.

SMLS851-JANUARY 1993

switching characteristics over full ranges of recommended operating conditions (see Notes 4)

	PARAMETER	TEST CONDITIONS	'87C51 '87PC5	0-100 10-100	'87C51 '87PC5 '87C5 '87C5	0-120 10-120 10-12 510-12	'87C51 '87PC5 '87C5 '87C5	0-150 10-150 10-15 510-15	'87C51 '87PC5 '87C5 '87C5	0-200 10-200 10-20 10-20	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{a(A)}	Access time from address			100		120		150		200	ns
t _{a(E1)}	Access time from chip enable E1			50		60		75		100	ns
t _{a(E2)}	Access time from chip enable $\overline{E2}$			100		120		150		200	ns
t _{en(G)}	Enable time, output from $\overline{\mathbf{G}}$			50		55		75		75	ns
t _{dis}	Disable time, output from G or E1 or E2, whichever occurs first [†]	$\begin{array}{l} C_L = 100 \text{ pF},\\ 1 \text{ Series 74 TTL load,}\\ \text{Input } t_r \leq 20 \text{ ns,}\\ \text{Input } t_f \leq 20 \text{ ns,} \end{array}$	0	50	0	50	0	60	0	60	ns
t _{w(AL)des}	Address latch deselect duration		25		30		50		50		ns
t _{su(ALE)}	Setup time, address to latch enable		6		10		30		30		ns
t _{h(LEA)}	Hold time, address from latch enable		10		10		20		20		ns
$t_{t(DLE)}$	Data transfer to latch enable		10		10		10		10		ns

[†] Value calculated from 0.5 V delta to measured level.

recommended timing requirements for programming: VCC = 5 V and VPP = 13 V (SNAP! Pulse programming), TA = 25° C (see Note 4)

	PARAMETER	MIN	NOM	MAX	UNIT
t _{w(P)}	Internal program operation duration	95	100	105	μs
t _{w(W)}	Pulse duration, write	50			ns
t _{w(R)}	Pulse duration, read	50			ns
t _{su(E1)}	Setup time, E1	80			ns
t _{su(E2)}	Setup time, E2	25			ns
t _{su(D)}	Setup time, data	40			ns
t _{h(D)}	Hold time, data				ns
t _{su(VPP)}	Setup time, V _{PP}	800			μs
t _{c(ALE)}	Cycle time, ALE				

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2.0 V for logic high and 0.8 V for logic low (reference AC Testing Wave Form).



SMLS851-JANUARY 1993

PARAMETER MEASUREMENT INFORMATION



Figure 4. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.



SMLS851-JANUARY 1993









SMLS851-JANUARY 1993







PRODUCT PREVIEW

SMLS851-JANUARY 1993



B. MOTOROLA mode, MODE = GND.





SMLS851-JANUARY 1993







PRODUCT PREVIEW

SMLS851-JANUARY 1993



PARAMETER MEASUREMENT INFORMATION



SMLS851-JANUARY 1993





20

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2012, Texas Instruments Incorporated