------------------------------------------------------
LIBRARY ieee;
USE ieee.std\_logic\_1164.ALL;
USE ieee.std\_logic\_arith.ALL;
USE IEEE.std\_logic\_unsigned.ALL;
----------------------------------------------------------
ENTITY Binary\_counter IS
    PORT(
        clk            : in    std\_logic;
        reset\_n        : in    std\_logic;
        clk\_in      : in    std\_logic;
        LED            : out   std\_logic\_vector(2 downto 0)
        );
END Binary\_counter;
----------------------------------------------------------
architecture beh of Binary\_counter is
signal  clk\_temp\_old  : std\_logic;
signal   cnt          : std\_logic\_vector(2 downto 0);
signal clk\_temp       : std\_logic;

----------------------------------------------------------
  begin

    process(clk,clk\_temp,reset\_n)
    begin

        if reset\_n = '0' then
            cnt <= (others =>'0');
        elsif clk'event and clk ='1' then
            if clk\_temp = '1' and clk\_temp\_old = '0' then
                cnt <= cnt + 1;
            end if;
        clk\_temp\_old <= clk\_temp;
        end if;
    end process bin;
    LED <= cnt;

end beh;
----------------------------------------------------------