TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

JBT6K71-AS (A)

256-Output Source Driver with On-Chip RAM and Power Supply System for Low-Temperature Poly-Si TFT-LCD

The JBT6K71-AS(A) is a 64-level, 256-output source driver for TFT-LCDs. It incorporates a RAM for 262,1440-color display, as well as a timing controller and oscillator. The JBT6K71-AS(A) can implement a 256 (240)-RGB x 352(320) QVGA mobile module by 1-chip in conjunction with a low-temperature poly-si TFT-LCD which integerates a power supply system on the glass substrate. It also has an RGB interface for supporting moving images in addition to an MPU interface, thus enabling easy switching between still and moving images with low power and improving efficiency in data transfer.

For mobile equipment that supports different modes with display performance varied, the JBT6K71-AS(A) provides software-controlled standby and sleep modes as well as normal display modes, in order to reduce power dissipation for battery-powered applications.

Features

- Supports 262,144-color, low-temperature Poly-Si TFT-LCD
- LCD driver output pins: 256 pins (3-multiplex switching)
- Display RAM: 202,752 bytes
- Interfaces: 18-/16-/9-/8-bit 80-series MPU interface (with any selected number of data transfers)
  Clock synchronous serial (SPI) interface
  18-/16-/6-bit RGB interface (with any selected number of data transfers)
- Gray scale: 64 levels (supporting γ correction) with software-programmable display color modes
- High-speed interface operation: 20 MHz max. (when high-speed write function is used)
- A broad range of display color control (batch display switching by software)
  - 262,144-color mode
  - 65,536-color mode
  - 8-color mode
- Supply voltage: Digital supply voltage (V_{SYS}) … 1.7 to 3.3V
  Power circuit supply voltage (VBAT) …2.4V to 3.3V, (VSYS ≦ VBAT)
- Display screen control features:
  - Deep standby mode … only the system power is turned on.
  - Standby (low-power) mode … Clock stopped and register data maintained.
  - Sleep mode … Display RAM data maintained. A command restores normal mode.
  - 2-screen partial display … the number of lines can be configured.
  - Normal display … Full-screen display

- Graphic features
  - Superimposition

    Compares the display data input through the RGB interface with the data stored in the display RAM to overlay a moving image window on the screen displaying the contents of the display RAM.
  - OSD function

    While writing display data through the MPU interface, overwrites part of it with an icon or other static display data read from OSD memory.
  - Bit operation

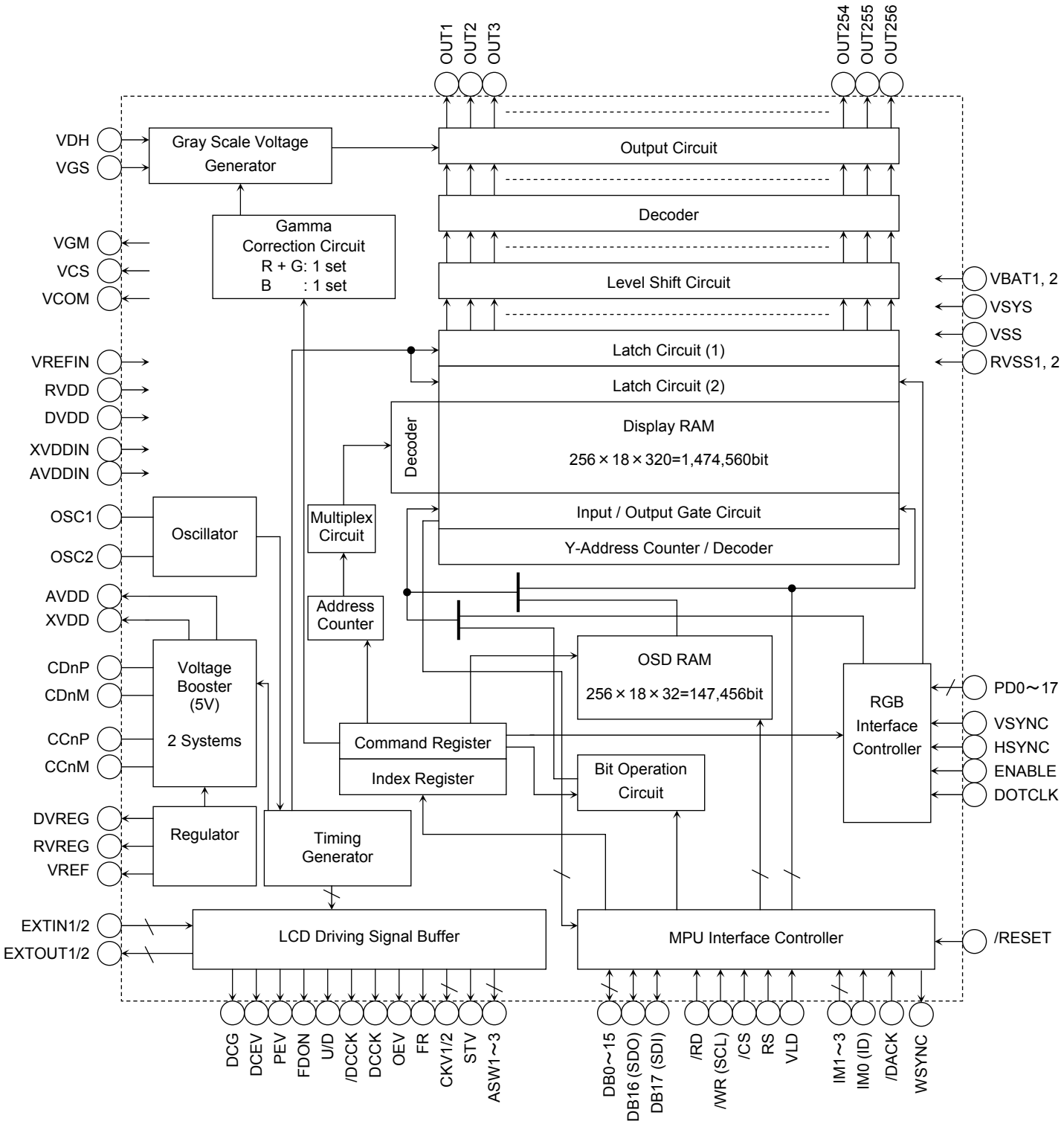
    Masks write data in bit units.
  - Window addressing and high-speed RAM write (20 MHz max.)
  - Direct memory access control

    JBT6K71-AS (A) can take display data directly from an external memory.
  - Gray scale control only for Blue

    JBT6K71-AS(A) can be changed to the two line control which divides gray scale data of Blue other than usually used RGB common control by software.
  - AUTO command (display ON/OFF sequence)

    The Clock signal control and a power supply command in display on/off sequence are automatically processed with AUTO command.
- On-chip circuits: oscillator, LCD driving voltage follower circuit, DCDC converter for 5V, and internal power supply regulator
- Operating temperature: −20 to 75°C
- Package: Gold bumped chip
- CMOS process

Block Diagram



Note 1: Test pins and blocks used by Toshiba are not shown.

Note 2: Dummy pins are not shown.

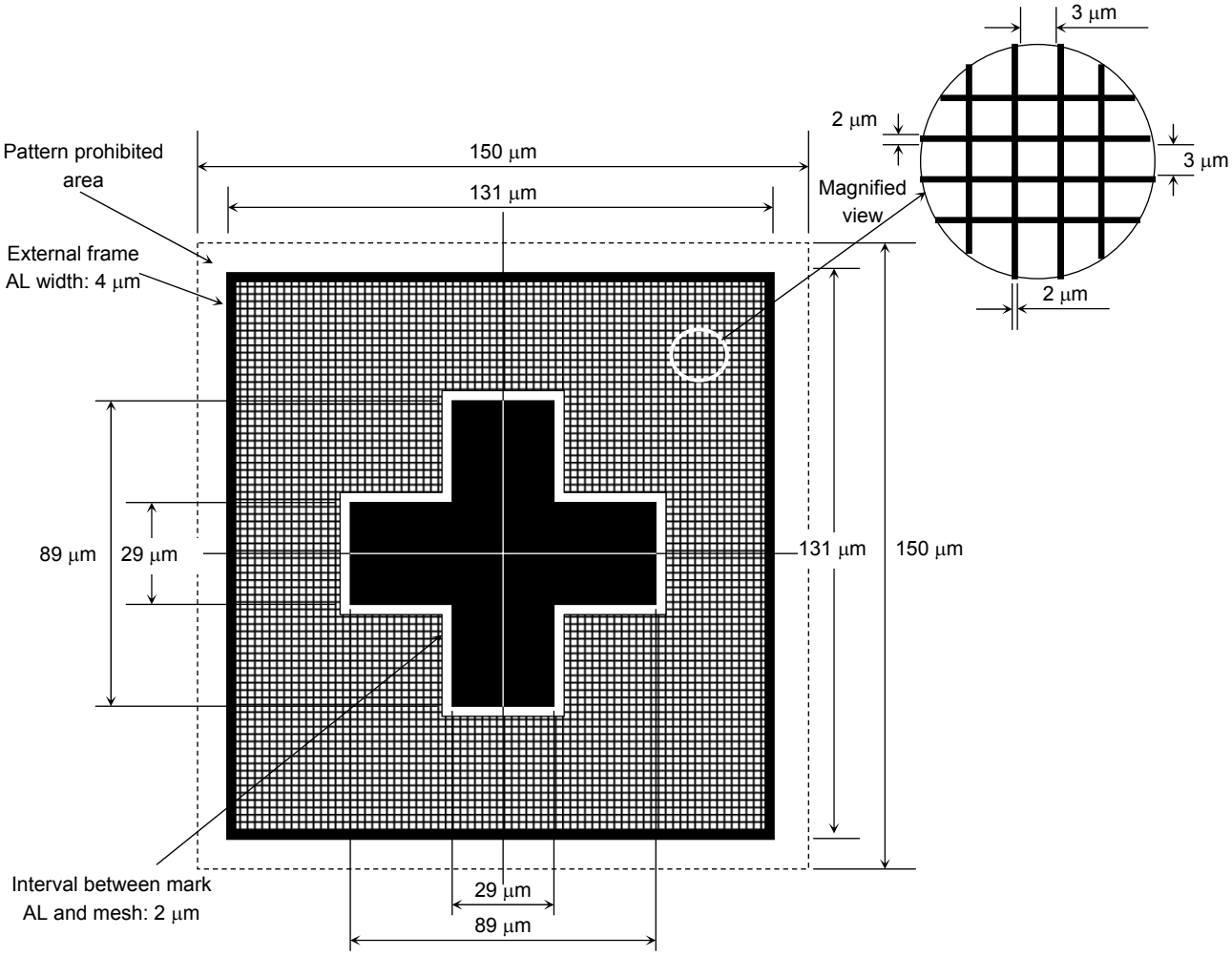
Pad Specifications

Characteristics		Size	Unit
Chip size		13,400 × 2,150	μm
Chip thickness		400	μm
Chip corner coordinate	(1)	−6,700, −1,075	μm
	(2)	6,700, −1,075	
	(3)	6,700, 1,075	
	(4)	−6,700, 1,075	
Bump pitch		88(Min.) Staggered Layout	μm
Bump height		15	μm

Characteristics	Number of Pins
Input pins	126
Output pins	256 + 26
Power supply pins	26
Test pins	2
TEG/FUSE pins	24
Dummy pins	39
Alignment marks	2

Note 1: TEG pins are used to test electrical characteristics at Toshiba. The user cannot use these pins and should leave them open.

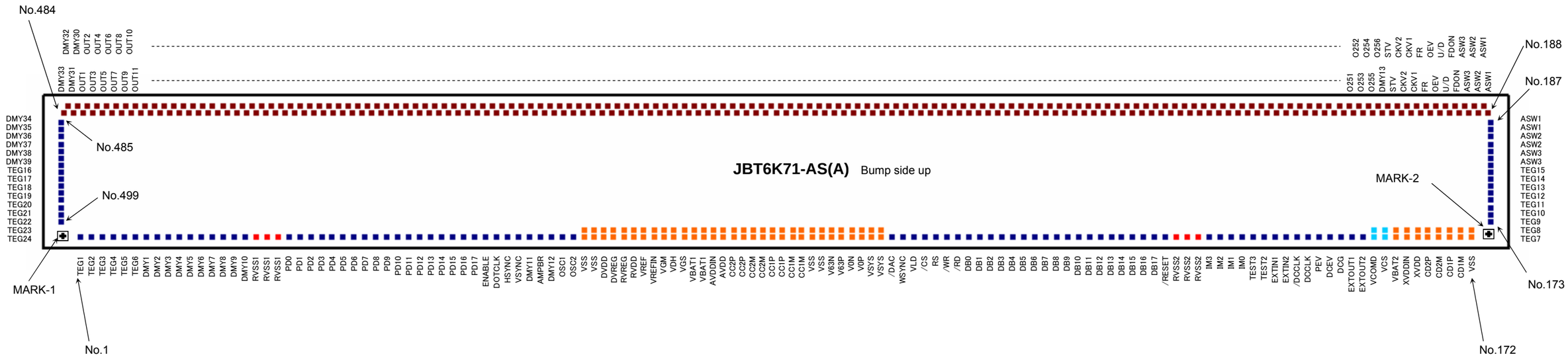
Alignment Mark Specifications



PAD Layout (Chip Image)

Chip size : 13.4mm x 2.15mm

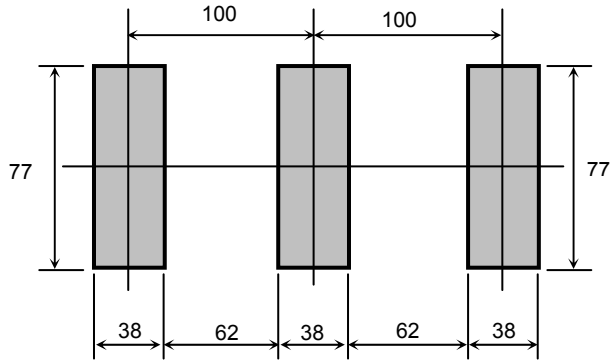
Alignment Mark : MARK-1 (-6538.0 , -913.0) MARK-2 (6538.0 , -913.0)



Bump Type	PAD No.
A-type	1-16, 20-46, 109-134, 138-152, 173-187, 485-499
B-type	17-19, 135-137
C-type	47-108, 157-172
D-type	188-484
E-type	153-156

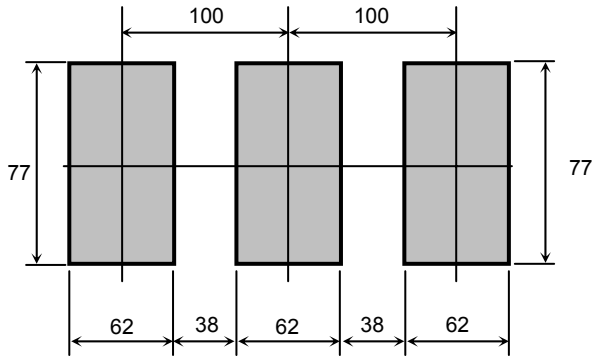
Bump type

Bump type -A



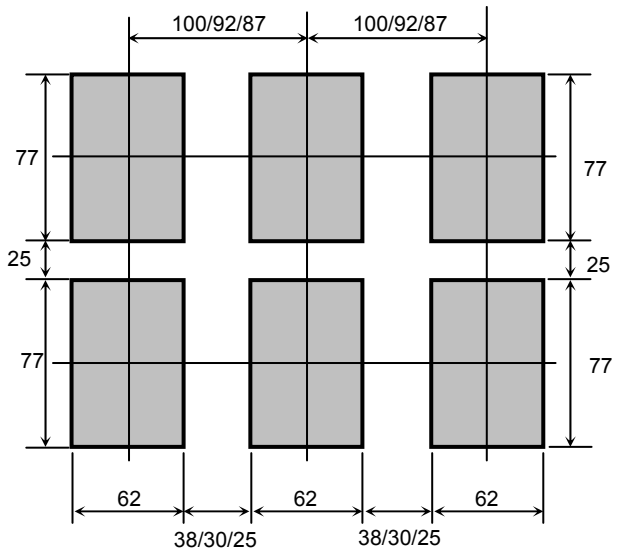
Unit: μm

Bump type - B



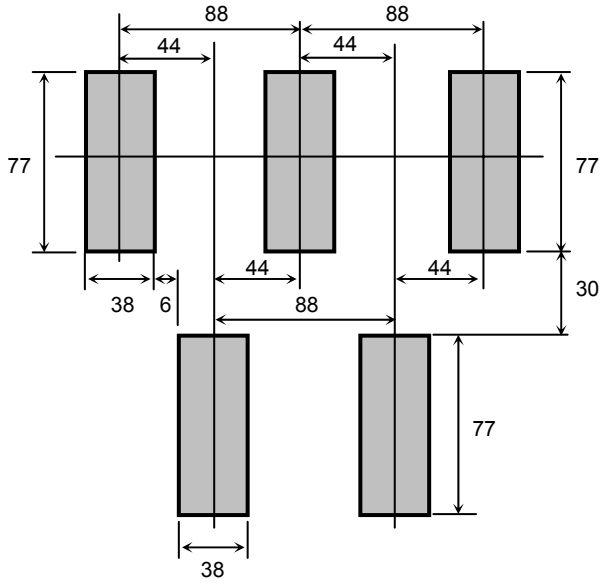
Unit: μm

Bump type - C



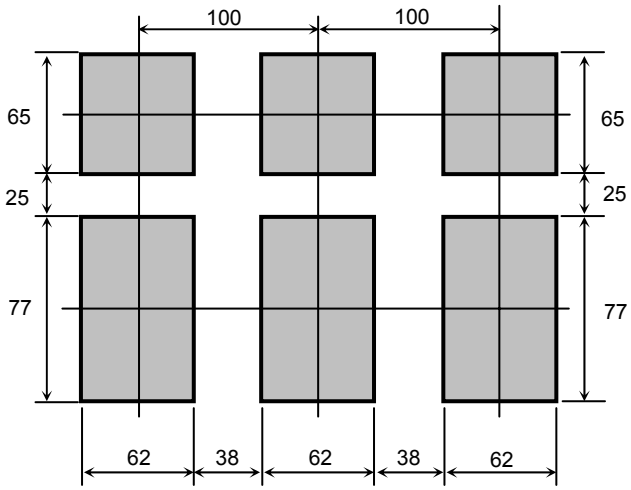
Unit: μm

Bump type - D



Unit: μm

Bump type - E



Unit: μm

Pad Coordinates (1)

[Unit: μm]

No.	Pin Name	X-Coordinate	Y-Coordinate
1	TEG1	-6356	-930
2	TEG2	-6256	-930
3	TEG3	-6156	-930
4	TEG4	-6056	-930
5	TEG5	-5956	-930
6	TEG6	-5856	-930
7	DMY1	-5756	-930
8	DMY2	-5656	-930
9	DMY3	-5556	-930
10	DMY4	-5456	-930
11	DMY5	-5356	-930
12	DMY6	-5256	-930
13	DMY7	-5156	-930
14	DMY8	-5056	-930
15	DMY9	-4956	-930
16	DMY10	-4856	-930
17	RVSS1	-4756	-930
18	RVSS1	-4656	-930
19	RVSS1	-4556	-930
20	PD0	-4456	-930
21	PD1	-4356	-930
22	PD2	-4256	-930
23	PD3	-4156	-930
24	PD4	-4056	-930
25	PD5	-3956	-930
26	PD6	-3856	-930
27	PD7	-3756	-930
28	PD8	-3656	-930
29	PD9	-3556	-930
30	PD10	-3456	-930
31	PD11	-3356	-930
32	PD12	-3256	-930
33	PD13	-3156	-930
34	PD14	-3056	-930
35	PD15	-2956	-930
36	PD16	-2856	-930
37	PD17	-2756	-930
38	ENABLE	-2656	-930
39	DOTCLK	-2556	-930
40	HSYNC	-2456	-930
41	VSYNC	-2356	-930
42	DMY11	-2256	-930
43	AMPBR	-2156	-930
44	DMY12	-2056	-930
45	OSC1	-1956	-930
46	OSC2	-1856	-930
47	VSS	-1756	-828
48	VSS	-1756	-930
49	VSS	-1669	-828
50	VSS	-1669	-930
51	DVDD	-1577	-828
52	DVDD	-1577	-930
53	DVREG	-1485	-828
54	DVREG	-1485	-930
55	RVREG	-1393	-828
56	RVREG	-1393	-930
57	RVDD	-1301	-828
58	RVDD	-1301	-930
59	VREF	-1209	-828
60	VREF	-1209	-930
61	VREFIN	-1117	-828
62	VREFIN	-1117	-930
63	VGM	-1025	-828
64	VGM	-1025	-930
65	VDH	-933	-828
66	VDH	-933	-930
67	VGS	-841	-828
68	VGS	-841	-930
69	VBAT1	-749	-828
70	VBAT1	-749	-930
71	VBAT1	-662	-828
72	VBAT1	-662	-930
73	AVDDIN	-570	-828
74	AVDDIN	-570	-930
75	AVDD	-478	-828
76	AVDD	-478	-930
77	CC2P	-386	-828
78	CC2P	-386	-930
79	CC2P	-299	-828
80	CC2P	-299	-930
81	CC2M	-207	-828
82	CC2M	-207	-930
83	CC2M	-120	-828
84	CC2M	-120	-930
85	CC1P	-28	-828
86	CC1P	-28	-930
87	CC1P	59	-828
88	CC1P	59	-930
89	CC1M	151	-828
90	CC1M	151	-930
91	CC1M	238	-828
92	CC1M	238	-930
93	VSS	330	-828
94	VSS	330	-930
95	VSS	417	-828
96	VSS	417	-930
97	V63N	509	-828
98	V63N	509	-930
99	V63P	601	-828
100	V63P	601	-930
101	V0N	693	-828
102	V0N	693	-930
103	V0P	785	-828
104	V0P	785	-930
105	VSYS	877	-828
106	VSYS	877	-930
107	VSYS	964	-828
108	VSYS	964	-930
109	/DAC	1064	-930
110	WSYNC	1164	-930
111	VLD	1264	-930
112	/CS	1364	-930
113	RS	1464	-930
114	/WR	1564	-930
115	/RD	1664	-930
116	DB0	1764	-930
117	DB1	1864	-930
118	DB2	1964	-930
119	DB3	2064	-930
120	DB4	2164	-930

Pad Coordinates (2)

[Unit: μm]

No.	Pin Name	X-Coordinate	Y-Coordinate
121	DB5	2264	-930
122	DB6	2364	-930
123	DB7	2464	-930
124	DB8	2564	-930
125	DB9	2664	-930
126	DB10	2764	-930
127	DB11	2864	-930
128	DB12	2964	-930
129	DB13	3064	-930
130	DB14	3164	-930
131	DB15	3264	-930
132	DB16	3364	-930
133	DB17	3464	-930
134	/RESET	3564	-930
135	RVSS2	3664	-930
136	RVSS2	3764	-930
137	RVSS2	3864	-930
138	IM3	3964	-930
139	IM2	4064	-930
140	IM1	4164	-930
141	IM0	4264	-930
142	TEST3	4364	-930
143	TEST2	4464	-930
144	EXTIN1	4564	-930
145	EXTIN2	4664	-930
146	/DCCLK	4764	-930
147	DCCLK	4864	-930
148	PEV	4964	-930
149	DCEV	5064	-930
150	DCG	5164	-930
151	EXTOUT1	5264	-930
152	EXTOUT2	5364	-930
153	VCOMD	5464	-834
154	VCOMD	5464	-930
155	VCS	5564	-834
156	VCS	5564	-930
157	VBAT2	5664	-828
158	VBAT2	5664	-930
159	XVDDIN	5764	-828
160	XVDDIN	5764	-930
161	XVDD	5864	-828
162	XVDD	5864	-930
163	CD2P	5964	-828
164	CD2P	5964	-930
165	CD2M	6064	-828
166	CD2M	6064	-930
167	CD1P	6164	-828
168	CD1P	6164	-930
169	CD1M	6264	-828
170	CD1M	6264	-930
171	VSS	6364	-828
172	VSS	6364	-930
173	TEG7	6535	-710
174	TEG8	6535	-610
175	TEG9	6535	-510
176	TEG10	6535	-410
177	TEG11	6535	-310
178	TEG12	6535	-210
179	TEG13	6535	-110
180	TEG14	6535	-10
181	TEG15	6535	90
182	ASW3	6535	190
183	ASW3	6535	290
184	ASW2	6535	390
185	ASW2	6535	490
186	ASW1	6535	590
187	ASW1	6535	690
188	ASW1	6512	823
189	ASW1	6468	930
190	ASW2	6424	823
191	ASW2	6380	930
192	ASW3	6336	823
193	ASW3	6292	930
194	FDON	6248	823
195	FDON	6204	930
196	UD	6160	823
197	UD	6116	930
198	OEV	6072	823
199	OEV	6028	930
200	FR	5984	823
201	FR	5940	930
202	CKV1	5896	823
203	CKV1	5852	930
204	CKV2	5808	823
205	CKV2	5764	930
206	STV	5720	823
207	STV	5676	930
208	DMY13	5632	823
209	OUT256	5588	930
210	OUT255	5544	823
211	OUT254	5500	930
212	OUT253	5456	823
213	OUT252	5412	930
214	OUT251	5368	823
215	OUT250	5324	930
216	OUT249	5280	823
217	OUT248	5236	930
218	OUT247	5192	823
219	OUT246	5148	930
220	OUT245	5104	823
221	OUT244	5060	930
222	OUT243	5016	823
223	OUT242	4972	930
224	OUT241	4928	823
225	OUT240	4884	930
226	OUT239	4840	823
227	OUT238	4796	930
228	OUT237	4752	823
229	OUT236	4708	930
230	OUT235	4664	823
231	OUT234	4620	930
232	OUT233	4576	823
233	OUT232	4532	930
234	OUT231	4488	823
235	OUT230	4444	930
236	OUT229	4400	823
237	OUT228	4356	930
238	OUT227	4312	823
239	OUT226	4268	930
240	OUT225	4224	823

Pad Coordinates (3)

[Unit: μm]

No.	Pin Name	X-Coordinate	Y-Coordinate
241	OUT224	4180	930
242	OUT223	4136	823
243	OUT222	4092	930
244	OUT221	4048	823
245	OUT220	4004	930
246	OUT219	3960	823
247	OUT218	3916	930
248	OUT217	3872	823
249	OUT216	3828	930
250	OUT215	3784	823
251	OUT214	3740	930
252	OUT213	3696	823
253	OUT212	3652	930
254	OUT211	3608	823
255	OUT210	3564	930
256	OUT209	3520	823
257	OUT208	3476	930
258	OUT207	3432	823
259	OUT206	3388	930
260	OUT205	3344	823
261	OUT204	3300	930
262	OUT203	3256	823
263	OUT202	3212	930
264	OUT201	3168	823
265	OUT200	3124	930
266	OUT199	3080	823
267	OUT198	3036	930
268	OUT197	2992	823
269	OUT196	2948	930
270	OUT195	2904	823
271	OUT194	2860	930
272	OUT193	2816	823
273	OUT192	2772	930
274	OUT191	2728	823
275	OUT190	2684	930
276	OUT189	2640	823
277	OUT188	2596	930
278	OUT187	2552	823
279	OUT186	2508	930
280	OUT185	2464	823
281	OUT184	2420	930
282	OUT183	2376	823
283	OUT182	2332	930
284	OUT181	2288	823
285	OUT180	2244	930
286	OUT179	2200	823
287	OUT178	2156	930
288	OUT177	2112	823
289	OUT176	2068	930
290	OUT175	2024	823
291	OUT174	1980	930
292	OUT173	1936	823
293	OUT172	1892	930
294	OUT171	1848	823
295	OUT170	1804	930
296	OUT169	1760	823
297	OUT168	1716	930
298	OUT167	1672	823
299	OUT166	1628	930
300	OUT165	1584	823
301	OUT164	1540	930
302	OUT163	1496	823
303	OUT162	1452	930
304	OUT161	1408	823
305	OUT160	1364	930
306	OUT159	1320	823
307	OUT158	1276	930
308	OUT157	1232	823
309	OUT156	1188	930
310	OUT155	1144	823
311	OUT154	1100	930
312	OUT153	1056	823
313	OUT152	1012	930
314	OUT151	968	823
315	OUT150	924	930
316	OUT149	880	823
317	OUT148	836	930
318	OUT147	792	823
319	OUT146	748	930
320	OUT145	704	823
321	OUT144	660	930
322	OUT143	616	823
323	OUT142	572	930
324	OUT141	528	823
325	OUT140	484	930
326	OUT139	440	823
327	OUT138	396	930
328	OUT137	352	823
329	OUT136	308	930
330	OUT135	264	823
331	OUT134	220	930
332	OUT133	176	823
333	OUT132	132	930
334	OUT131	88	823
335	OUT130	44	930
336	OUT129	0	823
337	DMY14	-44	930
338	DMY15	-88	823
339	DMY16	-132	930
340	DMY17	-176	823
341	DMY18	-220	930
342	DMY19	-264	823
343	DMY20	-308	930
344	DMY21	-352	823
345	DMY22	-396	930
346	DMY23	-440	823
347	DMY24	-484	930
348	DMY25	-528	823
349	DMY26	-572	930
350	DMY27	-616	823
351	DMY28	-660	930
352	DMY29	-704	823
353	OUT128	-748	930
354	OUT127	-792	823
355	OUT126	-836	930
356	OUT125	-880	823
357	OUT124	-924	930
358	OUT123	-968	823
359	OUT122	-1012	930
360	OUT121	-1056	823

Pad Coordinates (4)

[Unit: μm]

No.	Pin Name	X-Coordinate	Y-Coordinate
361	OUT120	-1100	930
362	OUT119	-1144	823
363	OUT118	-1188	930
364	OUT117	-1232	823
365	OUT116	-1276	930
366	OUT115	-1320	823
367	OUT114	-1364	930
368	OUT113	-1408	823
369	OUT112	-1452	930
370	OUT111	-1496	823
371	OUT110	-1540	930
372	OUT109	-1584	823
373	OUT108	-1628	930
374	OUT107	-1672	823
375	OUT106	-1716	930
376	OUT105	-1760	823
377	OUT104	-1804	930
378	OUT103	-1848	823
379	OUT102	-1892	930
380	OUT101	-1936	823
381	OUT100	-1980	930
382	OUT99	-2024	823
383	OUT98	-2068	930
384	OUT97	-2112	823
385	OUT96	-2156	930
386	OUT95	-2200	823
387	OUT94	-2244	930
388	OUT93	-2288	823
389	OUT92	-2332	930
390	OUT91	-2376	823
391	OUT90	-2420	930
392	OUT89	-2464	823
393	OUT88	-2508	930
394	OUT87	-2552	823
395	OUT86	-2596	930
396	OUT85	-2640	823
397	OUT84	-2684	930
398	OUT83	-2728	823
399	OUT82	-2772	930
400	OUT81	-2816	823

No.	Pin Name	X-Coordinate	Y-Coordinate
401	OUT80	-2860	930
402	OUT79	-2904	823
403	OUT78	-2948	930
404	OUT77	-2992	823
405	OUT76	-3036	930
406	OUT75	-3080	823
407	OUT74	-3124	930
408	OUT73	-3168	823
409	OUT72	-3212	930
410	OUT71	-3256	823
411	OUT70	-3300	930
412	OUT69	-3344	823
413	OUT68	-3388	930
414	OUT67	-3432	823
415	OUT66	-3476	930
416	OUT65	-3520	823
417	OUT64	-3564	930
418	OUT63	-3608	823
419	OUT62	-3652	930
420	OUT61	-3696	823
421	OUT60	-3740	930
422	OUT59	-3784	823
423	OUT58	-3828	930
424	OUT57	-3872	823
425	OUT56	-3916	930
426	OUT55	-3960	823
427	OUT54	-4004	930
428	OUT53	-4048	823
429	OUT52	-4092	930
430	OUT51	-4136	823
431	OUT50	-4180	930
432	OUT49	-4224	823
433	OUT48	-4268	930
434	OUT47	-4312	823
435	OUT46	-4356	930
436	OUT45	-4400	823
437	OUT44	-4444	930
438	OUT43	-4488	823
439	OUT42	-4532	930
440	OUT41	-4576	823

No.	Pin Name	X-Coordinate	Y-Coordinate
441	OUT40	-4620	930
442	OUT39	-4664	823
443	OUT38	-4708	930
444	OUT37	-4752	823
445	OUT36	-4796	930
446	OUT35	-4840	823
447	OUT34	-4884	930
448	OUT33	-4928	823
449	OUT32	-4972	930
450	OUT31	-5016	823
451	OUT30	-5060	930
452	OUT29	-5104	823
453	OUT28	-5148	930
454	OUT27	-5192	823
455	OUT26	-5236	930
456	OUT25	-5280	823
457	OUT24	-5324	930
458	OUT23	-5368	823
459	OUT22	-5412	930
460	OUT21	-5456	823
461	OUT20	-5500	930
462	OUT19	-5544	823
463	OUT18	-5588	930
464	OUT17	-5632	823
465	OUT16	-5676	930
466	OUT15	-5720	823
467	OUT14	-5764	930
468	OUT13	-5808	823
469	OUT12	-5852	930
470	OUT11	-5896	823
471	OUT10	-5940	930
472	OUT9	-5984	823
473	OUT8	-6028	930
474	OUT7	-6072	823
475	OUT6	-6116	930
476	OUT5	-6160	823
477	OUT4	-6204	930
478	OUT3	-6248	823
479	OUT2	-6292	930
480	OUT1	-6336	823

Pad Coordinates (5)

[Unit: μm]

No.	Pin Name	X-Coordinate	Y-Coordinate
481	DMY30	-6380	930
482	DMY31	-6424	823
483	DMY32	-6468	930
484	DMY33	-6512	823
485	DMY34	-6535	690
486	DMY35	-6535	590
487	DMY36	-6535	490
488	DMY37	-6535	390
489	DMY38	-6535	290
490	DMY39	-6535	190
491	TEG16	-6535	90
492	TEG17	-6535	-10
493	TEG18	-6535	-110
494	TEG19	-6535	-210
495	TEG20	-6535	-310
496	TEG21	-6535	-410
497	TEG22	-6535	-510
498	TEG23	-6535	-610
499	TEG24	-6535	-710

No.	Pin Name	X-Coordinate	Y-Coordinate

No.	Pin Name	X-Coordinate	Y-Coordinate

Pin Functions (1)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>OUT1~OUT256</td><td>O</td><td>Output pins for driving LCD
The direction of output can be specified using a command.</td></tr>
<tr><td>/RESET</td><td>I</td><td>Reset pin
A low on this pin causes the internal status of the JBT6K71-AS(A) to be initialized. Upon powering up the JBT6K71-AS(A), be sure to enable a reset.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select signal input pin
When pulled to the VSS level, this signal selects an index/status (000h). When pulled to the VSYS level, this signal selects a data. The selected state is written using /WR. Pulling RS to VSS terminates deep standby mode. When the serial interface is used, the RS pin must be tied to the VSS or VSYS level.</td></tr>
<tr><td>/CS</td><td>I</td><td>Chip select signal input pin
When this signal is pulled to the VSS level, the JBT6K71-AS(A) is made accessible. When it is pulled to the VSYS level, the JBT6K71-AS(A) does not accept transmitted interface signal data.</td></tr>
<tr><td>/WR (/SCL)</td><td>I</td><td>/WR signal input pin
When an 80-series MPU is selected, /WR functions as a write signal. Data is read on the rising edge of the /WR signal. When the serial interface is used, /WR functions as a synchronous clock input signal.</td></tr>
<tr><td>/RD</td><td>I</td><td>/RD signal input pin
When an 80-series MPU is selected, /RD functions as a write signal. Data is read when the /RD signal is low. When the serial interface is used, the /RD pin must be tied to the VSS or VSYS level.</td></tr>
<tr><td>DB17 (SDI)</td><td>I/O</td><td>18-bit data bus
This pin may not be used depending on the interface mode. When the serial interface is used, the DB17 pin functions as a serial data input pin. Input data is fetched on the rising edge of the SCL signal.</td></tr>
<tr><td>DB16 (SDO)</td><td>I/O</td><td>18-bit data bus
This pin may not be used depending on the interface mode. When the serial interface is used, the DB16 pin functions as a serial data output pin. Data output starts on the falling edge of the SCL signal.</td></tr>
<tr><td>DB0~DB15</td><td>I/O</td><td>18-bit data bus
These pins may not be used depending on the interface mode. When not used, the pins must be tied to the VSYS or VSS level.</td></tr>
<tr><td>VLD</td><td>I</td><td>RAM write enable signal input pin
VLD = “Low”: RAM write enabled
VLD = “High”: RAM write disabled
Every write to the RAM results in the RAM address being updated, regardless of the VLD pin state. When not using the VLD pin, tie it to the VSS level to enable RAM write. The VLD signal is also valid when the RGB interface is used. The VPL signal reverses the effects of the VLD signal.
<table>
<tr><th>VPL</th><th>/CS</th><th>VLD</th><th>RAM write</th><th>RAM address</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Enabled</td><td>Updated</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Disabled</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>*</td><td>Disabled</td><td>Maintained</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Disabled</td><td>Updated</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Enabled</td><td>Updated</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>Disabled</td><td>Maintained</td></tr>
</table>
</td></tr>
</table>

Pin Functions (2)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM0 (ID)~IM3</td><td>I</td><td>Interface mode setting input pins
These pins determine the MPU interface mode. The following table shows the relationship between the interface mode and the data bus pins used:
<table><tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU interface mode</th></tr><tr><td>VSS</td><td>VSS</td><td>VSYS</td><td>VSS</td><td>16-bit MPU interface (1), (2), (3)</td></tr><tr><td>VSS</td><td>VSS</td><td>VSYS</td><td>VSYS</td><td>8-bit MPU interface (1), (2), (3), (4)</td></tr><tr><td>VSS</td><td>VSYS</td><td>VSS</td><td>ID</td><td>Serial interface</td></tr><tr><td>VSYS</td><td>VSS</td><td>VSYS</td><td>VSS</td><td>18-bit MPU interface</td></tr><tr><td>VSYS</td><td>VSS</td><td>VSYS</td><td>VSYS</td><td>9-bit MPU interface</td></tr></table>These pins cause the number of bits used for the MPU interface to be changed. The TRI, DFM1, and DFM0 register bits in an instruction command determine the transfer format. For information on applicable DB pins, refer to “DB Assignment for the MPU Interface.”</td></tr>
<tr><td>ENABLE</td><td>I</td><td>Data enable input signal for RGB interface
ENABLE = “Low”: Accessible
ENABLE = “High”: Not accessible
The EPL signal reverses the effects of the ENABLE signal. When the ENABLE pin is not used, it must be tied to the VSS or VSYS level.
<table><tr><th>EPL</th><th>ENABLE</th><th>VLD</th><th>RAM write</th><th>RAM address</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Enabled</td><td>Updated</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Disabled</td><td>Updated</td></tr><tr><td>0</td><td>1</td><td>*</td><td>Disabled</td><td>Maintained</td></tr><tr><td>1</td><td>0</td><td>*</td><td>Disabled</td><td>Maintained</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Enabled</td><td>Updated</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Disabled</td><td>Updated</td></tr></table></td></tr>
<tr><td>VSYNC</td><td>I</td><td>Frame synchronization signal input pin
The VSPL command register setting reverses the effects of the VSYNC signal.
<table><tr><th>VSPL</th><th>VSYNC</th><th>When not used</th></tr><tr><td>0</td><td>Low Active</td><td>“VSYS” or “VSS”</td></tr><tr><td>1</td><td>High Active</td><td>“VSYS” or “VSS”</td></tr></table>When this pin is not used, it must be tied to the VSS or VDD level.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>Line synchronization signal input pin
The HSPL command register setting reverses the effects of the HSYNC signal.
<table><tr><th>HSPL</th><th>HSYNC</th><th>When not used</th></tr><tr><td>0</td><td>Low Active</td><td>“VSTYS” or “VSS”</td></tr><tr><td>1</td><td>High Active</td><td>“VSYS” or “VSS”</td></tr></table>When this pin is not used, it must be tied to the VSS or VSYS level.</td></tr>
<tr><td>/DACK</td><td>I</td><td>Input pin for DMA function
When this signal is pulled to the VSS level, the DMA function is enabled.</td></tr>
</table>

Pin Functions (3)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>DOTCLK</td><td>I</td><td>Dot clock signal input pin
The DPL command register setting reverses the effects of the DOTCLK signal.
<table><tr><th>DPL</th><th>DOTCLK</th><th>When not used</th></tr><tr><td>0</td><td>Fetch data when DOTCLK is low</td><td>“VSYS” or “VSS”</td></tr><tr><td>1</td><td>Fetch data when DOTCLK is high</td><td>“VSYS” or “VSS”</td></tr></table>When this pin is not used, it must be tied to the VSS or VSYS level.</td></tr>
<tr><td>PD0~PD17</td><td>I</td><td>RGB data bus input pin
The RIM3 and RIM2 command register settings vary the transfer format.
<table><tr><th>RIM3</th><th>RIM2</th><th>Transfer format</th></tr><tr><td>0</td><td>0</td><td>1 transfer of 18 bits</td></tr><tr><td>0</td><td>1</td><td>1 transfer of 16 bits</td></tr><tr><td>1</td><td>0</td><td>3 transfers of 6 bits</td></tr><tr><td>1</td><td>1</td><td>Setting prohibited</td></tr></table>When this pin is not used, it must be tied to the VSS or VSYS level.</td></tr>
<tr><td>WSYNC</td><td>O</td><td>Blanking start pulse output pin
This pin outputs a pulse which is 1H length from the starting point of blanking term (FP).</td></tr>
<tr><td>OSC1</td><td>I/O</td><td>Oscillator pin (1)
For information on how to use the oscillator, refer to “Oscillator.”</td></tr>
<tr><td>OSC2</td><td>—</td><td>Oscillator pin (2)
For information on how to use the oscillator, refer to “Oscillator.”</td></tr>
<tr><td>EXTIN1
EXTIN2</td><td>I</td><td>Input pins for LCD driving signals
These pins input external signal for LCD driving, and level translating signal output from EXTOUT1/2 pins.</td></tr>
<tr><td>EXTOUT1
EXTOUT2</td><td>O</td><td>Output pins for LCD driving signals
These pins output level translating signal which is external input signal from EXTIN1/2 pins</td></tr>
</table>

Pin Functions (4)

Pin Name	I/O	Description
ASW1~ASW3	O	R/G/B switching control signal output pins
STV	O	Frame start pulse output pin for LTPS
CKV1, CKV2	O	Gate shift clock output pins for LTPS
FR	O	AC signal output pin for LTPS
OEV	O	Gate control signal output pin for LTPS
DCCLK /DCCLK	O	Booster control clock signal for LTPS Outputs as 2-phase clock signal for voltage booster.
U/D	O	Gate scan switching signal output pin for LTPS
FDON	O	Power-up sequence output pin (1) for driving LCD Output varies with register command settings.
PEV	O	Power-up sequence output pin (2) for driving LCD Output varies with register command settings.
DCG	O	LCD discharge signal output pin Output varies with register command settings.
DCEV	O	Booster control clock enable signal for LTPS

Pin Functions (5)

Pin Name	I/O	Description
VSYS	—	Interface power supply pin Supply the interface system power to this pin.
VBAT1, VBAT2	—	Analog circuit power supply pin Supply the DC-DC converter power to this pin from a battery. The condition VBAT ≥ VSYS must be met.
VSS	—	Logic power supply pin GND pin for the logic system power supply.
RVSS1, RVSS2	—	Logic power supply pin GND pin for the logic system power supply.
VREF	O	Output pin for on-chip reference power supply It outputs 1.5V (typ.) for internal logic circuit. Usually, connect this pin to the VREFIN pin. When using the on-chip reference power supply, connect a stabilizing capacitor (1 μF recommended) to this pin.
VREFIN	I	Input pin for on-chip reference power supply Usually, connect this pin to the VREFI pin. When not using the on-chip reference power supply, connect an external power supply to this pin. VREFIN = 1.5 V ±10 mV
DVREG	O	Internal logic regulator output pin
DVDD	I	Internal logic regulator feedback input pin
RVREG	O	Display RAM regulator output pin
RVDD	I	Display RAM regulator feedback input pin
CC1P/CC2P CC1M/CC2M	I/O	AVDD Booster capacitor pins Usually, connect a capacitor for booster between CC1P and CC1M, and connect a capacitor between CC2P and CC2M , too (1 μF recommended). When not using booster, leave this pin open.
AVDD	O	AVDD Booster output pin Supply the LCD driving power to this pin.
AVDDIN	I	AVDD Booster feedback input pin
CD1P/CD2P CD1M/CD2M	I/O	XVDD Booster capacitor pins Usually, connect a capacitor for booster between CD1P and CD1M, and connect a capacitor between CD2P and CD2M , too (1 μF recommended). When not using booster, leave this pin open.
XVDD	O	XVDD Booster output pin
XVDDIN	I	XVDD Booster feedback input pin
VGM	O	Gamma circuit output pin Gray scale voltage level for γ output varies with register command settings.
VDH	I	Gamma circuit power supply pin
VGS	I	Resistor connection pin for generating gray scale voltage This pin determines the reference level for the gray scale voltage generator. When using the source driver to adjust the level for each panel, connect a variable resistor to this pin and adjust the resistance.
VCS	O	VCS voltage output pin for LTPS
VCOMD	O	VCOMD regulator output pin for LTPS When using VCOMD, connect a stabilizing capacitor (1 μF recommended) to this pin.

Pin Functions (6)

Pin Name	I/O	Description
V0P, V63P	O	On-chip operational amplifier output pin (1) To this pin, connect a capacitor for maintaining the power for the on-chip positive operational amplifier.
V0N, V63N	O	On-chip operational amplifier output pin (2) To this pin, connect a capacitor for maintaining the power for the on-chip negative operational amplifier.
AMPBR	I	Bias setting pin for on-chip operational amplifier When an external resistor is connected to this pin, it determines the bias current for the on-chip operational amplifier. Normally, Connect a 100kΩ resistor. Resistor fitting by module evaluation.
TEST2, TEST3	I	Test pin Usually, connect to GND.
TEG1-TEG24		TEG pin for Toshiba. Need to open.
DMY1 - DMY39		Dummy pin. Not tie to internal JBT6K71-AS(A). Normally tie to open.

Functional Specifications and Operational Description

(1) MPU interface controller

The JBT6K71-AS(A) has a wide range of interface modes, including the 18-/16-/9-/8-bit bus MPU interface and clock synchronous serial (SPI) interface. A combination of IM3-IM0 pin settings and command-based control selects an interface.

The JBT6K71-AS(A) has an index register, display data write register, and display data read register. The 16-bit index register temporarily stores settings for each mode. The display data write register is used to temporarily store data to be written to the display RAM. The 18-bit display data read register temporarily stores data from the display RAM so that a sequence of data can be read continuously. The first data read from the register is, however, invalid. The second and subsequent data should be used as valid data.

Table 1 Register selection (MPU interface)

80-series MPU		RS	Operation
/WR	/RD		
0	1	0	Write an index to the IR.
1	0	0	Read internal device code (000h) data.
0	1	1	Write data to the control register and GRAM through the input register.
1	0	1	Read data from the GRAM through the output register.

Table 2 Register selection (clock synchronous serial interface)

Start Byte		Operation
R/W bit	RS bit	
0	0	Write an index to the IR.
1	0	Read internal device code (000h) data.
0	1	Write data to the control register and display RAM through the input register.
1	1	Read data from the display RAM through the output register.

(2) RGB interface controller

The JBT6K71-AS(A) can directly control RGB data from the graphic controller to support moving images. It can manage still and moving image data simultaneously by using two functional paths to handle data fetched from the RGB interface: one path to write the data to the display RAM and the other to transfer the data directly to the LCD.

The JBT6K71-AS(A) can be connected to a wide range of graphic controllers, including 18-bit, 16-bit, and 6-bit data buses.

(3) Oscillator

The JBT6K71-AS(A) incorporates a CR oscillator.

(4) Display RAM

The display RAM consists of 256 (output) × RGB (18 bits) × 320 lines = 1,474,560 bits.

(5) OSD RAM

The OSD RAM consists of 256 (output) × {RGB (17 bits) + Flag (1bit)}× 16 lines × 2 = 147,456 bits.

(6) Power supply management / LCD driving signal buffer

The JBT6K71-AS(A) can control the LCD built-in power supply circuit. The JBT6K71-AS(A) can also operate as a master chip for the LCD module by managing control signals for the LCD built-in gate circuit.

(7) Regulator

The JBT6K71-AS(A) incorporates a regulator for generating internal system power. It reduces the externally supplied supply voltage for low-power operation. When the JBT6K71-AS(A) uses less than regulated voltage, please turn off using a command, and please connect an external power supply to this pin.

(8) Bit operation circuit

The bit operation circuit processes display RAM data from the MPU and transfers the results to the display RAM. The circuit can be turned on or off using a command.

(9) Output circuit

The JBT6K71-AS(A) has an output circuit consisting of 256 source driver outputs. Once a single line of data has been accumulated, the ASW signal outputs RGB data in three steps: R data, G data, and then B data. The output circuit supports an instruction command for changing the direction in which the output is shifted according to the hosting cellular phone.

(10) Decoder

The decoder selects a gray scale voltage to be used for the data latched from the display RAM.

(11) Timing signal generator

The timing signal generator generates signals for the operation of internal circuits, including display RAM and gate synchronization signals. Timing signals operate internally and are asynchronous to signals from the MPU. They do not affect display RAM write operation. The timing generator also generates control signals used to operate the LCD built-in power supply circuit and gate driving circuit.

(12) Index register

The 16-bit index register stores an index address. It distributes instruction command data by index to control command registers.

(13) Command registers

The 16-bit command registers store instruction control data. The JBT6K71-AS(A) writes data to a command register corresponding to the index specified with the index register. The command registers also store instruction data for the LCD built-in power supply circuit.

(14) Address counter

The address counter controls an X-address specified with a command register.

(15) Y-address counter/decoder

The Y-address counter/decoder returns an address specified with a command register in response to the Y-address (page address).

(16) Latch circuits (1) / (2)

The latch circuits are temporary storages controlled by the timing signal generator. They manipulate display data from the display RAM and the RGB interface and transfer the results to the output circuit.

(17) Gray scale voltage generator

The JBT6K71-AS(A) generates gray scale voltages, the gray scale voltage generator creates 64 levels of voltage. For information on the output voltage table, refer to “Gray Scale Data Assignment.”

(18) Gamma adjustment circuit

The JBT6K71-AS(A) incorporates a gamma adjustment circuit that can manipulate a gamma curve to support different types of LCD. By controlling a gamma curve using an instruction command, the JBT6K71-AS(A) can always use an optimum output voltage curve for gray scale data.

Summary of Instructions

Major Category (Index)	Minor Category		Upper Bits								Lower Bits							
	Index	Command Name	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
—	—	Index	*	*	*	*	*	IX10	IX9	IX8	IX7	IX6	IX5	IX4	IX3	IX2	IX1	IX0
0**h	000h	Oscillation setting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSC
	001h	Driver output control setting	0	0	0	0	0	0	0	SS	0	0	NL5	NL4	NL3	NL2	NL1	NL0
	002h	LCD driving signal setting	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
	003h	Entry mode	TRI	DFM1	DFM0	BGR	IF18	0	0	HWM	0	0	ID1	ID0	AM	0	0	0
	004h~ 005h	Non registers																
	006h	Horizontal valid width setting	HWS7	HWS6	HWS5	HWS4	HWS3	HWS2	HSW1	HWS0	0	0	0	HBP4	HBP3	HBP2	HBP1	HBP0
	007h	Display mode (1)	COL1	COL0	0	0	0	VLE1	VLE0	SPT	PT1	PT0	0	NWB	0	REV	0	0
	008h	Display mode (2)	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
	009h	Display mode (3)	0	0	0	0	0	0	0	0	RSE	0	RSB1	RSB0	RSH3	RSH2	RSH1	RSH0
	00Ah	Non register																
	00Bh	Display mode (4)	0	0	0	0	0	0	0	0	XYON	X2	Y2	0	0	0	0	SIP
	00Ch	External display signal setting (1)	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
	00Dh	FR frequency adjustment setting	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
	00Eh	External display signal setting (2)	0	0	0	0	0	0	DIVE1	DIVE0	RTNE7	RTNE6	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
	00Fh	External display signal setting (3)	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	VPL	EPL	DPL
	010h~ 011h	Non registers																
	012h	LTPS control setting (1)	0	0	0	0	CLWI3	CLWI2	CLWI1	CLWI0	0	0	0	0	0	0	CLTI1	CLTI0
	013h	LTPS control setting (2)	0	0	0	0	0	0	OEVBI1	OEVBI0	0	0	0	0	0	0	OEVFI1	OEVFI0
	014h	LTPS control setting (3)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SHI1	SHI0
	015h	LTPS control setting (4)	0	0	CKBI1	CKBI0	0	0	CKFI1	CKFI0	0	0	0	0	0	0	0	0
	016h~ 017h	Non registers																
	018h	LTPS control setting (5)	0	0	CLWE5	CLWE4	CLWE3	CLWE2	CLWE1	CLWE0	0	0	0	0	CLTE3	CLTE2	CLTE1	CLTE0
	019h	LTPS control setting (6)	0	0	0	0	OEVBE3	OEVBE2	OEVBE1	OEVBE0	0	0	0	0	OEVFE3	OEVFE2	OEVFE1	OEVFE0
	01Ah	LTPS control setting (7)	0	0	0	0	0	0	0	0	0	0	0	0	SHE3	SHE2	SHE1	SHE0
	01Bh	LTPS control setting (8)	CKBE3	CKBE2	CKBE1	CKBE0	CKFE3	CKFE2	CKFE1	CKFE0								
	01Ch	Amplifier capability setting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ABSW1	ABSW0
	01Dh	Mode setting														DSTB		STB
	01Eh	Power-off line count setting	0	0	0	0	0	0	0	0	0	0	0	0	POFH3	POFH2	POFH1	POFH0
	01Fh~ 0FFh	Non registers																
1**h	100h	Display control	PO	CONT	PEV	DCEV	UD	CON	OEV	VCS	ASW1	ASW0	D1	D0	FR	FDON	DCG	VGAM
	101h	Auto management control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AUTO
	102h	Power supply control (1)	0	0	0	0	VCD3	VCD2	VCD1	VCD0	VCS3	VCS2	VCS1	VCS0	VGM3	VGM2	VGM1	VGM0
	103h	Power supply control (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	XVD2	XVD1	XVD0
	104h	Power supply control (3)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BXV	BAV
	105h	Power supply control (4)	0	0	0	0	0	0	DCW1	DCW0	0	0	CK31	CK30	CK21	CK20	CK11	CK10
	106h~ 107h	Non registers																
	108h	External polarity control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EXTC2	EXTC1
	109h~ 1FFh	Non registers	Setting prohibited (if set inadvertently, should be reset.)															
2**h	200h	RAM address setting (1)	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
	201h	RAM address setting (2)	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
	202h	Data read/write	RAM write data/read data * Bit assignment varies with the selected interface.															
	203h	Graphic operation (1)	0	0	WM11	WM10	WM9	WM8	WM7	WM6	0	0	WM5	WM4	WM3	WM2	WM1	WM0
	204h	Graphic operation (2)	0	0	0	0	0	0	0	0	0	0	WM17	WM16	WM15	WM14	WM13	WM12
	205h~ 2FFh	Non registers																
3**h	300h	Gray scale setting (1)	0	0	0	0	0	PK12	PK11	PK10	0	0	0	0	0	PK02	PK01	PK00
	301h	Gray scale setting (2)	0	0	0	0	0	PK32	PK31	PK30	0	0	0	0	0	PK22	PK21	PK20
	302h	Gray scale setting (3)	0	0	0	0	0	PK52	PK51	PK50	0	0	0	0	0	PK42	PK41	PK40
	303h	Gray scale setting (4)	0	0	0	0	0	PR12	PR11	PR10	0	0	0	0	0	PR02	PR01	PR00
	304h	Gray scale setting (5)	0	0	0	0	0	VR12	VR11	V10	0	0	0	0	0	VR02	VR01	VR00
	305h	Blue offset setting	0	0	0	0	0	0	0	BLON	0	BUP2	BUP1	BUP0	0	BOFS2	BOFS1	BOFS0
	306h~ 3FFh	Non registers																
4**h	400h	Vertical scroll control (1)	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	401h	Vertical scroll control (2)	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	402h	First screen drive position (1)	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	403h	First screen drive position (2)	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	404h	Second screen drive position (1)	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	405h	Second screen drive position (2)	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	406h	Horizontal RAM address location (1)	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	407h	Horizontal RAM address location (2)	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	408h	Vertical RAM address location (1)	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	409h	Vertical RAM address location (2)	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
	40Ah~ 4FFh	Non registers																
5**h	500h	OSD feature ON/OFF	0	0	0	0	0	0	0	OSDW	0	0	0	0	0	0	0	OSDON
	501h~ 503h	Non registers																
	504h	OSD screen 1 start address	0	0	0	0	0	0	0	ST18	ST17	ST16	ST15	ST14	ST13	ST12	ST11	ST10
	505h	OSD screen 2 start address	0	0	0	0	0	0	0	ST28	ST27	ST26	ST25	ST24	ST23	ST22	ST21	ST20
	506h~ 5FFh	Non registers																
6**h	600h~ 6FFh	Non operation	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
7**h	700h~ 7FFh	Non registers	Setting prohibited (if set inadvertently, should be reset.)															

Initial data after the Deep St/by

Minor Category		USB								LSB							
Index	Command Name	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
000h	Oscillation setting																0
001h	Driver output control setting								0			1	0	0	1	1	1
002h	LCD driving signal setting							0									
003h	Entry mode	0	0	0	0	0			0			1	1	0			
006h	Horizontal valid width setting	1	1	1	1	1	1	1	1				0	0	0	1	0
007h	Display mode (1)	0	0				0	0	0	0	0		0		0		
008h	Display mode (2)	0	0	0	0	1	0	0	0					1	0	0	0
009h	Display mode (3)									0		0	0	0	0	0	1
00Bh	Display mode (4)									0	0	0					0
00Ch	External display signal setting (1)								0			0	0			0	0
00Dh	FR frequency adjustment setting							0	0				1	0	0	0	0
00Eh	External display signal setting (2)							1	0	0	0	1	0	0	0	0	1
00Fh	External display signal setting (3)												0	0	0	0	0
012h	LTPS control setting (1)					0	0	0	1							0	0
013h	LTPS control setting (2)							0	0							0	0
014h	LTPS control setting (3)															0	0
015h	LTPS control setting (4)			0	0			0	0								
018h	LTPS control setting (5)			0	0	0	0	0	1					0	0	0	0
019h	LTPS control setting (6)					0	0	0	0					0	0	0	0
01Ah	LTPS control setting (7)													0	0	0	0
01Bh	LTPS control setting (8)	0	0	0	0	0	0	0	0								
01Ch	Amplifier capability setting															1	0
01Dh	Mode setting														1		0
01Eh	Power-off line count setting													1	0	1	0
100h	Display control	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
101h	Auto management control																0
102h	Power supply control (1)					0	0	0	0	0	0	0	0	0	0	0	0
103h	Power supply control (2)			0	0										0	0	0
104h	Power supply control (3)															0	0
105h	Power supply control (4)							0	0			0	0	0	0	0	0
108h	External polarity control															0	0
200h	RAM address setting (1)									0	0	0	0	0	0	0	0
201h	RAM address setting (2)								0	0	0	0	0	0	0	0	0
203h	Graphic operation (1)			0	0	0	0	0	0			0	0	0	0	0	0
204h	Graphic operation (2)											0	0	0	0	0	0
300h	Gray scale setting (1)						1	0	0						0	1	1
301h	Gray scale setting (2)						0	1	1						1	0	0
302h	Gray scale setting (3)						1	0	0						0	1	1
303h	Gray scale setting (4)						0	1	1						0	1	1
304h	Gray scale setting (5)						0	0	1						0	0	1
305h	Blue offset setting								0		0	0	0		0	0	0
400h	Vertical scroll control (1)								0	0	0	0	0	0	0	0	0
401h	Vertical scroll control (2)								0	0	0	0	0	0	0	0	0
402h	First screen drive position (1)								0	0	0	0	0	0	0	0	0
403h	First screen drive position (2)								1	0	0	1	1	1	1	1	1
404h	Second screen drive position (1)								0	0	0	0	0	0	0	0	0
405h	Second screen drive position (2)								1	0	0	1	1	1	1	1	1
406h	Horizontal RAM address location (1)									0	0	0	0	0	0	0	0
407h	Horizontal RAM address location (2)									1	1	1	1	1	1	1	1
408h	Vertical RAM address location (1)								0	0	0	0	0	0	0	0	0
409h	Vertical RAM address location (2)								1	0	0	1	1	1	1	1	1
500h	OSD feature ON/OFF								0								0
504h	OSD screen 1 start address								0	0	0	0	0	0	0	0	0
505h	OSD screen 2 start address								0	0	0	0	1	0	0	0	0

Details of Instructions

The JBT6K71-AS(A) requires an index to be selected before writing data to a register. Registers are divided into major and minor categories. A major category specifies a block while a minor category specifies details for the block, thus facilitating modification to register data.

The JBT6K71-AS(A) has the following major categories of instructions:

(1) Display setting instructions
(2) JBT6K71-AS(A) power supply setting instructions
(3) Data access (write/read) instructions
(4) Gray scale setting instructions
(5) Window setting instructions
(6) OSD setting instructions

These instructions are asynchronous to the JBT6K71-AS(A) internal clock, requiring no wait cycles. Because the writing of instruction data does not interfere with the MPU processing, instructions can be handled smoothly and efficiently. The following describes details of instruction settings.

(1) Index setting

Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Index	*	*	*	*	*	IX10	IX9	IX8	IX7	IX6	IX5	IX4	IX3	IX2	IX1	IX0

This code is specifies the address (index) of the register to be selected. Bits IX10 to IX8 specify a major category while bits IX7 to IX0 specify a minor category. Write a register number as binary (“00000000000” to “11111111111”) before writing the data to be written to the register (register data write). Registers 700h (“11100000000”) to 7FFh (“11111111111”) are setting-prohibited. Do not specify an address in that area.

(2) Oscillation setting

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
000h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Specify this command while oscillation is stopped in sleep mode. Once sleep mode has been terminated, the on-chip CR oscillator starts operating, but it requires approximately 10ms to stabilize oscillation. This command should, therefore, be set at the beginning of the initial setting sequence.

If RS = “1”, /WR = “1”, and /RD = “0” are specified after the Index is set to 000h, code of “71**”h will be read.

Read	0	1	1	1	0	0	0	1	*	*	*	*	*	*	*	*

(3) Driver output control setting

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
001h	0	0	0	0	0	0	0	SS	0	0	NL5	NL4	NL3	NL2	NL1	NL0

This register specifies the direction in which the source driver output is shifted and the number of lines to be displayed on the LCD.

SS: Selects the direction in which the source driver output is shifted.
SS = 0: From OUT1 to OUT256
SS = 1: From OUT256 to OUT1

SS	Relationship between output shift direction
0	OUT1, OUT2, OUT3 --------> OUT254, OUT255, OUT256
1	OUT256, OUT255, OUT254 ------> OUT3, OUT2, OUT1

NL5-0: Adjusts the number of lines to be driven on the LCD in eight line units, as shown in the table. This setting determines the size of the display RAM. Note that it changes the way the address counter is updated (auto-increment/decrement).

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	Number of Driven LCD Lines
0	0	0	0	0	0	Setting prohibited	Setting prohibited
0	0	0	0	0	1	256 × 16 dots	16
0	0	0	0	1	0	256 × 24 dots	24
0	0	0	0	1	1	256 × 32 dots	32
0	0	0	1	0	0	256 × 40 dots	40
0	0	0	1	0	1	256 × 48 dots	48
0	0	0	1	1	0	256 × 56 dots	56
1	0	0	0	0	1	256 × 272 dots	272
1	0	0	0	1	0	256 × 280 dots	280
1	0	0	0	1	1	256 × 288 dots	288
1	0	0	1	0	0	256 × 296 dots	296
1	0	0	1	0	1	256 × 304 dots	304
1	0	0	1	1	0	256 × 312 dots	312
1	0	0	1	1	1	256 × 320 dots	320

When OSD command is off, the JBT6K71-AS(A) can use OSD RAM area for graphic display. So, display area size expands 256 x 320 dots to 256 x 352 dots.

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	Number of Driven LCD Lines
1	0	1	0	0	0	256 × 328 dots	328
1	0	1	0	0	1	256 × 336 dots	336
1	0	1	0	1	0	256 × 344 dots	344
1	0	1	0	1	1	256 × 352 dots	352
1	0	1	1	0	0	Setting prohibited	

(4) LCD driving signal setting

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
002h	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0

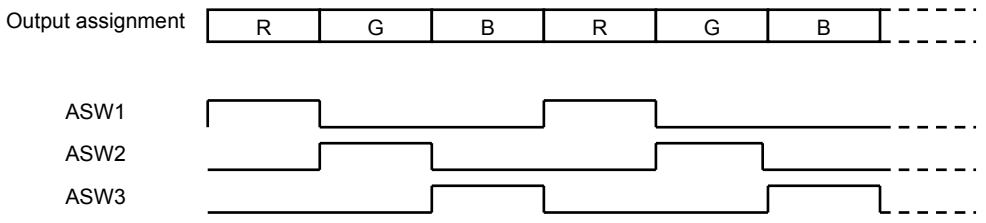
This register selects either a frame AC waveform or line AC waveform. Clearing B/C to 0 specifies a frame AC waveform, with which AC conversion is performed in screen units to drive the LCD. Setting B/C to 1 specifies AC conversion in line units.

(5) Entry mode

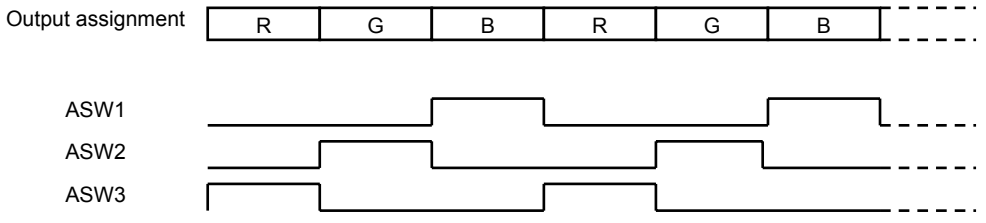
Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
003h	TRI	DFM1	DFM0	BGR	IF18	0	0	HWM	0	0	ID1	ID0	AM	0	0	0

This register specifies the interface format and the types of high-speed RAM write and address counter.

BGR: Converts the sequence of 18-bit data transferred from the display RAM to the output circuit, from (R) (G) (B) to (B) (G) (R).
The data is converted by changing the order of pulses in the ASW1-ASW3 LCD control signals.



When BGR = “0”

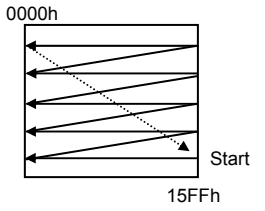
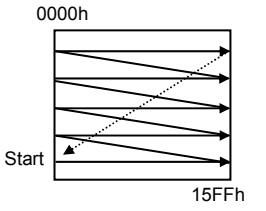
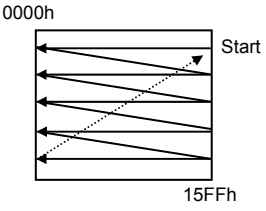
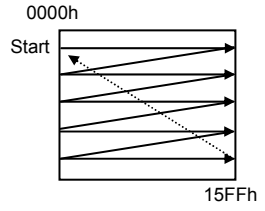
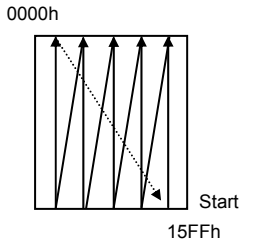
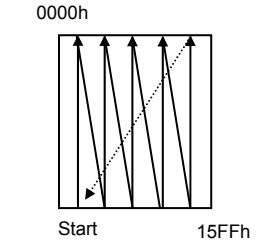
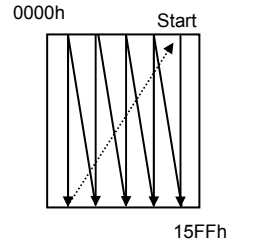
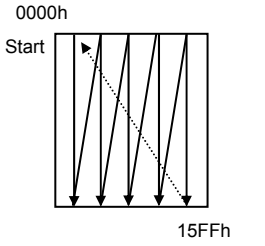


When BGR = “1”

HWM: Specifies the high-speed RAM write mode. Setting HWM to "1" enables high-speed RAM write, which stores a specified amount of data temporarily and writes the data in a batch. Note that, in high-speed RAM write mode, batch display RAM write is not performed until N bytes of data are written. For details, refer to "High-Speed RAM Write Mode."
When using the serial interface, need setting the HWM = "0".

ID1/0: Specifies the direction in which the address is incremented or decremented when writing data to the display RAM. In combination with the "AM" register bit, the ID1 and ID0 bits specify eight types of automatic address increment/decrement. For details, see the table below.

AM: Specifies the direction in which the address is updated when writing data to the display RAM. When AM = "0", the address is updated in the horizontal direction; it is incremented or decremented as specified with the ID1/ID0 register bits. When AM = "1", the address is updated in the vertical direction; it is incremented or decremented as specified with the ID1/ID0 register bits. When window addressing is used, the address is automatically updated according to the states of the AM, ID1, and ID0 register bits.

	ID1-0 = "00" Horizontal: Decrement Vertical: Decrement	ID1-0 = "01" Horizontal: Increment Vertical: Decrement	ID1-0 = "10" Horizontal: Decrement Vertical: Increment	ID1-0 = "11" Horizontal: Increment Vertical: Increment
AM = "0" Horizontal				
AM = "1" Vertical				

Note: When window addressing is used, these register bits are only valid for display RAM addresses within the window.

TRI: Specifies the data transfer rate for the MPU interface.

DFM1/0: Specifies bit assignment for the transfer rate specified with the TRI command bit.

IM3	IM2	IM1	IM0	TRI	DFM1	DFM0	Interface Mode	Number of Data Transfers	Bit Assignment	Display Data Bits
0	0	1	0	0	0	0	16-bit mode (1)	1 time	16 bits	16 bits
0	0	1	0	0	0	1	16-bit mode (2)	2 times	16 bits + 2 bits	18 bits
0	0	1	0	0	1	0	16-bit mode (3)	2 times	2 bits + 16 bits	18 bits
0	0	1	1	0	0	0	8-bit mode (1)	2 times	8 bits + 8 bits	16 bits
0	0	1	1	1	0	1	8-bit mode (2)	3 times	8 bits + 8 bits + 2 bits	18 bits
0	0	1	1	1	1	0	8-bit mode (3)	3 times	2 bits + 8 bits + 8 bits	18 bits
0	0	1	1	1	1	1	8-bit mode (4)	3 times	6 bits + 6 bits + 6 bits	18 bits
0	1	0	ID	*	*	*	Serial mode	2 times	8 bits + 8 bits	16 bits
1	0	1	0	*	*	*	18-bit mode	1 time	18 bits	18 bits
1	0	1	1	*	*	*	9-bit mode	2 times	9 bits + 9 bits	18 bits

For information on how the interface mode is determined from the combination of the IM3 to IM0 pin settings and TRI and DFM1/0 register settings, refer to "Interface Mode Settings."

JBT6K71-AS(A) have different the color variations by interface mode.

IM3	IM2	IM1	IM0	TRI	DFM1	DFM0	Display Data Bits	Color variations	note
0	0	1	0	0	0	0	16 bits	65,536 colors	Supply at 2bit color data
0	0	1	0	0	0	1	18 bits	262,144 colors	
0	0	1	0	0	1	0	18 bits	262,144 colors	
0	0	1	1	0	0	0	16 bits	65,536 colors	Supply at 2bit color data
0	0	1	1	1	0	1	18 bits	262,144 colors	
0	0	1	1	1	1	0	18 bits	262,144 colors	
0	0	1	1	1	1	1	18 bits	262,144 colors	
0	1	0	ID	*	*	*	16 bits	65,536 colors	Supply at 2bit color data
1	0	1	0	*	*	*	18 bits	262,144 colors	
1	0	1	1	*	*	*	18 bits	262,144 colors	

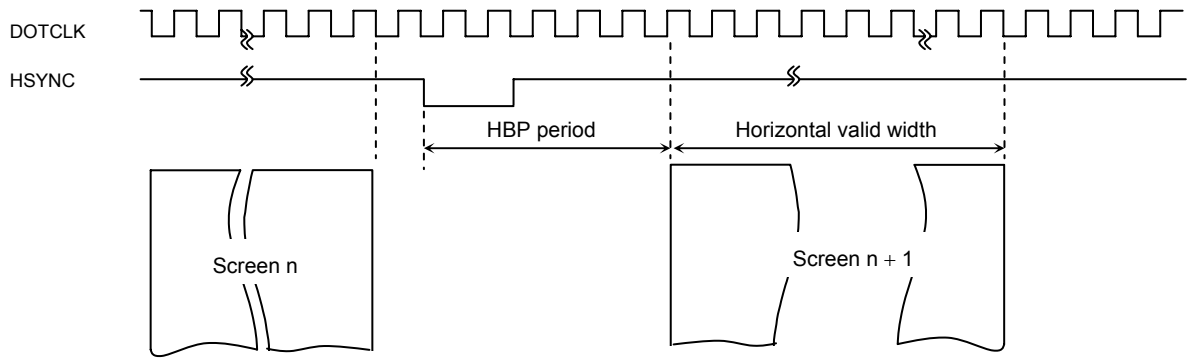
IF18: Changed the color variation for 16-bit mode at MPU interface.

IF18	COL1/0	I/F mode	Display color	Position the OSD flag bit	Position the SIP flag bit
0	0/0	16bit	65,536	G	G
	(262k)	18bit	262,144	B	B
	0/1	16bit	65,536	G	G
	(65k)	18bit	65,536	B	B
1	0/0	16bit	262,144	B	B
	(262k)	18bit	262,144	B	B
	0/1	16bit	65,536	B	B
	(65k)	18bit	65,536	B	B

(6) Horizontal valid width setting

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
006h	HWS7	HWS6	HWS5	HWS4	HWS3	HWS2	HWS1	HWS0	0	0	0	HBP4	HBP3	HBP2	HBP1	HBP0

This register specifies the horizontal screen start position in terms of the number of clock cycles. Set this register to synchronize horizontally with the controller. Refer to the following tables for how to set the register:



Setting a horizontal valid width

HWS7	HWS6	HWS5	HWS4	HWS3	HWS2	HWS1	HWS0	Number of DOTCLK Cycles
0	0	0	0	0	0	0	0	Setting prohibited
⋮								⋮
0	0	1	1	1	1	1	1	Setting prohibited
0	1	0	0	0	0	0	0	64
0	1	0	0	0	0	0	1	65
⋮								⋮
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Setting the clock cycles during the back porch period

HBP4	HBP3	HBP2	HBP1	HBP0	Number of DOTCLK Cycles
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	2
0	0	0	1	1	3
⋮					⋮
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

(7) Display mode (1)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
007h	COL1	COL0	0	0	0	VLE2	VLE1	SPT	PT1	PT0	0	NBW	0	REV	0	0

This register specifies the status of normal display, including the display color, scroll feature, and color reversal.

COL1-0: Selects the display color mode. This 2-bit field allows software to increase or reduce the number of colors at one time. Three color modes are available: 262K, 65K, and eight colors. These command translations are valid after next frame.

COL1	COL0	Display Colors
0	0	262,144
0	1	65,536
1	0	Setting prohibited
1	1	8

When selecting eight-color mode, refer to “Selecting a Gray Scale Level in Eight-Color Mode.”

VLE1-0: Specifies the location in which the scroll feature is used. When VLE1 = “1”, vertical scroll is performed on the first screen. When VLE2 = “1”, vertical scroll is performed on the second screen. This feature cannot be used with the RGB interface. When using the RGB interface, need the VLE2/1 = L/L.

VLE2	VLE1	Second Screen	First Screen
0	0	Fixed display	Fixed display
0	1	Fixed display	Scrollable display
1	0	Scrollable display	Fixed display
1	1	Scrollable display	Scrollable display

SPT: When SPT = “1”, the LCD is driven as two split screens. For details, refer to “Split Screens.” This feature cannot be used with the RGB interface. When using the RGB interface, need the SPT = “L”.

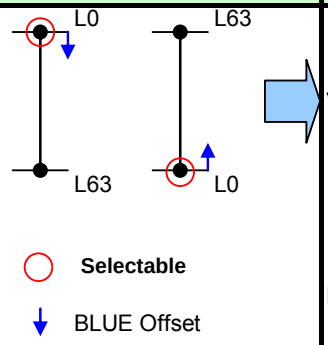
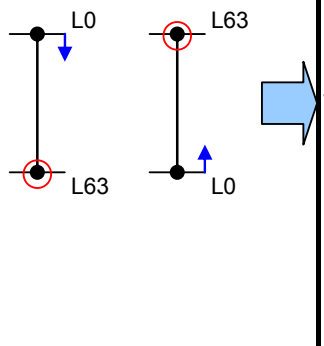
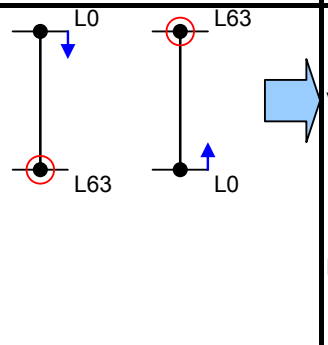
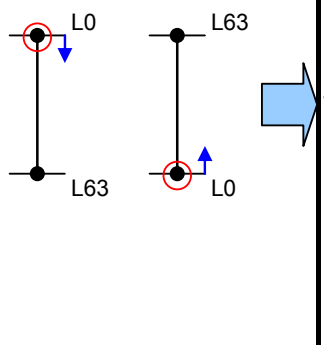
NBW: The FR data and REV data transfer for kind of display condition.

REV: When REV = “1”, displayed data is reversed (negative or positive). This feature reverses the display only by modifying register data, without having to modify actual display data stored in the display RAM. The settings of PT1 and PT0, however, take precedence for source output in the front and back porches or during the blank period for two split screen display.

PT1-0: Specifies the status of source output when driving a non-display area in partial display mode.

PT1	PT0	Source Output in Non-display Area				ASW Output in Non-display Area	The refresh function for Non-display Area
		NBW=0		NBW=1			
		Positive	Negative	Positive	Negative		
0	0	L63	L63	L0	L0	Normal drive	Invalid
0	1	L63	L63	L0	L0	“Low”	Valid
1	0	VSS		VSS		“Low”	Valid
1	1	Hi-Z		Hi-Z		“Low”	Valid

Relation of NBW, REV and display data

DATA	REV	GAM POSI / NEGA	007h(IB4) NBW="0"	007h(IB4) NBW="1"
			FR	FR
3F	1		VSIG PT,D1-0	VSIG PT,D1-0
00	1		VSIG PT,D1-0	VSIG PT,D1-0
3F	0		VSIG PT,D1-0	VSIG PT,D1-0
00	0		VSIG PT,D1-0	VSIG PT,D1-0

(8) Display mode (2)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
008h	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

This register specifies blanking periods to be added before and after the display screen. As shown below, blanking periods are inserted into the vertical synchronization signal: a back porch before the display area and a front porch after the display area. Note that the blanking periods vary the frame frequency.

When specifying blanking periods, ensure that the following conditions are satisfied:

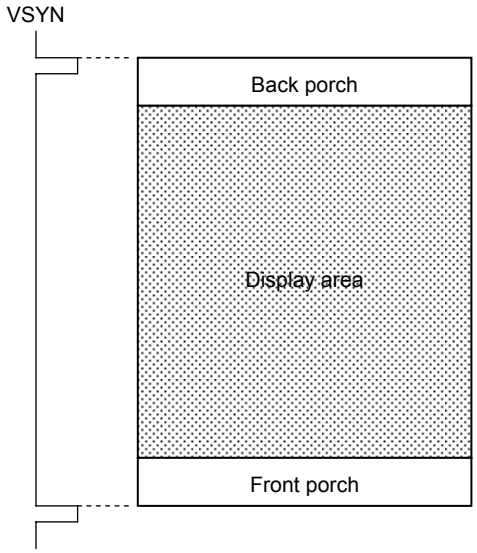
(1) Front porch (FP) + back porch (BP) ≥ 4 lines

(2) Front porch (FP) ≥ 2 lines

(3) Back porch (BP) ≥ 2 lines

FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0	Number of Front Porch Lines
0	0	0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	0	0	1	Setting prohibited
0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	1	1	3 lines
0	0	0	0	0	1	0	0	4 lines
0	0	0	0	0	1	0	1	5 lines
				⋮				⋮
1	1	1	1	1	1	0	0	252 lines
1	1	1	1	1	1	0	1	253 lines
1	1	1	1	1	1	1	0	254 lines
1	1	1	1	1	1	1	1	Setting prohibited

BP3	BP2	BP1	BP0	Number of Back Porch Lines
0	0	0	0	Setting prohibited
0	0	0	1	Setting prohibited
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Setting prohibited



(9) Display mode (3)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
009h	0	0	0	0	0	0	0	0	RSE	0	RSB1	RSB0	RSH3	RSH2	RSH1	RSH0

This register specifies whether all lines will be refreshed every time a specified period (fields) elapses in partial display mode. This function must be need the PT1/0=0/0 setting. For other setting of PT1/0, this function is invalid operation.

RSE: Specifies whether the refresh feature is used for partial display.
RSE = "0": Not refreshed
RSE = "1": Refreshed

RSB1-0: Specifies a magnification factor for the number of refresh fields.

RSB1	RSB0	Factor
0	0	× 2
0	1	× 4
1	0	× 8
1	1	× 16

RSH3-0: Specifies the number of refresh fields.

RSH3	RSH2	RSH1	RSH0	Number of Fields
0	0	0	0	Setting prohibited
0	0	0	1	2 fields
0	0	1	0	3 fields
0	0	1	1	4 fields
		⋮		⋮
1	1	0	1	14 fields
1	1	1	0	15 fields
1	1	1	1	16 fields

All lines will be refreshed at intervals of the following number of fields:

Number of refresh fields (RSH3-0) × magnification factor (RSB1-0) -1 = final refresh fields

(10) Display mode (4)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
00Bh	0	0	0	0	0	0	0	0	XYON	X2	Y2	0	0	0	0	SIP

This register enables or disables the feature that vertically and horizontally doubles the image data from the MPU before writing it to the display RAM. When using this feature, set this register before writing image data to the display RAM.

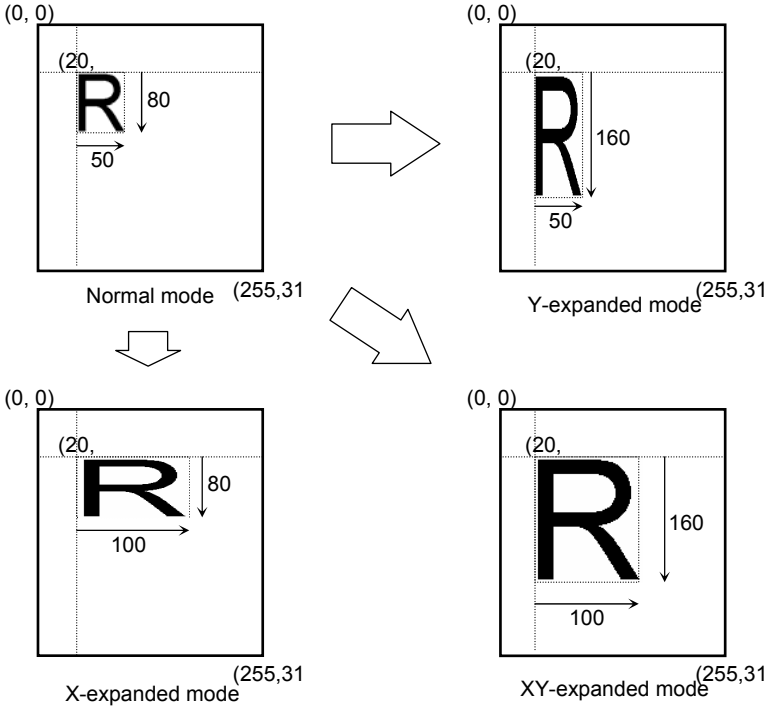
XYON: Enables or disables the XY expansion feature.
XYON = "0": Disables the XY expansion feature.
XYON = "1": Enables the XY expansion feature and the IB5/IB6 data.

X2/Y2: Specifies the direction(s) in which the image is expanded. For details, see the following table:

XYON	X2	Y2	Description
0	*	*	XY expansion disabled
1	0	1	Expansion (×2) in Y direction
1	1	0	Expansion (×2) in X direction
1	1	1	Expansion (×2) in both X and Y directions

When the XY expansion feature is used, the graphic operation feature cannot be used. Note that the display RAM stores expanded data. To restore normal display, retransfer the original image data.

Once XY expansion has been enabled, a display RAM read obtains the expanded XY data from the display RAM. When using the display data read, disable the XY expansion.



Note: In case of XY expansion function, the even number address set is indispensable this function.

SIP: Enables or disables the SIP function.
SIP = "0": Disables the SIP function.
SIP = "1": Enables the SIP function.

For details, refer to "Superimposition Feature".

(11) External display signal setting (1)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
00Ch	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

This register specifies the interface operation mode and the RGB interface transfer rate.

RM: Specifies the interface mode(s) to be used for RAM accesses.
RM = "0": MPU and VSYNC interfaces
RM = "1": RGB interface

Accesses to the display RAM are only enabled in the interface mode(s) specified with the RM register bit. When manipulating the display RAM through the MPU interface, clear RM= "0". When operate the display RAM data by RGB interface mode, set RM= "1". The manipulation of data in the display RAM is asynchronous to the display synchronization signals so that any display RAM data can be manipulated in any sequence.

DM1-0: Specifies the synchronization signal mode for display.

DM1	DM0	Synchronization Signal Setting
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting prohibited

Table of RM, DM1-0 condition

RM	DM1	DM0	Mode
0	0	0	MPU Interface mode The OSD function is possible, But the SIP function is not possible.
0	0	1	RGB Interface mode(1) Display RAM data is not control by RGB interface. If using the SIP function, display data control by MPU interface.
1			RGB Interface mode(2) Display data : RGB interface / Instruction data : Serial interface
0	1	0	VSYNC Interface mode Standard operation controlled by MPU Interface. The display synchronize signal data is external VSYNC signal.

RIM1-0: Specifies the mode when using the RGB interface.

RIM1	RIM0	Interface Setting	Transfer Rate
0	0	18-bit RGB interface	1 time of 18 bits
0	1	16-bit RGB interface	1 time of 16 bits
1	0	6-bit RGB interface	3 times of 6 bits
1	1	Setting prohibited	—

The RGB interface can only transfer display data. It does not support commands for instruction setting; they must be transferred through the MPU interface.

(12) FR period adjustment setting

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
00Dh	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0

This register specifies the number of lines corresponding to 1H when using the on-chip oscillator. The following tables show the relationship between the oscillation frequency and the number of lines:

RTNI4-0: Specifies the number of lines corresponding to 1H.

RTNI4	RTNI3	RTNI2	RTNI1	RTNI0	Number of 1-line Clock Cycles
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
⋮					⋮
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16
1	0	0	0	1	17
⋮					⋮
1	1	1	1	0	30
1	1	1	1	1	31

DIVI1-0: Specifies the frequency division ratio for the on-chip oscillator. The internal operation clock is created by dividing the oscillator frequency by the number specified with these register bits.

DIVI1	DIVI0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc ÷ 1
0	1	2	fosc ÷ 2
1	0	4	fosc ÷ 4
1	1	8	fosc ÷ 8

* fosc: CR oscillation frequency

(13) External display signal setting (2)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
00Eh	0	0	0	0	0	0	DIVE1	DIVE0	RTNE7	RTNE6	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0

RTNE7-0: Specifies the 1H line period in external display mode.

RTNE7	RTNE6	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Number of 1-line Clock Cycles
0	0	0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	0	0	1	Setting prohibited
⋮								⋮
0	0	0	0	1	1	1	1	Setting prohibited
0	0	0	1	0	0	0	0	16
0	0	0	1	0	0	0	1	17
⋮								⋮
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

DIVE1-0: Specifies the frequency division ratio for DOTCLK. The internal operation clock is created by dividing the DOTCLK frequency by the number specified with these register bits.

DIVE1	DIVE0	Division Ratio	Internal Operation Clock Frequency
0	0	2	Setting prohibited
0	1	4	fdotclk ÷ 4
1	0	8	fdotclk ÷ 8
1	1	16	fdotclk ÷ 16

* fdotclk: DOTCLK frequency

(14) External display signal setting (3)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
00Fh	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	VPL	EPL	DPL

VSPL: Selects the polarity of the VSYNC signal.
VSPL = "0": Low active
VSPL = "1": High active

HSPL: Selects the polarity of the HSYNC signal.
HSPL = "0": Low active
HSPL = "1": High active

VPL: Selects the polarity of the VLD signal.
VLD = "0": Low active. Display data write is enabled at low. Display data write is disabled at high.
VLD = "1": High active. Display data write is enabled at high. Display data write is disabled at low.

EPL: Selects the polarity of the ENABLE signal.
ENABLE = "0": Low active. Display data write from the RGB bus is enabled at low. Display data write is disabled at high.
ENABLE = "1": High active. Display data write from the RGB bus is enabled at high. Display data write is disabled at low.

DPL: Selects the polarity of the DOTCLK signal.
DPL = "0": Fetch data on the rising edge of DOTCLK.
DPL = "1": Fetch data on the falling edge of DOTCLK.

(15) LTPS control setting (1)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
012h	0	0	0	0	CLWI3	CLWI2	CLWI1	CLWI0	0	0	0	0	0	0	CLTI1	CLTI0

This register controls LTPS panel switch timing.

CLWI3-0: Specifies the high width for ASW1, ASW2, and ASW3.

CLWI3	CLWI2	CLWI1	CLWI0	ASW1/2/3 High Period
0	0	0	0	Setting prohibited
0	0	0	1	3.0 clock
0	0	1	0	3.5 clock
0	0	1	1	4.0 clock
		⋮		⋮
1	1	1	0	9.5 clock
1	1	1	1	Setting prohibited

CLTI1-0: Specifies the position at which ASW1 rises.

CLTI1	CLTI0	ASW1 Rise Position
0	0	0.0 clock
0	1	0.5 clock
1	0	1.0 clock
1	1	1.5 clock

(16) LTPS control setting (2)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
013h	0	0	0	0	0	0	OEVBI1	OEVBI0	0	0	0	0	0	0	OEVFI1	OEVFI0

This register controls LTPS panel switch timing.

OEVBI1-0: Specifies the position at which OE rises.

OEVBI1	OEVBI0	OE Signal Rise Position
0	0	0.0 clock
0	1	0.5 clock
1	0	1.0 clock
1	1	1.5 clock

OEVFI1-0: Specifies the position at which OE falls.

OEVFI1	OEVFI0	OE Signal Fall Position
0	0	0.0 clock
0	1	0.5 clock
1	0	1.0 clock
1	1	1.5 clock

(17) LTPS control setting (3)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
014h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SHI1	SHI0

This register controls LTPS panel switch timing.

SHI1-0: Specifies the hold time from the falling edge of ASW1, ASW2, and ASW3.

SHI1	SHI0	Hold Time
0	0	0.5 clock
0	1	1.0 clock
1	0	1.5 clock
1	1	2.0 clock

Restrictions

When controlling LTPS panel switch timing, ensure that the following conditions are satisfied:

(1) CLTI (1-0) + CLWI (3-0) ≥ 3 clock cycles
(2) CLWI (3-0) + SHI (1-0) ≥ 3 clock cycles
(3) 1H > CLTI + (CLWI × 3) + (SHI × 2) + 0.5

(18) LTPS control setting (4)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
015h	0	0	CKBI1	CKBI0	0	0	CKFI1	CKFI0	0	0	0	0	0	0	0	0

This register control timing of CKV1/2 signal corresponds to internal CPV signal for LTPS panel.

CKFI1-0: Specifies the rising edge position of CKV1/2 signal.

CKFI1	CKFI0	CKV1/2 signal Falling edge
0	0	0.0 clock
0	1	0.5 clock
1	0	1.0 clock
1	1	1.5 clock

CKBI1-0: Specifies the falling edge position of CKV1/2 signal.

CKBI1	CKBI0	CKV1/2 signal Rising edge
0	0	0.0 clock
0	1	0.5 clock
1	0	1.0 clock
1	1	1.5 clock

(19) LTPS control setting (5)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
018h	0	0	CLWE5	CLWE4	CLWE3	CLWE2	CLWE1	CLWE0	0	0	0	0	CLTE3	CLTE2	CLTE1	CLTE0

This register controls LTPS panel switch timing in external clock mode.

CLWE5-0: Specifies the high width for ASW1, ASW2, and ASW3.

CLWE5	CLWE4	CLWE3	CLWE2	CLWE1	CLWE0	ASW1/2/3 High Period
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	3.0 clock
0	0	0	0	1	0	3.5 clock
0	0	0	0	1	1	4.0 clock
⋮						⋮
1	1	1	1	0	1	33.0 clock
1	1	1	1	1	0	33.5 clock
1	1	1	1	1	1	34.0 clock

CLTE3-0: Specifies the position at which ASW1 rises.

CLTE3	CLTE2	CLTE1	CLTE0	ASW1 Rise Position
0	0	0	0	0.0 clock
0	0	0	1	0.5 clock
0	0	1	0	1.0 clock
⋮				⋮
1	1	1	0	7.0 clock
1	1	1	1	7.5 clock

(20) LTPS control setting (6)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
019h	0	0	0	0	OEVBE3	OEVBE2	OEVBE1	OEVBE0	0	0	0	0	OEVFE3	OEVFE2	OEVFE1	OEVFE0

This register controls LTPS panel switch timing in external clock mode.

OEVBE3-0: Specifies the position at which OE rises.

OEVBE3	OEVBE2	OEVBE1	OEVBE0	OE Signal Rise Position
0	0	0	0	0.0 clock
0	0	0	1	0.5 clock
0	0	1	0	1.0 clock
		⋮		⋮
1	1	1	0	7.0 clock
1	1	1	1	7.5 clock

OEVFE3-0: Specifies the position at which OE falls.

OEVFE3	OEVFE2	OEVFE1	OEVFE0	OE Signal Fall Position
0	0	0	0	0.0 clock
0	0	0	1	0.5 clock
0	0	1	0	1.0 clock
		⋮		⋮
1	1	1	0	7.0 clock
1	1	1	1	7.5 clock

(21) LTPS control setting (7)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
01Ah	0	0	0	0	0	0	0	0	0	0	0	0	SHE3	SHE2	SHE1	SHE0

This register controls LTPS panel switch timing in external clock mode.

SHE3-0: Specifies the hold time from the falling edge of ASW1, ASW2, and ASW3.

SHE3	SHE2	SHE1	SHE0	Hold Time
0	0	0	0	0.5 clock
0	0	0	1	1.0 clock
0	0	1	0	1.5 clock
⋮	⋮	⋮	⋮	⋮
1	1	1	0	7.5 clock
1	1	1	1	8.0 clock

Restrictions

When controlling LTPS panel switch timing, ensure that the following conditions are satisfied:

(1) CLTE (1-0) + CLWE (3-0) ≥ 3 clock cycles
(2) CLWE (3-0) + SHE (1-0) ≥ 3 clock cycles
(3) 1H > CLTE + (CLWE × 3) + (SHE × 2) + 0.5

(22) LTPS control setting (8)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
01Bh	CKBE3	CKBE2	CKBE1	CKBE0	CKFE3	CKFE2	CKFE1	CKFE0	0	0	0	0	0	0	0	0

This register controls timing of CKV1/2 signal correspond to internal CPV signal for LTPS panel.

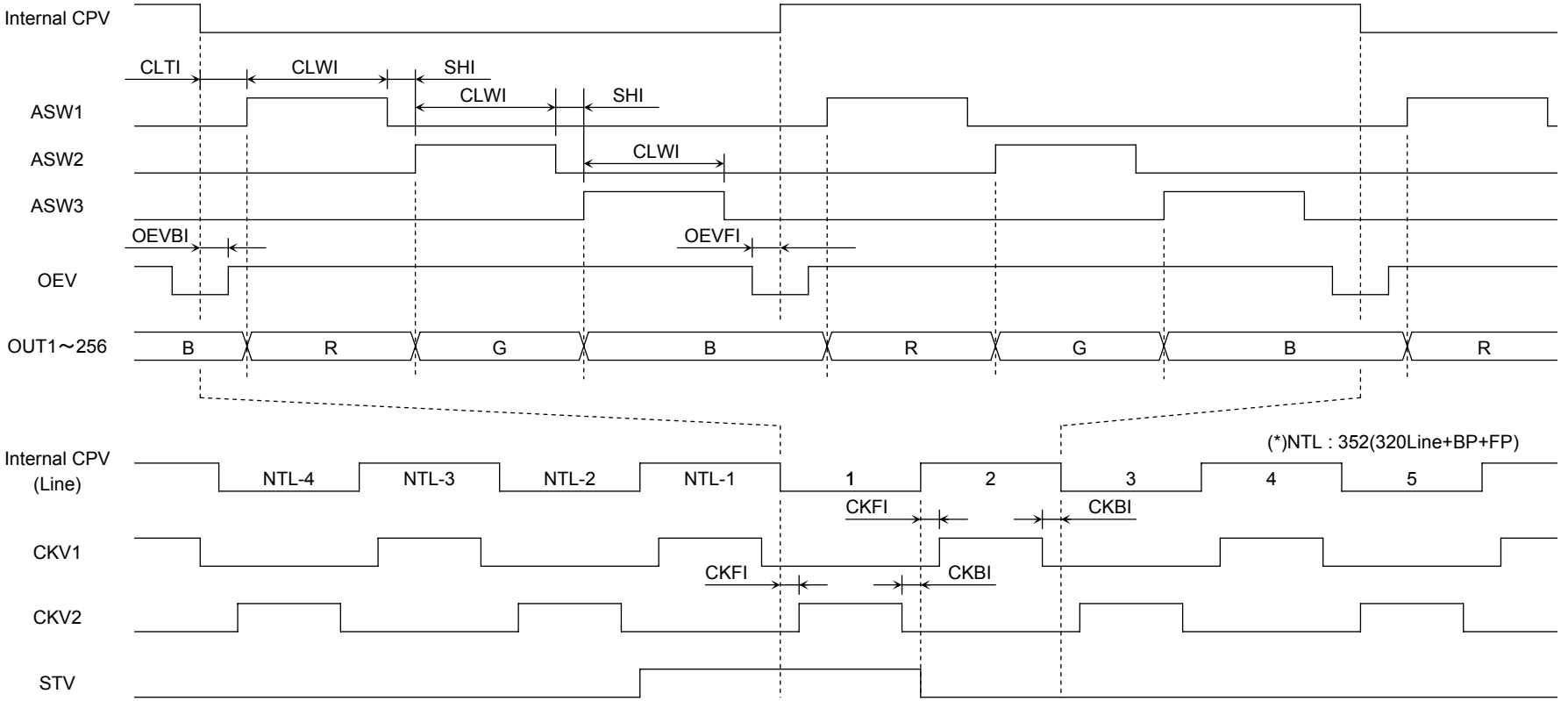
CKFE1-0: Specifies the rising edge position of CKV1/2 signal.

CKFE3	CKFE2	CKFE1	CKFE0	CKV1/2 signal Falling position
0	0	0	0	0.0 clock
0	0	0	1	0.5 clock
0	0	1	0	1.0 clock
⋮				⋮
1	1	1	0	7.0 clock
1	1	1	1	7.5 clock

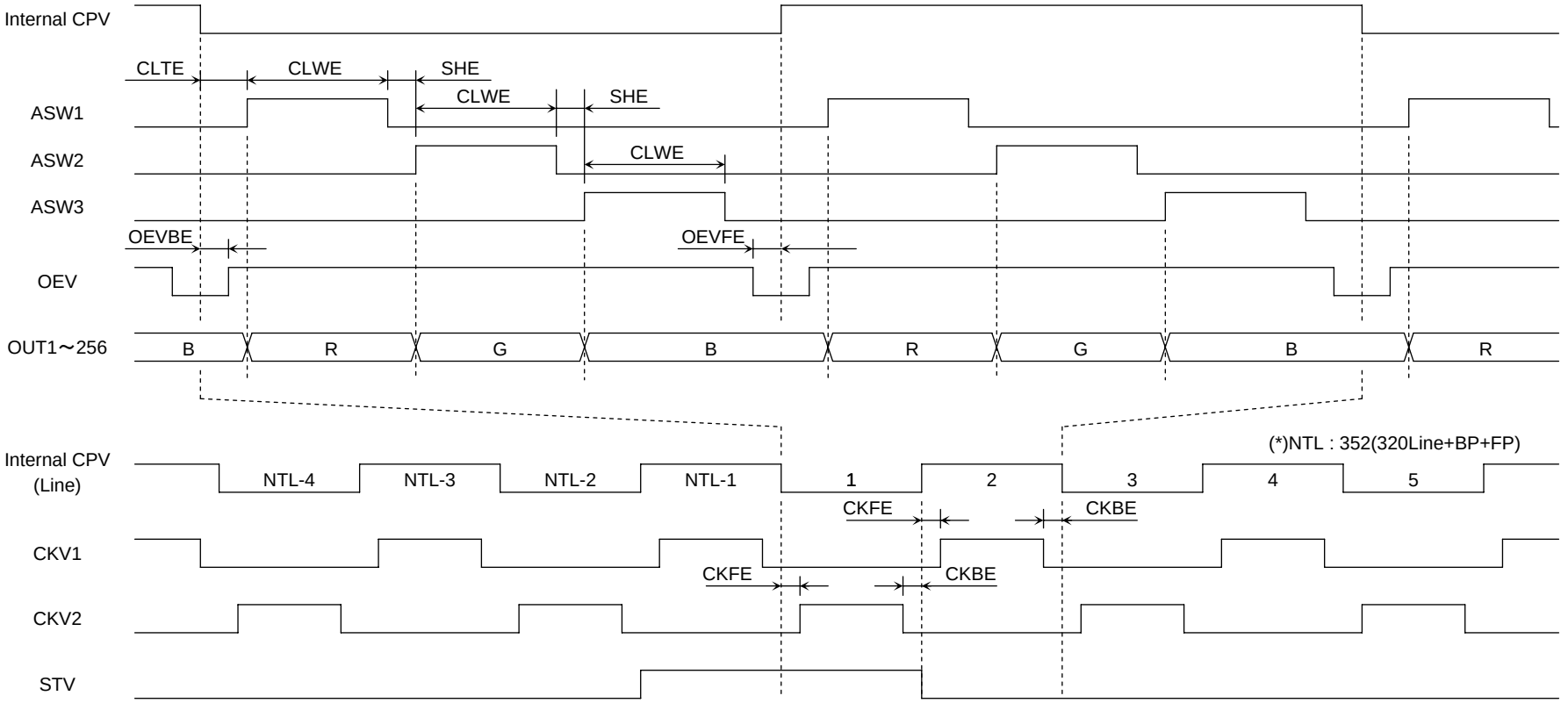
CKBE1-0: Specifies the falling edge position of CKV1/2 signal.

CKBE3	CKBE2	CKBE1	CKBE0	CKV1/2 signal Rising position
0	0	0	0	0.0 clock
0	0	0	1	0.5 clock
0	0	1	0	1.0 clock
⋮				⋮
1	1	1	0	7.0 clock
1	1	1	1	7.5 clock

Timing chart when the internal clock is used



Timing chart when an external clock (DOTCLK) is used



(23) Amplifier capability setting

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
01Ch	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ABSW1	ABSW0

This register specifies the current capability of the on-chip operational amplifier.

ABSW1	ABSW0	Amplifier Capability
0	0	Maximum
0	1	Bias / AMP OFF mode
1	0	Optimum
1	1	Minimum

(24) Mode setting

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
01Dh	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB	0	STB

This register specifies the display mode.

DSTB: Specifies the deep standby state.
Clearing DSTB to "0" initiates the deep standby state, in which the JBT6K71-AS(A) internal logic power supply is turned off. Note that registers cannot be used to trigger a transition from the deep standby state to standby state.

STB: Specifies the standby state.
After the reset function, STB register data is "0". Setting STB to "1" clears the standby state.

This register can only change the mode from the standby state to deep standby state, not vice versa.

(25) Power-off line setting

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
01Eh	0	0	0	0	0	0	0	0	0	0	0	0	POFH3	POFH2	POFH1	POFH0

This register specifies the timing of VCS signal turning to "H" to "L". After the reset function, register number is 10H select.

POFH3	POFH2	POFH1	POFH0	Number of Lines
0	0	0	0	Setting prohibited
0	0	0	1	2H
0	0	1	0	3H
0	0	1	1	4H
		⋮		⋮
1	1	1	0	15H
1	1	1	1	16H

(26) Display Control

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
100h	PO	CONT	PEV	DCEV	UD	CON	OEV	VCS	ASW1	ASW0	D1	D0	FR	FDON	VGAM	DCG

This register holds command data to controls the JBT6K71-AS(A) power-up and power-down sequence. To change register command data, it can control power-up and power down sequence by one register, simply. Setting "index=100h", starting from the field next to that where the register is set.
For details, refer to "Display ON Sequence."

PO: Triggers sleep mode. Transferring a command with PO cleared to "0" to the JBT6K71-AS(A) to enter sleep mode. Setting PO to "1" terminates sleep mode. After terminating sleep mode, internal AVDD booster and XVDD booster turns on. For information on how to use the command, refer to "Display ON Sequence (1)/ (2)" and "Display OFF Sequence."

CONT: Turns on/off internal signals generated from the JBT6K71-AS(A).

PEV: Turns on/off voltage booster for LCD. PEV command is linked with PEV pin. When PEV command setting is "1", PEV pin outputs High level.

DCEV: Turns on/off DCCK, /DCCK and DCEV signal generated from the JBT6K71-AS(A). These signals use for voltage booster circuit on LCD. DCCK and /DCCK signals use for clock of voltage booster on LCD. DCEV uses to mask the edge of DCCK and /DCCK signals.

UD: Setting of gate scan direction which uses gate circuit on LCD. UD command is linked with UD pin. When UD command setting is "1", UD pin outputs High level.

CON: Turns on/off the STV, CKV1 and CKV2 signals generated from the JBT6K71-AS(A). Setting CON to "1" causes the STV, CKV1 and CKV2 signals to be output, starting from the field next to that where the register is set.

OEV: Turns on/off the OEV signal generated from the JBT6K71-AS(A). Setting OEV to "1" causes the OEV signal to be output, starting from the field next to that where the register is set.

VCS: Turns on/off the VCS signal and VCOMD signal generated from the JBT6K71-AS(A). Setting VCS to "1" causes the VCS signal and VCOMD signal to be output, starting from the field next to that where the register is set.

ASW1-0: Turns on/off the ASW signal generated from the JBT6K71-AS(A) and varies the level of the ASW.

ASW1	ASW0	Description
0	0	Fixed to VSS
0	1	
1	0	Fixed to VDD
1	1	Operating (normal drive)

D1-0: Specifies the state of the output pins.

D1	D0	Description
0	0	Setting prohibited
0	1	VSS
1	0	Operating (white data)
1	1	Operating (normal drive)

FR: Turns on/off the FR signal generated from the JBT6K71-AS(A). Setting FR to “1” causes the FR signal to be output, starting from the field next to that where the register is set.

FDON: Turns on/off FDON signal generated from the JBT6K71-AS(A). Setting FDON to "1" causes the FDON signal to be output, starting from the field next to that where the register is set.

VGAM: Turns on/off VGAMMA power supply for gray scale generated from the JBT6K71-AS(A).

DCG: Turns on/off DCG signal generated from the JBT6K71-AS(A). Setting DCG to "1" causes the DCG signal to be output, starting from the field next to that where the register is set.

(27) Auto sequence Control

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
101h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AUTO

This register is auto sequence control flag between powers on to display on.

(28) Power supply control (1)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
102h	0	0	0	0	VCD3	VCD2	VCD1	VCD0	VCS3	VCS2	VCS1	VCS0	AGM3	AGM2	AGM1	AGM0

This register holds command data to control output voltage of internal voltage booster circuit. For details, refer to below table.

VCD3-0: Specifies the VCOMD output voltage.

VCD3	VCD2	VCD1	VCD0	VCOMD Output voltage
0	0	0	0	1.4V(Initial)
0	0	0	1	1.5V
0	0	1	0	1.6V
0	0	1	1	1.7V
0	1	0	0	1.8V
0	1	0	1	1.9V
0	1	1	0	2.0V
0	1	1	1	2.1V
1	0	0	0	2.2V
1	0	0	1	2.3V
1	0	1	0	2.4V
1	0	1	1	2.5V
1	1	0	0	2.6V
1	1	0	1	2.7V
1	1	1	0	2.8V
1	1	1	1	2.9V

VCS3-0: Specifies the VCS output voltage.

VCS3	VCS2	VCS1	VCS0	VCS output voltage
0	0	0	0	3.0V(Initial)
0	0	0	1	3.1V
0	0	1	0	3.2V
0	0	1	1	3.3V
0	1	0	0	3.4V
0	1	0	1	3.5V
0	1	1	0	3.6V
0	1	1	1	3.7V
1	0	0	0	3.8V
1	0	0	1	3.9V
1	0	1	0	4.0V
1	0	1	1	4.1V
1	1	0	0	4.2V
1	1	0	1	4.3V
1	1	1	0	4.4V
1	1	1	1	4.5V

VGM3-0: Specifies the VGM output voltage.

VGM3	VGM2	VGM1	VGM0	VGM output voltage
0	0	0	0	3.7V
0	0	0	1	3.8V
0	0	1	0	3.9V
0	0	1	1	4.0V
0	1	0	0	4.1V
0	1	0	1	4.2V
0	1	1	0	4.3V
0	1	1	1	4.4V
1	0	0	0	4.5V
1	0	0	1	4.6V
1	0	1	0	4.7V
1	0	1	1	4.8V
1	1	0	0	4.9V(Initial)
1	1	0	1	5.0V
1	1	1	0	5.1V
1	1	1	1	5.2V

(29) Power Supply Control (2)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
103h	0	0	WSEL 2	WSEL 1	0	0	0	0	0	0	0	0	0	XVD 2	XVD 1	XVD 0

This register holds command data to control output voltage of internal XVDD voltage booster circuit and boosting clock mode. For details, refer to below table.

XVD2-0: Specifies the XVDD output voltage

XVD2	XVD1	XVD0	XVDD output voltage
0	0	0	4.7V
0	0	1	4.8V
0	1	0	4.9V
0	1	1	5.0V(Initial)
1	0	0	5.1V
1	0	1	5.2V
1	1	0	5.3V
1	1	1	5.4V

WSEL1: Specifies the clock mode of AVDD voltage booster

BAV	WSEL1	Boosting clock mode
0	0	Dual mode
0	1	Single mode
1	*	Single mode

Note: WSEL1 setting is valid at x2 boosting system (BAV="0"). When x3 boosting system (BAV=”1”) uses, WSEL1 setting is invalid, and boosting clock becomes single mode.

WSEL2: Specifies the clock mode of XVDD voltage booster

BXV	WSEL2	Boosting clock mode
0	0	Dual mode
0	1	Single mode
1	*	Single mode

Note: WSEL2 setting is valid at x2 boosting system (BXV="0"). When x3 boosting system (BXV=”1”) uses, WSEL2 setting is invalid, and boosting clock becomes single mode.

(30) Power Supply Control (3)

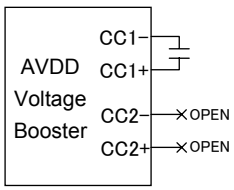
Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
104h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BXV	BAV

This register sets the regulate level of AVDD and XVDD regulator circuit.
Please reference the below regulate level setting of each regulator circuit.

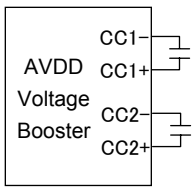
BAV: Specifies the boosting steps of AVDD voltage booster

BAV	AVDD booster steps
0	X2 mode
1	X3 mode

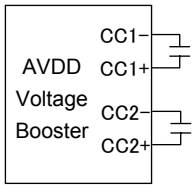
For connection of boosting capacitor, refer to below figure.



In case of BAV="0"(x2 mode)
WSEL1="1"(single)



In case of BAV="0"(x2 mode)
WSEL1="0"(dual)



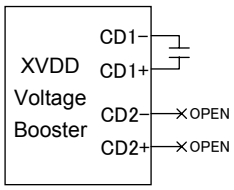
In case of BAV="1"(x3 mode)
WSEL1="0" or "1"(single)

]

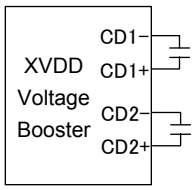
BAV: Specifies the boosting steps of XVDD voltage booster

BXV	XVDD booster steps
0	X2 mode
1	X3 mode

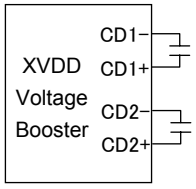
For connection of boosting capacitor, refer to below figure.



In case of BXV="0"(x2 mode)
WSEL2="1"(single)



In case of 0BXV="0"(x2 mode)
WSEL2="0"(dual)



In case of BXV="1"(x3 mode)
WSEL2="0" or "1"(single)

(31) Power supply control (4)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
105h	0	0	0	0	0	0	DCW1	DCW0	0	0	CK31	CK30	CK21	CK20	CK11	CK10

This register sets the divided clock of regulator in JBT6K71-AS(A).

Divided frequency can set per each regulator circuits. Please reference below register data and divided frequency setting.

CK11-10: Set the divided level of regulate clock for AVDD regulate circuit

CK11	CK10	DCCLK frequency
0	0	1/2H
0	1	1H
1	0	2H
1	1	4H

CK21-20: Set the divided level of regulate clock for XVDD regulate circuit

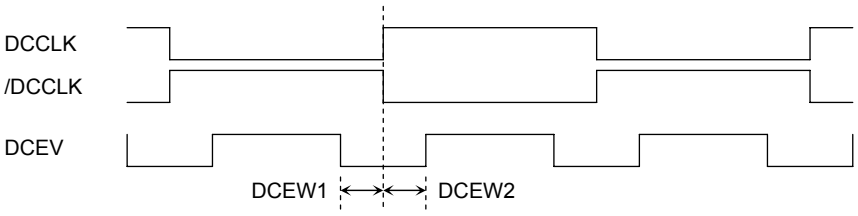
CK21	CK20	DCCLK frequency
0	0	1/2H
0	1	1H
1	0	2H
1	1	4H

CK31-30: Set the divided level of regulate clock for external regulate circuit

CK31	CK30	DCCLK frequency
0	0	1/2H
0	1	1H
1	0	2H
1	1	4H

DCW1-0: Set mask period of DCCLK signal

DCW1	DCW0	Mask period (DCEW1/DCEW2)
0	0	0.5 clock
0	1	1.0 clock
1	0	1.5 clock
1	1	2.0 clock



Note) Set 00Dh register of 1H clock setting up as even. When set 1/2H

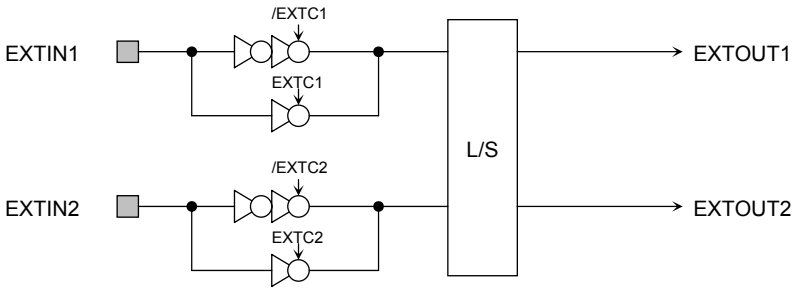
Note) select the best condition after the module evaluation.

(32) EXT polarity control

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
108h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EXTC2	EXTC1

This register changes level sifted EXTOUT1/2 signal polarity with register data as the below figure.

EXTCn	EXTOUTn
0	The signal from EXTINn outputs positive.
1	The signal from EXTINn outputs negative.



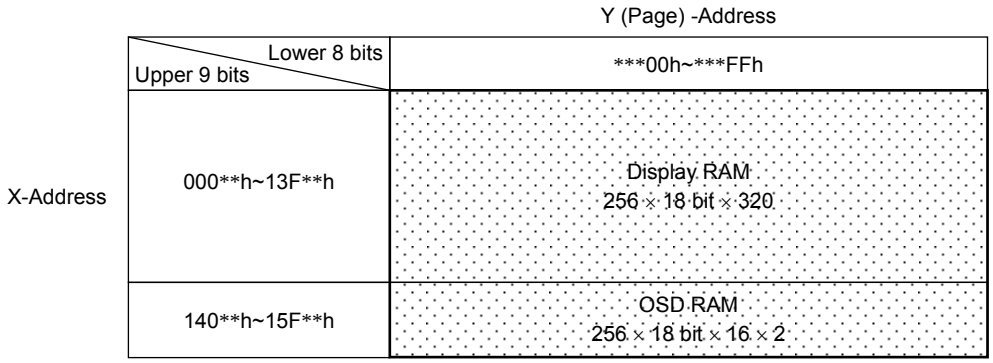
(33) RAM address setting (1), (2)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
200h	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
201h	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

These registers specify the display RAM address at which data is to be written. Once the display RAM address has been set, the JBT6K71-AS(A) can automatically write a sequence of data by incrementing or decrementing the address counter as specified with the entry mode. The address counter is incremented or decremented within the range specified by window addressing.

Note that the display RAM cannot be accessed in the standby state.

The following table shows the address ranges:



The OSD RAM uses the address area of 14000h to 15FFFh, continuous to the display RAM area. For information on how to specify an address, refer to “OSD Register Setting.” Note that the OSD RAM uses the same address counter as that for the display RAM, as specified with the entry mode.

(34) RAM data write

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
202h	Write data * Bit assignment varies with the selected interface.															

This register internally expands display RAM data to 18 bits before writing it. The format of 18-bit expansion varies with the interface. Once data has been written to the display RAM, the address is updated automatically according to the AM and I/D bits. Note that the display RAM cannot be accessed in the standby state. When the 8- or 16-bit interface is used, the R and B most significant bits are copied to the R and B least significant bits, respectively, to expand the data to 18 bits.

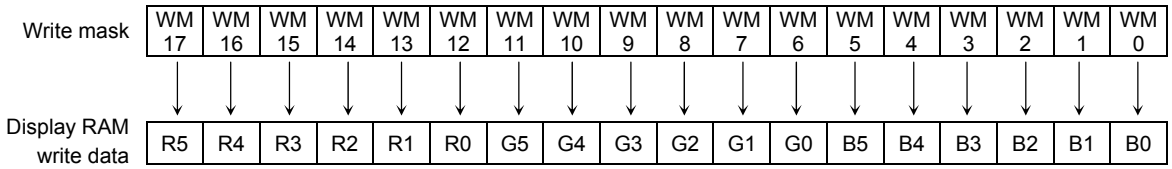
*: If a RAM write through the system interface is required when the RGB interface is used, ensure that writes through both interfaces do not conflict. When the 18-bit RGB interface is used, 18-bit data can be written through the PD17-PD0 pins to use 262,144 colors. When the 16-bit interface is used, the R and B most significant bits are copied to the R and B least significant bits, respectively, to use 65,536 colors.

(35) Graphic operation (1), (2)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
203h	0	0	WM11	WM10	WM9	WM8	WM7	WM6	0	0	WM5	WM4	WM3	WM2	WM1	WM0
204h	0	0	0	0	0	0	0	0	0	0	WM17	WM16	WM15	WM14	WM13	WM12

These registers specify a bitwise mask for a write to the display RAM. When WM17 = "1", the most significant bit of the write data for the display RAM is masked so that no data will be written to the display RAM. The WM16 to WM0 bits mask the corresponding bits in the data to be written to the display RAM. For details, refer to the "Graphic Operation Feature." Note that a write mask is applied to 18-bit data to be written to the display RAM.

*: This feature cannot be used with the RGB interface.



(36) Gray scale setting

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
300h	0	0	0	0	0	PK12	PK11	PK10	0	0	0	0	0	PK02	PK01	PK00
301h	0	0	0	0	0	PK32	PK31	PK30	0	0	0	0	0	PK22	PK21	PK20
302h	0	0	0	0	0	PK52	PK51	PK50	0	0	0	0	0	PK42	PK41	PK40
303h	0	0	0	0	0	PR12	PR11	PR10	0	0	0	0	0	PR02	PR01	PR00
304h	0	0	0	0	0	VR12	VR11	VR10	0	0	0	0	0	VR02	VR01	VR00

This register enables the gamma curve value to be programmatically adjusted according to the user LCD. When registers 300h to 304h are set, the gamma curve varies symmetrically for positive and negative poles. For details, refer to the “Gamma Adjustment Feature.”

PK52-00: Gamma fine tuning register for positive/negative polarity output
PR12-00: Inclination adjustment registers for positive/negative polarity output
VR14-00: Amplitude adjustment registers for positive/negative polarity output

(37) Setting for Gray scale offset amounts

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
305h	0	0	0	0	0	0	0	BLON	0	BUP2	BUP1	BUP0	0	BOFS2	BOFS1	BOFS0

This register selects one or two system of only blue gray scale and red and green gray scale.
Two gray scale systems are enable as BLON="1". BOFS2-0 sets the offset amounts.
Please reference the below tables.

BLON: Select the offset “on” or “off” of gray scale offset.

BLON	Offset
0	OFF
1	ON

BOFS2-0: Set the gray scale offset amounts.

BOFS2	BOFS1	BOFS0	Offset
0	0	0	0.0V
0	0	1	0.1V
0	1	0	0.2V
0	1	1	0.3V
1	0	0	0.4V
1	0	1	0.5V
1	1	0	0.6V
1	1	1	0.7V

BUP2-0: Adjust the voltage between L63 and L62, L1 and L0.

BUP2	BUP1	BUP0	Offset
0	0	0	0.0V
0	0	1	0.1V
0	1	0	0.2V
0	1	1	0.3V
1	0	0	0.4V
1	0	1	0.5V
1	1	0	0.6V
1	1	1	0.7V

(38) Vertical scroll control (1), (2)

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
400h	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
401h	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20

These registers specify the amount of vertical line scroll.

VL18-10: Specifies the amount of scroll when the first screen is scrollable for vertical smooth scroll display. The screen can be scrolled by any number of lines between 0 and 319. Once the last line, 320, has been displayed, display is started from line 1 again. The amount of scroll (VL18-10) is valid when the first screen vertical scroll enable bit VLE1 is set to "1". When VLE1 = "0", the screen is displayed with fixed lines.

*: This feature cannot be used with the external interface.

VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10	Amount of Scroll
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	0	1	1	3 lines
				⋮					⋮
1	0	0	1	1	1	1	0	1	317 lines
1	0	0	1	1	1	1	1	0	318 lines
1	0	0	1	1	1	1	1	1	319 lines

Note: In case of OSD="1", do not set a value exceeding 319.

Note: if the window area is set to other than the maximum effective screen size, the number of lines to be scrolled must not exceed the maximum number of lines in the window.

And when OSD=0. OSD-RAM area is available for normal RAM.
Then MAX scroll amounts is 352 lines

1	0	1	0	0	0	0	0	0	320 lines
1	0	1	0	0	0	0	0	1	321 lines
				⋮					⋮
1	0	1	0	1	1	1	1	0	350 lines
1	0	1	0	1	1	1	1	1	351 lines

VL28-20: Set the scroll amounts with the displaying 2nd display scroll. Display ups and downs smooth scroll.
And can display the optional line scroll between 0 line and 319 lines.
After the final 320 lines, next is forehand 1st line repetition.
The scroll amounts is enable, When 1st vertical scroll enable bit is VLE2=1. And when VLE2=0. Display the fixed line.

VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	Scroll amounts
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	0	1	1	3 lines
				⋮					⋮
1	0	0	1	1	1	1	0	1	317 lines
1	0	0	1	1	1	1	1	0	318 lines
1	0	0	1	1	1	1	1	1	319 lines

Note: Prohibited to set 319 lines over.

When OSD=0 as 1st display. OSD-RAM is available as a normal RAM. Then MAX scroll amounts are 351 lines.

1	0	1	0	0	0	0	0	0	320 lines
1	0	1	0	0	0	0	0	1	321 lines
				⋮					⋮
1	0	1	0	1	1	1	1	0	350 lines
1	0	1	0	1	1	1	1	1	351 lines

(39) First/second screen drive positions

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
402h	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
403h	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
404h	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
405h	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20

SS18-10: Specifies the first screen start position in line units. The JBT6K71-AS(A) starts driving the LCD at the line having the number of the specified value plus one.

SE18-10: Specifies the first screen end position in line units. The JBT6K71-AS(A) drives the LCD until the line having the number of the specified value plus one. If SS18-10 and SE18-10 are set to "07"H and "10"H, respectively, for example, the JBT6K71-AS(A) drives the LCD between line 8 and line 17, not displaying lines 1 to 7, line 18 and subsequent lines. Ensure that following condition is satisfied: SS18-10 ≤ SE18-10 ≤ "13F"H. For details, refer to "Split Screen Drive Feature."

SS28-20: Specifies the second screen start position in line units. The JBT6K71-AS(A) starts driving the LCD at the line having the number of the specified value plus one. The second screen is driven only when SPT = "1".

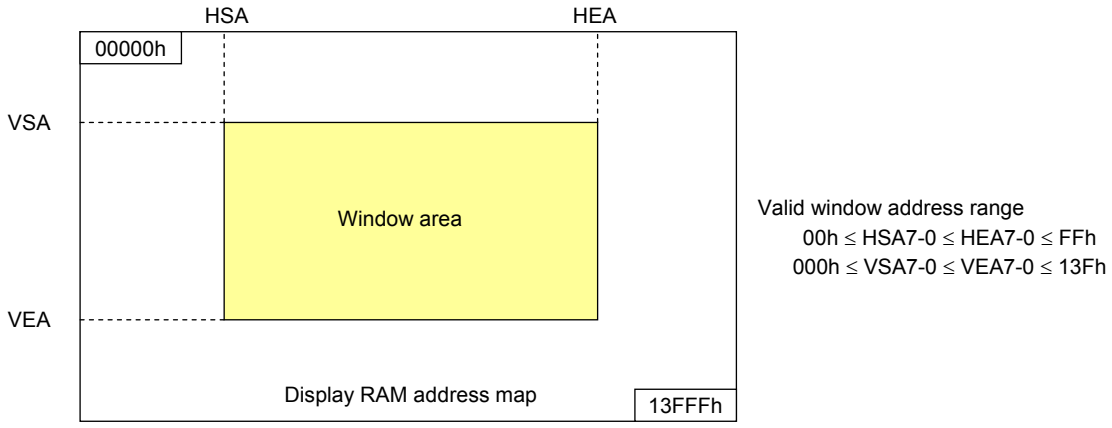
SE28-20: Specifies the second screen end position in line units. The JBT6K71-AS(A) drives the LCD until the line having the number of the specified value plus one. If SPT is set to "1" with SS28-20 and SE28-20 set to "20"H and "4F"H, respectively, for example, the JBT6K71-AS(A) drives the LCD between line 33 and line 80. Ensure that following condition is satisfied: SS18-10 ≤ SE18-10 < SS28-20 ≤ SE28-20 ≤ "13F"H. For details, refer to "Split Screen Drive Feature."

(40) Horizontal/vertical RAM address location

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
406h	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
407h	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
408h	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
409h	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0

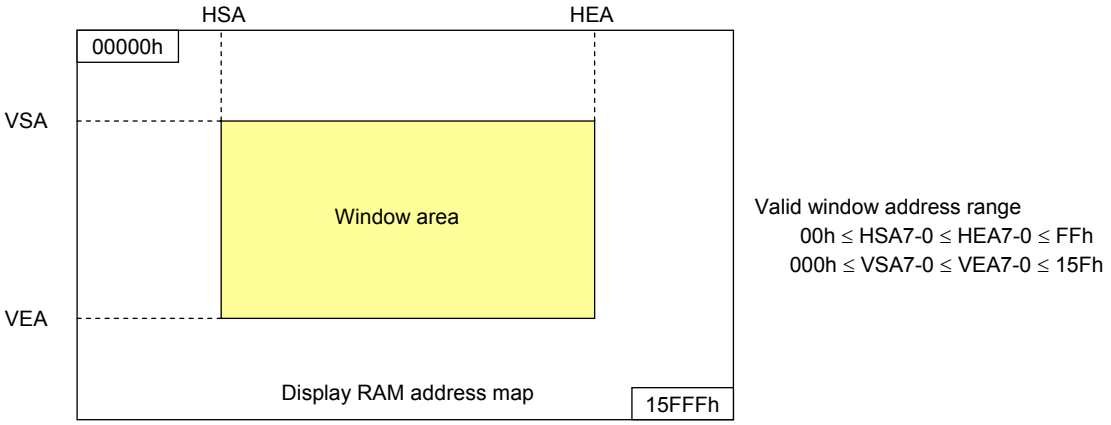
HSA7-0/HEA7-0: Specifies the horizontal window start/end addresses. Data can be written to the display RAM area within the range from the address specified with HSA7-0 to that specified with HEA7-0. Set the addresses before attempting to write data to RAM. Ensure that the following condition is satisfied: "00h" ≤ HSA7-0 ≤ HEA7-0 ≤ "FFh".

VSA8-0/VEA8-0: Specifies the vertical window start/end addresses. Data can be written to the display RAM area within the range from the address specified with VSA8-0 to that specified with VEA8-0. Set the addresses before attempting to write data to RAM. Ensure that the following condition is satisfied: "000h" ≤ VSA8-0 ≤ VEA8-0 ≤ "13Fh".



Note: The specified window area must be included in the available display RAM address space. The XY-address counter is incremented and decremented within the window area.

In case of OSD="0", The OSD-RAM can use as Normal display RAM. This case, Display RAM area change the maximum of vertical address.



Note: The specified window area must be included in the available display RAM address space. The XY-address counter is incremented and decremented within the window area.

(41) OSD function ON/OFF

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
500h	0	0	0	0	0	0	0	OSDW	0	0	0	0	0	0	0	OSDON

This register enables or disables the OSD function and specifies the OSD RAM addressing method.

OSDON: Enables or disables the OSD feature.
When OSDON = "1", the OSD function is enabled. The OSD RAM addressing method varies with the OSDW register bit.
When OSDON = "0", the OSD feature is disabled.

OSDW: Specifies the addressing method for writing data to the OSD RAM area. Note that the OSDON register bit also affects how the OSD RAM area is addressed.

For details, refer to "Display RAM and OSD RAM Configurations."

(42) OSD first/second screen start addresses

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
504h	0	0	0	0	0	0	0	ST18	ST17	ST16	ST15	ST14	ST13	ST12	ST11	ST10
505h	0	0	0	0	0	0	0	ST28	ST27	ST26	ST25	ST24	ST23	ST22	ST21	ST20

These registers specify the address locations of the first and second screens when the OSD feature is used. The valid address range is lines 0 to 319. For information on the positional relationship between the first and second screens, refer to "OSD Feature."

(43) NOP

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
600h~ 6FFh	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

This register is non operation.

(44) TEST MODE SETTING

Index	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
700h ～70Fh	Test mode register area															

JBT6K71-AS(A) has resister for test mode in TOSHIBA. If you miss-setting these register, need the reset function and restart of power on sequence.

Interface mode specification table

		T6K71 command/data bus terminal name																																															Terminal condition				Command condition					
	Interface mode	/DACK	/RST	/RD	/WR	/CS	RS	VLD	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	VSYNC	HSTNC	ENABLE	DOTCLK	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	IM3	IM2	IM1	IM0	TRI	DFM1	DFM0	RIM1	RIM0	Number of connect
MPU terminal name	Setting prohibited	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	0	0	0	0	*	*	*	*	*	–
	Setting prohibited	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	0	0	0	1	*	*	*	*	*	–
	16bit interface(1)	/DACK	/RST	/RD	/WR	/CS	RS	VLD	D15	D14	D13	D12	D11	D10	D9	D8		D7	D6	D5	D4	D3	D2	D1	D0																								0	0	1	0	0	0	0	*	*	23
	16bit interface(2)	/DACK	/RST	/RD	/WR	/CS	RS	VLD	D15	D14	D13	D12	D11	D10	D9	D8		D7	D6	D5	D4	D3	D2	D1	D0																												0	0	1	*	*	23
	16bit interface(3)	/DACK	/RST	/RD	/WR	/CS	RS	VLD	D15	D14	D13	D12	D11	D10	D9	D8		D7	D6	D5	D4	D3	D2	D1	D0																												0	1	0	*	*	23
	8bit interface(1)	/DACK	/RST	/RD	/WR	/CS	RS	VLD	D7	D6	D5	D4	D3	D2	D1	D0																																	0	0	1	1	0	0	0	*	*	15
	8bit interface (2)	/DACK	/RST	/RD	/WR	/CS	RS	VLD	D7	D6	D5	D4	D3	D2	D1	D0																																					1	0	1	*	*	15
	8bit interface (3)	/DACK	/RST	/RD	/WR	/CS	RS	VLD	D7	D6	D5	D4	D3	D2	D1	D0																																					1	1	0	*	*	15
	8bit interface (4)	/DACK	/RST	/RD	/WR	/CS	RS	VLD	D7	D6	D5	D4	D3	D2	D1*	D0*																																					1	1	1	*	*	15
	SERIAL+18bit RGB interface	/DACK	/RST		SCL	/CS		VLD	SDI	SDO																	VSYNC	HSYNC	ENABLE	DOTCLK	pd17	pd16	pd15	pd14	pd13	pd12	pd11	pd10	pd9	pd8	pd7	pd6	pd5	pd4	pd3	pd2	pd1	pd0	0	1	0	ID	*	*	*	0	0	29
	SERIAL+16bit RGB interface	/DACK	/RST		SCL	/CS		VLD	SDI	SDO																	VSYNC	HSYNC	ENABLE	DOTCLK	pd15	pd14	pd13	pd12	pd11		pd10	pd9	pd8	pd7	pd6	pd5	pd4	pd3	pd2	pd1	pd0									0	1	27
	SERIAL+6bit RGB interface	/DACK	/RST		SCL	/CS		VLD	SDI	SDO																	VSYNC	HSYNC	ENABLE	DOTCLK	pd5	pd4	pd3	pd2	pd1	pd0																				1	0	17
	Setting prohibited	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	0	1	1	0	*	*	*	*	*	–
	Setting prohibited	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	0	1	1	1	*	*	*	*	*	–
	Setting prohibited	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	0	0	0	*	*	*	*	*	–
	Setting prohibited	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	0	0	1	*	*	*	*	*	–
	18bit interface	/DACK	/RST	/RD	/WR	/CS	RS	VLD	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0																							1	0	1	0	*	*	*	*	*	25
	9bit interface	/DACK	/RST	/RD	/WR	/CS	RS	VLD	D8	D7	D6	D5	D4	D3	D2	D1	D0																																1	0	1	1	*	*	*	*	*	16
	Setting prohibited		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	1	0	0	*	*	*	*	*	–
	Setting prohibited		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	1	0	1	*	*	*	*	*	–
	Setting prohibited		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	1	1	0	*	*	*	*	*	–
	Setting prohibited		–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	1	1	1	*	*	*	*	*	–
	For All function interface mode (262k colors)	/DACK	/RST	/RD	/WR	/CS	RS	VLD	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	VSYNC	HSYNC	ENABLE	DOTCLK	pd17	pd16	pd15	pd14	pd13	pd12	pd11	pd10	pd9	pd8	pd7	pd6	pd5	pd4	pd3	pd2	pd1	pd0	1	0	1	0	*	*	*	*	*	47
	VSYNC interface	/DACK	/RST	/RD	/WR	/CS	RS	VLD	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	VSYNC																						1	0	1	1	*	*	*	*	*	26

Note: The JBT6K71-AS(A) have not pulled up/down about input terminal. If not using the input terminal, connect to VSS terminal.

MPU Interface Mode Settings

The JBT6K71-AS supports a wide range of interface mode settings according to the combination of the IM3-IM0 pin and TRI and DFM1/0 register settings. The IM3-IM0 pins specify the number of data bus bits used for the MPU interface. Available modes are 8-bit, 9-bit, 16-bit, 18-bit, and serial interface. The TRI and DFM1/0 register bits specify the data transfer rate and bit assignment to configure an appropriate transfer format according to the MPU conditions.

IM3	IM2	IM1	IM0	TRI	DFM1	DFM0	Interface Mode	Number of RAM Data Transfers	Bit Assignment	Display Data Bits	Number of index data transfers
0	0	1	0	0	0	0	16-bit mode (1)	1	16 bits	16 bits	1
0	0	1	0	0	0	1	16-bit mode (2)	2	16 bits + 2 bits	18 bits	1
0	0	1	0	0	1	0	16-bit mode (3)	2	2 bits + 16 bits	18 bits	1
0	0	1	1	0	0	0	8-bit mode (1)	2	8 bits + 8 bits	16 bits	2
0	0	1	1	1	0	1	8-bit mode (2)	3	8 bits + 8 bits + 2 bits	18 bits	2
0	0	1	1	1	1	0	8-bit mode (3)	3	2 bits + 8 bits + 8 bits	18 bits	2
0	0	1	1	1	1	1	8-bit mode (4)	3	6 bits + 6 bits + 6 bits	18 bits	2
0	1	0	ID	*	*	*	Serial mode	2	8 bits + 8 bits	16 bits	2
1	0	1	0	*	*	*	18-bit mode	1	18 bits	18 bits	1
1	0	1	1	*	*	*	9-bit mode	2	9 bits + 9 bits	18 bits	2

1) 18-bit MPU interface

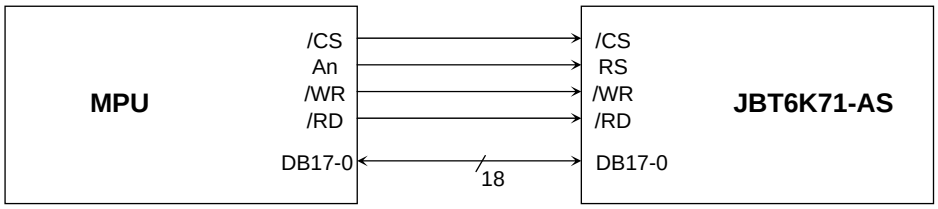
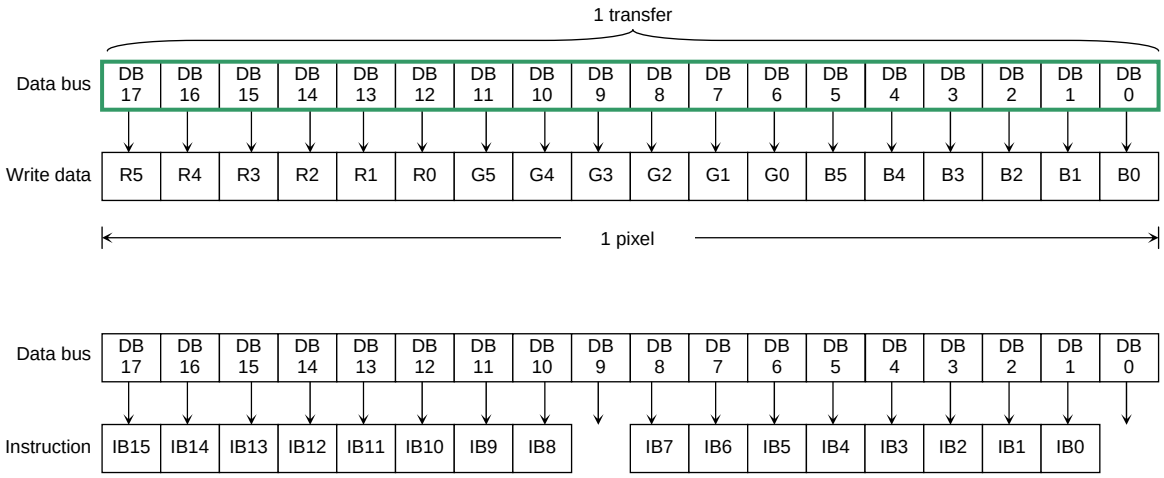


Figure 1 Example connection for the 18-bit MPU interface

a) 18-bit MPU interface (1 transfer)



2) 16-bit MPU interface

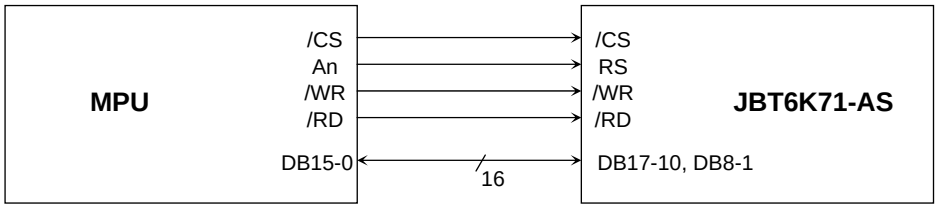
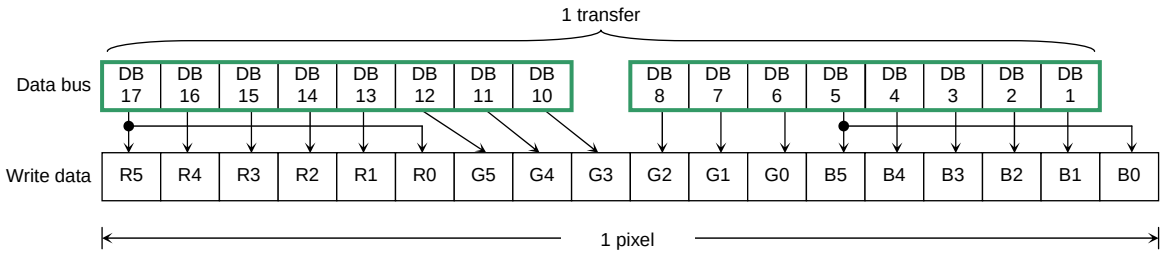
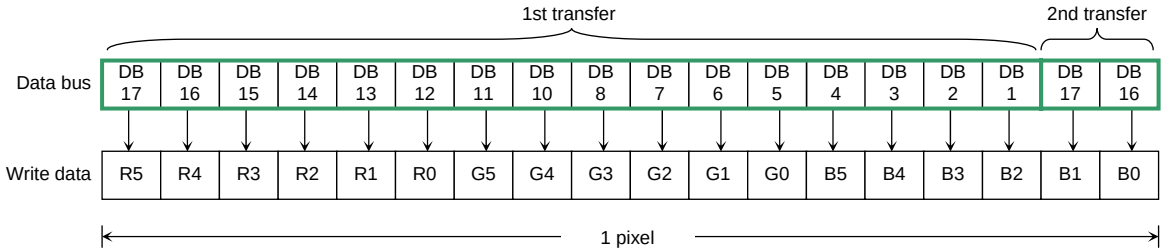


Figure 2 Example connection for the 16-bit MPU interface

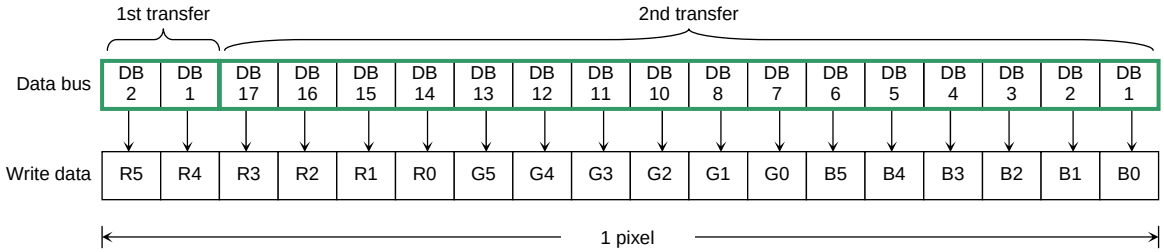
a) 16-bit MPU interface (1 transfer)

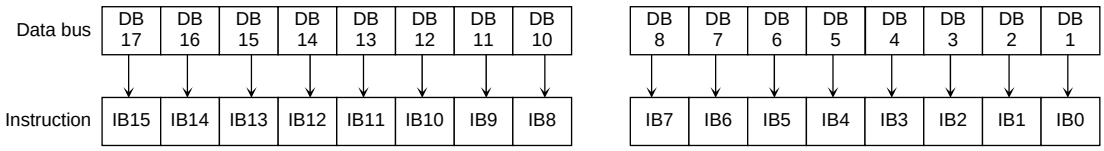


b) 16-bit MPU interface (2 transfers)



c) 16-bit MPU interface (2 transfers)





3) 9-bit MPU interface

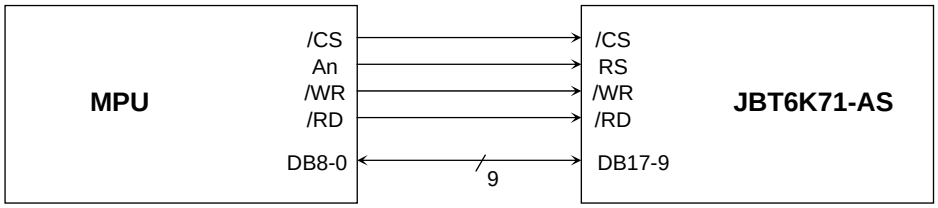
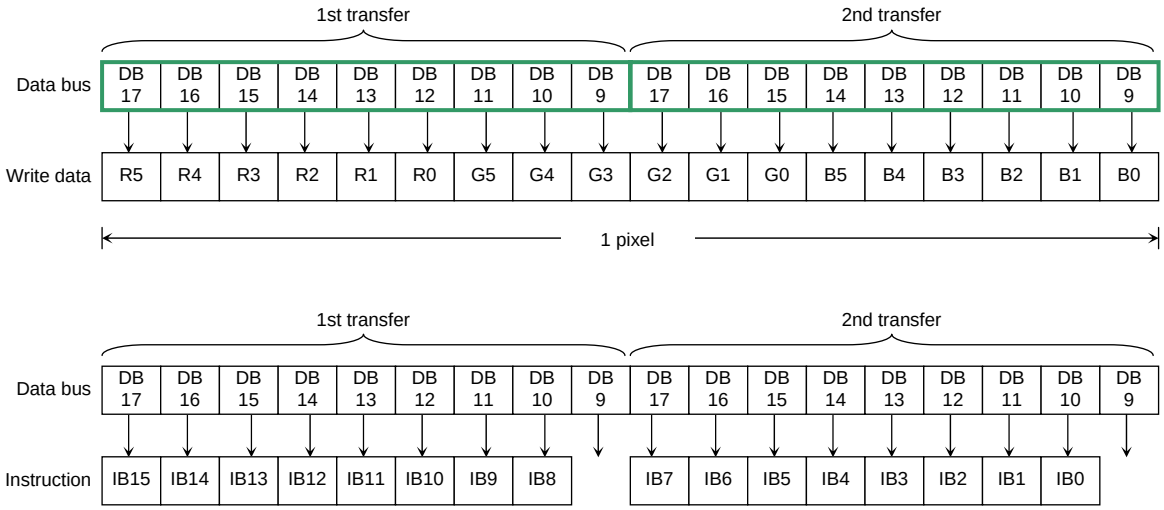


Figure 3 Example connection for the 9-bit MPU interface

a) 9-bit MPU interface (2 transfers)



4) 8-bit MPU interface

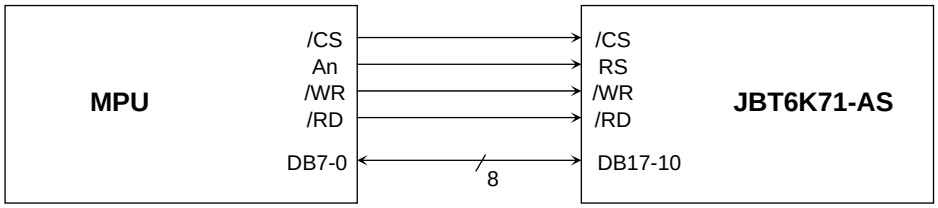
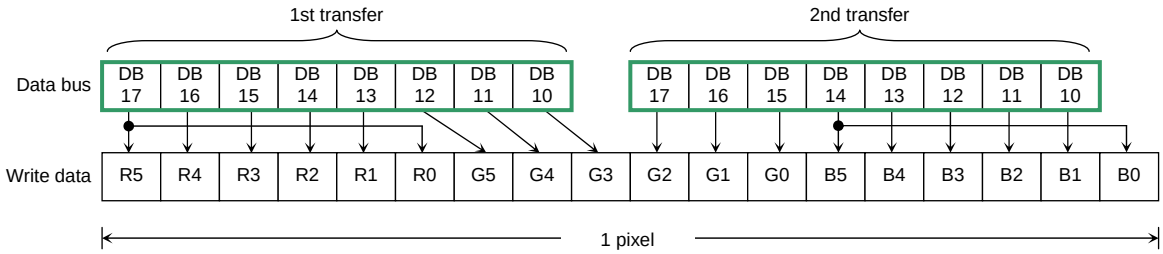
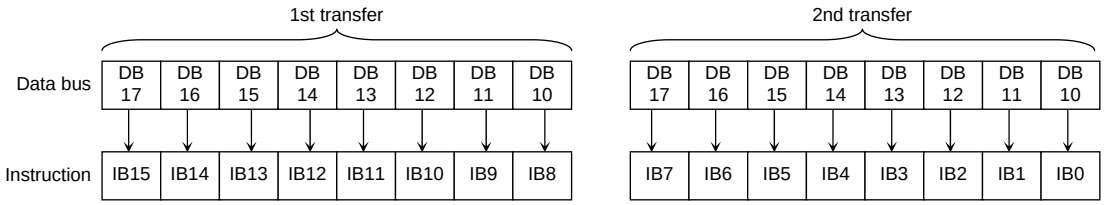


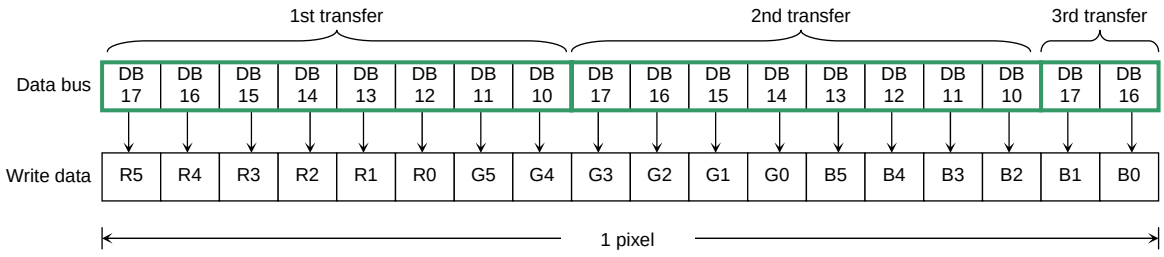
Figure 4 Example connection for the 8-bit MPU interface

a) 8-bit MPU interface (2 transfers)

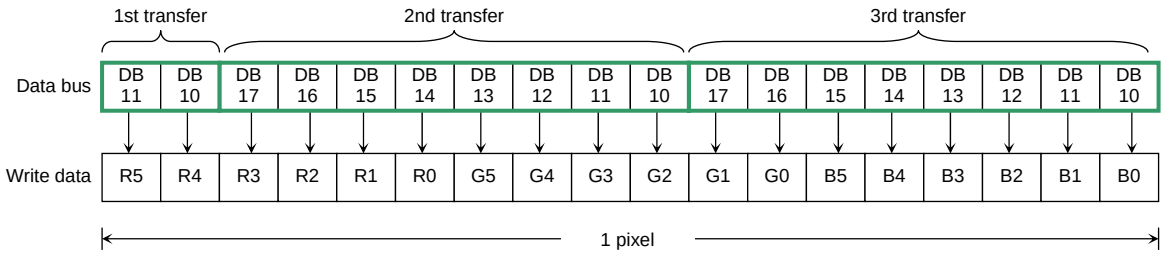




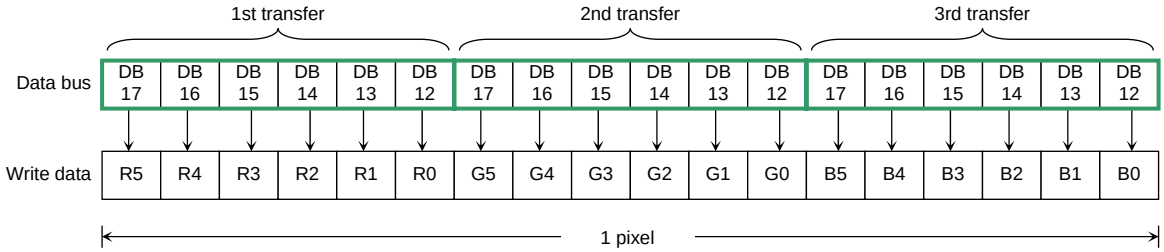
b) 8-bit MPU interface (3 transfers)



c) 8-bit MPU interface (3 transfers)

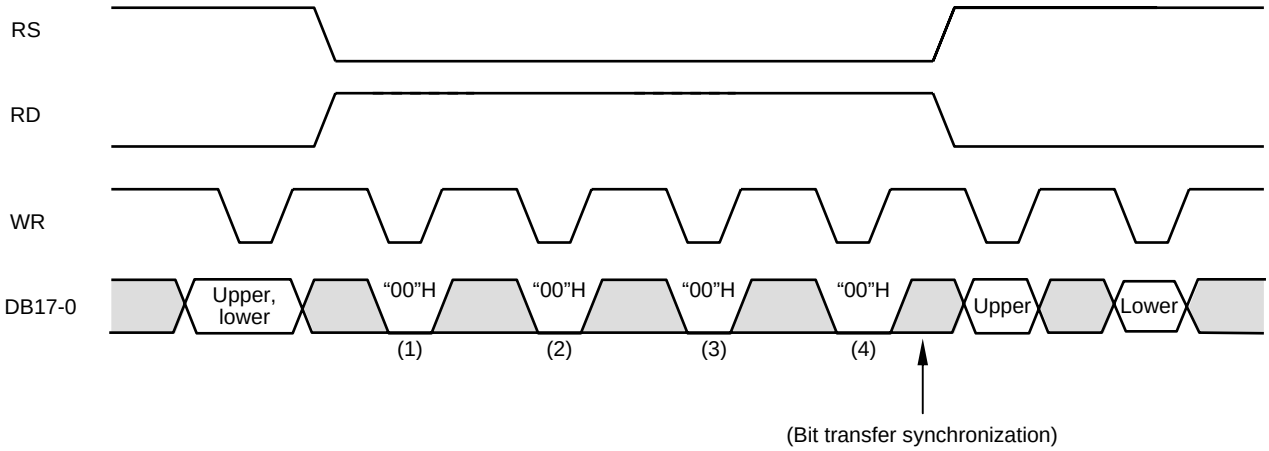


d) 8-bit MPU interface (3 transfers)



Note: Transfer synchronization for multiple-transfer interface

The JBT6K71-AS supports the transfer synchronization feature, which forcibly resets the upper/lower counters for 16-/9-/8-bit data transfers in 16-/9-/8-bit bus interface modes. If the transfers of upper and lower bit data are misaligned due to noise or other factors, four consecutive writes of “00”H instructions cause the upper/lower counters to be reset, thus ensuring that the next transfer is restarted with the upper bits. Periodically applying this synchronization can recover the device from any malfunction in the display system.



5) Serial interface

Driving the IM3, IM2, and IM1 pins to VSS, VSYS, and VSS, respectively, enables clock synchronous serial interface (SPI) transfer. The interface uses four lines: chip select (/CS), serial transfer clock (SCL), serial input data (SDI), and serial output data (SDO). When the serial interface is used, the IM0/ID pin functions as the ID pin. The DB15-DB2 pins, which are not used for the serial interface, must be tied to VSYS or VSS.

The falling edge of the /CS input represents the "start of transfer" condition, with which the JBT6K71-AS starts transferring a start byte. The rising edge of the /CS input represents the "end of transfer" condition. For chip selection, the JBT6K71-AS compares the 6-bit chip address from the sender with the 6-bit device ID code assigned to the JBT6K71-AS and, if they match, starts latching data from the next data sequence. The least significant bit of the device ID code can be specified with the ID pin. The upper five bits of the ID code must be "01110". Bit 7 of the start byte is assigned to RS (register selection) in the JBT6K71-AS. A value of "0" indicates a index register write or status read while a value of "1" indicates a data write to RAM or a data read from RAM. Two chip addresses must, therefore, be assigned to a single JBT6K71-AS device. Bit 8 of the start byte is the R/W bit. A value of "0" in the R/W bit indicates reception while a value of "1" indicates transmission.

When using the serial interface to write data to the GRAM, it is necessary to transfer two bytes of data before they are written to the GRAM. A single additional bit is appended to the least significant bit of each RB data byte (the added bit has the same content as the most significant bit of RB), after which 18 bits in total are written. After the start byte, the JBT6K71-AS sequentially sends or receives data in byte units. The transfer data format is MSB first.

All instructions of the JBT6K71-AS consist of 16 bits. An instruction is transferred by MSB-first 2-byte transfer (DB15-DB0) before being executed internally (RAM write data is internally expanded to 18 bits). Following the start byte, the JBT6K71-AS latches the first byte as the upper eight bits of the instruction and the second byte as the lower eight bits.

Note that two bytes read from RAM immediately after the start bytes are invalid. A normal data read starts from the third byte.

Table 3 Start byte format

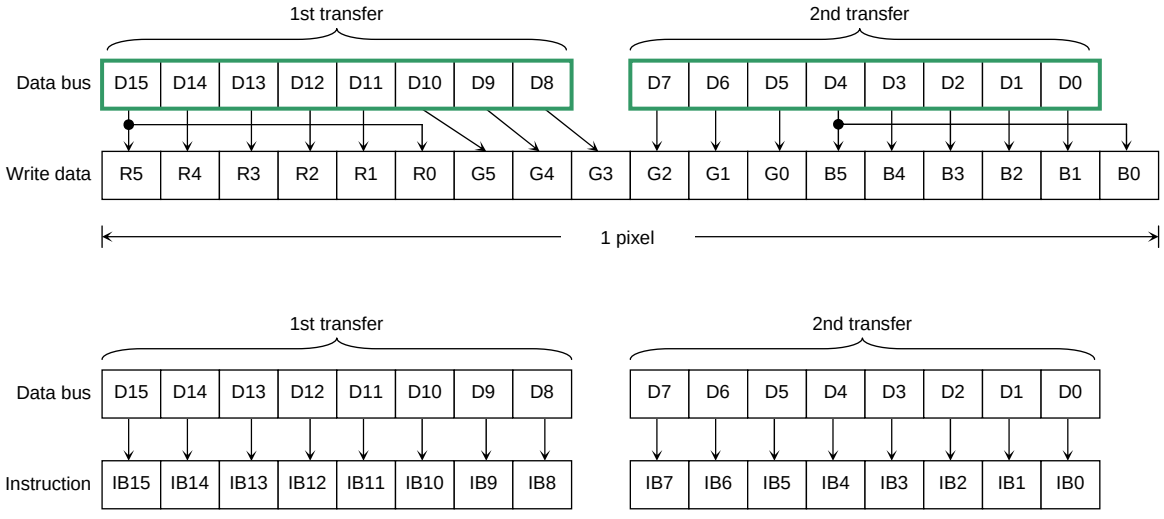
Transfer Bit Sequence	S	1	2	3	4	5	6	7	8
Start byte format	Start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: The ID bit is selected using the IM0/ID pin.

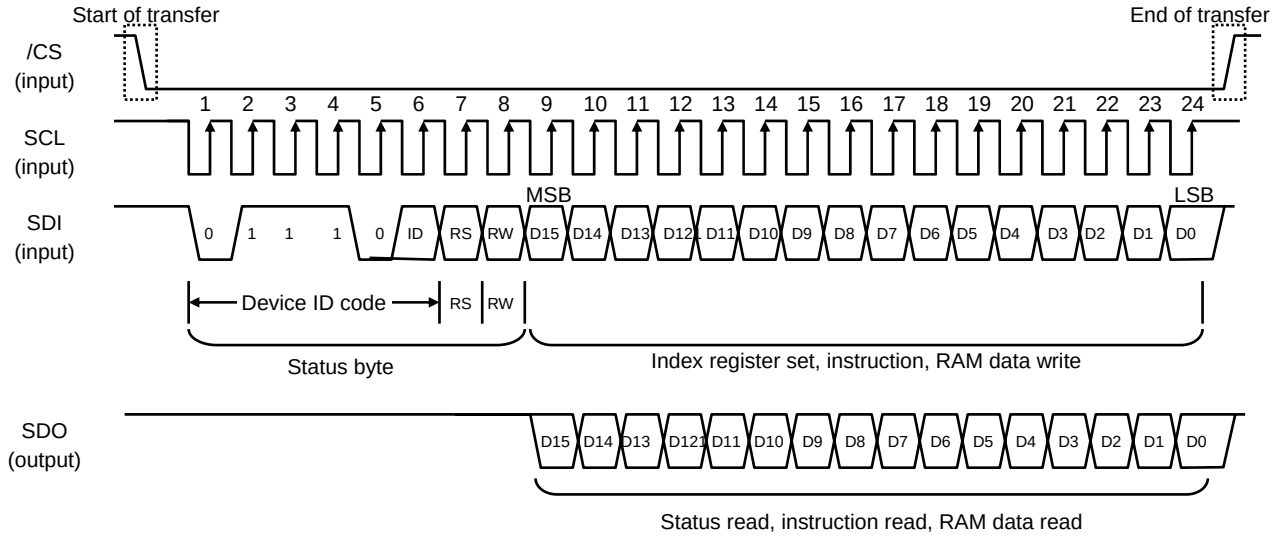
Table 4 Functions of the RS and R/W bits

RS	R/W	Function
0	0	Set the index register.
1	0	Write an instruction. Write RAM data.
1	1	Read an instruction (after 000h). Read RAM data (after 202h).

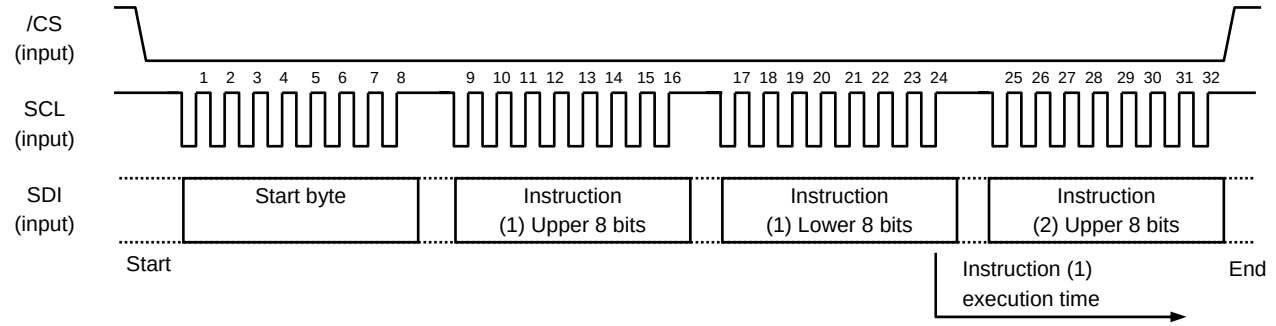
Serial interface data format:



a) Basic transfer in clock synchronous serial transfer mode

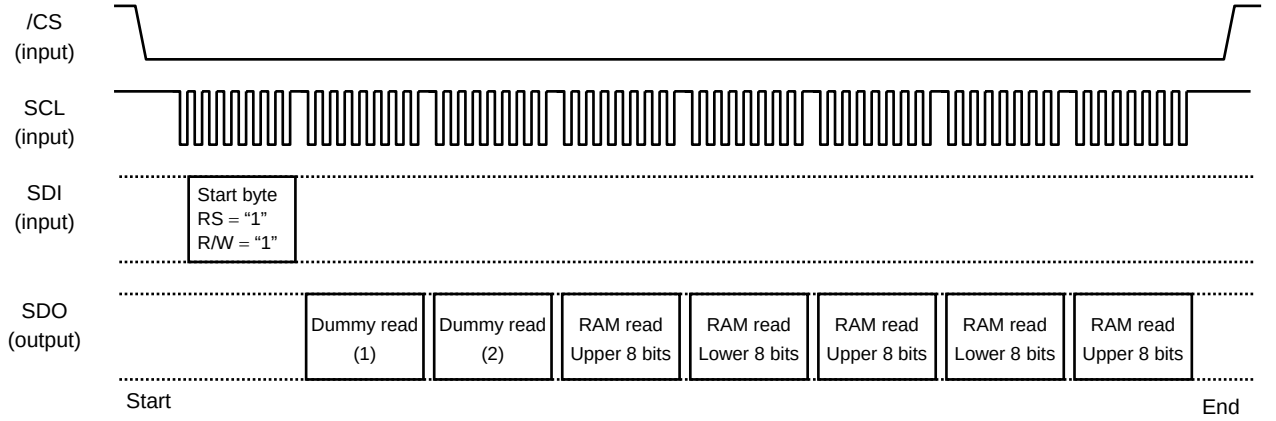


b) Continuous data transfer in clock synchronous serial transfer mode



*: The first byte after the start byte is always the upper eight bits of data.

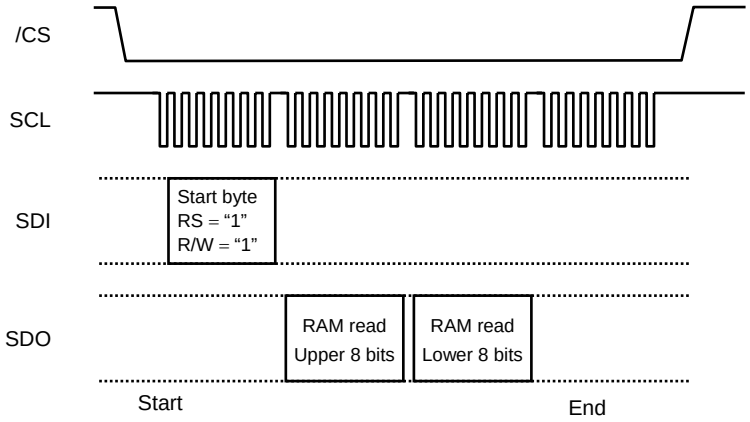
c) RAM read transfer



*: Two bytes read from RAM immediately after the start byte contains invalid data.
A normal RAM data read starts from the third byte.

Figure 5 Transfer format for clock synchronous serial interface (1)

d) Instruction read (000h)



*: Valid data is read immediately after the start byte. In this case, read data is "71xxh".

Figure 6 Transfer format for clock synchronous serial interface (2)

Data bus pins used for transferring display data

Number of Colors	Interface Mode	Number of Transfers	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
262k	18-bit mode	1 transfer	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	16-bit mode	2 transfers	O	O	O	O	O	O	O	O	—	O	O	O	O	O	O	O	O	—
	9-bit mode	2 transfers	O	O	O	O	O	O	O	O	O	—	—	—	—	—	—	—	—	—
	8-bit mode	3 transfers (1)	O	O	O	O	O	O	O	O	—	—	—	—	—	—	—	—	—	—
		3 transfers (2)	O	O	O	O	O	O	—	—	—	—	—	—	—	—	—	—	—	—
65k	16-bit mode	1 transfer	O	O	O	O	O	O	O	O	—	O	O	O	O	O	O	O	O	—
	8-bit mode	2 transfers	O	O	O	O	O	O	O	O	—	—	—	—	—	—	—	—	—	—

VSYNC Interface

The JBT6K71-AS incorporates the VSYNC interface, which can display moving images by merely using a frame synchronization signal (VSYNC) with the conventional system interface. The VSYBC interface enables display of moving images with minimum modification to the conventional system.

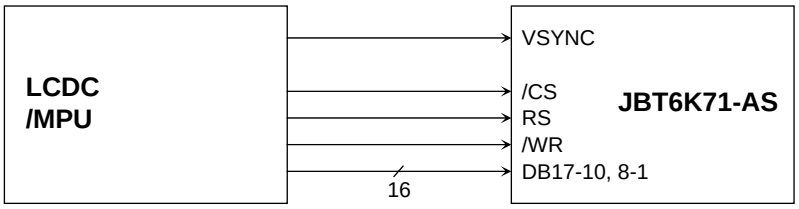
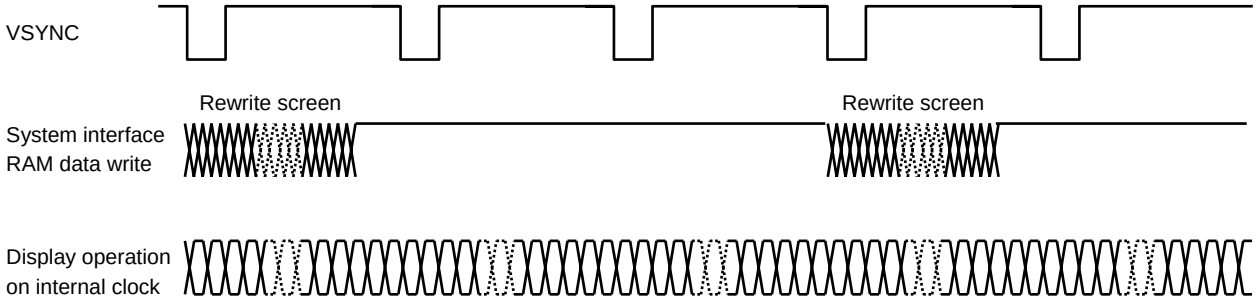


Figure 7 Example VSYNC interface

The VSYNC interface is enabled when DM1-0 = "10" and RM = "0". The VSYNC interface uses a frame synchronization signal (VSYNC) to synchronize internal display operation. The system interface can write display data to RAM a specified speed faster than internal display operation, so that the JBT6K71-AS can display moving images with the conventional interface and it can switch the screen to a moving image with no flicker.

Display operation is only based on internal clock operation and the VSYNC input. All display data is stored in RAM, so that the JBT6K71-AS can display moving images by merely transferring rewrite screen data, thus minimizing the amount of data transferred to display moving images. When the VSYNC interface is used, specifying high-speed write mode (HWM = "1") enables "low-power but high-speed" access.

- Moving image data transfer with the VSYNC interface



Note: When using the VSYNC interface, write display data in high-speed write mode (HWM = "1").

The VSYNC interface requires that the minimum RAM write speed through the system interface and the frequency of the internal oscillator satisfy the following conditions:

- The internal oscillator frequency (fosc) [Hz] = frame frequency × (display lines (NL) + front porch (FP) + back porch (BP)) × 16 clock cycles × deviation factor
- RAM write speed (min.) [Hz] > 256 × display lines (NL) / { ((back porch (BP) + display lines (NL) – margin) × 16 clock cycles) / fosc }

Note 1: If start of RAM-write does not start just after falling edge of VSYNC. It is required to count the time between falling edge of VSTNC and RAM-write.

The following shows an example of how to calculate the RAM write speed and internal oscillator frequency when the VSYNC interface is used:

Example:
- Display size: 256 RGB × 320 lines
- Number of display lines: 320 lines (NL = 100111)
- Back/front porch: 14 lines/2 lines (BP = 1110/FP = 0010)
- Frame frequency 60 Hz

The internal oscillator frequency = 60 Hz × (320 + 2 + 14) lines × 16 clock cycles × 1.1 / 0.9 = 394 kHz

Note 2: The internal oscillator frequency needs to take a deviation factor into account, as shown above. The above example considers a deviation of at least ±10% from the center value and requires the setting to fall within the VSYNC period, as shown in the following chart.

Note 3: The deviation factor for the internal oscillator in the above example includes variations due to the LSI manufacturing process and ambient temperature. It does not include external resistor or voltage variations. When designing an actual application, ensure that sufficient margins are added.

Minimum RAM write speed > 256 × 320 / { ((14 + 320 – 2) lines × 16 clock cycles) / 394 kHz } = 6.08 MHz

Note 4: The above example assumes that data is written to RAM through the VSYNC input.

Note 5: A RAM data write for a single screen must be completed with a margin of at least two lines from the display lines.

In the above example, data is written at a constant write speed higher than 6.08 MHz simultaneously with the VSYNC input, so that the RAM data for the entire screen can be rewritten faster than display operation. This prevents the rewrite screen for moving images from causing flicker.

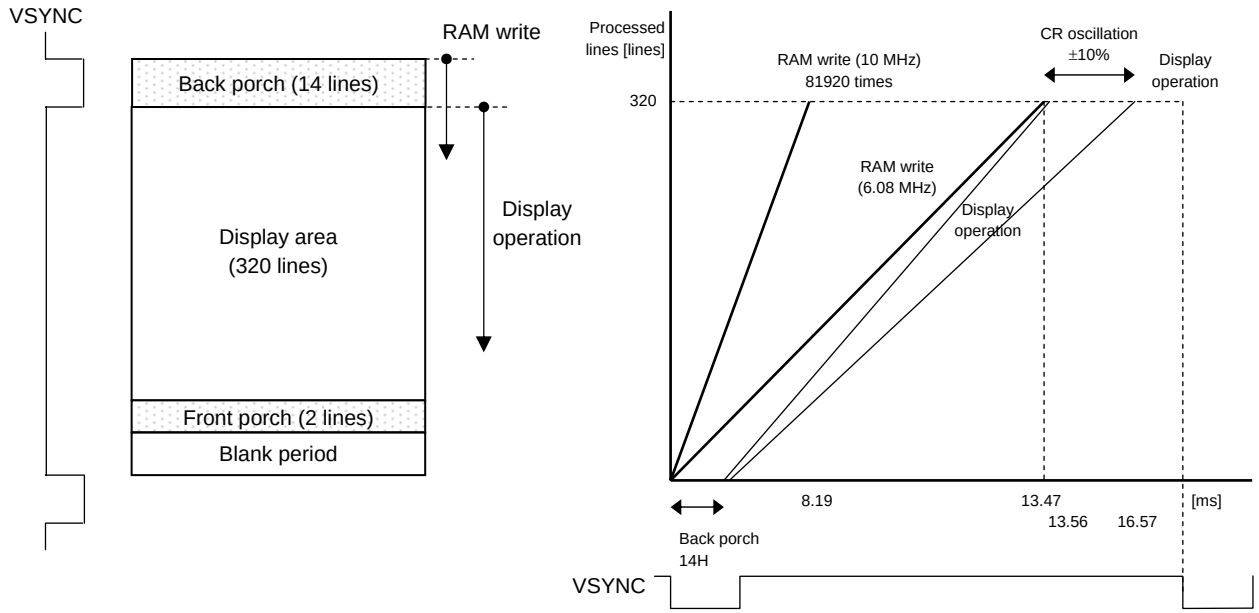


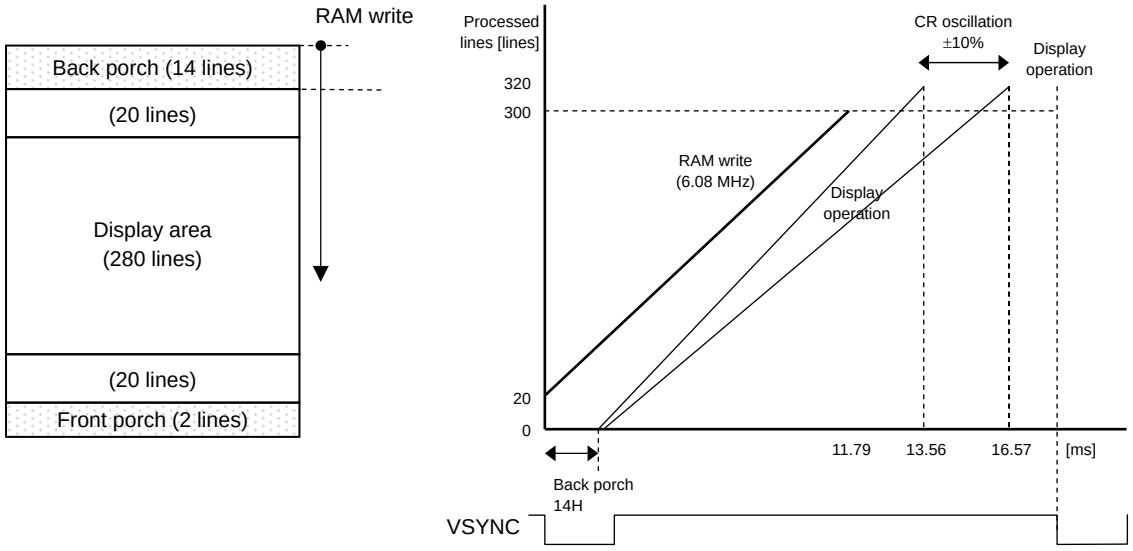
Figure 8 VSYNC interface operation

Notes on using the VSYNC interface

1) The above example only provides calculated values. The RAM write speed should be determined with a sufficient margin because the VSYNC interface requires consideration of several deviation factors with the internal oscillator.

2) The above example provides calculated values when the entire screen is rewritten. Limiting the moving image display area helps introducing a margin in the RAM write speed.

Example: Moving image display area (lines 20 to 300)



3) Once a single frame has been displayed, the front porch continues until the next VSYNC input is detected.

4) Switching between internal clock operation mode (DM1-0 = "00") and VSYNC interface mode is enabled each time a single screen has been displayed with an instruction specified.

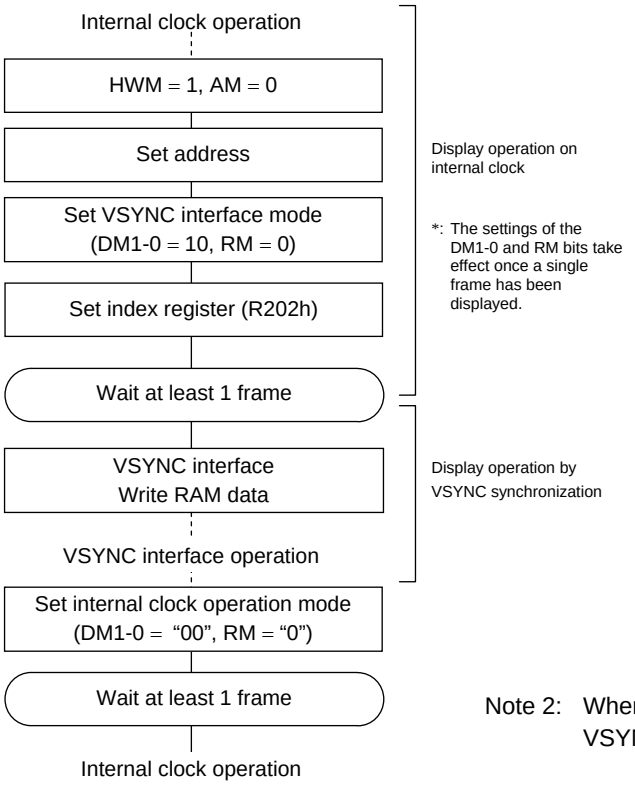
5) When the VSYNC interface is used, the split screen, vertical scroll, and interlaced drive features are disabled.

6) The VSYNC interface must be used with AM set to 0 because of the above display data transfer format.

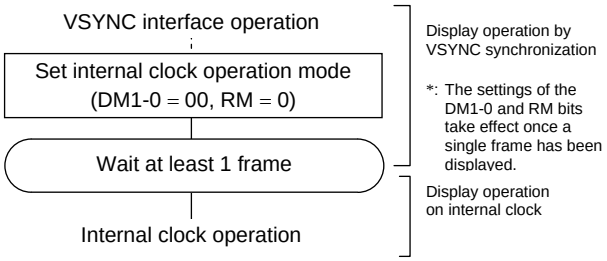
7) When using the VSYNC interface, write display data in high-speed write mode (HWM = "1").

8) When using the high-speed write mode, the fosc frequency value variation at internal oscillator. After the evaluation of module fixed synchronous condition.

[Flow of transition from internal clock operation to VSYNC interface]



[Flow of transition from VSYNC interface to internal clock operation]



Note 1: When switching to internal clock operation, supply the VSYNC signal until a wait time of at least one frame has passed.

Note 2: When switching to the VSYNC interface, input the VSYNC signal using the DM1-0 and RM settings.

External Display Interface

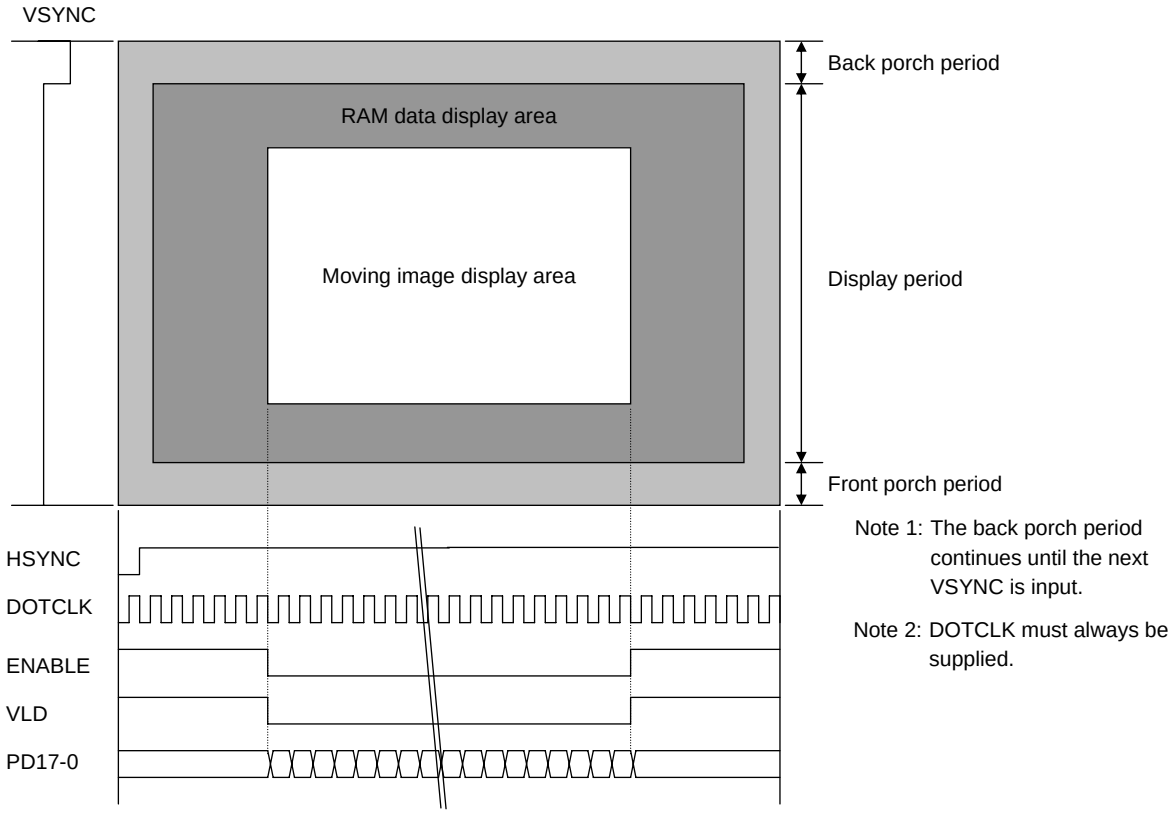
The following RGB interfaces can be selected by setting the RIM1 and RIM0 register bits. The RGB interface can also write data to the display RAM.

RIM1	RIM0	RGB Interface	PD Pins Used
0	0	18-bit RGB interface	PD17-0
0	1	16-bit RGB interface	PD17-13, 11-1
1	0	6-bit RGB interface (3 transfers)	PD17-12
1	1	Setting prohibited	

*: More than one interface cannot be used simultaneously.

1) RGB interface

The RGB interface displays data according to synchronization signals (VSYNC, HSYNC, and DOTCLK). In combination with high-speed write mode (HWM = 1) and the window addressing feature, the RGB interface can transfer data for only the area to be rewritten with low power dissipation. Front and back porches must be specified before and after the display period.



VSYNC:	Frame synchronization signal
HSYNC:	Line synchronization signal
DOTCLK:	Dot clock
ENABLE:	Data enable signal
VLD:	Data valid signal
PD17-0:	RGB (6:6:6) display data

Total Blanking Period:	268H ≥ FPP + BPP ≥ 4H
Back porch period (BPP):	14H ≥ BP3-0 ≥ 2H
Front porch period (FPP):	254H ≥ FP7-0 ≥ 2H
Display period (DP):	NL5-0 ≤ 320H
Number of lines in 1 frame:	FPP + DP + BPP

- VLD and ENABLE signals

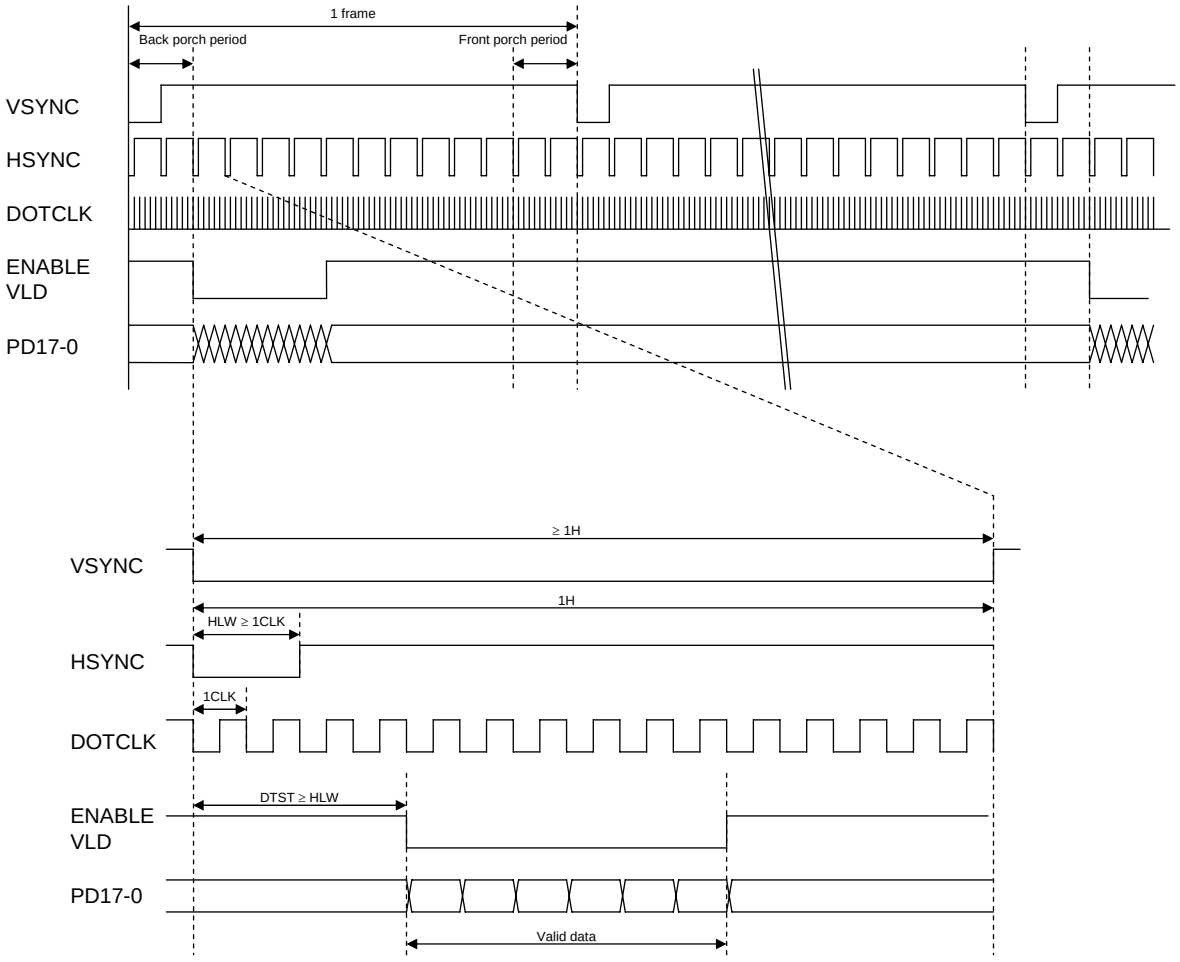
  The following table shows the relationship between the VLD and ENABLE signals.

ENABLE	VLD	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disabled	Updated
1	*	Disabled	Maintained

2) RGB interface timing

- 16-/18-bit RGB interface

  The following chart shows timing for each signal when the RGB interface is used:

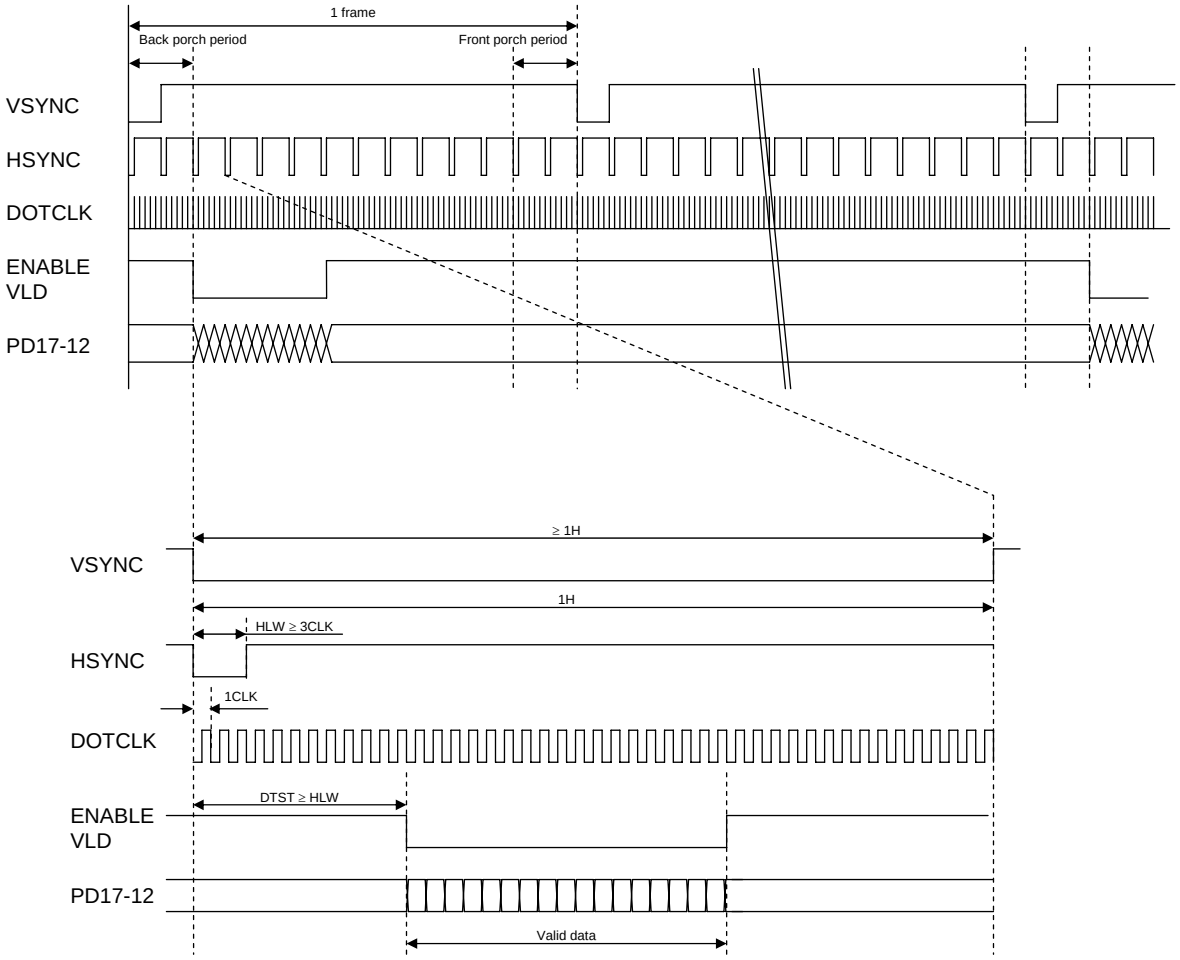


VLW: VSYNC “Low” period
HLW: HSYNC “Low” period
DTST: Data transfer start time

Note 1: When using the RGB interface, write display data in high-speed write mode (HWM = “1”).

- 6-bit RGB interface

  The following chart shows timing for each signal when the RGB interface is used:



VLW: VSYNC “Low” period
HLW: HSYNC “Low” period
DTST: Data transfer start time

Note 1: When the 6-bit interface is used, transfer data by using 3 clock cycles per pixel (RGB).

Note 2: VSYNC, HSYNC, ENABLE, DOTCLK, VLD, and PD17-12 must all operate in 3 clock cycle units.

Note 3: When using the RGB interface, write display data in high-speed write mode (HWM = “1”).

Note 4: The RGB interface can use after the fixed condition of operation clock.

3) Displaying moving images

The JBT6K71-AS incorporates an RGB interface that supports moving image display and a RAM that stores display data. Those provide the following benefits in moving image display:

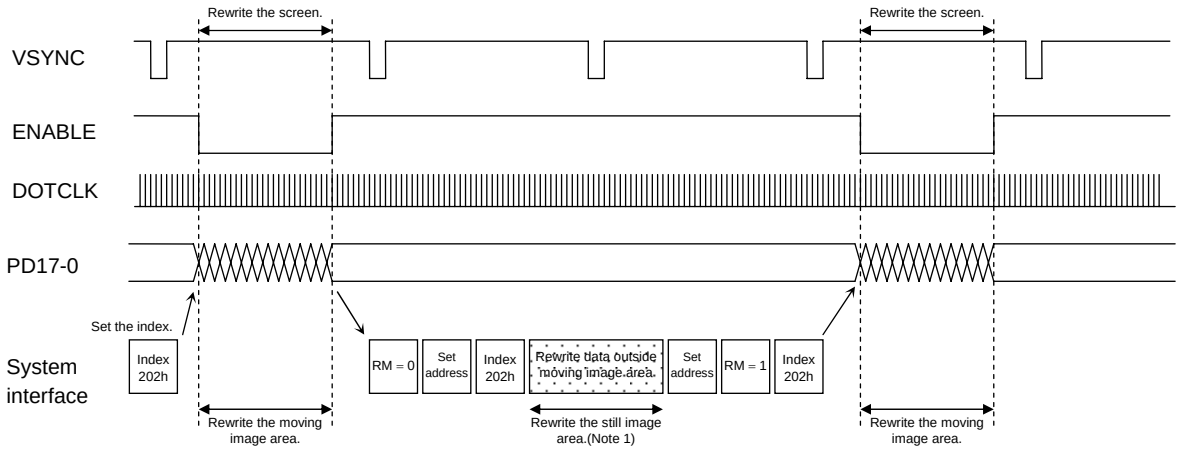
- Window addressing enables transfer of data only for a moving image area.
- High-speed write mode enables low-power, high-speed access.
- Only the rewrite screen data need to be transferred.
- Reduction in the amount of transferred data results in low power dissipation in the entire system.
- The system interface can be simultaneously used to update a still image area (such as an icon) while a moving image is displayed.

- Using the system interface for RAM access while using the RGB interface

When using the RGB interface, it is also possible to access RAM through the system interface. When the RGB interface is used, however, RAM writes are constantly performed for the DOTCLK input while ENABLE = "Low". When writing data to RAM using the system interface, first drive ENABLE high to stop display data writes from the RGB interface. Clearing RM to 0 enables RAM accesses through the system interface. When returning to the RGB interface, wait for a specified write/read bus cycle time and then set RM to 1 and the index to R202h before starting a RAM access through the RGB interface. If RAM accesses from the system and RGB interfaces conflict, write data is not guaranteed.

In the following example, the system interface updates display data for a still image area while the RGB interface displays a moving image:

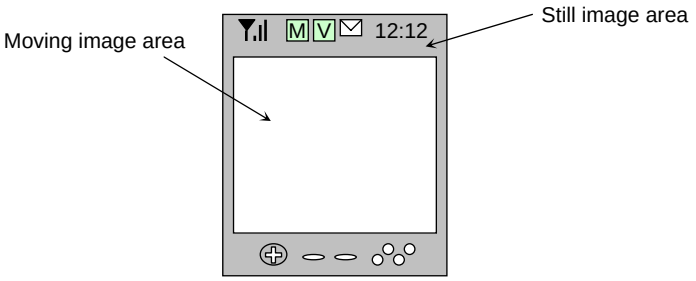
Example: Rewriting a still image area while displaying a moving image



Note 1: When the RGB interface is used, an address is set on each falling edge of VSYNC.

Note 2: The address and index must be set before the RGB interface starts a RAM access.

Note 3: When using the RGB interface, always use high-speed write mode.



4) 6-bit RGB interface

Setting RIM1-0 to "10" enables the 6-bit interface. In this mode, the JBT6K71-AS displays data using the VSYNC, HSYNC, and DOTCLK synchronization signals. 6 bits of RGB data (PD17-PD12) are transferred to the display RAM in synchronization with display operation, using the data valid signal (VLD) and data enable signal (ENABLE). The PD11-PD0 pins, which are not used, must be tied to the VDD or VSS level. Instructions can only be set from the MPU interface.

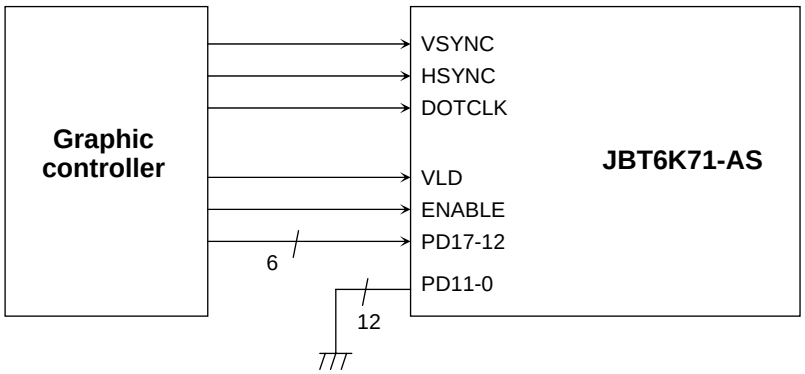


Figure 9 6-bit RGB interface

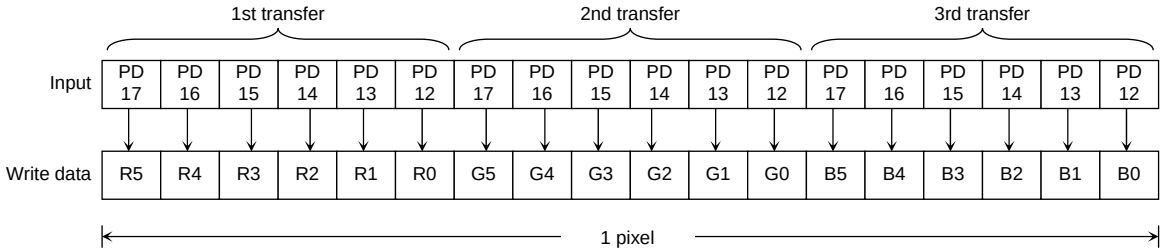
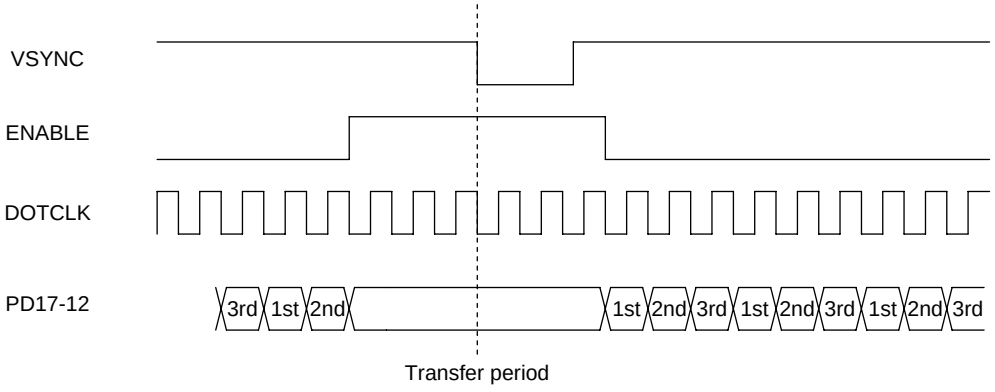


Figure 10 Data format for the 6-bit interface

Note: Transfer synchronization for the 6-bit interface

The JBT6K71-AS incorporates a transfer counter that counts the first, second, and third data transfers for the 6-bit RGB interface. The falling edge of VSYNC resets the transfer counter to the first transfer state. If a misaligned transfer occurs, the transfer is always reset to the first data transfer at the beginning of each frame (on the falling edge of VSYNC), so that data transfer can be restarted normally from the next frame. This feature enables the JBT6K71-AS to restore normal display with effects of any misaligned transfer minimized, when displaying a moving image or transferring a sequence of data.

Note: Internal display operation is performed in pixel units (RGB: 3DOTCLK). If the number of DOTCLK cycles for a single frame is other than a multiple of the pixel unit, clock misalignment occurs, resulting in the current and next frames being displayed incorrectly.



5) 16-bit RGB interface

Setting RIM1-0 to "01" enables the 16-bit interface. In this mode, the JBT6K71-AS displays data using the VSYNC, HSYNC, and DOTCLK synchronization signals. 16 bits of RGB data (PD17-PD13 and PD11-PD1) are transferred to the display RAM in synchronization with display operation, using the data valid signal (VLD) and data enable signal (ENABLE). The PD12 and PD0 pins, which are not used, must be tied to the VDD or VSS level. Instructions can only be set from the MPU interface.

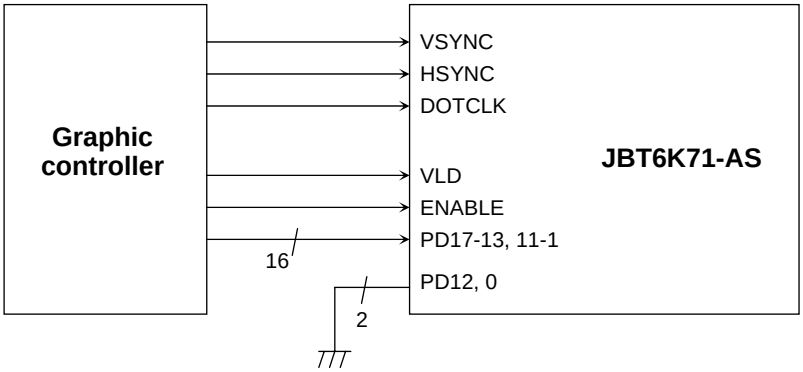


Figure 11 16-bit RGB interface

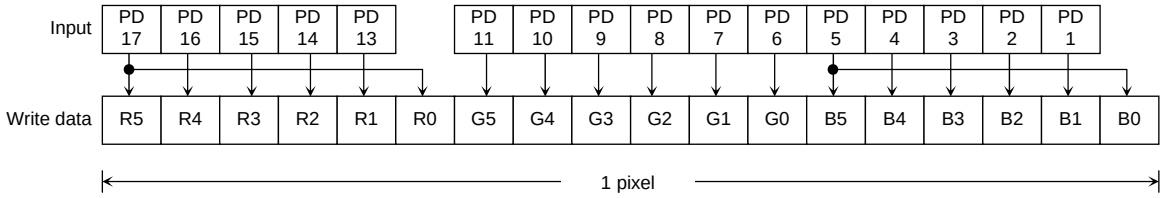


Figure 12 Data format for the 16-bit interface

6) 18-bit RGB interface

Setting RIM1-0 to "00" enables the 18-bit interface. In this mode, the JBT6K71-AS displays data using the VSYNC, HSYNC, and DOTCLK synchronization signals. 18 bits of RGB data (PD17-PD0) are transferred to the display RAM in synchronization with display operation, using the data valid signal (VLD) and data enable signal (ENABLE). Instructions can only be set from the MPU interface.

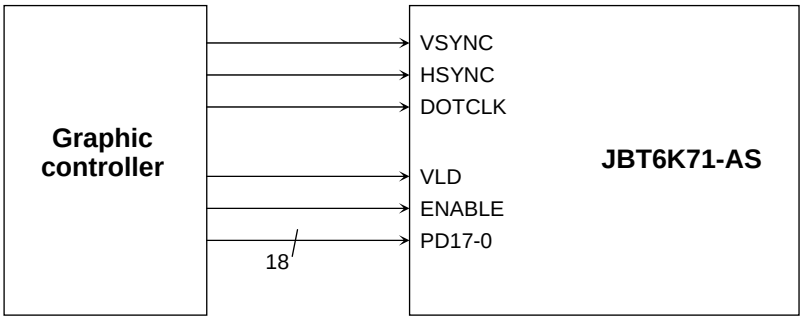


Figure 13 18-bit RGB interface

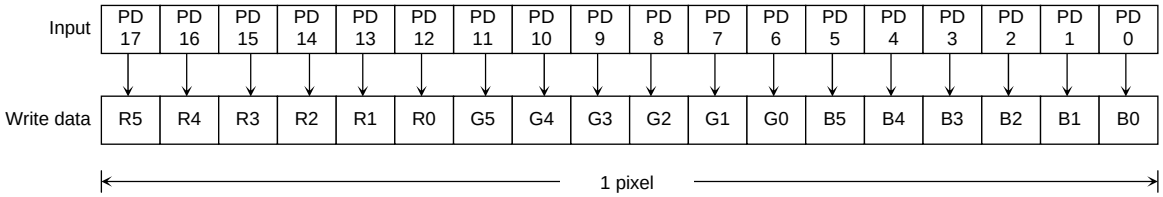


Figure 14 Data format for the 18-bit interface

* The 18-bit RGB interface enables the use of 262,144 colors.

7) Notes on using the external display interface

a) Note that the following features are disabled when the external display interface is used.

Feature	External Display Interface	Internal Display Operation
Split screen display	Disabled	Enabled
Scrollable display	Disabled	Enabled
Graphic operation	Disabled	Enabled

b) VSYNC, HSYNC, and DOTCLK must be supplied constantly while the RGB interface is used for display.

c) The 6-bit RGB interface transfers RGB data using three clock cycles. Data must always be transferred in RGB units.

d) When using the 6-bit RGB interface, set interface signals (VSYNC, HSYNC, DOTCLK, ENABLE, VLD, and PD17-PD0) in pixel (RGB) units according to RGB transfer.

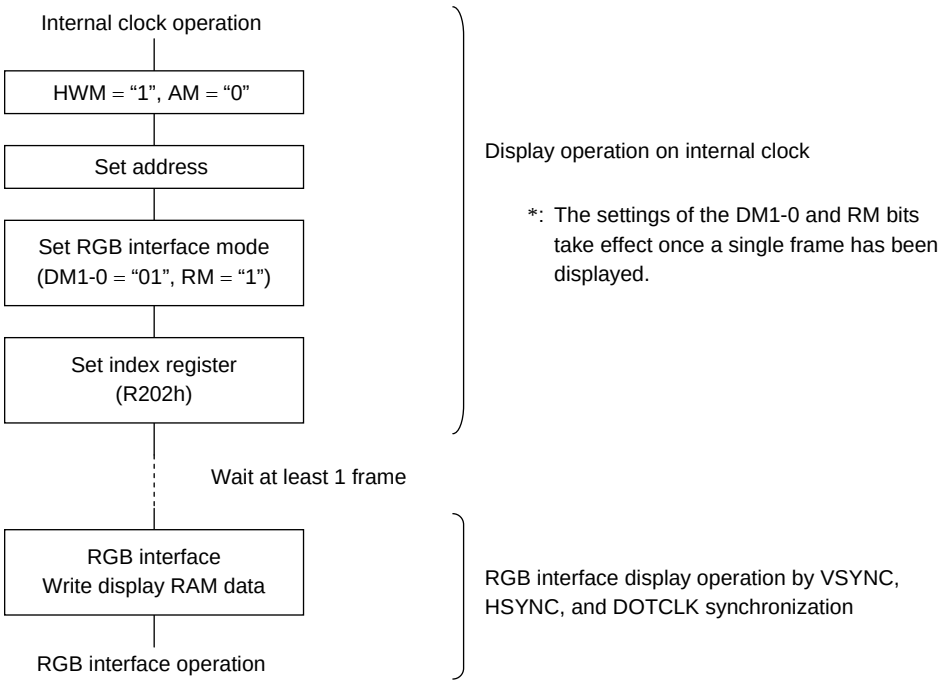
e) When switching between internal operation mode and external display interface mode, use the following mode switching sequence.

f) Once a single frame has been displayed with the RGB interface, the front porch continues until the next VSYNC input is detected.

g) The RGB interface must be used in high-speed write mode (HWM = "1").

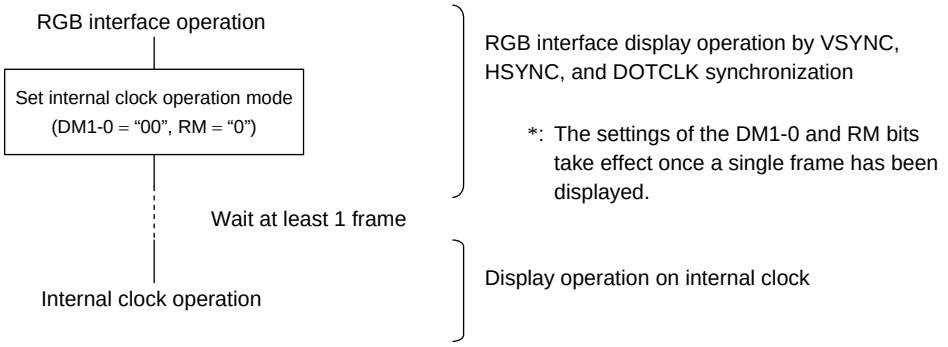
h) When the RGB interface is used, an address is set on the falling edge of VSYNC for each frame.

i) When the RGB interface is used, not changed the operation clock condition.



Note: When switching to the RGB interface, input the RGB interface signals (VSYNC, HSYNC, DOTCLK, and ENABLE) before setting DM1-0.

Figure 15 Flow of transition from internal clock operation to RGB interface (1)



Note: When switching to internal operation, supply the RGB interface signals (VSYNC, HSYNC, DOTCLK, and ENABLE) until a wait time of at least one frame has passed.

Figure 16 Flow of transition from RGB interface (1) to internal clock operation

Flow of RAM data write from the system interface during display using the RGB interface

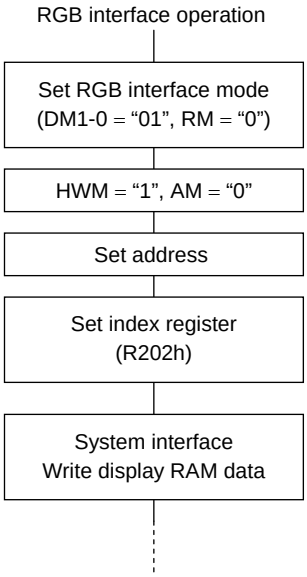


Figure 17 Flow of transition from RGB interface (1) to RGB interface (2)

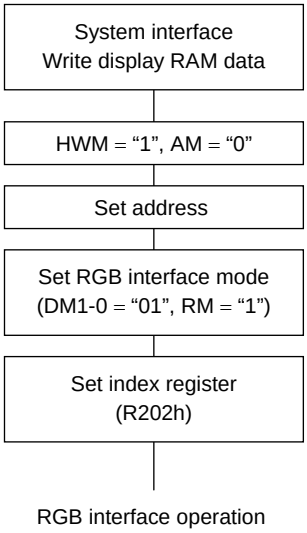


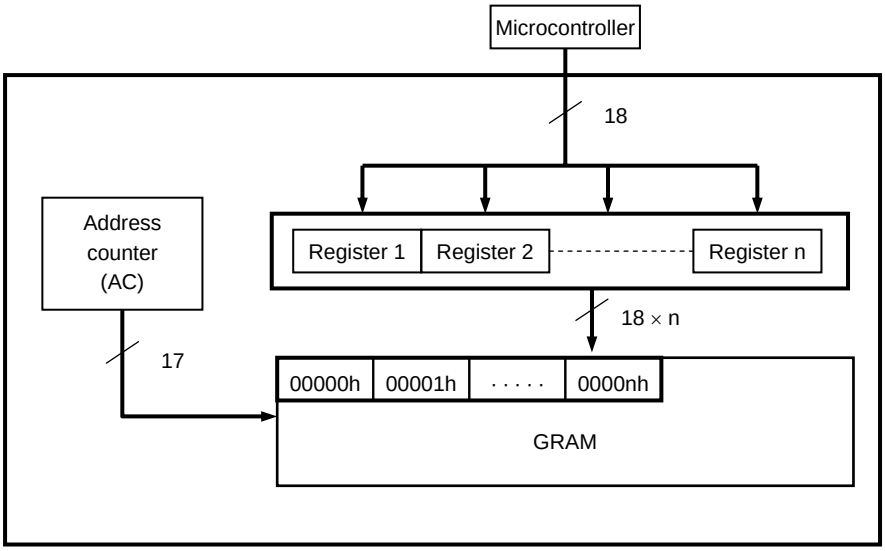
Figure 18 Flow of transition from RGB interface (2) to RGB interface (1)

High-Speed Burst RAM Write

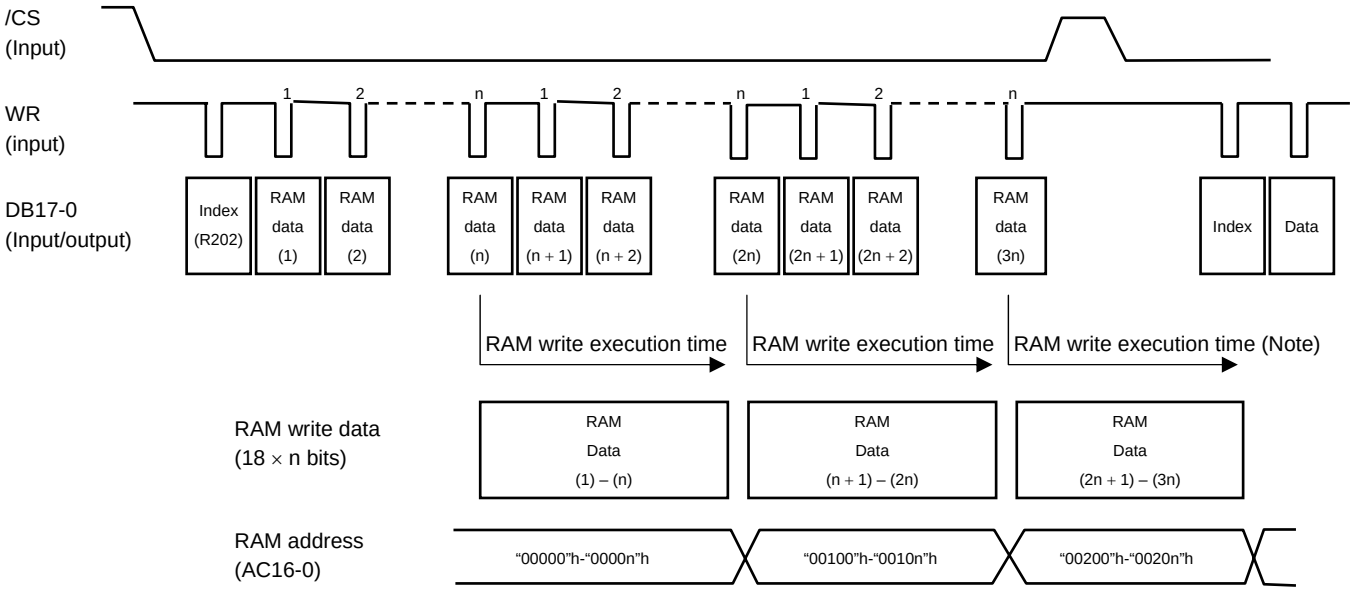
The JBT6K71-AS supports a high-speed burst RAM write feature. The JBT6K71-AS is thus suitable for an application that requires fast rewriting of display data, such as displaying color moving images.

When high-speed RAM write mode (HWM="1") is selected, RAM write data is temporarily stored in a T6K65 internal register. Once data corresponding to a single line in the window has been stored, the data is written to internal RAM at one time. Next data can be written to the internal register during a batch write to RAM. This capability enables fast, continuous RAM write operation, required for displaying moving images.

a) Flow of high-speed, continuous RAM writes operation

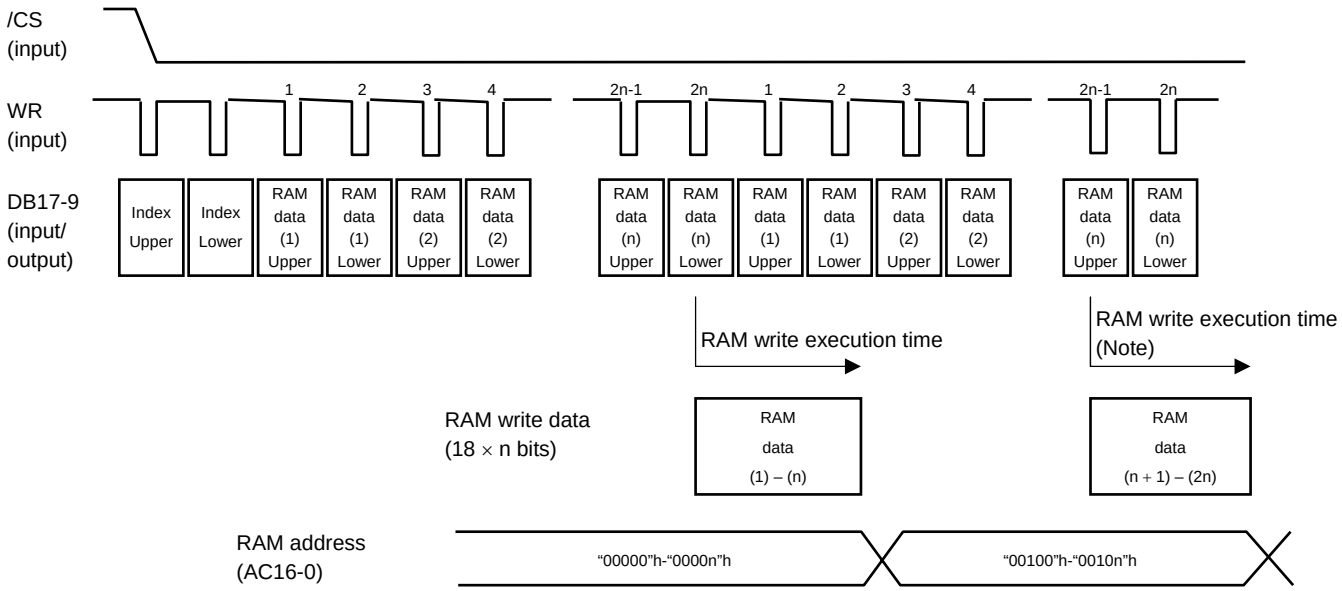


b) Example of high-speed, continuous RAM writes operation



Note: When exiting from high-speed RAM write mode, first wait as long as the RAM write execution time, which equals to the bus cycle time (tCYC) in normal write mode, before issuing the next instruction.

c) Example of high-speed, continuous RAM writes operation (with the 9-bit interface)



Note: The high-speed burst RAM write feature performs a single write per n words. When the 9-bit interface is used, a RAM write takes place every time n × 2 data units have been written.

When using high-speed RAM write mode, note the following:

Note 1: Because RAM writes are performed in line units, any data ending before the window width is not written to RAM.

Note 2: Immediately after the index register is set to RAM data write mode (“202”H), the first write takes place. A RAM data read cannot be performed simultaneously. When reading data from RAM, set HWM to “0”.

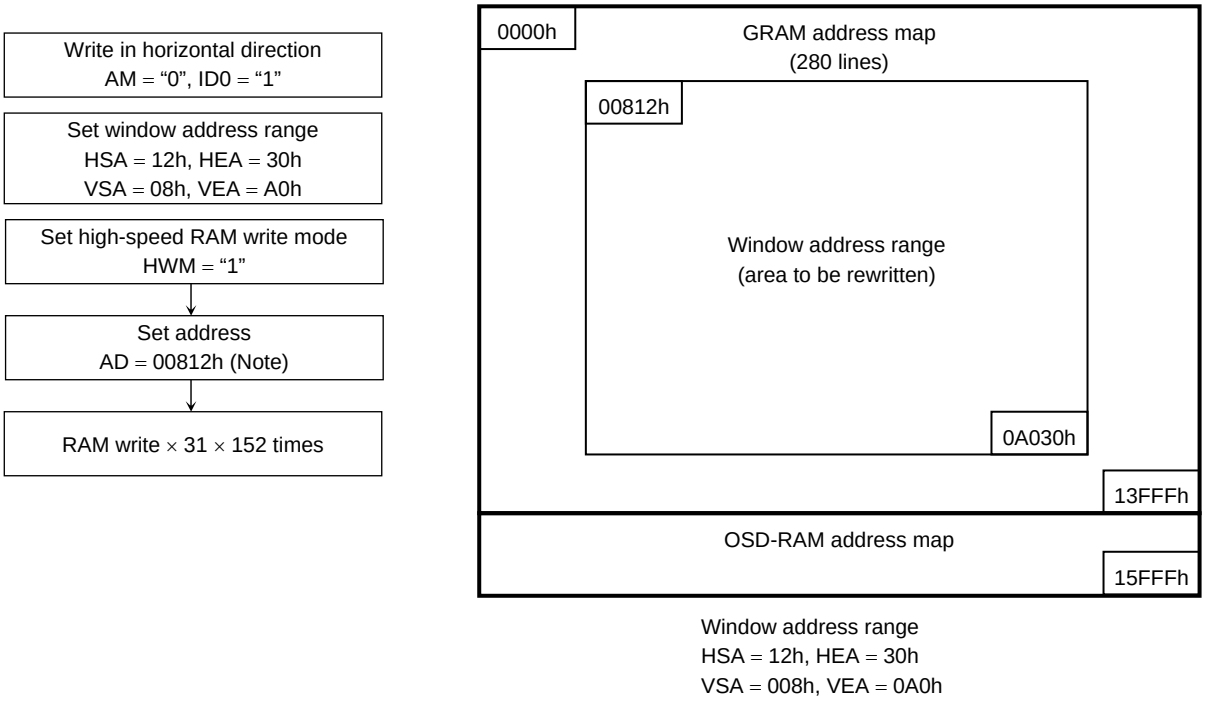
Note 3: A high-speed RAM write and a normal write cannot be used together. When using the other write mode, change the mode and set an address before restarting write operation.

	Normal RAM Write (HWM = “0”)	High-speed RAM Write (HWM = “1”)
BGR feature	Available	Available
Write mask	Available	Available
Setting a RAM address	Can be specified in word units	Can be specified in word units
RAM read	Can be read in word units	Not allowed
RAM write	Can be written in word units	Can be written in line units
Window address	Can be specified in word units (Minimum range: 1 word × 1 line)	Can be specified in word units; at least eight words (Minimum range: 8 words × 1 line)
RGB interface	RAM write not available	RAM write available

High-speed RAM write with window addressing

Window addressing enables RAM data within a specified rectangular area to be rewritten continuously at high speed.

The following shows an example of high-speed RAM write with window addresses specified.
The area within the window range specified with the HSA7-0 and HEA7-0 bits can be rewritten continuously at high speed.

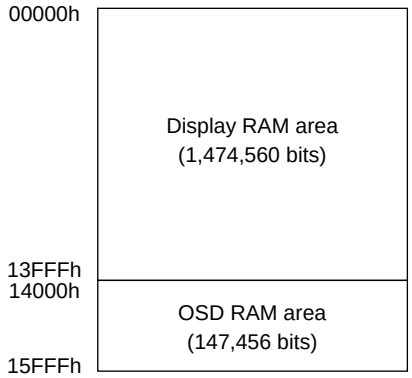


Note: An address within the window must be set.

Note: Without the window data is not agreement.

Display RAM and OSD RAM Configurations

The JBT6K71-AS (AS) incorporates display RAM and OSD RAM. The display RAM consists of 256 × 18 (bits) × 320 (lines) = 1,474,560 bits. The OSD RAM consists of 256 × 18 (bits) × 16 (lines) × 2 (windows) = 147,456 bits. The total of 1,622,016 bits for display RAM and OSD RAM are mapped continuously in memory space, so that a write to display RAM can be directly followed by a write to OSD RAM.



The following table shows the addresses assigned to display RAM and OSD RAM:

OSDW	Display RAM Address	OSD (1) RAM Address	OSD (2) RAM Address
0	“00000”h~“13FFF”h	“14000”h~“14FFF”h	“15000”h~“15FFF”h
1	Cannot be accessed.	“00000”h~“00FFF”h	“01000”h~“01FFF”h

Display RAM

The display RAM consists of 18 bits (RGB) per dot. Memory addresses are allocated to different JBT6K71-AS(A) output pins, thus facilitating image processing. The following table shows the correspondence between RAM addresses and display locations:

Display RAM address assignment when SS = "0"

Output Pin/ Display Line	S1	S2	S3	S4	S5		S255	S256
	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0		PD PD 17 ····· 0	PD PD 17 ····· 0
Line 1	"00000"h	"00001"h	"00002"h	"00003"h	"00004"h	·····	"000FE"h	"000FF"h
Line 2	"00100"h	"00101"h	"00102"h	"00103"h	"00104"h	·····	"001FE"h	"001FF"h
Line 3	"00200"h	"00201"h	"00202"h	"00203"h	"00204"h	·····	"002FE"h	"002FF"h
Line 4	"00300"h	"00301"h	"00302"h	"00303"h	"00304"h	·····	"003FE"h	"003FF"h
Line 5	"00400"h	"00401"h	"00402"h	"00403"h	"00404"h	·····	"004FE"h	"004FF"h
Line 6	"00500"h	"00501"h	"00502"h	"00503"h	"00504"h	·····	"005FE"h	"005FF"h
Line 7	"00600"h	"00601"h	"00602"h	"00603"h	"00604"h	·····	"006FE"h	"006FF"h
Line 8	"00700"h	"00701"h	"00702"h	"00703"h	"00704"h	·····	"007FE"h	"007FF"h
Line 9	"00800"h	"00801"h	"00802"h	"00803"h	"00804"h	·····	"008FE"h	"008FF"h
Line 10	"00900"h	"00901"h	"00902"h	"00903"h	"00904"h	·····	"009FE"h	"009FF"h
Line 11	"00A00"h	"00A01"h	"00A02"h	"00A03"h	"00A04"h	·····	"00AFE"h	"00AFF"h
Line 12	"00B00"h	"00B01"h	"00B02"h	"00B03"h	"00B04"h	·····	"00BFE"h	"00BFF"h
Line 13	"00C00"h	"00C01"h	"00C02"h	"00C03"h	"00C04"h	·····	"00CFE"h	"00CFF"h
Line 14	"00D00"h	"00D01"h	"00D02"h	"00D03"h	"00D04"h	·····	"00DFE"h	"00DFF"h
Line 15	"00E00"h	"00E01"h	"00E02"h	"00E03"h	"00E04"h	·····	"00EFE"h	"00EFF"h
Line 16	"00F00"h	"00F01"h	"00F02"h	"00F03"h	"00F04"h	·····	"00FFE"h	"00FFF"h
Line 17	"01000"h	"01001"h	"01002"h	"01003"h	"01004"h	·····	"010FE"h	"010FF"h
Line 18	"01100"h	"01101"h	"01102"h	"01103"h	"01104"h	·····	"011FE"h	"011FF"h
Line 19	"01200"h	"01201"h	"01202"h	"01203"h	"01204"h	·····	"012FE"h	"012FF"h
Line 20	"01300"h	"01301"h	"01302"h	"01303"h	"01304"h	·····	"013FE"h	"013FF"h
• • • •	• • • •	• • • •	• • • •	• • • •	• • • •	• • • •	• • • •	• • • •
Line 317	"13C00"h	"13C01"h	"13C02"h	"13C03"h	"13C04"h	·····	"13CFE"h	"13CFF"h
Line 318	"13D00"h	"13D01"h	"13D02"h	"13D03"h	"13D04"h	·····	"13DFE"h	"13DFF"h
Line 319	"13E00"h	"13E01"h	"13E02"h	"13E03"h	"13E04"h	·····	"13EFE"h	"13EFF"h
Line 320	"13F00"h	"13F01"h	"13F02"h	"13F03"h	"13F04"h	·····	"13FFE"h	"13FFF"h

Display RAM address assignment when SS = “1”

Output Pin/ Display Line	S1	S2	S3	S4	S5		S255	S256
	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0		PD PD 17 ····· 0	PD PD 17 ····· 0
Line 1	“000FF”h	“000FE”h	“000FD”h	“000FC”h	“000FB”h	·····	“00001”h	“00000”h
Line 2	“001FF”h	“001FE”h	“001FD”h	“001FC”h	“001FB”h	·····	“00101”h	“00100”h
Line 3	“002FF”h	“002FE”h	“002FD”h	“002FC”h	“002FB”h	·····	“00201”h	“00200”h
Line 4	“003FF”h	“003FE”h	“003FD”h	“003FC”h	“003FB”h	·····	“00301”h	“00300”h
Line 5	“004FF”h	“004FE”h	“004FD”h	“004FC”h	“004FB”h	·····	“00401”h	“00400”h
Line 6	“005FF”h	“005FE”h	“005FD”h	“005FC”h	“005FB”h	·····	“00501”h	“00500”h
Line 7	“006FF”h	“006FE”h	“006FD”h	“006FC”h	“006FB”h	·····	“00601”h	“00600”h
Line 8	“007FF”h	“007FE”h	“007FD”h	“007FC”h	“007FB”h	·····	“00701”h	“00700”h
Line 9	“008FF”h	“008FE”h	“008FD”h	“008FC”h	“008FB”h	·····	“00801”h	“00800”h
Line 10	“009FF”h	“009FE”h	“009FD”h	“009FC”h	“009FB”h	·····	“00901”h	“00900”h
Line 11	“00AFF”h	“00AFE”h	“00AFD”h	“00AFC”h	“00AFB”h	·····	“00A01”h	“00A00”h
Line 12	“00BFF”h	“00BFE”h	“00BFD”h	“00BFC”h	“00BFB”h	·····	“00B01”h	“00B00”h
Line 13	“00CFF”h	“00CFE”h	“00CFD”h	“00CFC”h	“00CFB”h	·····	“00C01”h	“00C00”h
Line 14	“00DFF”h	“00DFE”h	“00DFD”h	“00DFC”h	“00DFB”h	·····	“00D01”h	“00D00”h
Line 15	“00EFF”h	“00EFE”h	“00EFD”h	“00EFC”h	“00EFB”h	·····	“00E01”h	“00E00”h
Line 16	“00FFF”h	“00FFE”h	“00FFD”h	“00FFC”h	“00FFB”h	·····	“00F01”h	“00F00”h
Line 17	“010FF”h	“010FE”h	“010FD”h	“010FC”h	“010FB”h	·····	“01001”h	“01000”h
Line 18	“011FF”h	“011FE”h	“011FD”h	“011FC”h	“011FB”h	·····	“01101”h	“01100”h
Line 19	“012FF”h	“012FE”h	“012FD”h	“012FC”h	“012FB”h	·····	“01201”h	“01200”h
Line 20	“013FF”h	“013FE”h	“013FD”h	“013FC”h	“013FB”h	·····	“01301”h	“01300”h
• • • •	• • • •	• • • •	• • • •	• • • •	• • • •	• • • •	• • • •	• • • •
Line 317	“13CFF”h	“13CFE”h	“13CFD”h	“13CFC”h	“13CFB”h	·····	“13C01”h	“13C00”h
Line 318	“13DFF”h	“13DFE”h	“13DFD”h	“13DFC”h	“13DFB”h	·····	“13D01”h	“13D00”h
Line 319	“13EFF”h	“13EFE”h	“13EFD”h	“13EFC”h	“13EFB”h	·····	“13E01”h	“13E00”h
Line 320	“13FFF”h	“13FFE”h	“13FFD”h	“13FFC”h	“13FFB”h	·····	“13F01”h	“13F00”h

OSD RAM

The OSD RAM consists of 18 bits (RGB) per dot. The OSD RAM addresses are mapped immediately after the display RAM addresses, so that a write to OSD RAM can easily follow a write to display RAM.

Managing the OSD RAM area is also easy because a command can specify the OSD RAM as an independent address space.

OSD (1) RAM address assignment when SS = "0" (OSDON = "*" / OSDW = "1")

Output Pin/ Display Line	S1	S2	S3	S4	S5		S255	S256
	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0		PD PD 17 ····· 0	PD PD 17 ····· 0
Line 1	"00000"h	"00001"h	"00002"h	"00003"h	"00004"h	·····	"000FE"h	"000FF"h
Line 2	"00100"h	"00101"h	"00102"h	"00103"h	"00104"h	·····	"001FE"h	"001FF"h
Line 3	"00200"h	"00201"h	"00202"h	"00203"h	"00204"h	·····	"002FE"h	"002FF"h
• •	• •	• •	• •	• •	• •	• •	• •	• •
Line 15	"00E00"h	"00E01"h	"00E02"h	"00E03"h	"00E04"h	·····	"00EFE"h	"00EFF"h
Line 16	"00F00"h	"00F01"h	"00F02"h	"00F03"h	"00F04"h	·····	"00FFE"h	"00FFF"h

OSD (2) RAM address assignment when SS = "0" (OSDON = "*" / OSDW = "1")

Output Pin/ Display Line	S1	S2	S3	S4	S5		S255	S256
	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0		PD PD 17 ····· 0	PD PD 17 ····· 0
Line 1	"01000"h	"01001"h	"01002"h	"01003"h	"01004"h	·····	"010FE"h	"010FF"h
Line 2	"01100"h	"01101"h	"01102"h	"01103"h	"01104"h	·····	"011FE"h	"011FF"h
Line 3	"01200"h	"01201"h	"01202"h	"01203"h	"01204"h	·····	"012FE"h	"012FF"h
• •	• •	• •	• •	• •	• •	• •	• •	• •
Line 15	"01E00"h	"01E01"h	"01E02"h	"01E03"h	"01E04"h	·····	"01EFE"h	"01EFF"h
Line 16	"01F00"h	"01F01"h	"01F02"h	"01F03"h	"01F04"h	·····	"01FFE"h	"01FFF"h

OSD (1) RAM address assignment when SS = "0" (OSDON = "1" / OSDW = "0")

Output Pin/ Display Line	S1	S2	S3	S4	S5		S255	S256
	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0		PD PD 17 ····· 0	PD PD 17 ····· 0
Line 1	"14000"h	"14001"h	"14002"h	"14003"h	"14004"h	·····	"140FE"h	"140FF"h
Line 2	"14100"h	"14101"h	"14102"h	"14103"h	"14104"h	·····	"141FE"h	"141FF"h
Line 3	"14200"h	"14201"h	"14202"h	"14203"h	"14204"h	·····	"142FE"h	"142FF"h
• •	• •	• •	• •	• •	• •	• •	• •	• •
Line 15	"14E00"h	"14E01"h	"14E02"h	"14E03"h	"14E04"h	·····	"14EFE"h	"14EFF"h
Line 16	"14F00"h	"14F01"h	"14F02"h	"14F03"h	"14F04"h	·····	"14FFE"h	"14FFF"h

OSD (2) RAM address assignment when SS = "0" (OSDON = "1" / OSDW = "0")

Output Pin/ Display Line	S1	S2	S3	S4	S5		S255	S256
	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0		PD PD 17 ····· 0	PD PD 17 ····· 0
Line 1	"15000"h	"15001"h	"15002"h	"15003"h	"15004"h	·····	"150FE"h	"150FF"h
Line 2	"15100"h	"15101"h	"15102"h	"15103"h	"15104"h	·····	"151FE"h	"151FF"h
Line 3	"15200"h	"15201"h	"15202"h	"15203"h	"15204"h	·····	"152FE"h	"152FF"h
• •	• •	• •	• •	• •	• •	• •	• •	• •
Line 15	"15E00"h	"15E01"h	"15E02"h	"15E03"h	"15E04"h	·····	"15EFE"h	"15EFF"h
Line 16	"15F00"h	"15F01"h	"15F02"h	"15F03"h	"15F04"h	·····	"15FFE"h	"15FFF"h

OSD (1) RAM address assignment when SS = "1" (OSDON = "*" / OSDW = "1")

Output Pin/ Display Line	S1	S2	S3	S4	S5		S255	S256
	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0		PD PD 17 ····· 0	PD PD 17 ····· 0
Line 1	"000FF"h	"000FE"h	"000FD"h	"000FC"h	"000FB"h	·····	"00001"h	"00000"h
Line 2	"001FF"h	"001FE"h	"001FD"h	"001FC"h	"001FB"h	·····	"00101"h	"00100"h
Line 3	"002FF"h	"002FE"h	"002FD"h	"002FC"h	"002FB"h	·····	"00201"h	"00200"h
• •	• •	• •	• •	• •	• •	• •	• •	• •
Line 15	"00EFF"h	"00EFE"h	"00EFD"h	"00EFC"h	"00EFB"h	·····	"00E01"h	"00E00"h
Line 16	"00FFF"h	"00FFE"h	"00FFD"h	"00FFC"h	"00FFB"h	·····	"00F01"h	"00F00"h

OSD (2) RAM address assignment when SS = "1" (OSDON = "*" / OSDW = "1")

Output Pin/ Display Line	S1	S2	S3	S4	S5		S255	S256
	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0		PD PD 17 ····· 0	PD PD 17 ····· 0
Line 1	"010FF"h	"010FE"h	"010FD"h	"010FC"h	"010FB"h	·····	"01001"h	"01000"h
Line 2	"011FF"h	"011FE"h	"011FD"h	"011FC"h	"011FB"h	·····	"01101"h	"01100"h
Line 3	"012FF"h	"012FE"h	"012FD"h	"012FC"h	"012FB"h	·····	"01201"h	"01200"h
• •	• •	• •	• •	• •	• •	• •	• •	• •
Line 15	"01EFF"h	"01EFE"h	"01EFD"h	"01EFC"h	"01EFB"h	·····	"01E01"h	"01E00"h
Line 16	"01FFF"h	"01FFE"h	"01FFD"h	"01FFC"h	"01FFB"h	·····	"01F01"h	"01F00"h

OSD (1) RAM address assignment when SS = "1" (OSDON = "1" / OSDW = "0")

Output Pin/ Display Line	S1	S2	S3	S4	S5		S255	S256
	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0		PD PD 17 ····· 0	PD PD 17 ····· 0
Line 1	"140FF"h	"140FE"h	"140FD"h	"140FC"h	"140FB"h	·····	"14001"h	"14000"h
Line 2	"141FF"h	"141FE"h	"141FD"h	"141FC"h	"141FB"h	·····	"14101"h	"14100"h
Line 3	"142FF"h	"142FE"h	"142FD"h	"142FC"h	"142FB"h	·····	"14201"h	"14200"h
• •	• •	• •	• •	• •	• •	• •	• •	• •
Line 15	"14EFF"h	"14EFE"h	"14EFD"h	"14EFC"h	"14EFB"h	·····	"14E01"h	"14E00"h
Line 16	"14FFF"h	"14FFE"h	"14FFD"h	"14FFC"h	"14FFB"h	·····	"14F01"h	"14F00"h

OSD (2) RAM address assignment when SS = "1" (OSDON = "1" / OSDW = "0")

Output Pin/ Display Line	S1	S2	S3	S4	S5		S255	S256
	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0	PD PD 17 ····· 0		PD PD 17 ····· 0	PD PD 17 ····· 0
Line 1	"150FF"h	"150FE"h	"150FD"h	"150FC"h	"150FB"h	·····	"15001"h	"15000"h
Line 2	"151FF"h	"151FE"h	"151FD"h	"151FC"h	"151FB"h	·····	"15101"h	"15100"h
Line 3	"152FF"h	"152FE"h	"152FD"h	"152FC"h	"152FB"h	·····	"15201"h	"15200"h
• •	• •	• •	• •	• •	• •	• •	• •	• •
Line 15	"15EFF"h	"15EFE"h	"15EFD"h	"15EFC"h	"15EFB"h	·····	"15E01"h	"15E00"h
Line 16	"15FFF"h	"15FFE"h	"15FFD"h	"15FFC"h	"15FFB"h	·····	"15F01"h	"15F00"h

Duty Settings

The JBT6K71-AS(A) allows the user to modify the number of lines to be driven on the LCD. For details, see the following table.

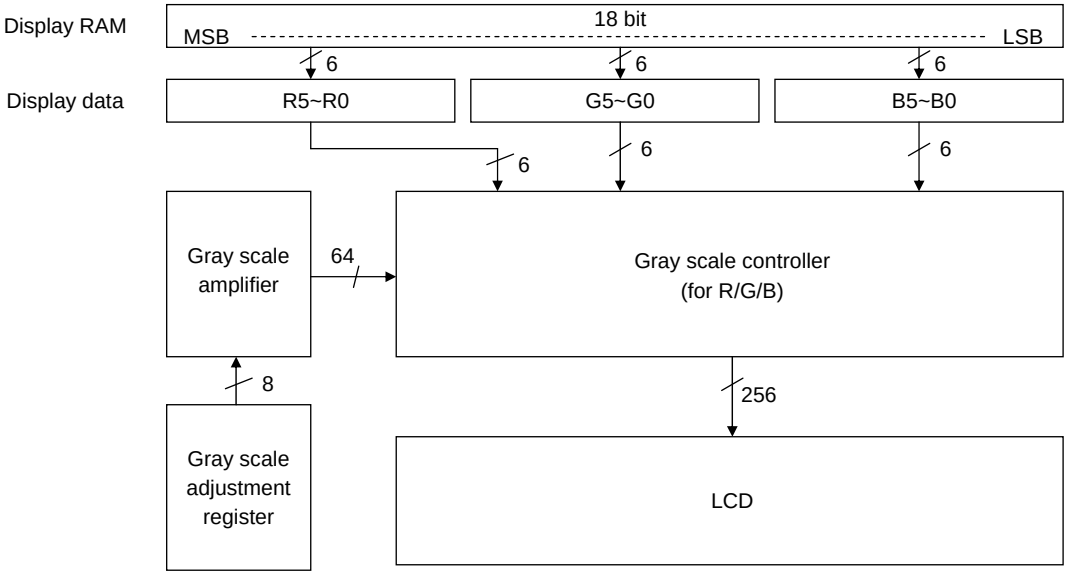
NL5	NL4	NL3	NL2	NL1	NL0	Display Size	Number of Driven LCD Lines
0	0	0	0	0	0	Setting prohibited	Setting prohibited
0	0	0	0	0	1	256 × 16 dots	16
0	0	0	0	1	0	256 × 24 dots	24
0	0	0	0	1	1	256 × 32 dots	32
0	0	0	1	0	0	256 × 40 dots	40
0	0	0	1	0	1	256 × 48 dots	48
0	0	0	1	1	0	256 × 56 dots	56
0	0	0	1	1	1	256 × 64 dots	64
0	0	1	0	0	0	256 × 72 dots	72
0	0	1	0	0	1	256 × 80 dots	80
0	0	1	0	1	0	256 × 88 dots	88
0	0	1	0	1	1	256 × 96 dots	96
0	0	1	1	0	0	256 × 104 dots	104
0	0	1	1	0	1	256 × 112 dots	112
0	0	1	1	1	0	256 × 120 dots	120
0	0	1	1	1	1	256 × 128 dots	128
0	1	0	0	0	0	256 × 136 dots	136
0	1	0	0	0	1	256 × 144 dots	144
0	1	0	0	1	0	256 × 152 dots	152
0	1	0	0	1	1	256 × 160 dots	160
0	1	0	1	0	0	256 × 168 dots	168
0	1	0	1	0	1	256 × 176 dots	176
0	1	0	1	1	0	256 × 184 dots	184
0	1	0	1	1	1	256 × 192 dots	192
0	1	1	0	0	0	256 × 200 dots	200
0	1	1	0	0	1	256 × 208 dots	208
0	1	1	0	1	0	256 × 216 dots	216
0	1	1	0	1	1	256 × 224 dots	224
0	1	1	1	0	0	256 × 232 dots	232
0	1	1	1	0	1	256 × 240 dots	240
0	1	1	1	1	0	256 × 248 dots	248
0	1	1	1	1	1	256 × 256 dots	256
1	0	0	0	0	0	256 × 264 dots	264
1	0	0	0	0	1	256 × 272 dots	272
1	0	0	0	1	0	256 × 280 dots	280
1	0	0	0	1	1	256 × 288 dots	288
1	0	0	1	0	0	256 × 296 dots	296
1	0	0	1	0	1	256 × 304 dots	304
1	0	0	1	1	0	256 × 312 dots	312
1	0	0	1	1	1	256 × 320 dots	320
"101000" or greater: Setting prohibited						—	—

If it does not use OSD function. It is possible for number of line to increase within 352 lines.
Then, it takes notice that the setting MAX value is changed for it.

1	0	1	0	0	0	256x328dots	328
1	0	1	0	0	1	256x336dots	336
1	0	1	0	1	0	256x344dots	344
1	0	1	0	1	1	256x352dots	352
Prohibited setting over "101011"						-	-

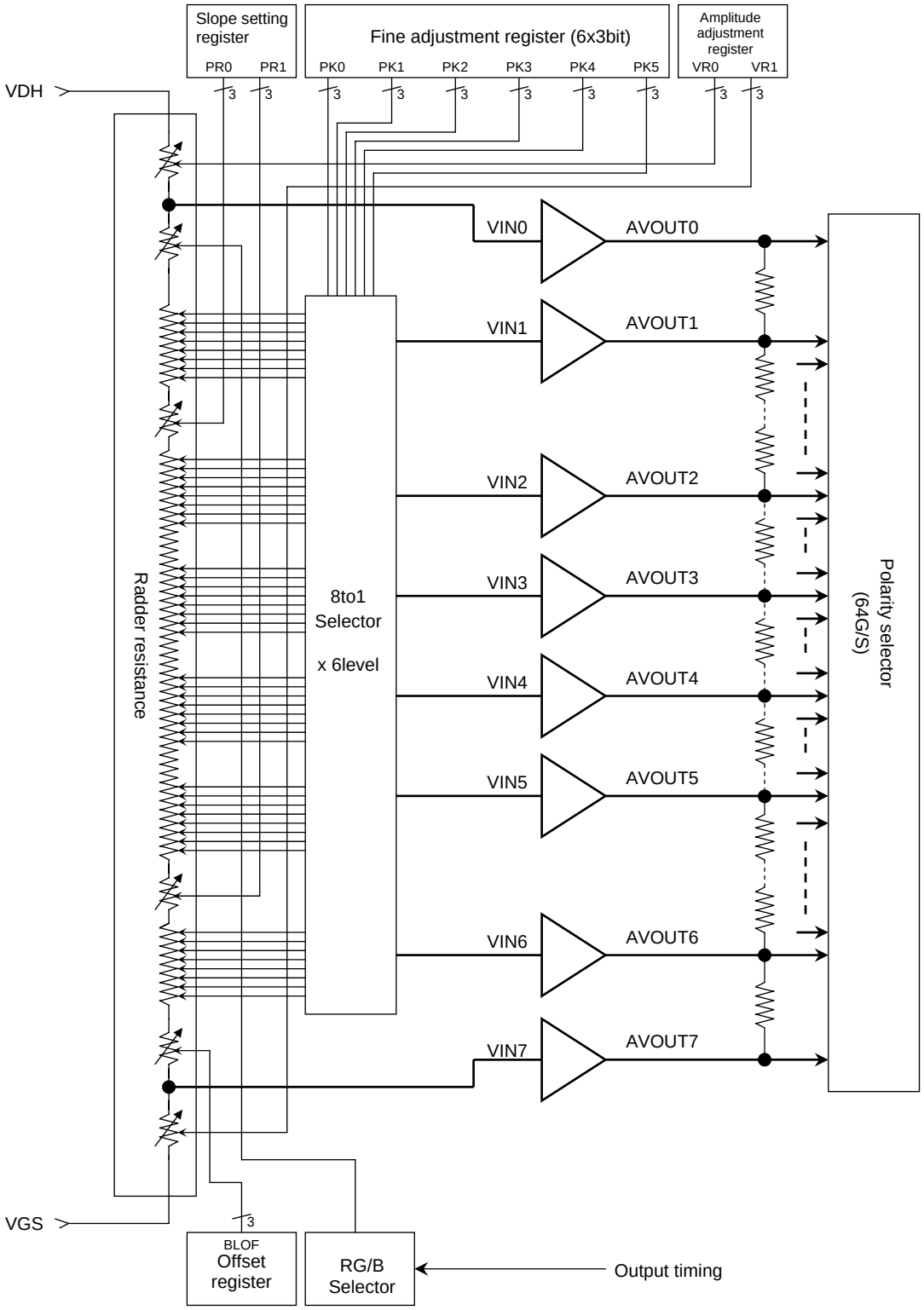
Gamma Adjustment Circuit

The JBT6K71-AS incorporates a gamma adjustment circuit to display 262,144 colors simultaneously. Gamma adjustment is performed by using inclination adjustment registers and fine tuning registers to specify one of eight levels of gray scale. The gamma adjustment circuit contains separate inclination adjustment and fine tuning registers for the positive and negative polarities, which can be set according to the LCD characteristics.

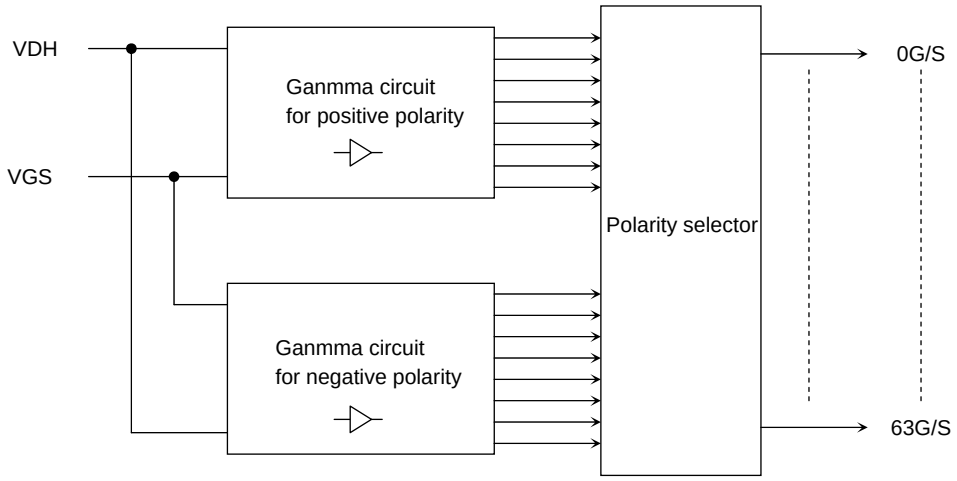


Also, Both RG common gray scale and excutive B gray scale as this two system can generate the voltage and display image simalteniously.

The following diagram shows the structure of the gray scale amplifier. The inclination adjustment and fine tuning registers determine one of eight levels (VIN0-VIN7). Levels are divided using built-in ladder resistors, generating 64 levels (V0 to V63).

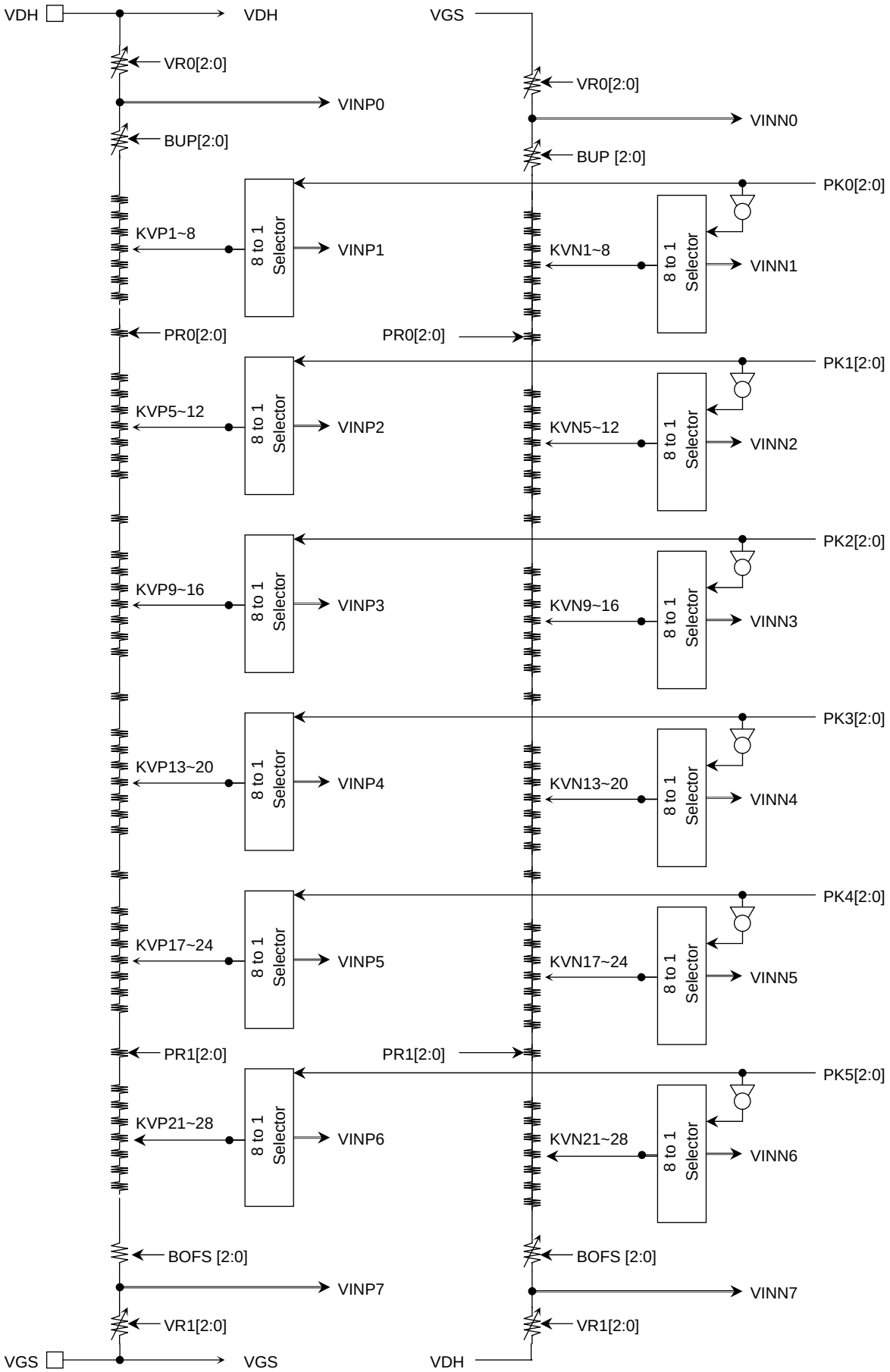


Gray scale amplifier structure (1)



Ganmma gray scale diagram (2)

Included the forward ganmma circuit as positive and negative polarity, And select positive or negative polarity. This system optimizes The LCD which has the different gannma level between positive and negative polarity. Also, Both RG common gray scale and excutive B gray scale as this two system can generate the voltage and display image simalteniously.

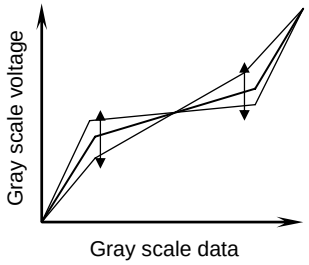

VDH
VDH
VGS
VR0[2:0]
VR0[2:0]
VINP0
VINN0
BUP[2:0]
BUP [2:0]
PK0[2:0]
KVP1~8
8 to 1 Selector
VINP1
KVN1~8
8 to 1 Selector
VINN1
PR0[2:0]
PR0[2:0]
PK1[2:0]
KVP5~12
8 to 1 Selector
VINP2
KVN5~12
8 to 1 Selector
VINN2
PK2[2:0]
KVP9~16
8 to 1 Selector
VINP3
KVN9~16
8 to 1 Selector
VINN3
PK3[2:0]
KVP13~20
8 to 1 Selector
VINP4
KVN13~20
8 to 1 Selector
VINN4
PK4[2:0]
KVP17~24
8 to 1 Selector
VINP5
KVN17~24
8 to 1 Selector
VINN5
PR1[2:0]
PR1[2:0]
PK5[2:0]
KVP21~28
8 to 1 Selector
VINP6
KVN21~28
8 to 1 Selector
VINN6
BOFS [2:0]
BOFS [2:0]
VINP7
VINN7
VR1[2:0]
VR1[2:0]
VGS
VGS
VDH

Gamma adjustment registers

These registers are used to specify a gray scale voltage according to the gamma characteristics of the LCD panel. The registers are classified into three groups, which are designed to set the inclination, amplitude, and fine tuning for the gray scale data-voltage characteristics, as shown below. Each adjustment can be specified separately for the positive and negative polarities (the reference value is used in common and the adjustment applies to all of R, G, and B simultaneously). The following describes the operation of each adjustment register:

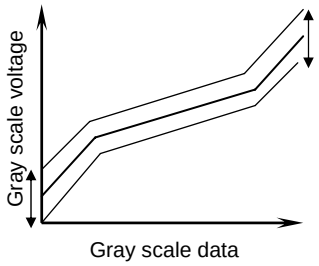
(1) Inclination adjustment registers

The inclination adjustment register is used to adjust inclination near the center of the gray scale data-voltage characteristics curve without modifying the dynamic range. Inclination is adjusted by controlling variable resistances (VRHP(N)/VRL(N)) in the ladder resistor for generating the gray scale voltage.



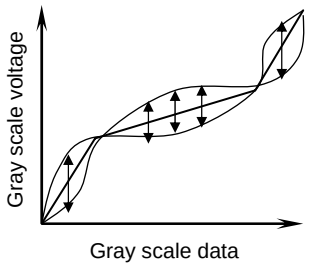
(2) Amplitude adjustment register

The amplitude adjustment register is used to adjust the amplitude of the gray scale voltage. The amplitude is adjusted by controlling top and bottom variable resistances (VRP(N)0/VRP(N)1) in the ladder resistor for generating the gray scale voltage.



(3) Fine tuning register

The fine tuning register is used to finely adjust the gray scale voltage level. The voltage level is adjusted by using an 8-to-1 selector to select a level for each reference voltage from eight reference voltage levels generated by ladder resistor.



Summary of output signal names

Register Classification	For Positive Polarity	Description
Inclination adjustment	PR0 [2:0]	Variable resistor VRH
	PR1 [2:0]	Variable resistor VRL
Amplitude adjustment	VR0 [2:0]	Variable resistor VR0
	VR1 [2:0]	Variable resistor VR1
Fine tuning	PK0 [2:0]	8-to-1 selector (gray scale level 1 voltage)
	PK1 [2:0]	8-to-1 selector (gray scale level 8 voltage)
	PK2 [2:0]	8-to-1 selector (gray scale level 20 voltage)
	PK3 [2:0]	8-to-1 selector (gray scale level 43 voltage)
	PK4 [2:0]	8-to-1 selector (gray scale level 55 voltage)
	PK5 [2:0]	8-to-1 selector (gray scale level 62 voltage)
RG/B offset amounts	BOFS[2:0]	RG-B adjustment on BLON
Raise the level	BUP[2:0]	Adjustment between L63 and L62, L1 and L0

Ladder resistor and 8-to-1 selector block

(1) Organization

This block consists of two ladder resistors including variable resistances and 8-to-1 selectors for selecting a level from voltages generated by ladder resistor to output a reference voltage for gray scale voltages. The variable resistances and 8-to-1 selectors are controlled using the gamma adjustment registers, described above. The block also has pins for connecting an external trimmer resistor to compensate for variations among different panels.

(2) Variable resistances

The ladder resistor contains two types of variable resistances, VRHP(N)/VRLP(N) for inclination adjustment and VRP(N)0/VRP(N)1 for amplitude adjustment, which are controlled with the inclination and amplitude adjustment registers, respectively. The following tables show the relationship between register settings and resistance values:

Inclination adjustment (1)

Register Setting PRP(N)0 [2:0]	Resistance VRHP(N)
000	0R
001	1R
010	2R
011	3R
100	4R
101	5R
110	6R
111	7R

Inclination adjustment (2)

Register Setting PRP(N)1 [2:0]	Resistance VRLP(N)
000	0R
001	1R
010	2R
011	3R
100	4R
101	5R
110	6R
111	7R

Amplitude adjustment (1)

Register Setting VRP(N)0 [2:0]	Resistance VRP(N)0
000	0R
001	2R
010	4R
011	6R
100	8R
101	10R
110	12R
111	14R

Amplitude adjustment (2)

Register Setting VRP(N)1 [2:0]	Resistance VRP(N)1
000	0R
001	2R
010	4R
011	6R
100	8R
101	10R
110	12R
111	14R

(3) 8-to-1 selectors

An 8-to-1 selector selects a voltage level from those given by the ladder resistor, based on the setting of the fine tune register, and outputs one of six reference voltages, VIN1 to VIN6. The following table shows the relationship between fine tuning register settings and selected voltages:

Register Setting PKn [2:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)5	KVP(N)9	KVP(N)13	KVP(N)17	KVP(N)21
001	KVP(N)2	KVP(N)6	KVP(N)10	KVP(N)14	KVP(N)18	KVP(N)22
010	KVP(N)3	KVP(N)7	KVP(N)11	KVP(N)15	KVP(N)19	KVP(N)23
011	KVP(N)4	KVP(N)8	KVP(N)12	KVP(N)16	KVP(N)20	KVP(N)24
100	KVP(N)5	KVP(N)9	KVP(N)13	KVP(N)17	KVP(N)21	KVP(N)25
101	KVP(N)6	KVP(N)10	KVP(N)14	KVP(N)18	KVP(N)22	KVP(N)26
110	KVP(N)7	KVP(N)11	KVP(N)15	KVP(N)19	KVP(N)23	KVP(N)27
111	KVP(N)8	KVP(N)12	KVP(N)16	KVP(N)20	KVP(N)24	KVP(N)28

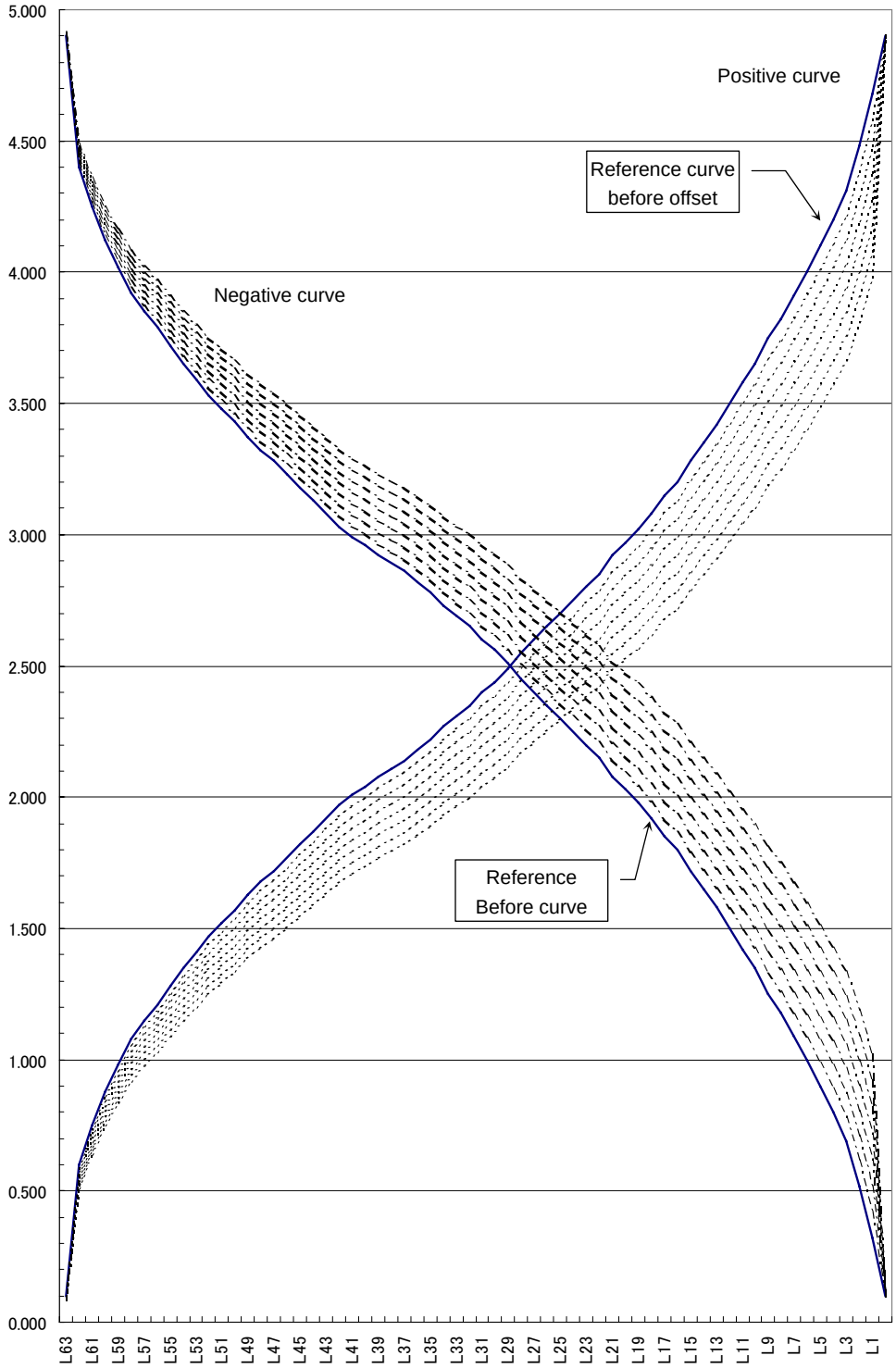
Gray Scale Voltage Table(1)

The following table shows the output values of the V0 to V63 gray scale voltages:

GAMMA offset voltage specification

GS	Reference		Ref–0.1V		Ref–0.2V		Ref–0.3V		Ref–0.4V		Ref–0.5V		Ref–0.6V		Ref–0.7V	
	Positive	Negative	Positive	Negative	Positive	Negative	Positive	Negative	Positive	Negative	Positive	Negative	Positive	Negative	Positive	Negative
L63	0.100	4.900	0.098	4.902	0.096	4.904	0.094	4.906	0.091	4.909	0.089	4.911	0.087	4.913	0.085	4.915
L62	0.600	4.400	0.587	4.413	0.574	4.426	0.562	4.438	0.549	4.451	0.536	4.464	0.523	4.477	0.510	4.490
L61	0.750	4.250	0.734	4.266	0.718	4.282	0.702	4.298	0.686	4.314	0.670	4.330	0.654	4.346	0.638	4.362
L60	0.880	4.120	0.861	4.139	0.842	4.158	0.824	4.176	0.805	4.195	0.786	4.214	0.767	4.233	0.748	4.252
L59	0.980	4.020	0.959	4.041	0.938	4.062	0.917	4.083	0.896	4.104	0.875	4.125	0.854	4.146	0.833	4.167
L58	1.080	3.920	1.057	3.943	1.034	3.966	1.011	3.989	0.988	4.012	0.965	4.035	0.942	4.058	0.918	4.082
L57	1.150	3.850	1.125	3.875	1.101	3.899	1.076	3.924	1.052	3.948	1.027	3.973	1.003	3.997	0.978	4.022
L56	1.210	3.790	1.184	3.816	1.158	3.842	1.132	3.868	1.107	3.893	1.081	3.919	1.055	3.945	1.029	3.971
L55	1.280	3.720	1.253	3.747	1.225	3.775	1.198	3.802	1.171	3.829	1.143	3.857	1.116	3.884	1.089	3.911
L54	1.350	3.650	1.321	3.679	1.292	3.708	1.263	3.737	1.235	3.765	1.206	3.794	1.177	3.823	1.148	3.852
L53	1.410	3.590	1.380	3.620	1.350	3.650	1.320	3.680	1.289	3.711	1.259	3.741	1.229	3.771	1.199	3.801
L52	1.470	3.530	1.439	3.561	1.407	3.593	1.376	3.624	1.344	3.656	1.313	3.687	1.282	3.718	1.250	3.750
L51	1.520	3.480	1.488	3.512	1.455	3.545	1.423	3.577	1.390	3.610	1.358	3.642	1.325	3.675	1.293	3.707
L50	1.570	3.430	1.536	3.464	1.503	3.497	1.469	3.531	1.436	3.564	1.402	3.598	1.369	3.631	1.335	3.665
L49	1.630	3.370	1.595	3.405	1.560	3.440	1.526	3.474	1.491	3.509	1.456	3.544	1.421	3.579	1.386	3.614
L48	1.680	3.320	1.644	3.356	1.608	3.392	1.572	3.428	1.536	3.464	1.501	3.499	1.465	3.535	1.429	3.571
L47	1.720	3.280	1.683	3.317	1.646	3.354	1.610	3.390	1.573	3.427	1.536	3.464	1.499	3.501	1.463	3.537
L46	1.770	3.230	1.732	3.268	1.694	3.306	1.657	3.343	1.619	3.381	1.581	3.419	1.543	3.457	1.505	3.495
L45	1.820	3.180	1.781	3.219	1.742	3.258	1.703	3.297	1.664	3.336	1.626	3.374	1.587	3.413	1.548	3.452
L44	1.870	3.130	1.830	3.170	1.790	3.210	1.750	3.250	1.710	3.290	1.670	3.330	1.630	3.370	1.590	3.410
L43	1.920	3.080	1.879	3.121	1.838	3.162	1.797	3.203	1.756	3.244	1.715	3.285	1.674	3.326	1.633	3.367
L42	1.970	3.030	1.928	3.072	1.886	3.114	1.844	3.156	1.802	3.198	1.760	3.240	1.717	3.283	1.675	3.325
L41	2.010	2.990	1.967	3.033	1.924	3.076	1.881	3.119	1.838	3.162	1.795	3.205	1.752	3.248	1.709	3.291
L40	2.040	2.960	1.996	3.004	1.953	3.047	1.909	3.091	1.866	3.134	1.822	3.178	1.778	3.222	1.735	3.265
L39	2.080	2.920	2.036	2.964	1.991	3.009	1.947	3.053	1.902	3.098	1.858	3.142	1.813	3.187	1.769	3.231
L38	2.110	2.890	2.065	2.935	2.020	2.980	1.975	3.025	1.930	3.070	1.885	3.115	1.839	3.161	1.794	3.206
L37	2.140	2.860	2.094	2.906	2.049	2.951	2.003	2.997	1.957	3.043	1.911	3.089	1.866	3.134	1.820	3.180
L36	2.180	2.820	2.133	2.867	2.087	2.913	2.040	2.960	1.994	3.006	1.947	3.053	1.901	3.099	1.854	3.146
L35	2.220	2.780	2.173	2.827	2.125	2.875	2.078	2.922	2.030	2.970	1.983	3.017	1.935	3.065	1.888	3.112
L34	2.270	2.730	2.221	2.779	2.173	2.827	2.124	2.876	2.076	2.924	2.027	2.973	1.979	3.021	1.930	3.070
L33	2.310	2.690	2.261	2.739	2.211	2.789	2.162	2.838	2.113	2.887	2.063	2.937	2.014	2.986	1.964	3.036
L32	2.350	2.650	2.300	2.700	2.250	2.750	2.199	2.801	2.149	2.851	2.099	2.901	2.049	2.951	1.999	3.001
L31	2.400	2.600	2.349	2.651	2.297	2.703	2.246	2.754	2.195	2.805	2.144	2.856	2.092	2.908	2.041	2.959
L30	2.440	2.560	2.388	2.612	2.336	2.664	2.284	2.716	2.231	2.769	2.179	2.821	2.127	2.873	2.075	2.925
L29	2.490	2.510	2.437	2.563	2.384	2.616	2.330	2.670	2.277	2.723	2.224	2.776	2.171	2.829	2.118	2.882
L28	2.550	2.450	2.496	2.504	2.441	2.559	2.387	2.613	2.332	2.668	2.278	2.722	2.223	2.777	2.169	2.831
L27	2.600	2.400	2.544	2.456	2.489	2.511	2.433	2.567	2.378	2.622	2.322	2.678	2.267	2.733	2.211	2.789
L26	2.650	2.350	2.593	2.407	2.537	2.463	2.480	2.520	2.424	2.576	2.367	2.633	2.310	2.690	2.254	2.746
L25	2.700	2.300	2.642	2.358	2.585	2.415	2.527	2.473	2.469	2.531	2.412	2.588	2.354	2.646	2.296	2.704
L24	2.750	2.250	2.691	2.309	2.632	2.368	2.574	2.426	2.515	2.485	2.456	2.544	2.397	2.603	2.339	2.661
L23	2.800	2.200	2.740	2.260	2.680	2.320	2.621	2.379	2.561	2.439	2.501	2.499	2.441	2.559	2.381	2.619
L22	2.850	2.150	2.789	2.211	2.728	2.272	2.667	2.333	2.606	2.394	2.546	2.454	2.485	2.515	2.424	2.576
L21	2.920	2.080	2.858	2.142	2.795	2.205	2.733	2.267	2.670	2.330	2.608	2.392	2.546	2.454	2.483	2.517
L20	2.970	2.030	2.907	2.093	2.843	2.157	2.780	2.220	2.716	2.284	2.653	2.347	2.589	2.411	2.526	2.474
L19	3.020	1.980	2.955	2.045	2.891	2.109	2.826	2.174	2.762	2.238	2.697	2.303	2.633	2.367	2.568	2.432
L18	3.080	1.920	3.014	1.986	2.948	2.052	2.883	2.117	2.817	2.183	2.751	2.249	2.685	2.315	2.619	2.381
L17	3.150	1.850	3.083	1.917	3.015	1.985	2.948	2.052	2.881	2.119	2.813	2.187	2.746	2.254	2.679	2.321
L16	3.200	1.800	3.132	1.868	3.063	1.937	2.995	2.005	2.926	2.074	2.858	2.142	2.790	2.210	2.721	2.279
L15	3.280	1.720	3.210	1.790	3.140	1.860	3.070	1.930	3.000	2.000	2.930	2.070	2.859	2.141	2.789	2.211
L14	3.350	1.650	3.278	1.722	3.207	1.793	3.135	1.865	3.064	1.936	2.992	2.008	2.921	2.079	2.849	2.151
L13	3.420	1.580	3.347	1.653	3.274	1.726	3.201	1.799	3.128	1.872	3.055	1.945	2.982	2.018	2.908	2.092
L12	3.500	1.500	3.425	1.575	3.350	1.650	3.276	1.724	3.201	1.799	3.126	1.874	3.051	1.949	2.976	2.024
L11	3.580	1.420	3.504	1.496	3.427	1.573	3.351	1.649	3.274	1.726	3.198	1.802	3.121	1.879	3.045	1.955
L10	3.650	1.350	3.572	1.428	3.494	1.506	3.416	1.584	3.338	1.662	3.260	1.740	3.182	1.818	3.104	1.896
L9	3.750	1.250	3.670	1.330	3.590	1.410	3.510	1.490	3.429	1.571	3.349	1.651	3.269	1.731	3.189	1.811
L8	3.820	1.180	3.738	1.262	3.657	1.343	3.575	1.425	3.494	1.506	3.412	1.588	3.330	1.670	3.249	1.751
L7	3.910	1.090	3.826	1.174	3.743	1.257	3.659	1.341	3.576	1.424	3.492	1.508	3.409	1.591	3.325	1.675
L6	4.000	1.000	3.915	1.085	3.829	1.171	3.744	1.256	3.658	1.342	3.573	1.427	3.487	1.513	3.402	1.598
L5	4.100	0.900	4.012	0.988	3.925	1.075	3.837	1.163	3.750	1.250	3.662	1.338	3.574	1.426	3.487	1.513
L4	4.200	0.800	4.110	0.890	4.021	0.979	3.931	1.069	3.841	1.159	3.751	1.249	3.662	1.338	3.572	1.428
L3	4.310	0.690	4.218	0.782	4.126	0.874	4.034	0.966	3.942	1.058	3.850	1.150	3.757	1.243	3.665	1.335
L2	4.480	0.520	4.384	0.616	4.289	0.711	4.193	0.807	4.097	0.903	4.001	0.999	3.906	1.094	3.810	1.190
L1	4.680	0.320	4.580	0.420	4.480	0.520	4.380	0.620	4.280	0.720	4.180	0.820	4.080	0.920	3.980	1.020
L0	4.900	0.100	4.900	0.100	4.900	0.100	4.900	0.100	4.900	0.100	4.900	0.100	4.900	0.100	4.900	0.100

Gray scale offset value graph



When adjust offset register data for the reference (The curve before offset) Can change the offset per 0.1V.

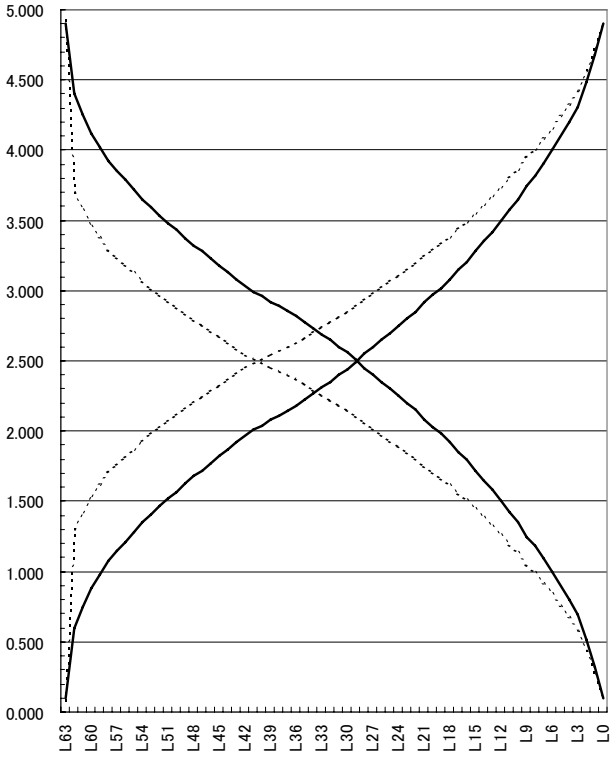
This change is enabling to use the exclusive BLUE gray scale curve and the offset RED-GREEN gray scale curve simulteniously. Initialised register after the reset is OFF for offset. And established RGB common curve is available.

Note) The setp voltage variation might be scattering result. Please set optimized voltage with actual evaluation.

Gray scale voltage table (2)

GAMMA offset L62&L1 voltage specification

GS	Reference		Offset		階調	Reference		Offset	
	Positive	Negative	Positive	Negative		Positive	Negative	Positive	Negative
L63	0.100	4.900	0.084	4.916	L31	2.400	2.600	2.814	2.186
L62	0.600	4.400	1.300	3.700	L30	2.440	2.560	2.847	2.153
L61	0.750	4.250	1.426	3.574	L29	2.490	2.510	2.889	2.111
L60	0.880	4.120	1.535	3.465	L28	2.550	2.450	2.940	2.060
L59	0.980	4.020	1.620	3.380	L27	2.600	2.400	2.982	2.018
L58	1.080	3.920	1.704	3.296	L26	2.650	2.350	3.024	1.976
L57	1.150	3.850	1.763	3.237	L25	2.700	2.300	3.066	1.934
L56	1.210	3.790	1.813	3.187	L24	2.750	2.250	3.108	1.892
L55	1.280	3.720	1.872	3.128	L23	2.800	2.200	3.150	1.850
L54	1.350	3.650	1.931	3.069	L22	2.850	2.150	3.192	1.808
L53	1.410	3.590	1.981	3.019	L21	2.920	2.080	3.251	1.749
L52	1.470	3.530	2.032	2.968	L20	2.970	2.030	3.293	1.707
L51	1.520	3.480	2.074	2.926	L19	3.020	1.980	3.335	1.665
L50	1.570	3.430	2.116	2.884	L18	3.080	1.920	3.385	1.615
L49	1.630	3.370	2.166	2.834	L17	3.150	1.850	3.444	1.556
L48	1.680	3.320	2.208	2.792	L16	3.200	1.800	3.486	1.514
L47	1.720	3.280	2.242	2.758	L15	3.280	1.720	3.554	1.446
L46	1.770	3.230	2.284	2.716	L14	3.350	1.650	3.613	1.387
L45	1.820	3.180	2.326	2.674	L13	3.420	1.580	3.671	1.329
L44	1.870	3.130	2.368	2.632	L12	3.500	1.500	3.739	1.261
L43	1.920	3.080	2.410	2.590	L11	3.580	1.420	3.806	1.194
L42	1.970	3.030	2.452	2.548	L10	3.650	1.350	3.865	1.135
L41	2.010	2.990	2.486	2.514	L9	3.750	1.250	3.949	1.051
L40	2.040	2.960	2.511	2.489	L8	3.820	1.180	4.008	0.992
L39	2.080	2.920	2.545	2.455	L7	3.910	1.090	4.083	0.917
L38	2.110	2.890	2.570	2.430	L6	4.000	1.000	4.159	0.841
L37	2.140	2.860	2.595	2.405	L5	4.100	0.900	4.243	0.757
L36	2.180	2.820	2.629	2.371	L4	4.200	0.800	4.327	0.673
L35	2.220	2.780	2.662	2.338	L3	4.310	0.690	4.420	0.580
L34	2.270	2.730	2.704	2.296	L2	4.480	0.520	4.563	0.437
L33	2.310	2.690	2.738	2.262	L1	4.680	0.320	4.731	0.269
L32	2.350	2.650	2.772	2.228	L0	4.900	0.100	4.916	0.084

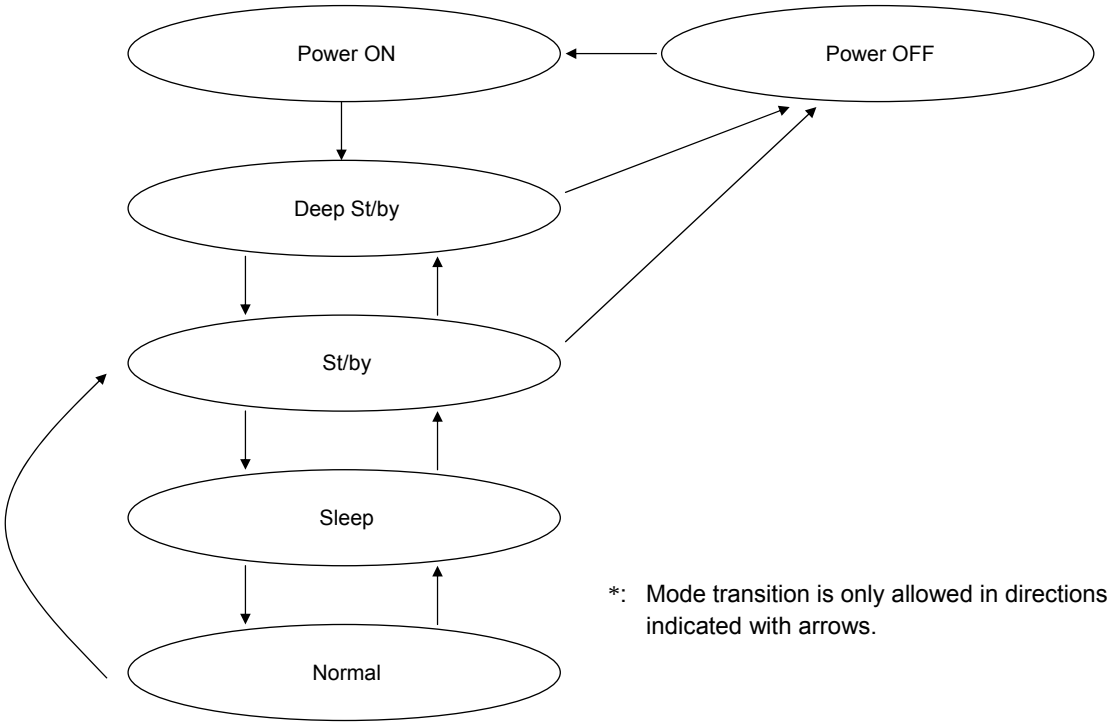


JBT6K71-AS has the adjustment function for between L62 and L63, L0-L1.The forward fugure is the gray scale curve included 0.7V offset (register"1111")Between L62 and L63, L0-L1 has 8 gradiations. The voltage is shifted from 0V to 0.7V.Can associate some LCD curves with combining frequency adjustment registers.

Note) The setp voltage variation might be scattering result. Please set optimized voltage with actual evaluation.

Mode Transition Diagram

The below diagram shows the direction in which the JBT6K71-AS changes the mode.
When power on the device, run the software reset once to initialize its registers.



*: Mode transition is only allowed in directions indicated with arrows.

Frame Frequency Adjustment

The JBT6K71-AS supports the adjustment of the frame frequency in internal clock operation mode. An instruction can modify register bits (DIV and RTN) to adjust the frame frequency for driving the LCD, without modifying the oscillation frequency.

With a high oscillation frequency specified, moving and still images can be displayed with different frame frequencies. Still images can be displayed with low power using a low frame frequency while fast screen switching for moving images can be supported using a high frame frequency.

- Relationship between LCD driving duty ratio and frame frequency

The following equation represents the relationship between the LCD driving duty ratio and the frame frequency. The frame frequency can be adjusted by using an instruction to modify the settings of the 1H period adjustment bit (RTN) and operating clock division bit (DIV).

Calculating the frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Number of 1-line clock cycles} \times \text{Frequency division ratio} \times (\text{Line} + \text{FP} + \text{BP})} \quad \text{(Hz)}$$

fosc: CR oscillation frequency
Line: Number of driven lines (NL bit)
Number of 1-line clock cycles: RTN bit
Frequency division ratio: DIV bit
FP: Front porch
BP: Back porch

- Example: When maximum frame frequency = 60 Hz

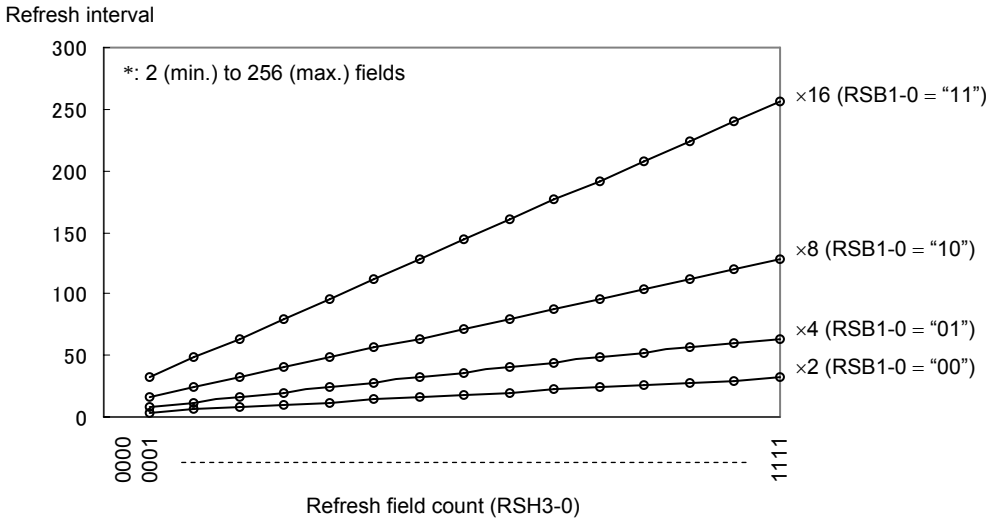
Number of driven lines: 320
1H period: 16 clock cycles (RTN4-0 = “1000”)
Operation clock division ratio: 1
Front porch + back porch: 16

$$\text{fosc} = 60\ \text{Hz} \times 16\ \text{clock cycles} \times 1 \times (320 + 16)\ \text{lines} = 323\ \text{(kHz)}$$

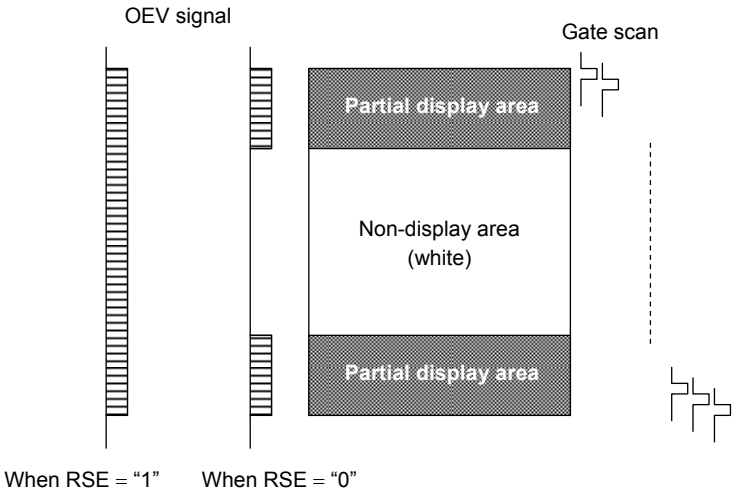
In this example, the determined CR oscillation frequency is 323 kHz. Adjust the external resistance for the CR oscillator so that the frequency becomes 323 kHz.

Refresh Driving for Partial Display

The JBT6K71-AS is supports partial display. An instruction can be used to refresh the non-display area, in white, at specified intervals during partial display. The refresh interval is determined from the refresh field magnification setting (RSB1-0) and the refresh field count setting (RSH3-0).



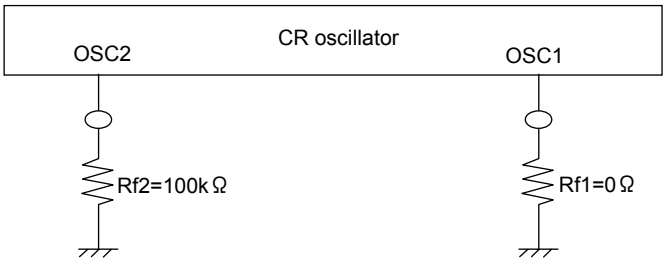
During partial display, the non-display area is disabled using to the OEV signal, with only the partial display areas driven. Setting the refresh driving bit (RSE) to "1" enables refresh driving during partial display. Setting RSE to "1" enables the OEV signal, thus enabling a gate scan signal for the LCD. The JBT6K71-AS outputs white display data to the non-display area.



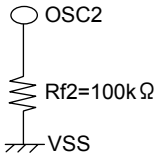
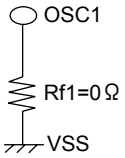
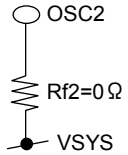
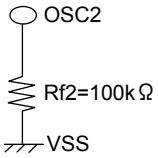
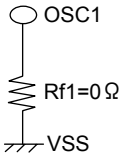
*: Disabling the OEV signal for the non-display area results in white display.
When RSE is set to "1" to enable refresh driving, the OEV signal is also enabled for the non-display area, thus writing white data to the LCD.

Internal CR Oscillator

The JBT6K71-AS incorporates a CR oscillator. With resistors connected to its OSC1 and OSC2 pins, the internal CR oscillator enters self-oscillating mode, which can be turned on or off using a register.



The JBT6K71-AS can also operate with an externally supplied clock without using the internal CR oscillator. To specify external clock mode, make the following connections:

Mode	OSC2(Rf2)	OSC1(Rf1)	Index / Data
Internal oscillator			Index = 000h Data = 0001h
External clock mode		Supply clock to OSC1	
RGB interface mode			

Note: In case of external clock mode, need the Index=”0000h” and Data=”0001h” setting for OSC ON.

Note: In case of external clock mode, need the internal clock in 1st action. The JBT6K71-AS(A) fixed condition of RGB interface mode that operation clock use the DOTCLK signal. (Booster circuit use the DOTCLK too)

Graphic Operation

The JBT6K71-AS supports an internal graphic operation feature, which, in combination with its 18-bit bus architecture, can greatly reduce the workload of the microcontroller graphic software. The graphic operation feature supports a write data mask feature, which rewrites part of 18-bit write data selectively. It can be controlled using the settings of entry mode register and RAM write data mask register bits in conjunction with write operation from the microcontroller.

Table 6 Graphic operations

No.	Operation Mode	Bit Settings		Description
		I/D	AM	
1	Write mode 1	0/1	0	Replaces data in the horizontal direction.
2	Write mode 2	0/1	1	Replaces data in the vertical direction.

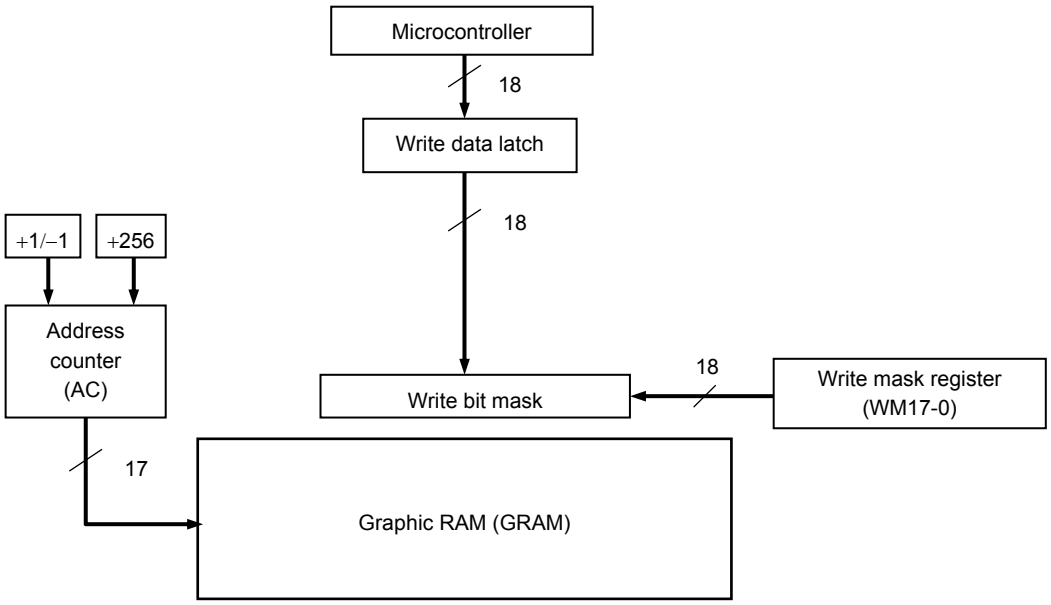
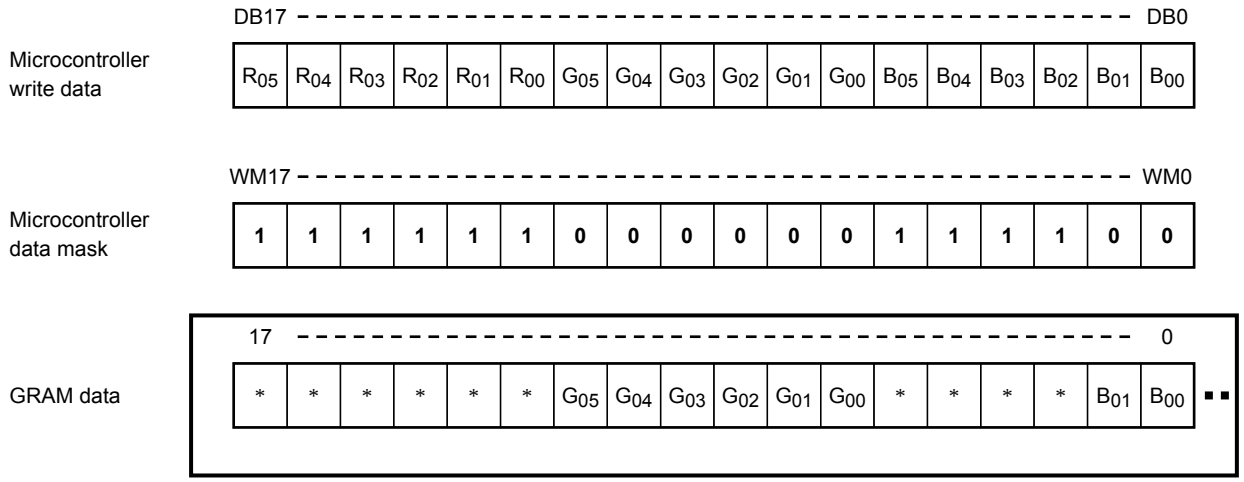


Figure 19 Graphic operation flow

Write Data Mask

The JBT6K71-AS receives 16-bit data from the microcontroller and internally expands the data to 18 bits, unless it is using the 18-bit interface. The JBT6K71-AS supports a write data mask feature, which controls the bits of the 18-bit data that will be written to the graphic RAM (GRAM). A bit as setting "0" in write data mask register (WM17-0) writes the graphic RAM (GRAM). A bit as setting "1" in the write data mask register prevents to write to the GRAM, maintaining previous data in the GRAM. This feature is useful for rewriting only a single pixel or selectively rewriting a particular color only.



Note: When the 8-/16-bit system interface or 16-bit RGB interface is used, data is internally expanded to 18 bits.

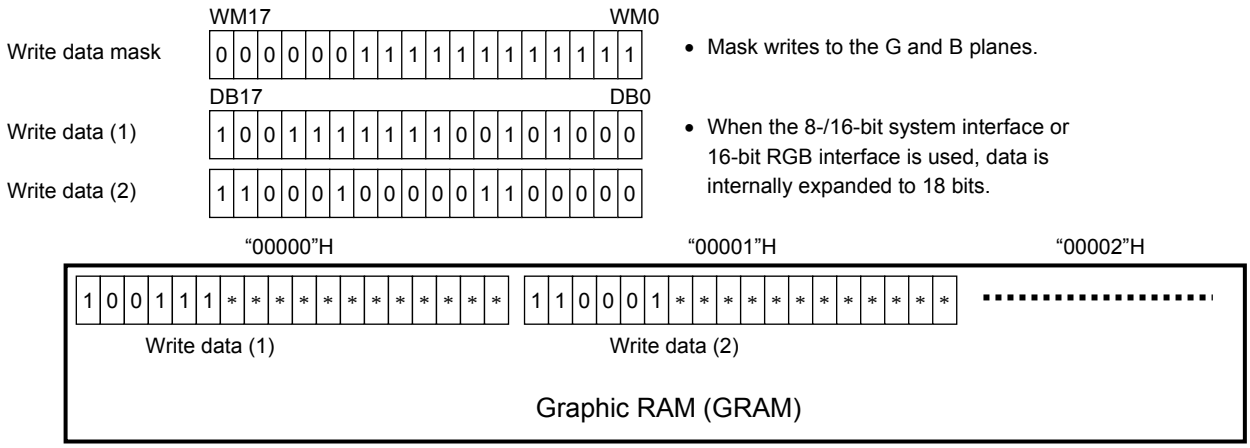
Figure 20 Example write data mask operation

Example graphic operation

(1) Write mode 1: AM = "0"

Write mode 1 is used to write data at high speed in the horizontal direction. It is useful for initializing the graphic RAM (GRAM) or drawing a horizontal rule. The write data mask feature (WM17-0) can also be used in this mode. Upon a write, the address counter (AC) automatically increments (I/D = "1") or decrements (I/D = "0") by one. Once the address reaches the left-edge or right-edge end of graphic RAM (GRAM), the address automatically jumps to the other end of the next line.

Example
1) I/D = "1", AM = "0"
2) WM17–0 = "007FF"H
3) AC = "00000"H

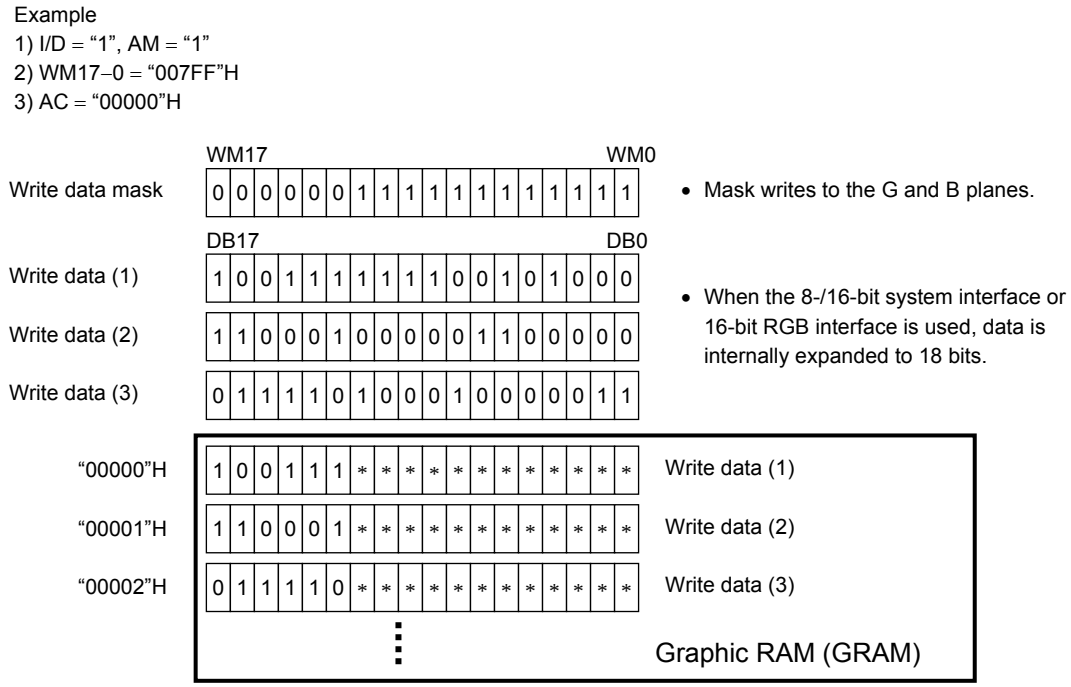


Note 1: The GRAM bits represented with an asterisk are not rewritten.

Figure 21 Example write operation in write mode 1

(2) Write mode 2: AM = "1"

Write mode 1 is used to write data at high speed in the vertical direction. It is useful for initializing the graphic RAM (GRAM), expanding the font pattern vertically, or drawing a vertical rule. The write data mask feature (WM17-0) can also be used in this mode. Upon a write, the address counter (AC) automatically increments by 256. Once the address reaches the bottom of graphic RAM (GRAM), the address automatically jumps to the top of the next vertical line to the right (I/D = "1") or to the left (I/D = "0").



Note 1: The GRAM bits represented with an asterisk are not rewritten.

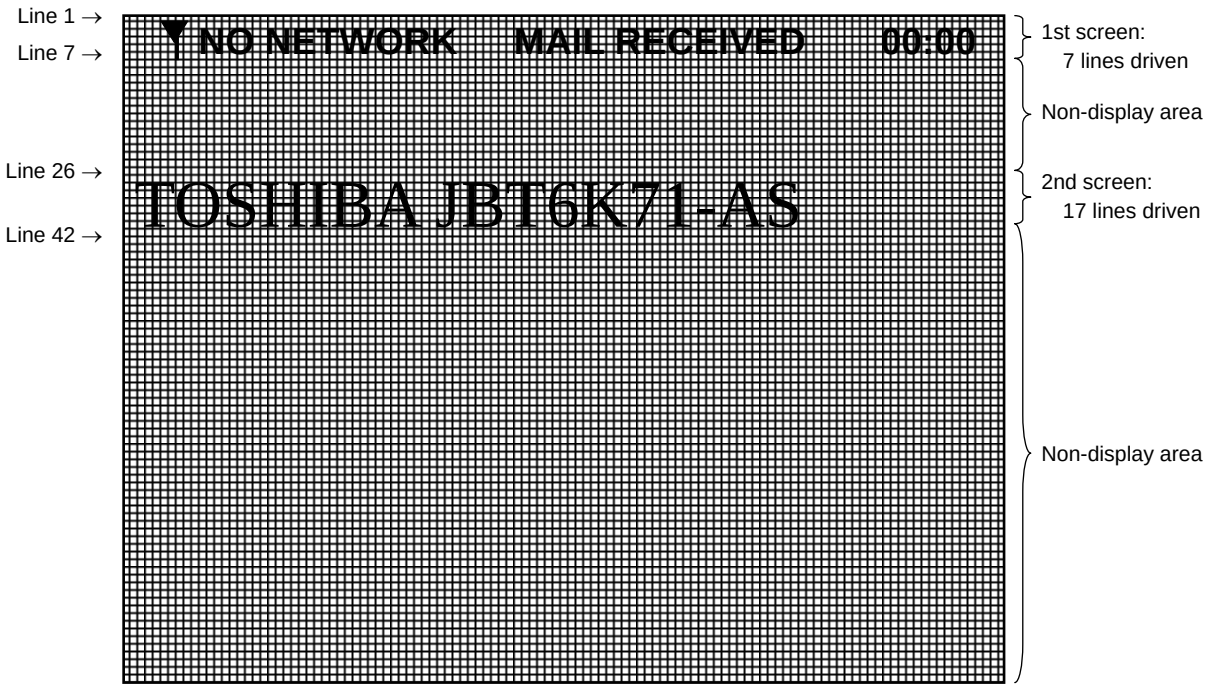
Note 2: Once address "13F00" H has been written, the address counter (AC) jumps to "00001" H.

Figure 22 Example write operation in write mode 2

Split Screen Driving

The JBT6K71-AS can use the screen driving position registers (R402-R405) to drive two screens at arbitrary positions. Selectively driving two screens that need to be displayed can contribute to reduction in power dissipation. For the first split screen, the first screen drive position registers (R402 and R403) specify the start line (SS18-10) and end line (SE18-10). For the second split screen, the second screen drive position registers (R404 and R405) specify the start line (SS28-20) and end line (SE28-20). Controlling the second screen is enabled only when the SPT bit is set to "1". Ensure that the total number of lines driven on the first and second screens does not exceed the specified number of LCD lines to be driven.

2-screen driving



- Number of lines driven: NL5-0 = "100111" (320 lines)
- First screen settings: SS1810 = "00"H, SE18-10 = "06"H
- Second screen settings: SS28-20 = "19"H, SE28-20 = "29"H, SPT = "1"

Figure 23 Example display with two split screens

The driver output for the non-display areas during partial display can be configured as follows. Specify appropriate configuration according to the panel characteristics.

PT1	PT0	Source Output in Non-display Area				ASW Output in Non-display Area	The refresh function for Non-display Area
		NBW=0		NBW=1			
		Positive	Negative	Positive	Negative		
0	0	L63	L63	L0	L0	Normal drive	Invalid
0	1	L63	L63	L0	L0	"Low"	Valid
1	0	VSS		VSS		"Low"	Valid
1	1	Hi-Z		Hi-Z		"Low"	Valid

Restrictions on the setting of the first/second screen drive position registers

The following restrictions are imposed on the start line (SS18-10) and end line (SE18-10) settings in the first screen drive position register and the start line (SS27-20) and end line (SE28-20) settings in the second screen drive position register. Note that failing to satisfy the requirements causes the JBT6K71-AS to malfunction.

Table 7 Display operation and restrictions when a single screen is driven (SPT = "0")

Register Settings	Display Operation
(SE18-10) − (SS18-10) = NL	Full screen display Normally display the range from (SE18-10) to (SS18-10).
(SE18-10) − (SS18-10) < NL	Partial display Normally display the range from (SE18-10) to (SS18-10). Other areas are not displayed regardless of the RAM data.
(SE18-10) − (SS18-10) > NL	Setting prohibited

Note 1: Ensure that SS18-10 ≤ SE18-0 ≤ "13F"H.

Note 2: Settings in SE28-20 and SS28-20 are invalid.

Table 8 Display operation and restrictions when two split screens are driven (SPT = "1")

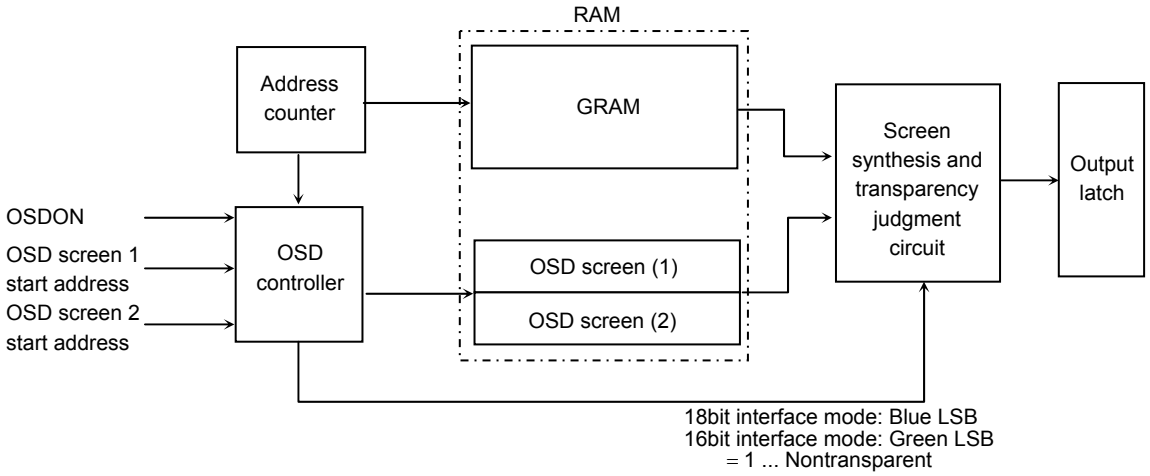
Register Settings	Display Operation
((SE18-10) − (SS18-10)) + ((SE28-20) − (SS28-20)) = NL	Full screen display Normally display the range from (SE18-10) to (SS18-10) and from (SE28-20) to (SS28-20).
((SE18-10) − (SS18-10)) + ((SE28-20) − (SS28-20)) < NL	Partial display Normally display the range from (SE18-10) to (SS18-10) and from (SE28-20) to (SS28-20). Other areas are not displayed regardless of the RAM data.
((SE18-10) − (SS18-10)) + ((SE28-20) − (SS28-20)) > NL	Setting prohibited

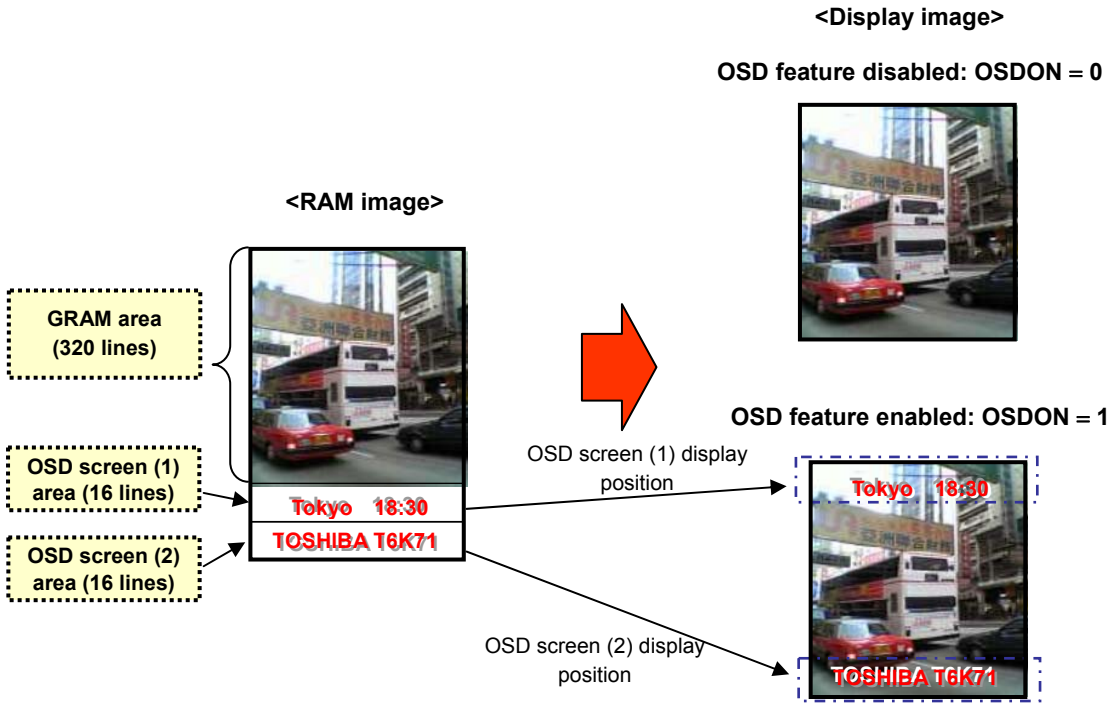
Note 3: Ensure that SS18-10 ≤ SE18-10 < SS28-20 ≤ SE28-20 ≤ "13F"H.

Note 4: Ensure that (SE28-20) − (SS18-10) ≤ NL.

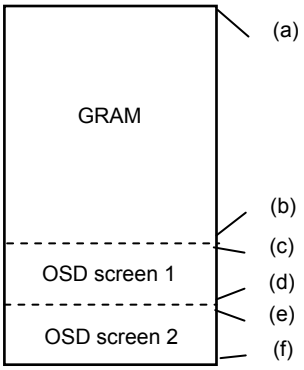
OSD Feature

The JBT6K71-AS supports an OSD feature, which can overlay icons or other images in MAX 130,000 colors without rewriting display data in GRAM. The OSD feature can be enabled or disabled using the OSDON bit. When the OSD feature is enabled, a bit of data stored in the OSD memory area (LSB of blue data in 18bit interface mode or LSB of green data in 16bit interface mode) specifies whether the OSD data will be transparent or not.





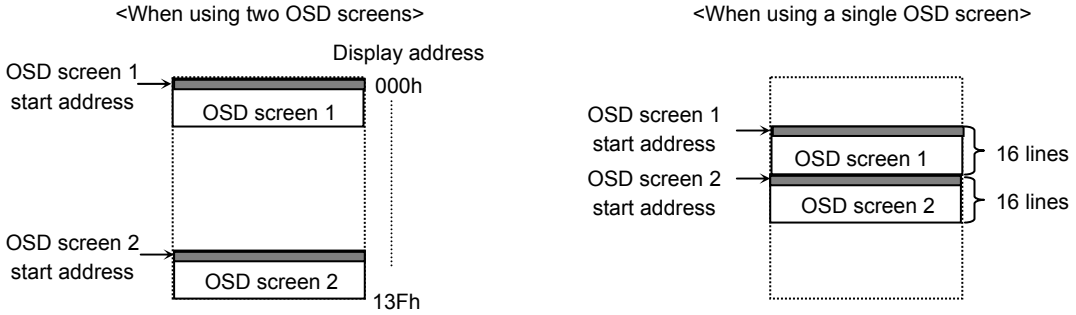
In the same way as GRAM addresses, memory addresses for OSD screens are specified using indexes 0200h and 0201h. Setting OSDW to 1 causes corresponding RAM addresses to be handled as OSD-dedicated memory addresses.



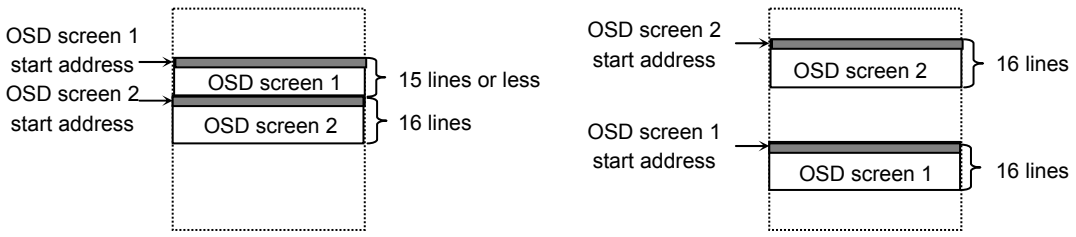
	RAM adr (AD16-AD8)	
	OSDW = 0	OSDW = 1
(a)	000h	—
(b)	13Fh	—
(c)	140h	000h
(d)	14Fh	00Fh
(e)	150h	010h
(f)	15Fh	01Fh

Figure 24 Memory address map for OSD screens

The OSD feature divides the OSD area into two 16-line screens (OSD screens 1 and 2). Each screen can be easily positioned by specifying its start address (index: 0504h, 0505h), thus facilitating the display of icons at the top or bottom of the LCD. The OSD feature also supports X/Y expansion mode when writing OSD data.



Note: The OSD screen 1 start address plus 16 lines must not exceed the OSD screen 2 start address.



Example: The OSD screen 1 area overlaps the OSD screen 2 area.

Example: The OSD screen 2 start address precedes the OSD screen 1 start address.

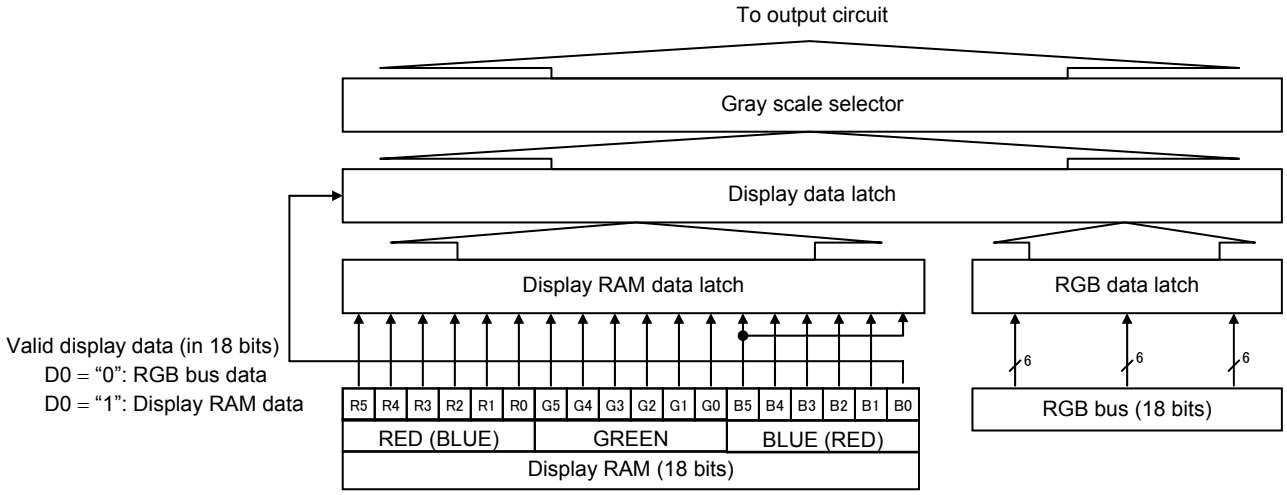
Figure 25 OSD screen start addresses

Superimposition Feature

The JBT6K71-AS supports a superimposition feature, which can enable display RAM data in pixel units within the moving image display area. This feature helps to easily implement an application that overwrites text on a moving image. The following details the feature:

When the SIP bit is set to "1", setting the display RAM transparency judgment bit (blue LSB for 18-bit data or green LSB for 16-bit data) to "1" in the moving image display area causes RAM data to be forcibly handled as valid data in pixel units. Data accesses to RAM are made through the MPU bus, so that RAM data can be modified independently of the moving image display.

When SIP = "1", RAM data can be displayed in 131,072 colors in 262,144-color mode and 32,768 colors in 65,536-color mode.



SIP	Transparency Judgment	Valid Display Data
0	*	Normal mode
1	0	RGB bus data
	1	Display RAM data

Display Data Bits	Transparency Judgment Bit
18-bit mode	Blue LSB (B0)
16-bit mode	Green LSB (G0)

*: For information on the relationship between the MPU bus bit lines and display data bits, refer to "MPU Interface Mode Settings."

Note 1: In superimposition mode, use the MPU interface (RM = 0) for RAM accesses.

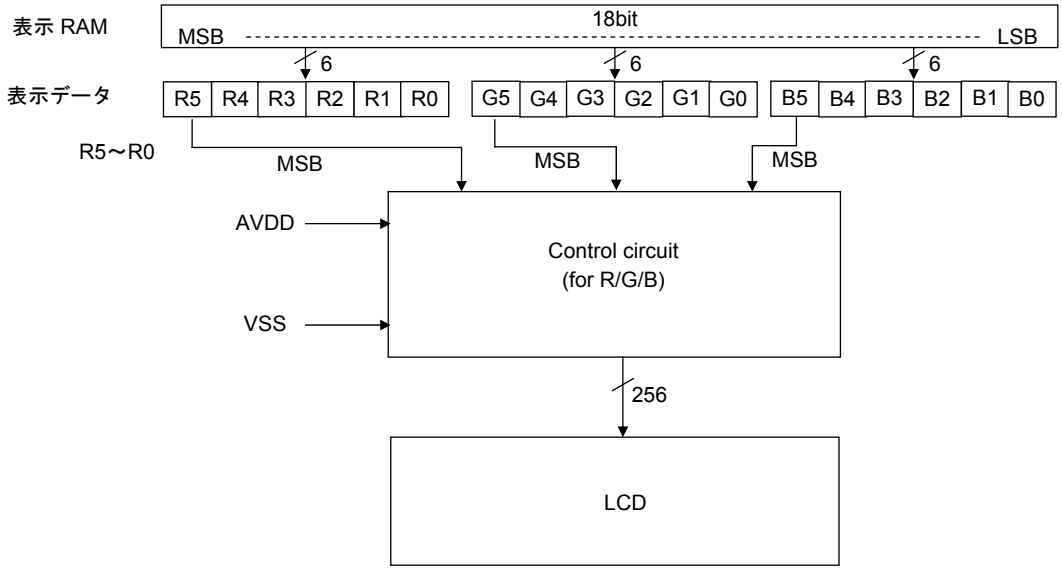
Note 2: When modifying MPU interface mode settings, update the contents of the display RAM using an appropriate data format according to the displayed data bits.

JBT6K71-AS mode table (00Ch for register)

No.	RM	DM1	DM0	Basic working interface	Clock for display	Writable RAM interface	Mode detail
1	0	0	0	MPU	OSC	MPU	MPU interface mode Not use superimposes (SIP) function. But OSD has same function.
2	0	0	1	RGB / MPU	RGB	MPU	RGB interface mode(1) The display data operation is controlled by RGB interface. When using the RGB interface mode, not changed the display RAM data. But using the superimpose function, valid the display RAM data.
3	0	1	0	MPU / VSYMC	OSC+VSYNC	MPU	VSYNC interface mode Internal display clock generates with synchronized clock of VSYNC. Operation detail is same as normal working mode
4	0	1	1	Setting prohibited			
5	1	0	0	Setting prohibited			
6	1	0	1	RGB	RGB	RGB	RGB interface mode(2) Instruction setting is controlled by MPU. But all display data operation is controlled by RGB interface.
7	1	1	0	Setting prohibited			
8	1	1	1	Setting prohibited			

Gray scale select for 8 colors display mode

JBT6K71-AS has 8 colors display mode. Gray scale level uses AVDD and VSS. So Low power consumption for no-use other level power (V0-V63). But R/G/B selects AVDD or VSS with MSB data in GRAM automatically. Only setting COL register, Change 8 colors or normal display mode without re-writing GRAM data.



Display Color mode command of JBT6K71-AS(COL1/COL0) is enable as next flame change after command access. But when AMP OFF→AMP ON. Need idling period until starting normal AMP circuit operation.

So, when 8 colors → 262Kcolors /65Kcolors, Need to set long blanking period (BP) for this idling period.

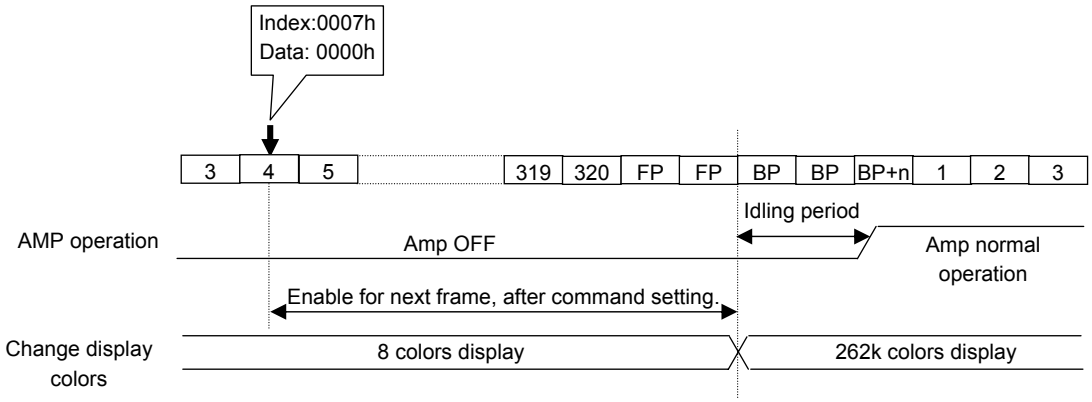
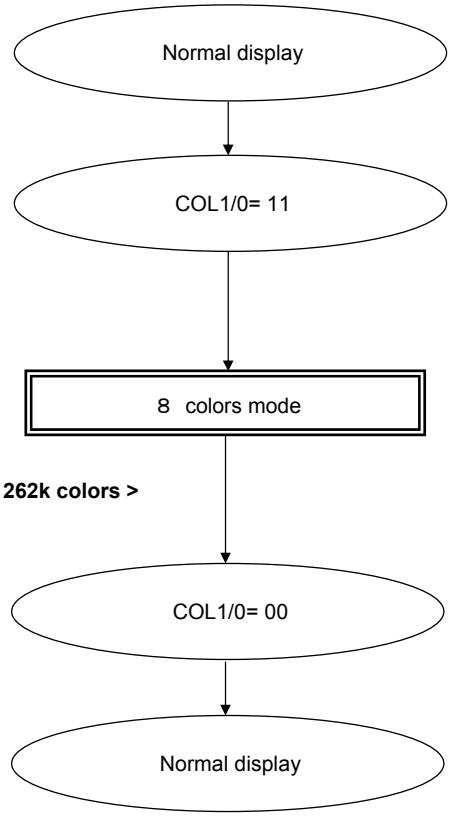


Figure The operation after 8 colors → 262K/65Kcolors display

The operation sequence of 8 colors display mode is the below.

< 262k Colors → 8 colors >



262k colors display

Index:007h Data: D15=1, D14=1
Simultaneously output AMP off and each level power is off for low power consumption mode,

< 8 colors → 262k colors >

Index:007h Data: D15=0, D14=0
This resister change 8 colors to 262k colors from next frame.
Also, Output AMP ON and each level power is ON.

Normal LCD display for 262k colors.

Display ON sequence (1)

Normal operation is enable next frame changing (Blanking between FP and BP)after command setting. And necessary command for display on/off build up NDEX:100h. Each circuit is ON simultaneously.

Need to set oscillate → ON(INDEX : 000h OSC=1) before setting PO=1 command. Raise up PO bit=0 →1 as well as VDD and XVDD regulator circuit.

Display ON sequence (2)

After setting INDEX: 101h=0001h(AUTO=1). Each circuits are ON as hardware with setting INDEX: 100h= FFFEh sequentially.

Display OFF sequence

The display off sequence of T6K71 is below. After the same display ON command setting. The basic operation is enable next frame changing (Between FP and BP at blanking). Then the regulator OFF for VCOM is enable after 10H after the changing frame. The FDON OFF is enable after 2H after the changing frame. And When ON(0→1). DCG bit is enable at the changing frame. When OFF(1→0). DCG bit is enable after the command setting. when PO=1→0. The INDEX:100h is all clear but DCG bit.

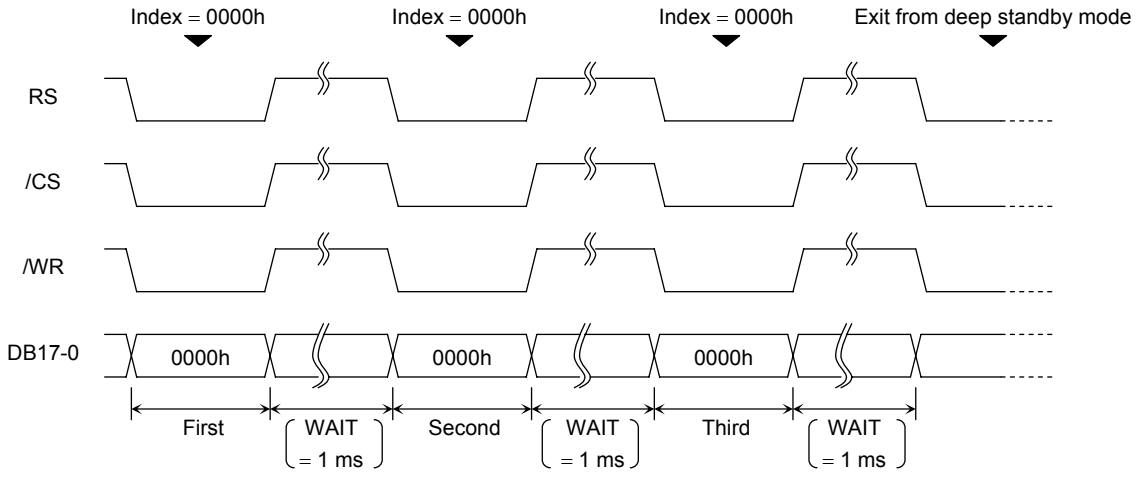
Note: For detail, refer to the application note.

Exiting from Deep Standby Mode

Upon powered up, the JBT6K71-AS enters deep standby mode. It can exit from deep standby mode only by applying the method described below. Terminating deep standby mode also requires a key code. Always use the following flow when releasing the JBT6K71-AS from deep standby mode:

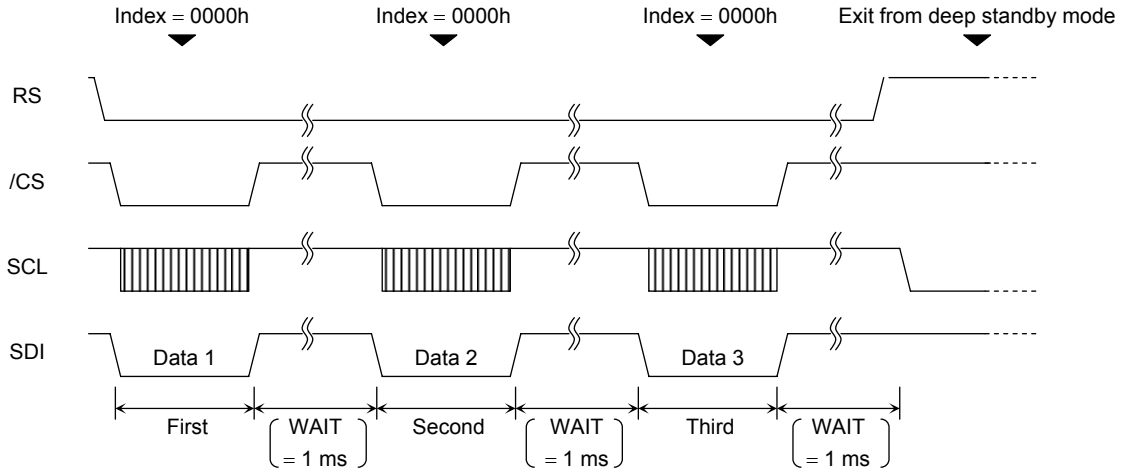
1) When using the parallel interface

Upon power-up, a sequence of three accesses to index register 0000h causes the JBT6K71-AS to exit from deep standby mode. The JBT6K71-AS does not exit from deep standby mode if an index register number other than 0000h is specified. Ensure that index register 0000h is written because 0000h is recognized as the access code. If another command (index data write, data read, or forced index read) is executed while index register numbers are being written, any previously written 0000h settings for terminating deep standby mode are reset and invalidated. To terminate deep standby mode, ensure that the index number (0000h) is written to the JBT6K71-AS three times in a row. The following figure shows how to write the index number:



2) When using the serial interface

Upon power-up, a sequence of three accesses to index register 0000h causes the JBT6K71-AS to exit from deep standby mode, in the same way as with the parallel interface. With the serial interface, data input to the JBT6K71-AS consists of (1) start byte, (2) index register upper byte, and (3) index register lower byte, totaling 24 bits. It is necessary to supply that 24-bit sequence three times to terminate deep standby mode. For details, see the following figure:

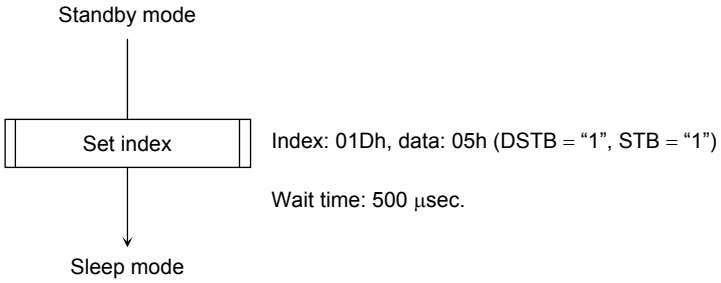


Contents of data 1/2/3

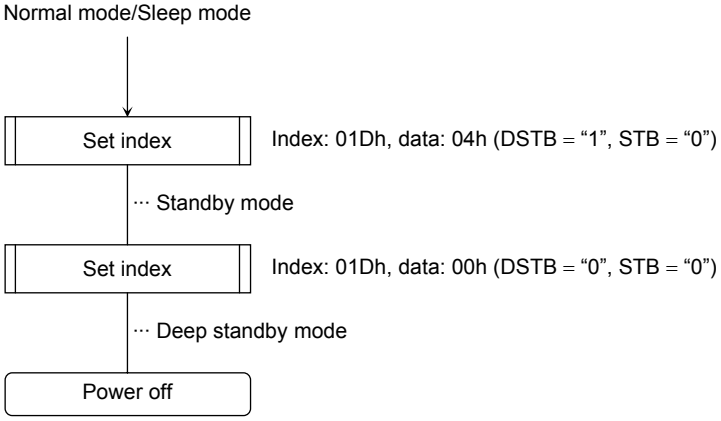
Start Byte (8 bits)								Set Index Register (16 bits)	
*	*	*	*	*	ID	RS	RW	Upper byte (8 bits)	Lower byte (8 bits)
0	0	0	0	0	0	0	0	00000000b	00000000b

Exiting from Standby Mode

A command can be used to release the JBT6K71-AS from standby mode. The command is input by setting an index register. A wait time is required before the JBT6K71-AS enters sleep mode. After entering a command for terminating standby mode, ensure that the JBT6K71-AS waits for sufficient time before starting operation. The following flowchart shows the sequence for terminating standby mode:



When turning off the power from normal or sleep mode, first place the JBT6K71-AS in standby mode and then in deep standby mode before powering the device off.



The circuit operation status for each mode

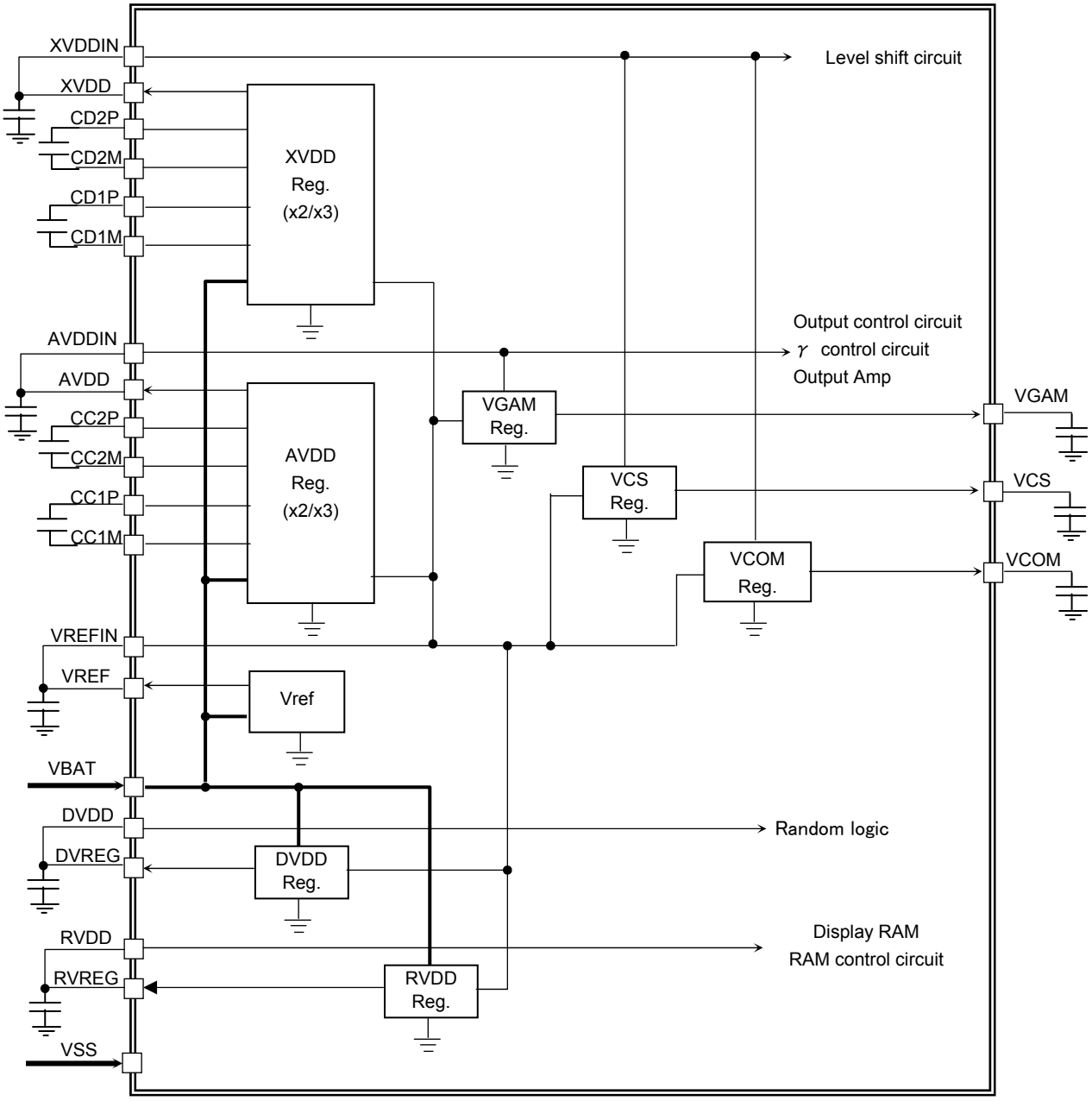
The circuit operation status for each mode of JBT6K71-AS is below

Function circuit	Deep st/by status	st/by status	Sleep status	Normal status
Vsys power circuit	Active	Active	Active	Active
Vref circuit	Disable	Active	Active	Active
Regulator for command	Disable	Active	Active	Active
MPU I/F(Logic)	Disable	Active	Active	Active
Command register (Logic)	Disable	Active	Active	Active
Regulator for RAM	Disable	Disable	Active	Active
RAM for display	Disable	Disable	Active	Active
Oscillator	Disable	Disable ※1	Disable ※1	Active
Timing generator circuit	Disable	Disable	Disable	Active
Output circuit	Disable	Disable	Disable	Active
Level shift circuit	Disable	Disable	Disable	Active
Regulator circuit	Disable	Disable	Disable	Active
Regulator circuit for display	Disable	Disable	Disable	Active

* When st/by and Sleep status, Control at OSC ON/OFF command.

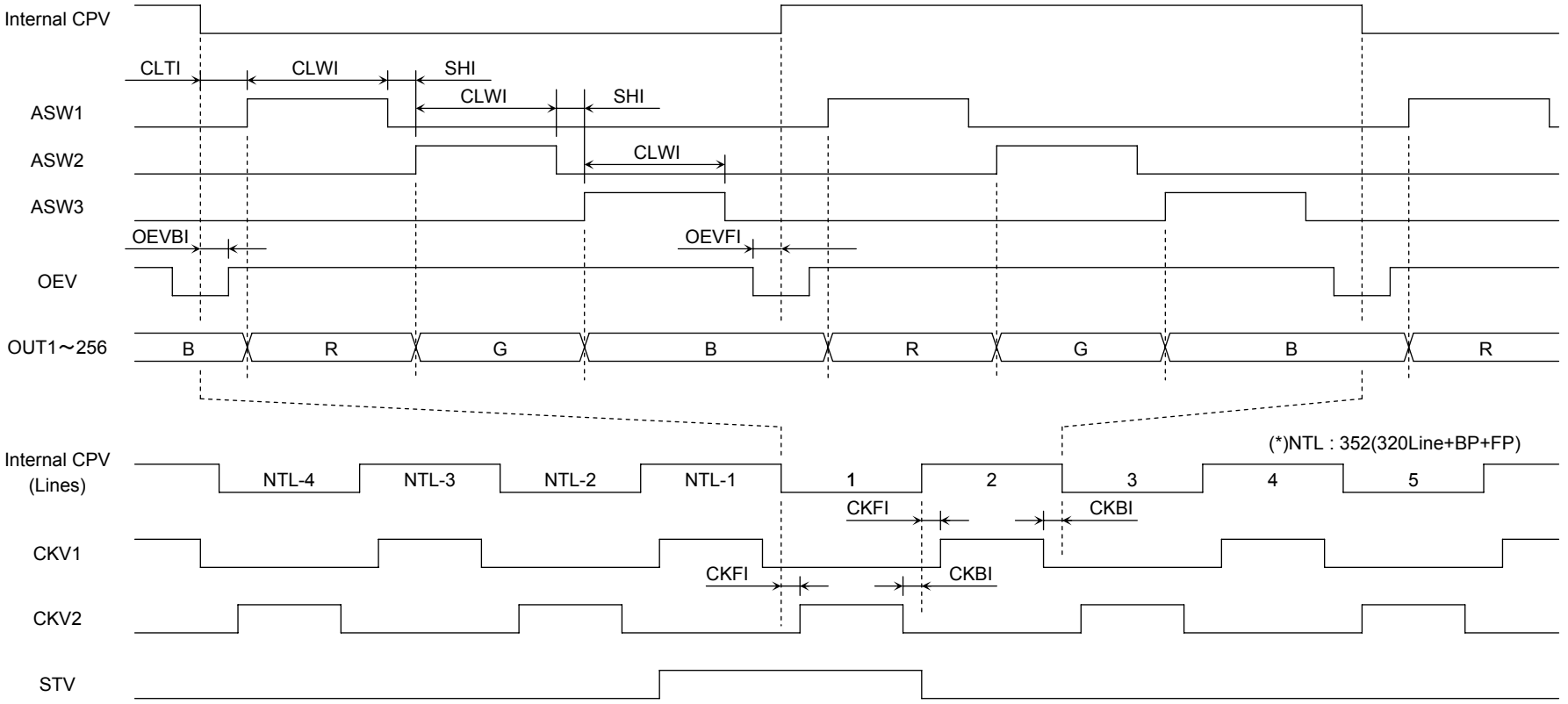
Power circuit diagram

JBT6K71-AS has 2 system regulator circuits and regulator for gamma and regulator for VCOM and regulator circuit for internal system power and DCDC circuit control function for LCD internal gate.



Power circuit diagram

Timing control sequence (Use internal OSC)



Timing variation for using Internal clock (internal OSC)

Index Command	012h	012h	014h	013h	013h	015h	015h

No.	BIN	CLTI		CLWI		SHI		OEVBI		OEVFI		CKFI		CKBI	
		CLK	Time	CLK	Time	CLK	Time	CLK	Time	CLK	Time	CLK	Time	CLK	Time
1	0000	0.0	0.0	Setting prohibited		0.5	1.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
2	0001	0.5	1.0	3.0	6.0	1.0	2.0	0.5	1.0	0.5	1.0	0.5	1.0	0.5	1.0
3	0010	1.0	2.0	3.5	7.0	1.5	3.0	1.0	2.0	1.0	2.0	1.0	2.0	1.0	2.0
4	0011	1.5	3.0	4.0	8.0	2.0	4.0	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0
5	0100			4.5	9.0										
6	0101			5.0	10.0										
7	0110			5.5	11.0										
8	0111			6.0	12.0										
9	1000			6.5	13.0										
10	1001			7.0	14.0										
11	1010			7.5	15.0										
12	1011			8.0	16.0										
13	1100			8.5	17.0										
14	1101			9.0	18.0										
15	1110			9.5	19.0										
16	1111			Setting prohibited											

Unit : μs

(Note)Please notice the below rule at making of internal timing.

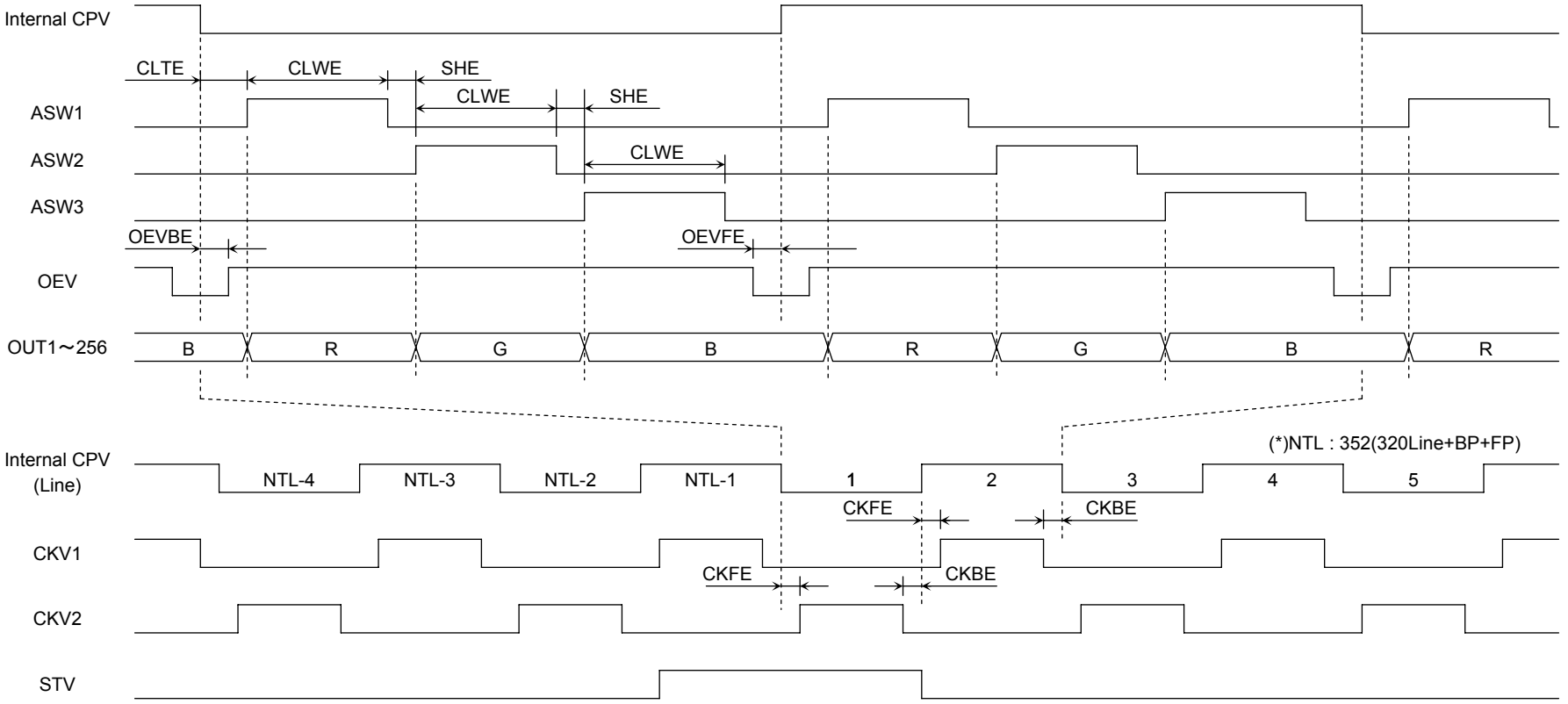
① CLTI(1-0) + CLWI(3-0) ≧ 3 CLOCK

② CLWI(3-0) + SHI(1-0) ≧ 3 CLOCK

*When use internal clock. Internal clock is generated by divided oscillator frequency. Then, The reference of internal clock is decided by DIVI(1-0). Please control the timing with divided frequency for DIVI.

*fosc = 500kHz, Time rate is 2μsec.

Timing control sequence (Use DOTCLK)



Timing variation of using external clock (DOTCLK)

Index Command	018h	018h	01Ah	019h	019h	01Bh	01Bh

No.	BIN	CLTE		CLWE		SHE		OEVBE		OEVFE		CKFE		CKBE	
		CLK	Time	CLK	Time	CLK	Time	CLK	Time	CLK	Time	CLK	Time	CLK	Time
1	000000	0.0	0.0	Setting prohibited		0.5	0.1	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
2	000001	0.5	0.1	3.0	0.6	1.0	0.2	0.5	0.1	0.5	0.1	0.5	0.1	0.5	0.1
3	000010	1.0	0.2	3.5	0.7	1.5	0.3	1.0	0.2	1.0	0.2	1.0	0.2	1.0	0.2
4	000011	1.5	0.3	4.0	0.8	2.0	0.4	1.5	0.3	1.5	0.3	1.5	0.3	1.5	0.3
5	000100	2.0	0.4	4.5	0.9	2.5	0.5	2.0	0.4	2.0	0.4	2.0	0.4	2.0	0.4
6	000101	2.5	0.5	5.0	1.0	3.0	0.6	2.5	0.5	2.5	0.5	2.5	0.5	2.5	0.5
7	000110	3.0	0.6	5.5	1.1	3.5	0.7	3.0	0.6	3.0	0.6	3.0	0.6	3.0	0.6
8	000111	3.5	0.7	6.0	1.2	4.0	0.8	3.5	0.7	3.5	0.7	3.5	0.7	3.5	0.7
9	001000	4.0	0.8	6.5	1.3	4.5	0.9	4.0	0.8	4.0	0.8	4.0	0.8	4.0	0.8
10	001001	4.5	0.9	7.0	1.4	5.0	1.0	4.5	0.9	4.5	0.9	4.5	0.9	4.5	0.9
11	001010	5.0	1.0	7.5	1.5	5.5	1.1	5.0	1.0	5.0	1.0	5.0	1.0	5.0	1.0
12	001011	5.5	1.1	8.0	1.6	6.0	1.2	5.5	1.1	5.5	1.1	5.5	1.1	5.5	1.1
13	001100	6.0	1.2	8.5	1.7	6.5	1.3	6.0	1.2	6.0	1.2	6.0	1.2	6.0	1.2
14	001101	6.5	1.3	9.0	1.8	7.0	1.4	6.5	1.3	6.5	1.3	6.5	1.3	6.5	1.3
15	001110	7.0	1.4	9.5	1.9	7.5	1.5	7.0	1.4	7.0	1.4	7.0	1.4	7.0	1.4
16	001111	7.5	1.5	10.0	2.0	8.0	1.6	7.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5
17	111100			10.5	2.1										
61	111101			33.0	6.5										
62	111110			33.5	6.7										
63	111111			34.0	6.8										

Unit : μs

(Note)Please notice the below rule at making of internal timing.

① CLTE(1-0) + CLWE3-0) ≧ 3 CLOCK

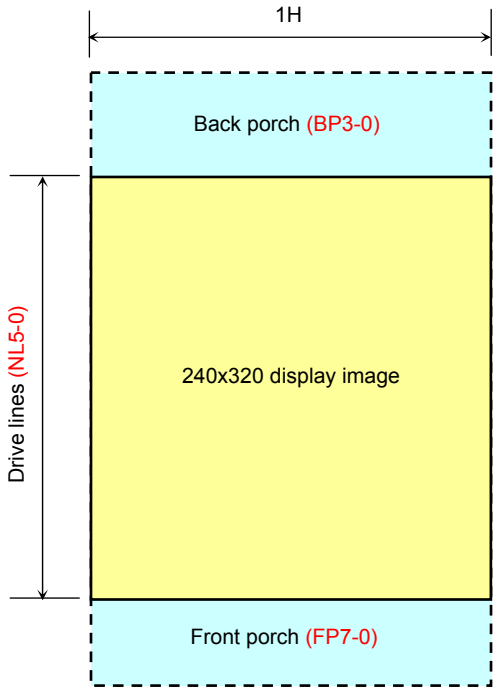
② CLWE(3-0) + SHE(1-0) ≧ 3 CLOCK

*DOTCLK =5MHz, Time rate is 0.2μsec.

*When use DOTCLK. Internal clock is generated by divided DOTCLK frequency.
Then, The reference of internal clock is decided by DIVI(3-0). Please control the timing with divided frequency for DIVI.

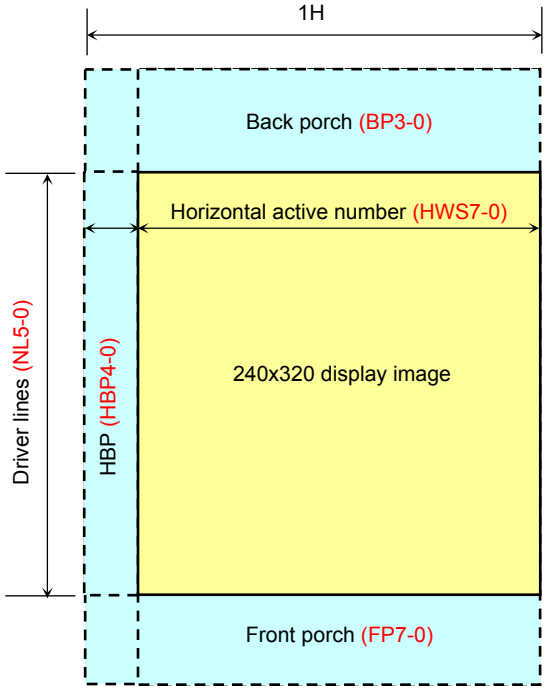
Register setting for display area condition

In case of internal oscillator, the JBT6K71-AS(A) need the register setting for display condition as below.



$$1H = \text{division rate(DIVI1-0)} \times \text{1H clock number(RTNI4-0)} \times \frac{1}{fosc}$$

If select the RGB interface mode, need the register setting for display condition as below.



$$1H = \text{division rate (DIVE1-0)} \times \text{1 line clock number(RTNE4-0)} \times \frac{1}{DOTCLK}$$

$$\text{1 line clock number} \geqq \text{HBP + Horizontal active number}$$

Note: The horizontal active number less than 256lines, changing the first output terminal and HBP number.

DMA function

The JBT6K71-AS(A) has DMA (Direct Memory Access) function. The Microprocessor writing access to external memory that the JBT6K71-AS(A) reading the display data by /DACK= “L”.

(1)DMA terminal function

/CS	: When using the DMA function, /CS=”Low” select.
/RD	: /DACK=”L”, mean the display data write clock.
/WR	: When using the DMA function, /WR=”High” select.
/DACK	: Mean the chip select signal
/RS	: When using the DMA function, internal condition is High level.
VLD	: When using the DMA function, need the display RAM active(ex. VPL=”Low”, VLLD=”L”)
DB15-DB0	: Data bus

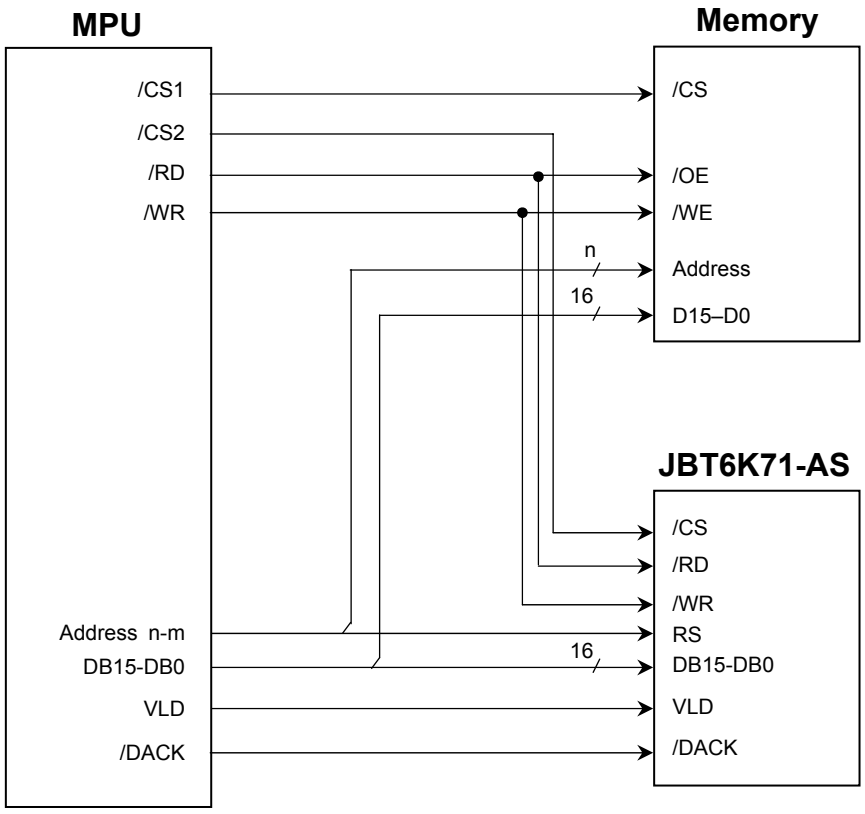


Figure Application circuit MPU, Memory and JBT6K71-AS(A)

(2)DMA data transfer

a) DMA single address mode (Cycle steel mode)

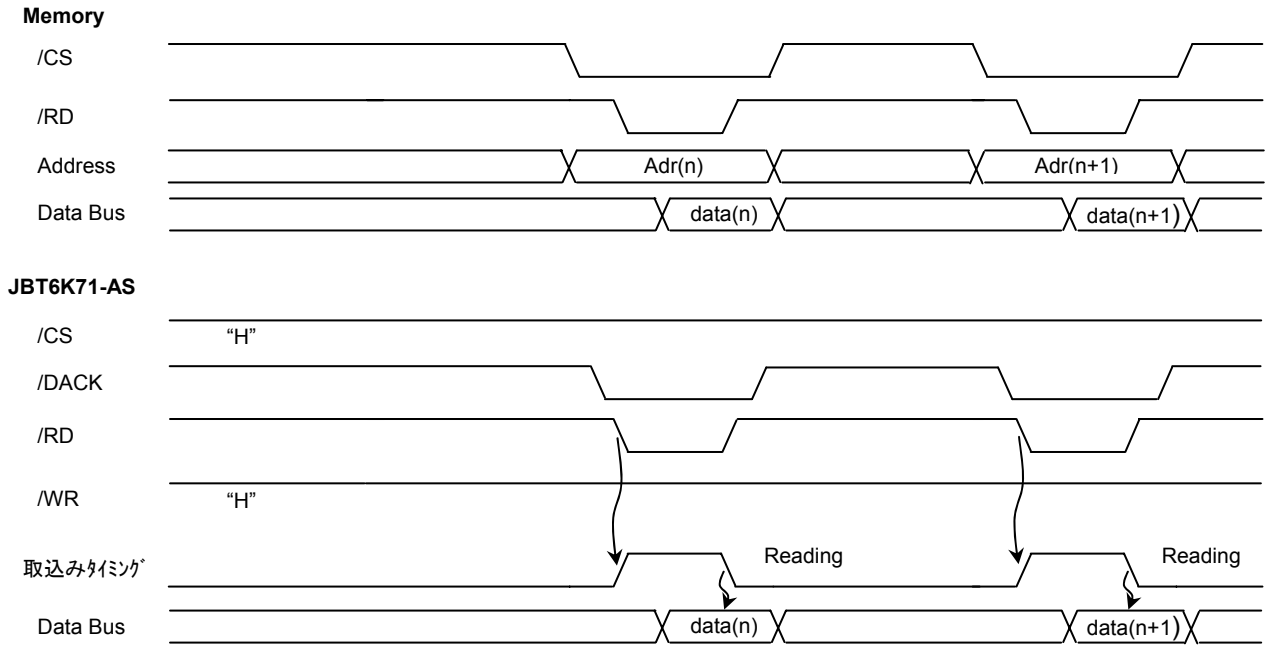
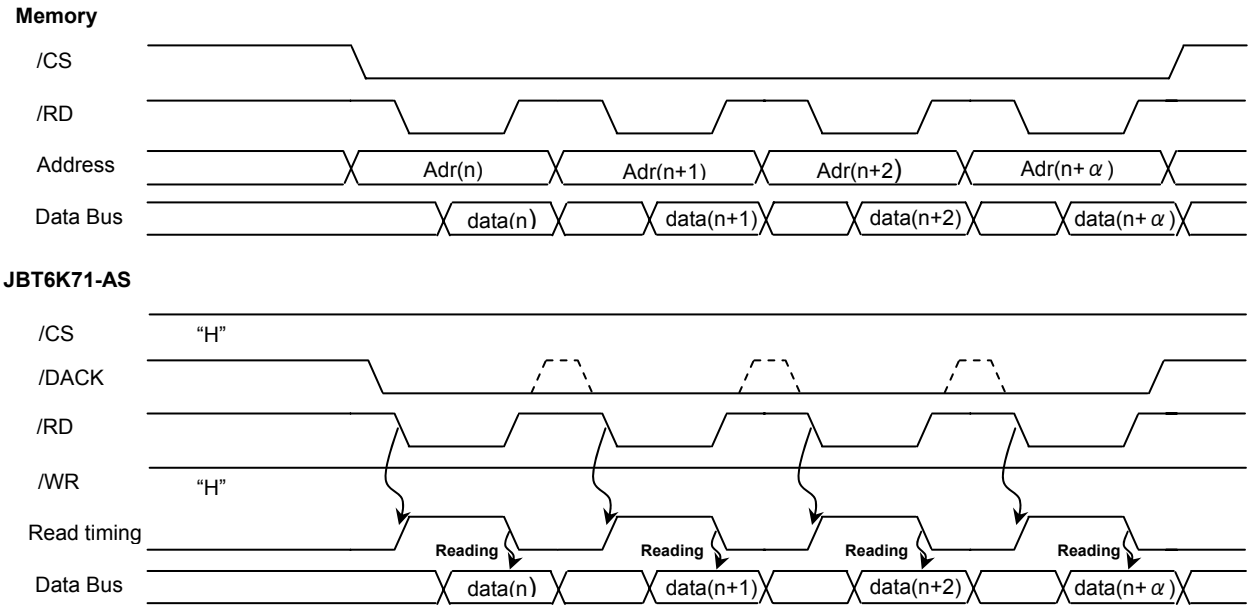


Table of JBT6K71-AS(A) terminal condition

Terminal	/DACK="H"	/DACK="L"
/RESET	/RESET	/RESET
/CS	/CS	"High" connect
RS	RS	Internal condition is "High"
/RD	/RD	display data write clock
/WR	/WR	"High" connect
DB15-DB0	DB15-DB0	DB15-DB0

Note: If microprocessor writing access to memory, can not use the DMA function (setting prohibited the /DACK="Low")

b) DMA single address mode (Burst mode)

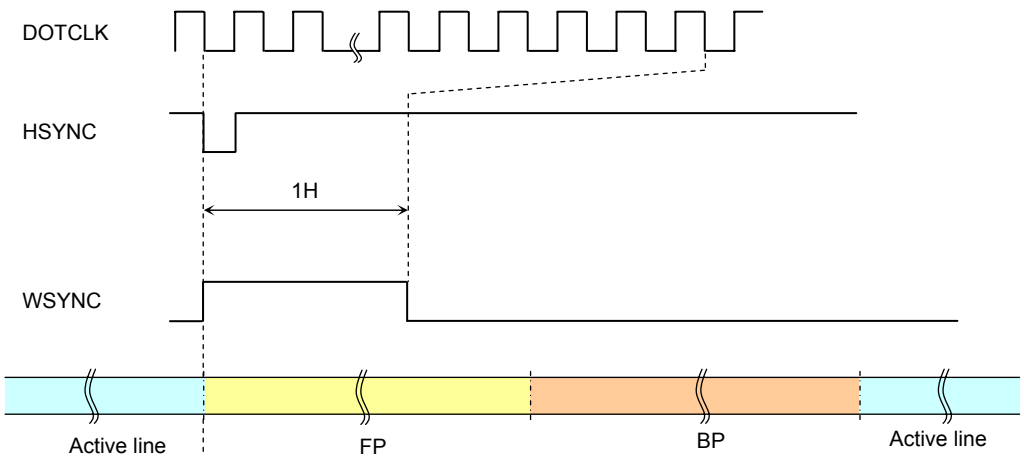


Notices:

- JBT6K71-AS(A) can not use the dual address mode. Only the single address mode(Cycle steel mode/Burst mode)
- JBT6K71-AS can not access to external memory by DMA function.
- JBT6K71-AS can not terminal condition of /DACK="Low" and /CS="Low"
- Setting the high-speed write mode (HMW="1") only.
- Need the same data number of window area data number and DMA transfer data number.
- Using the DMA function, AC characteristics rule
- Command access is prohibited between start of DMA function to finish the data transfer.
- Display RAM Access is prohibited that other data transfer on DMA function
- After the data transfer, need the wait time of run time of display RAM write to next instruction.

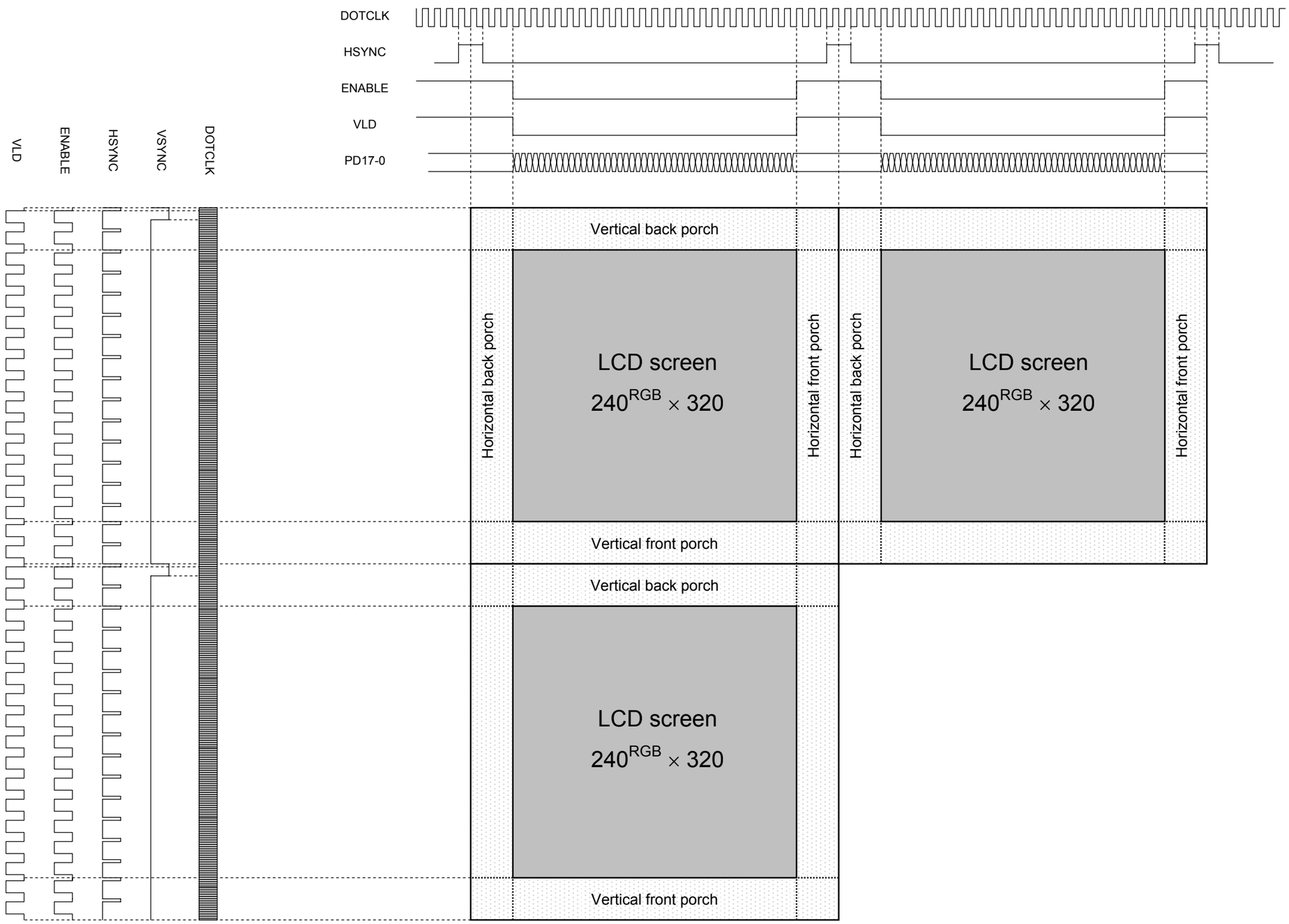
WSYNC signal

The JBT6K71-AS(A) is outputting the WSYNC signal as the management method for synchronizing a display control clock and the write-in control clock to Display RAM transmitted from microprocessor.
A WSYNC signal makes 1H high level output after the display end of an effective line. The position of a display line is able to manage this high level by managing by the microprocessor side. A collision and passing of data can be prevented because this manages two, the timing of display scan, and Display RAM data write-in timing.



JBT6K71-AS Timing Chart (1)

When using the RGB interface



Absolute Maximum Ratings
(AV_{SS} = DV_{SS} = 0 V and Ta = 25°C, unless otherwise specified)

Characteristics		Symbol	Rating	Unit
Supply voltage		V_{SYS}	−0.3 ~ 4.6	V
		V_{BAT}	−0.3 ~ 4.6	
		AV_{DD}	−0.3 ~ 6.5	
Input voltage		V_{IND}	−0.3 ~ VSYS + 0.3	V
		V_{INA}	−0.3 ~ AV_{DD} + 0.3	
Output voltage	I/O	V_{OUT1}	−0.3 ~ VSYS + 0.3	V
	OUT	V_{OUT2}	−0.3 ~ AV_{DD} + 0.3	
Operating temperature		T_{opr}	−20 ~ 75	°C
Storage temperature		T_{stg}	−55 ~ 125	°C

Note: Reference voltages must satisfy the following relationship: VSYS≦VBAT≦AVDD

Electrical Characteristics

DC Characteristics (1)

VBAT = 2.4~3.3 V, AVDD = 4.5~5.5 V, VSYS = 1.7~3.3 V, VREF = 1.5 V, Ta = -20~75°C unless otherwise specified. For typical values, VBAT = 3.0 V, AVDD = 5.0 V, VSYS = 3.0 V, VREF = 1.5 V, Ta = 25°C。

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Pins
Operating voltage (1)		V_{SYS}	—	—	1.7	—	3.3	V	V_{SYS}
Operating voltage (2)		V_{BAT}	—	—	2.4	—	3.3	V	V_{BAT}
Input voltage (1)		V_{REFIN}	—	(Note1)		1.5		V	V_{REFIN}
Input voltage (2)		RV_{DD}	—	(Note1)		1.5		V	RV_{DD}
Input voltage (3)		DV_{DD}	—	(Note1)		1.5		V	DV_{DD}
Input voltage (4)	Low	V_{IL}	—	—	0		0.2 V_{SYS}	V	(Note3)
	High	V_{IH}			0.8 V_{SYS}		V_{SYS}	V	
Input current	Low	I_{IL}	—	—			1	μA	(Note3)
	High	I_{IH}					1		
Output voltage(1)	Low	V_{OL}	—	I_{OL} = 0.1 mA	0		0.5	V	(Note4)
	High	V_{OH}		I_{OH} = −0.1 mA	V_{SYS} − 0.5		V_{SYS}		
Output voltage (2)	Low	V_{OL2}	—	I_{OL} = 0.1 mA	0		0.5	V	(Note5)
	High	V_{OH2}		I_{OH} = −0.1 mA	XV_{DD} − 0.5		XV_{DD}		
Output voltage (3)	Low	V_{OL3}	—		0		0.05	V	DCCK /DCCK
	High	V_{OH3}			XV_{DD} - 0.05		XV_{DD}		
Output voltage (4)		DV_{REG}	—	—		1.5		V	DV_{REG}
		RV_{REG}	—	—		1.5			RV_{REG}
		V_{REF}	—	—		1.5			V_{REF}
Output voltage		V_{OUT}	—	VG0~VG63	0.1		VDH − 0.1	V	O1～O256
Output voltage deviation		V_{OFF1}	—	C_L = 15 pF VG4 to 59	−25		15	mV	
		V_{OFF2}	—	C_L = 15 pF VG0 to 3, 60 to 63	−40		35	mV	
Output pin voltage deviation		$V_{OFFPIN1}$	—	C_L = 15 pF VG8 to 54			20	Vp-p	
		$V_{OFFPIN2}$	—	C_L = 15 pF VG0 to 7, 55 to 63			30	Vp-p	
Output load capacitance		C_{L1}	—	—			15	pF/pin	

Note1: Input voltage (1) (2)(3) feedbacks to the voltage which is generated internal regulator. Need not to use the external input

Note3: IM0～3, VLD, RS, /CS, /WR, /RD, DB0～DB17, PD0～17, VSYNC, HSYNC, ENABLE, DOTCLK, /DACK, EXTIN1,EXTIN2, OSC1, OSC2

Note4: DB0～DB17, WSYNC

Note5: DCG, DCEV, PEV, FDON, U/D, OEV, FR, CKV1/2, STV, ASW1/2/3, EXOUT1/2

DC Characteristics (2)

VBAT = 2.4~3.3 V, AVDD = 4.5~5.5 V, VSYS = 1.7~3.3 V, VREF = 1.5 V, Ta = -20~75°C unless otherwise specified. For typical values, VBAT = 3.0 V, AVDD = 5.0 V, VSYS = 3.0 V, VREF = 1.5 V, Ta = 25°C。

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Pins
Regulator circuit future(1)	AVD1	—	Iload = 100μA (Note6)	5.30	5.40	—	V	AVDD
	AVD2		Iload = 1.5mA ⊿=AVD1-AVD1' (Note6)	—	—	0.25		
Regulator circuit future (2)	VXD1	—	Iload = 0μA Ta=25°C (Note7)	4.9	5.0	5.1	V	XVDD
	VXD2		Iload = 1.0mA ⊿=VXD1 - VXD1' (Note7)	—	—	0.15		

Note6: VBAT=2.7V, Regulator level setting BAV=0(x2), Clock mode WSEL1=1(Dual mode), DCCLK=20kHz, DCWx=01b(1clk), Ta=25°C

Note7: VBAT=2.7V, Regulator level setting BXV=0(x2), Clock mode WSEL1=1(Dual mode), Voltage adjustment XVDx= 011b(5.0V), DCCLK=20kHz, DCWx=01b(1clk), Ta=25°C

DC Characteristics (3)

VBAT = 2.4~3.3 V, AVDD = 4.5~5.5 V, VSYS = 1.7~3.3 V, VREF = 1.5 V, Ta = -20~75°C unless otherwise specified. For typical values, VBAT = 3.0 V, AVDD = 5.0 V, VSYS = 3.0 V, VREF = 1.5 V, Ta = 25°C。

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Pins
Gamma output voltage future	VGM1	—	Iload = 0μA (Note8)	4.90	5.00	5.05	V	VGM
	VGM2		Iload = 100μA (Note9)	4.90				
COM voltage future (1)	VCD1	—	Iload = 0μA (Note10)	1.95	2.00	2.05	V	VCOM
	VCD2		Iload =100μA (Note11)	—	—	0.05		
COM voltage future (2)	VCS1	—	Iload = 0μA (Note12)	3.95	4.00	4.05	V	VCS
	VCS2		Iload=100μA (NOte13)	—	—	0.05		

Note8: VBAT=2.7V, Voltage adjustment RGMx= 1101b (5.0V), AVDD=5.4V, Ta=25°C

Note9: VGM1 at VGM1'= Load(100uA)

Note10: VBAT=2.7V, Voltage adjustment RCDx= 0110b (2.0V), AVDD=5.4V, Ta=25°C

Note11: VCD2= VCD1-VCD1', VCD1 at VCD1'= Load(100uA)

Note12: VBAT=2.7V, Voltage adjustment RCSx= 1010b (4.0V), AVDD=5.4V, Ta=25°C

Note13: VCS2= VCS1-VCS1', VCS1 at VCS1'= Load(100uA)

DC Characteristics (4)

VBAT = 2.4~3.3 V, AVDD = 4.5~5.5 V, VSYS = 1.7~3.3 V, VREF = 1.5 V, Ta = -20~75°C unless otherwise specified. For typical values, VBAT = 3.0 V, AVDD = 5.0 V, VSYS = 3.0 V, VREF = 1.5 V, Ta = 25°C。

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable Pins
Current consumption (1)	I_{BAT1}	—	(Note14)	—	1.85	3	mA	V_{BAT}
Current consumption (2)	I_{BAT2}	—	(Note15)	—	760	1500	μA	V_{BAT}
Current consumption (3)	I_{SYS1}	—	(Note16)	—	30	45	μA	V_{SYS}
Current consumption (4)	I_{OPE}	—	(Note17)	—	3.8	4.5	mA	V_{BAT}
Current consumption (5)	I_{STBY1}	—	(Note18)	—	65	150	μA	V_{SS}
Current consumption (6)	I_{STBY2}	—	(Note19)	—	25	50	μA	V_{SS}
Current consumption (7)	I_{STBY3}	—	(Note20)	-1	0.5	1	μA	V_{SS}

Note14: VSYS = 1.7 ~ 3.3V, AVDD = 4.5 ~ 5.5V, Frame=70Hz, 262,144colors mode, Ta=25°C

Note15: VSYS = 1.7 ~ 3.3V, AVDD = 4.5 ~ 5.5V, Frame=70Hz, No load, 8colors mode, Ta=25°C

Note16: VSYS = 1.7 ~ 3.3V, AVDD = 4.5 ~ 5.5V, Frame=70Hz, No load, Self oscillator (fosc=500kHz), 262,144colors mode, No data Access, Ta=25°C

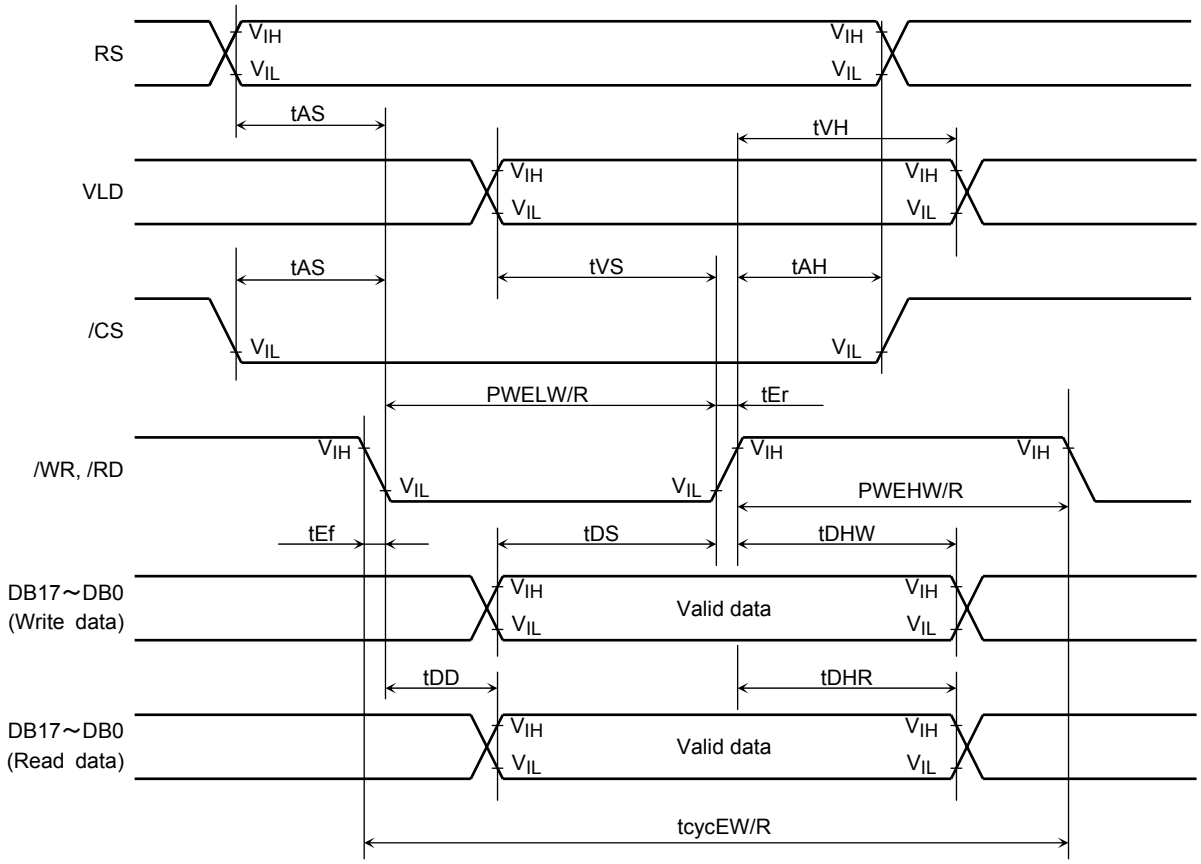
Note17: VSYS = 1.7 ~ 3.3V, AVDD = 4.5 ~ 5.5V, Frame=70Hz, No load, Self oscillator (fosc=500kHz), 262,144colors mode, Data Access (tcycE=10MHz by HWM="1" mode), Ta=25°C

Note18: VSYS = 1.7 ~ 3.3V, AVDD = 4.5 ~ 5.5V, No load, OSC halt condition, RAM data keep, Register data keep, Ta=25°C

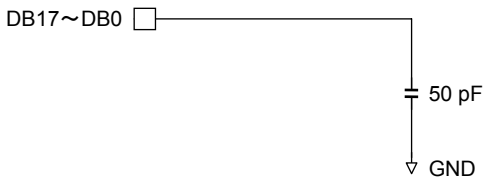
Note19: VSYS = 1.7 ~ 3.3V, AVDD = 4.5 ~ 5.5V, No load, OSC halt condition, Register data keep, Ta=25°C

Note20: VSYS = 1.7 ~ 3.3V, AVDD = 4.5 ~ 5.5V, No load, OSC halt condition, Ta=25°C

AC Characteristics (1): 80-Series Parallel MPU Interface



Note21: The following load is connected when measuring the data delay (tDD) and data hold time (tDHR):



Note: including tool and probe capacitance.

(Normal write mode, VSS = 0 V, VSYS = 1.7 to 2.4 V, VREF = 1.5 V, AVDD = 5.0 V, and Ta = –20 to 75°C)

Characteristics		Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
Enable cycle time	On write	tcycEW		250	—	—	ns
	On read	tcycER		800	—	—	ns
Enable pulse low width	On write	PWELW		25	—	—	ns
	On read	PWELR		350	—	—	ns
Enable pulse high width	On write	PWEHW		150	—	—	ns
	On read	PWEHR		400	—	—	ns
Enable rising/falling time		tEr, tEf		—	—	40	ns
Address setup time		tAS		-4	—	—	ns
Address hold time		tAH		15	—	—	ns
VLD setup time		tVS		18	—	—	ns
VLD hold time		tVH		10	—	—	ns
Write data setup time		tDS		18	—	—	ns
Write data hold time		tDHW		15	—	—	ns
Data delay		tDD (Note)		—	—	500	ns
Read data hold time		tDHR (Note)		5	—	—	ns

Note: t_{DD} and t_{DHR} added te lord circuit as the figure·

(High-speed write mode, VSS = 0 V, VSYS = 1.7 to 2.4 V, VREF = 1.5 V, AVDD = 5.0 V, and Ta = –20 to 75°C)

Characteristics		Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
Enable cycle time	On write	tcycEW		55	—	—	ns
	On read	tcycER		800	—	—	ns
Enable pulse low width	On write	PWELW		20	—	—	ns
	On read	PWELR		350	—	—	ns
Enable pulse high width	On write	PWEHW		20	—	—	ns
	On read	PWEHR		400	—	—	ns
Enable rising/falling time		tEr, tEf		—	—	40	ns
Address setup time		tAS		-4	—	—	ns
Address hold time		tAH		15	—	—	ns
VLD setup time		tVS		18	—	—	ns
VLD hold time		tVH		10	—	—	ns
Write data setup time		tDS		18	—	—	ns
Write data hold time		tDHW		15	—	—	ns
Data delay		tDD (Note)		—	—	500	ns
Read data hold time		tDHR (Note)		5	—	—	ns

Note: t_{DD} and t_{DHR} added te lord circuit as the figure·

(Normal write Mode, VSS = 0V, VSYS = 2.4～3.3V, VREF = 1.5V, AVDD = 5.0V, Ta = −20～75°C)

Characteristics		Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
Enable cycle time	On write	tcycEW		175	—	—	ns
	On read	tcycER		500	—	—	ns
Enable pulse low width	On write	PWELW		25	—	—	ns
	On read	PWELR		250	—	—	ns
Enable pulse high width	On write	PWEHW		150	—	—	ns
	On read	PWEHR		200	—	—	ns
Enable rising/falling time		tEr, tEf		—	—	40	ns
Address setup time		tAS		-4	—	—	ns
Address hold time		tAH		15	—	—	ns
VLD setup time		tVS		18	—	—	ns
VLD hold time		tVH		10	—	—	ns
Write data setup time		tDS		18	—	—	ns
Write data hold time		tDHW		15	—	—	ns
Data delay		tDD (注)		—	—	300	ns
Read data hold time		tDHR (注)		5	—	—	ns

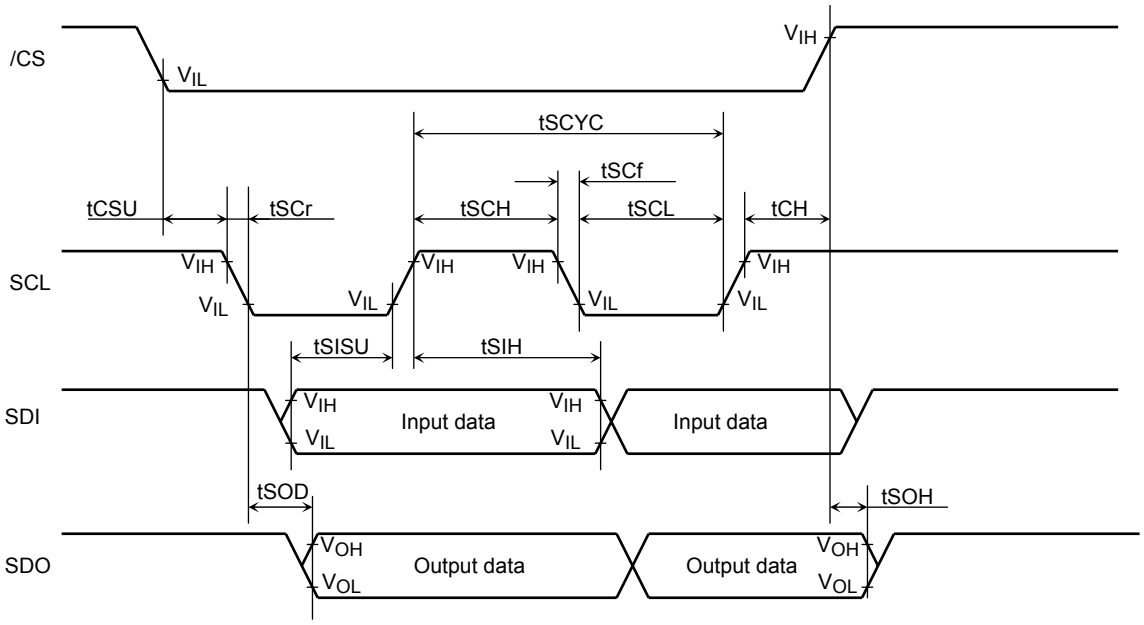
Note21: t_{DD} and t_{DHR} added te lord circuit as the figure·

(High speed write Mode, VSS = 0V, VSYS = 2.4～3.3V, VREF = 1.5V, AVDD = 5.0V, Ta = −20～75°C)

Characteristics		Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
Enable cycle time	On write	tcycEW		50	—	—	ns
	On read	tcycER		500	—	—	ns
Enable pulse low width	On write	PWELW		20	—	—	ns
	On read	PWELR		250	—	—	ns
Enable pulse high width	On write	PWEHW		20	—	—	ns
	On read	PWEHR		200	—	—	ns
Enable rising/falling time		tEr, tEf		—	—	40	ns
Address setup time		tAS		-4	—	—	ns
Address hold time		tAH		15	—	—	ns
VLD setup time		tVS		18	—	—	ns
VLD hold time		tVH		10	—	—	ns
Write data setup time		tDS		18	—	—	ns
Write data hold time		tDHW		15	—	—	ns
Data delay		tDD (注)		—	—	300	ns
Read data hold time		tDHR (注)		5	—	—	ns

Note21: t_{DD} and t_{DHR} added te lord circuit as the figure·

AC Characteristics (2): Serial Interface



(Note22) The following load is connected when measuring the data delay (tDD) and data hold time (tDHR):

Note: Including tppl and probe capacitance

(VSS = 0 V, VSYS = 1.7 to 2.4 V, VREF = 1.5 V, AVDD = 5.0 V, and Ta = –20 to 75°C)

Characteristics		Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
Serial clock cycle time	On write	tSCYC		0.1	—	20	μs
	On read	tSCYC		0.5	—	20	μs
Serial clock pulse low width	On write	tSCL		40	—	—	ns
	On read	tSCL		230	—	—	ns
Serial clock pulse high width	On write	tSCH		40	—	—	ns
	On read	tSCH		230	—	—	ns
Serial clock rising/falling time		tSCr/tSCf		—	—	20	ns
Chip select setup time		tCSU		20	—	—	ns
Chip select hold time		tCSH		60	—	—	ns
Serial input data setup time		tSISU		30	—	—	ns
Serial input data hold time		tSIH		30	—	—	ns
Serial output data delay		tSOD		—	—	200	ns
Serial output data hold time		tSOH		5	—	—	ns

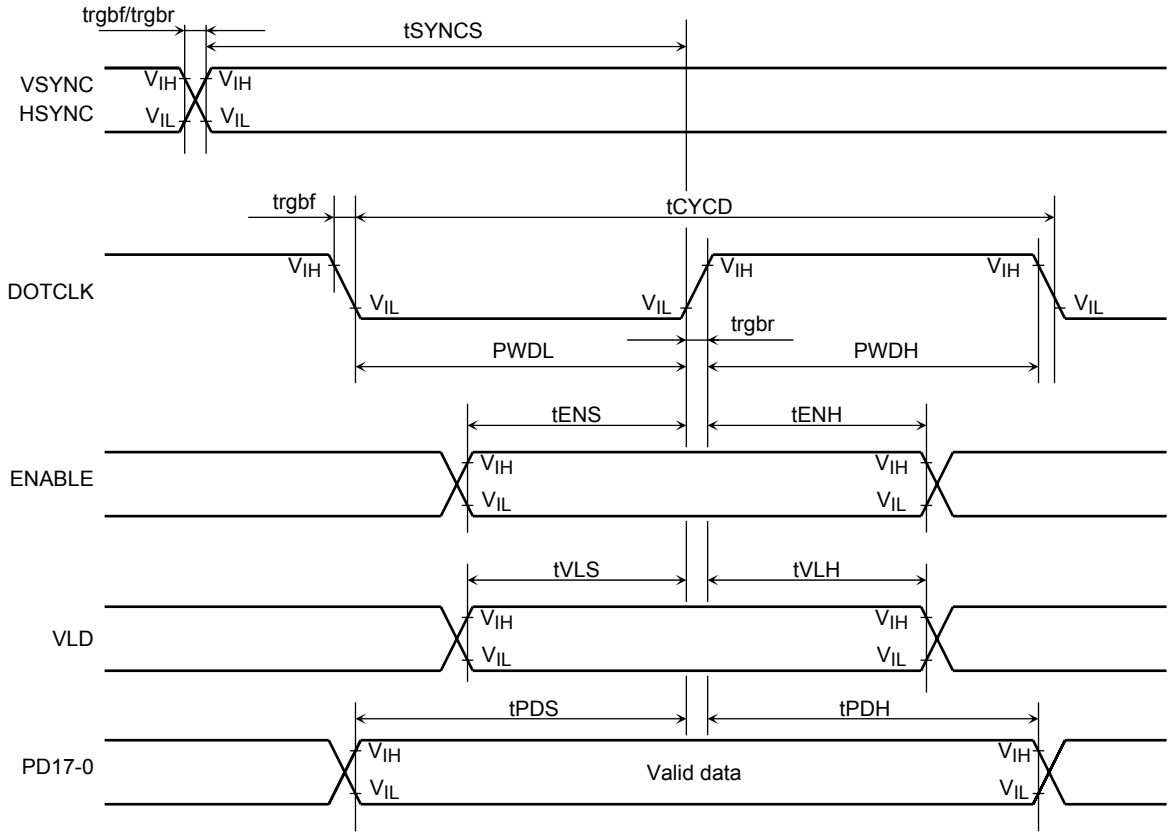
Note22: t_{SOD} and t_{SOH} t_{DD} and t_{DHR} added te lord circuit as the figure·

(V_{SS} = 0 V, V_{SYS} = 2.4 to 3.3 V, V_{REF} = 1.5 V, AV_{DD} = 5.0 V, and Ta = –20 to 75°C)

Characteristics		Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
Serial clock cycle time	On write	tSCYC		0.1	—	20	μs
	On read	tSCYC		0.35	—	20	μs
Serial clock pulse low width	On write	tSCL		40	—	—	ns
	On read	tSCL		150	—	—	ns
Serial clock pulse high width	On write	tSCH		40	—	—	ns
	On read	tSCH		150	—	—	ns
Serial clock rising/falling time		tSCr/tSCf		—	—	20	ns
Chip select setup time		tCSU		20	—	—	ns
Chip select hold time		tCSH		60	—	—	ns
Serial input data setup time		tSISU		30	—	—	ns
Serial input data hold time		tSIH		30	—	—	ns
Serial output data delay		tSOD		—	—	130	ns
Serial output data hold time		tSOH		5	—	—	ns

Note22: t_{SOD} and t_{SOH} t_{DD} and t_{DHR} added te lord circuit as the figure·

AC Characteristics (3): RGB Interface



a) 18bit/16bit RGB MODE

(V_{SS} = 0V, V_{SYS} = 1.7～2.4V, V_{REF} = 1.5V, AV_{DD} = 5.0V, Ta = −20～75°C)

Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
VSYNC/HSYNC setup time	tSYNCS		0	—	1	clock
DOTCLK low pulse width	PWDL		40	—	—	ns
DOTCLK high pulse width	PWDH		40	—	—	ns
DOTCLK cycle time	tCYCD		100	—	—	ns
ENABLE setup time	tENS		10	—	—	ns
ENABLE hold time	tENH		20	—	—	ns
VLD setup time	tVLS		10	—	—	ns
VLD hold time	tVLH		40	—	—	ns
Data setup time	tPDS		10	—	—	ns
Data hold time	tPDH		40	—	—	ns
DOTCLK, VSYNC, and HSYNC rising/falling time	trgbr/trgbf		—	—	25	ns

(V_{SS} = 0V, V_{SYS} = 2.4～3.3V, V_{REF} = 1.5V, AV_{DD} = 5.0V, Ta = −20～75°C)

Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
VSYNC/HSYNC setup time	tSYNCS		0	—	1	clock
DOTCLK low pulse width	PWDL		40	—	—	ns
DOTCLK high pulse width	PWDH		40	—	—	ns
DOTCLK cycle time	tCYCD		100	—	—	ns
ENABLE setup time	tENS		10	—	—	ns
ENABLE hold time	tENH		20	—	—	ns
VLD setup time	tVLS		10	—	—	ns
VLD hold time	tVLH		40	—	—	ns
Data setup time	tPDS		10	—	—	ns
Data hold time	tPDH		40	—	—	ns
DOTCLK, VSYNC, and HSYNC rising/falling time	trgbr/trgbf		—	—	25	ns

b) 6bit RGB MODE

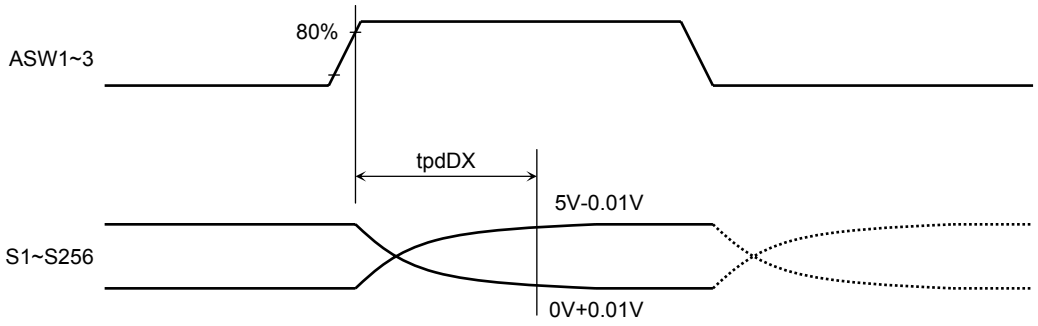
(V_{SS} = 0V, V_{SYS} = 1.7～2.4V, V_{REF} = 1.5V, AV_{DD} = 5.0V, Ta = −20～75°C)

Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
VSYNC/HSYNC setup time	tSYNCS		0	—	1	clock
DOTCLK low pulse width	PWDL		25	—	—	ns
DOTCLK high pulse width	PWDH		25	—	—	ns
DOTCLK cycle time	tCYCD		55	—	—	ns
ENABLE setup time	tENS		10	—	—	ns
ENABLE hold time	tENH		23	—	—	ns
VLD setup time	tVLS		10	—	—	ns
VLD hold time	tVLH		23	—	—	ns
Data setup time	tPDS		10	—	—	ns
Data hold time	tPDH		23	—	—	ns
DOTCLK, VSYNC, and HSYNC rising/falling time	trgbr/trgbf		—	—	25	ns

(V_{SS} = 0V, V_{SYS} = 2.4～3.3V, V_{REF} = 1.5V, AV_{DD} = 5.0V, Ta = −20～75°C)

Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
VSYNC/HSYNC setup time	tSYNCS		0	—	1	clock
DOTCLK low pulse width	PWDL		25	—	—	ns
DOTCLK high pulse width	PWDH		25	—	—	ns
DOTCLK cycle time	tCYCD		55	—	—	ns
ENABLE setup time	tENS		10	—	—	ns
ENABLE hold time	tENH		23	—	—	ns
VLD setup time	tVLS		10	—	—	ns
VLD hold time	tVLH		23	—	—	ns
Data setup time	tPDS		10	—	—	ns
Data hold time	tPDH		23	—	—	ns
DOTCLK, VSYNC, and HSYNC rising/falling time	trgbr/trgbf		—	—	25	ns

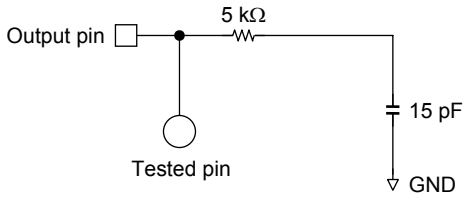
AC Characteristics (4): LCD Output Delay



(V_{SS} = 0 V, V_{SYS} = 1.7 to 3.3 V, V_{REF} = 1.5 V, AV_{DD} = 4.5 to 5.0 V, and Ta = –20 to 75°C)

Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
Output delay	tpdDX	(Note 23, 24, 27)	0	3	5	μs

Note 23: Applied when the following load model is connected



Note 2: Including probe and fixture capacitance

Note 24: High level is 5 - 0.01V point, amplitude is 5.0V and low level is 0 + 0.01V point.

Note 27: AMPBR=100kΩ

AC Characteristics (5)

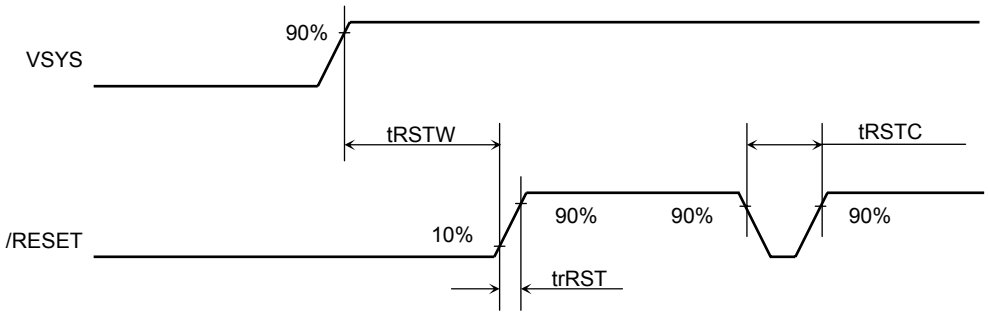
(V_{SS} = 0 V, V_{SYS} = 1.7 to 3.3 V, V_{REF} = 1.5 V, AV_{DD} = 4.5 to 5.0 V, and Ta = –20 to 75°C)

Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
Operating frequency	CLKIN		0.01		1	MHz
External clock frequency	Fex		0.01		1	MHz
External clock duty cycle	Fduty		45	50	55	%
External clock rising/falling time	tr/tf				10	ns
Oscillation frequency	OSC	(Note 25, 26)	500	550	600	kHz

Note25: Rf = 100kΩ

Note26: Oscillator frequency of internal oscillator is changed by external register (Rf)

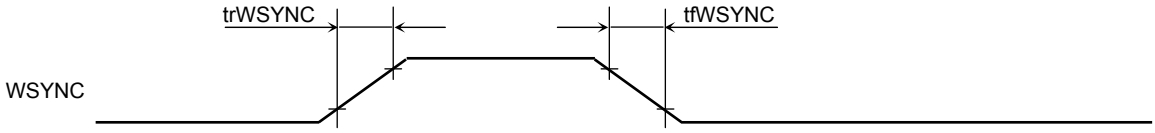
AC Characteristics (6)



(V_{SS} = 0 V, V_{SYS} = 1.7 to 3.3 V, V_{REF} = 1.5 V, AV_{DD} = 4.5 to 5.0 V, and Ta = –20 to 75°C)

Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
Reset signal effective delay	tRSTW		30			μs
Reset signal rising time	trRST				40	μs
Noise cancel pulse	tRSTC				300	ns

AC Characteristics (7)

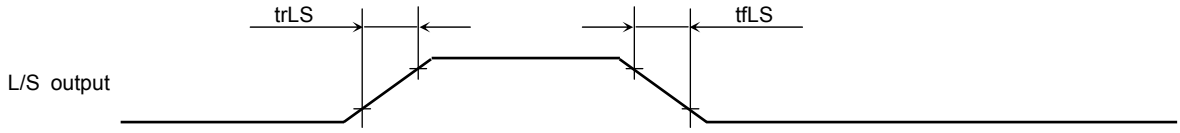


(V_{SS} = 0V、V_{SYS} = 1.7～3.3V、V_{REF} = 1.5V、AV_{DD} = 4.5～5.0V、Ta = −20～75°C)

Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
WSYNC output signal tr/tf	trWSYNC/ tfWSYNC	(Note29)		100	200	ns

Note29: WSYNC signal output voltage: VSYS-VSS

AC Characteristics (8)



(V_{SS} = 0V、V_{SYS} = 1.7～3.3V、V_{REF} = 1.5V、XV_{DD} = 4.5～5.0V、Ta = −20～75°C)

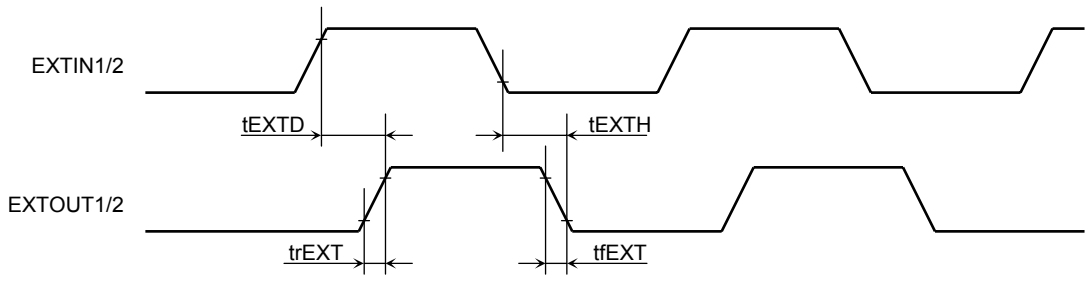
Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
Level shifter output signal tr/tf	trLS tfLS	(Note30,31,32)		70	200	ns

Note30: DCG, DCEB, PEV, FDON, U/D, FR, CKV1/2, STV, ASW1/2/3

Note31: Level shifter output signal voltage: XVDD-VSS

Note32: In case of load capacitor: C=150pF

AC Characteristics (9)

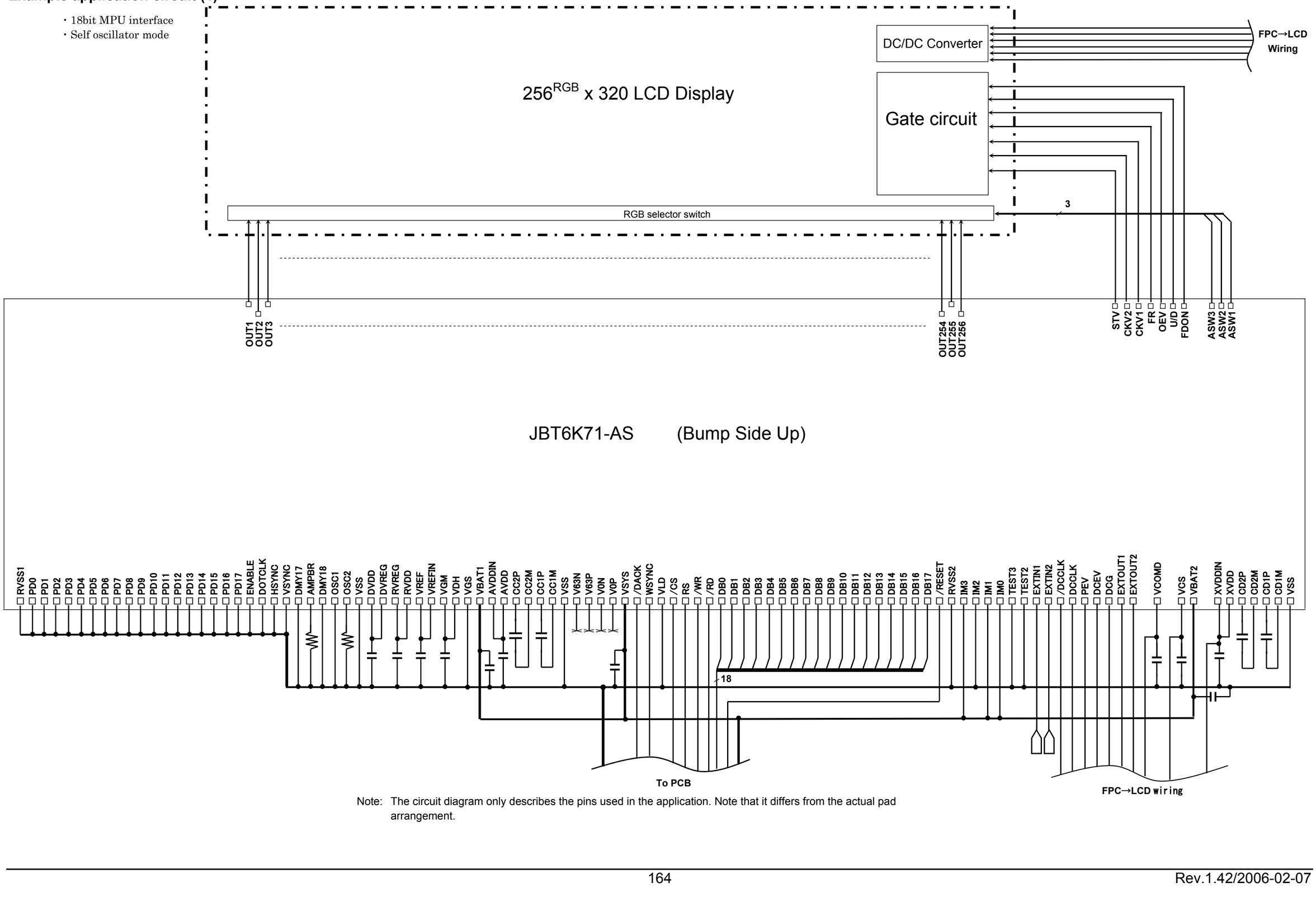


(V_{SS} = 0V, V_{SYS} = 1.7～3.3V, V_{REF} = 1.5V, AV_{DD} = 4.5～5.0V, Ta = −20～75°C)

Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
EXTOUT1/2 output delay time	tEXTD			70	200	ns
EXTOUT1/2output hold time	tEXTH			70	200	ns
EXTOUT1/2 rising/falling time	trEXT / tfEXT			60	200	ns

Example application circuit (1)

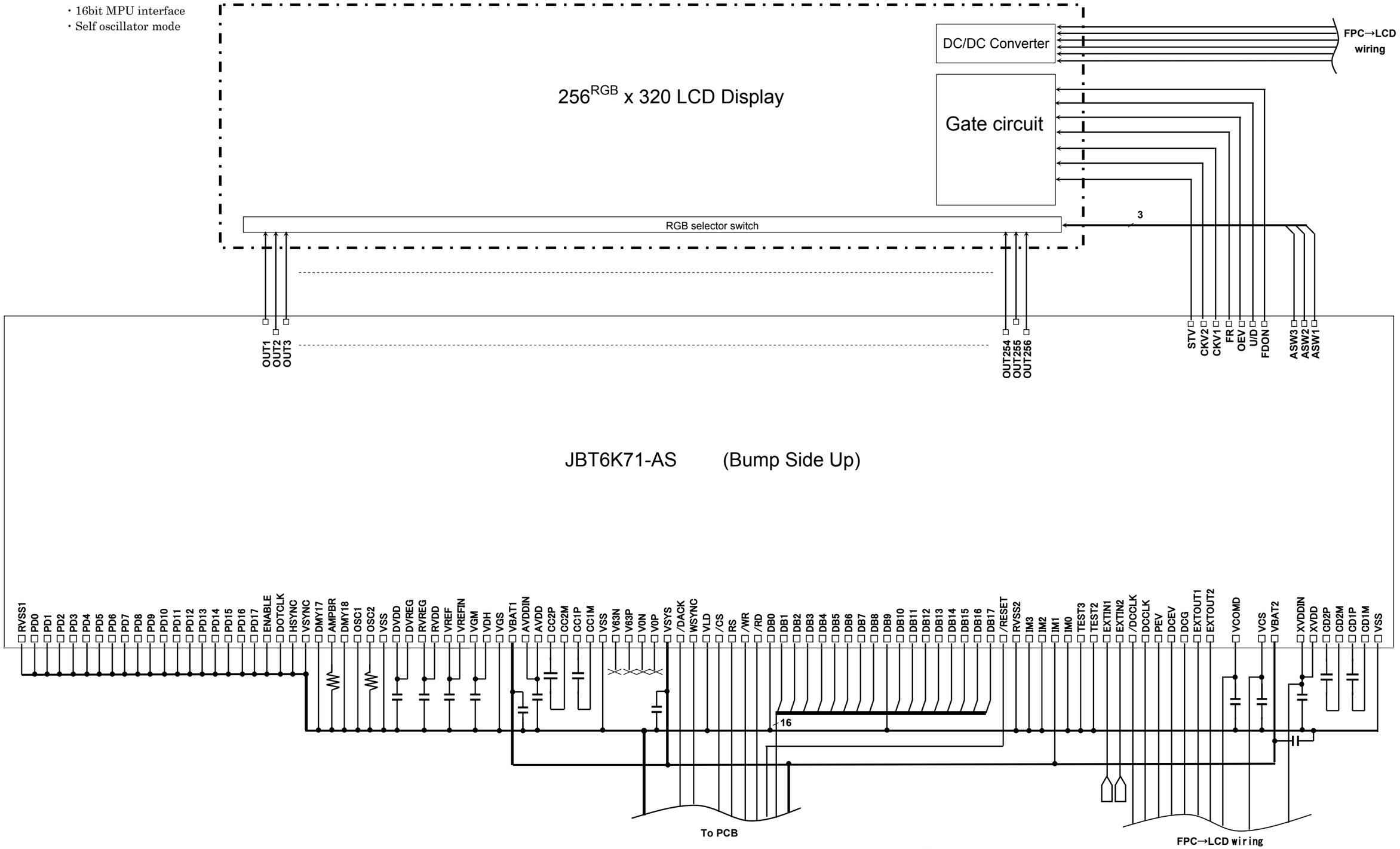
- 18bit MPU interface
- Self oscillator mode



Note: The circuit diagram only describes the pins used in the application. Note that it differs from the actual pad arrangement.

Example application circuit (2)

・16bit MPU interface
・Self oscillator mode



Note: The circuit diagram only describes the pins used in the application. Note that it differs from the actual pad arrangement.

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