TENTATIVE/CONFIDENTIAL

TECHNICAL LITERATURE

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DOC. NO. **LCY-2506804**

DATE **AUG.31.2006**

SHARP CORPORATION

PRESENTED

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SHARP CORPORATION

^{**} The technical literature is subject to be changed without notice

	RECORDS OF REVISION				DOC.FIRST ISSUE Aug.31.2006
DATE	REF.PAGE PARAGRAPH DRAWING No.	SPEC No.	REVISED NO.	SUN	MMARY



 $\begin{array}{c} \text{MODEL} \quad N_0. \\ LS022Q8UX05 \end{array}$

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[For handling and system design]

- (1) Do not scratch the surface of the polarizer film as it is easily damaged.
- (2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.
- (3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.
- (4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.
- (5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts(color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.
- (6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.
- (7) Do not expose LCD module to the direct sunlight, or to strong ultraviolet light for long time.
- (8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.
- (9) Do not disassemble the LCD module as it may cause permanent damage.

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(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below. Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body. Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

Floor

Floor is an important part to leak static electricity which is generated from human body or equipment.

There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure(electrostatic earth: 1×10^8) should be made.

Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

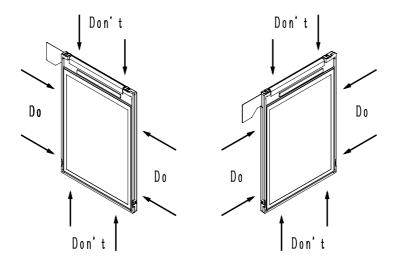
Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

Others

Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

- (11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.
- (12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.
- (13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers are also prohibited.
- (14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel ,COG and other electric parts are not damaged.



- (15) Do not touch the COG 's patterning area. Otherwise the circuit may be damaged.
- (16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.
- (17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.
- (18) LCD panel is susceptible to mechanical stress and even the slightest tress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

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- (19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.
- (20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.
- (21) This LCD module does not contain nor use any ODS(1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

[For operating LCD module]

- (1) Do not operate or store the LCD module under outside of specified environmental conditions.
- (2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.
- (3) As opto-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

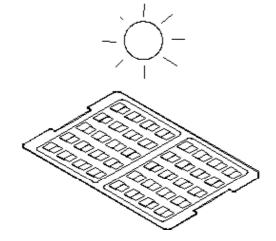
[Precautions for Storage]

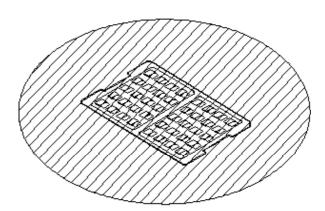
- (1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.
- (2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity $(25 \pm 5^{\circ}\text{C},60 \pm 10^{\circ}\text{RH})$ in order to avoid exposing the front polarizer to chronic humidity.
- (3) Keeping Method
 - a. Don't keeping under the direct sunlight.

b. Keeping in the tray under the dark place.

DON'T

DO





- (1) Do not operate or store the LCD module under outside of specified environmental conditions.
- (2) Be sure to prevent light striking the chip surface.



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[Other Notice]

- (1) Do not operate or store the LCD module under outside of specified environmental conditions.
- (2) As electrical impedance of power supply lines (VDD-VSS) are low when LCD module is working, place the de-coupling capacitor near by LCD module as close as possible.
- (3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.
- (4) Generally, At power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.
- (5) Don't touch to PWB surface, exposed IC chip, electric parts and other parts, to any electric, metalic materials.
- (6) No bromide specific fire-retardant material is used in this module.
- (7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.

[Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.

-Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenetic (Aims test: negative) material

material is employed.

FPC: Dispose of as similar way to circuit board from electric device.



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1. Application

This data sheet is to introduce the specification of LS022Q8UX05 active matrix 16,777,216 color LCD module. Color LCD module is controlled by Driver IC (R69406).

If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.

As to basic specification of driver IC refer to the IC specification and handbook.

2. Construction and Outline

Construction: LCD panel, Driver(COG), FPC with electric components,

(4) White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.

Outline: See page 19.

Connection: 27 pins; 0.3mm pitch

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

Rejection criteria shall be noted in Inspection Standard (S-U-056-xx)

In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory. So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

3. Mechanical Specification

Table 1

Parameter		Specifications	Unit
Outline dimensions (typ)		$(39.20) (W) \times (56.35) (H) \times (2.3) (D)$	mm
Main LCD	Active area	33.48 (W) × 44.64 (H)	mm
Panel	Display format	Display format $240 \times RGB(W) \times 320(H)$	
	Dot pitch	0.0465 (W) × 0.1395 (H)	mm
	Base color *1	Normally black	-
Mass		Approx (T.B.D)	g

^{*1} Due to the characteristics of the LC material, the colors vary with environmental temperature.

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4. Absolute Maximum Ratings

(4-1) Electrical absolute maximum ratings

Table 2

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Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage	VDD-GND	-0.3	4.2	V	
	VDDI-GND	-0.3	4.2	V	
Input Voltage	$V_{\rm IN}$	-0.3	V _{DDI} +0.5	٧	*1

^{*1} Input terminal of logic system. : Voltage value is based on GND = 0V.

Environment Conditions

Table 3

Item	Тор		Tstg		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperature	-10 °C	+60°C	-20 °C	+70°C	Note 2)
Humidity	Note 1)		Note 1)		No condensation

Note1) Ta ≤ 40 °C......95 % RH Max

Note2) Ta > 40 °C......Absolute humidity shall be less than Ta=40 °C /95 % RH.

As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable. Be sure not to exceed the rated voltage, otherwise a malfunction may occur.

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5. Electrical Specifications

(5-1) Electrical characteristics for main LCD

<u>Table 4</u>			Ta=2:	5, VDD	=2.8V, VDI	DI=1.8V	GND=0V
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit	Applicable Pin
Supply voltage	VDD- VSS	Ta=-10 ~ 60 °C	(2.7)	(2.8)	(2.9)	V	
Supply voltage	VDDI- VSS	Ta=-10 ~ 60 °C	(1.7)	(1.8)	(1.9)	V	
"H" level input voltage	$V_{\rm IH1}$	Ta=-10 ~ 60 °C	$0.7~\mathrm{V_{DD1}}$	-	-	V	(note1)
"L" level input voltage	$V_{\rm IL1}$	1a-10 % 60 °C	-	-	0.3 V _{DD1}	V	(note1)
Input leakage current	I_{LI1}	Ta=-10 ~ 60 °C	-10	-	10	μA	(note1)
Output leakage current	I_{LO}	V_{IN} = GND or VDDI	-10	-	10	μA	(note2)
"H" level output voltage	V_{OH1}	Ta=-10 ~ 60 °C	$0.8~\mathrm{V_{DD1}}$	-	-	V	(
"L" level output voltage	V_{OL1}	I_{OH1} =TBD mA I_{OL1} =TBD mA	-	-	$0.2~\mathrm{V_{DD1}}$	V	(note3)
C	I_{DD}	Ta=25 °C	1	(5.0)	(T.B.D.)	mA	(note4)
Current consumption	I_{DDI}	1a-25 °C	-	(0.2)	(T.B.D.)	mA	(note4)

- (note 1) Input mode of D0 ~ D7pins, CSX,WRX,RDX,D/CX,RESX
- (note 2) Output mode of D0 ~ D7pins, TE.
- (note 3) Output mode of $D0 \sim D7$ pins, TE.

(note4) Following Conditions

Ta=25 , frame frequency=60Hz

Display Pattern: All white. No Host CPU access.

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(5-2) LED back light

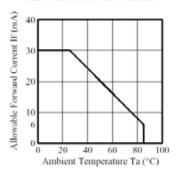
(1) At main panel the back light use 4pcs edge light type white LED.

Table 6

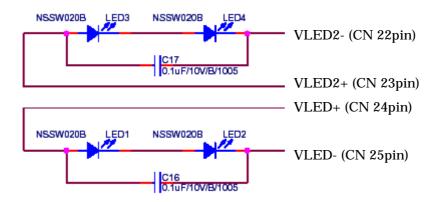
Parameter	Conditions	Symbol	Min.	Тур.	Max.	Unit	Remark
Forward current	Ta=25 °C	I_{LED1}	-	(20) *1	-	mA	VLED+~VLED-
		I_{LED2}	-	(20) *1	-	mA	VLED2+~VLED2-

LED lamp: NICHIA Corporation NSSW020BT

Luminous Intensity rank: V1 or V2 Color rank: b5(be1,be2,bf1,bf2) Ambient Temperature vs.
 Allowable Forward Current



LED circuit



^{*1} per one piece of LED

^{*}Please consider Allowable Forward Current on used temperature (refer to Ambient Temperature vs. Allowable Forward Current curve)

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(5-3) Interface signals

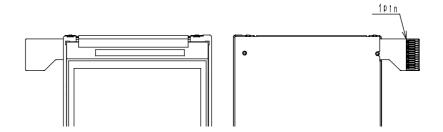
Table 7

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		<u> 14616 7</u>		
Pin No	Symbol	Description	I/O	Remarks
1	GND	Ground Level Pin		
2	VDDI	Power Supply (LCD Driver) for I/O		
3	VDD	Power Supply (LCD Driver) for Analog		
4	GND	Ground Level Pin		
5	TE	Tearing Effect Output	О	
6	RDX	Read enable	I	Low enable
7	WRX	Write enable	I	Low enable
8	D/CX	Data / Command selectable	I	Low :command High:display data / parameter
9	CSX	Chip Select	I	Low enable
10	GND	Ground Level Pin		
11	D0	Data Bus	I/O	
12	D1	Data Bus	I/O	
13	D2	Data Bus	I/O	
14	D3	Data Bus	I/O	
15	D4	Data Bus	I/O	
16	D5	Data Bus	I/O	
17	D6	Data Bus	I/O	
18	D7	Data Bus	I/O	
19	GND	Ground Level Pin		
20	RESX	Reset rnable	I	Low enable
21	GND	Ground Level Pin		
22	VLED2-	LED1~2 Cathode		
23	VLED2+	LED1~2 Anode		
24	VLED+	LED3~4 Anode		
25	LED-	LED3~4 Cathode	-	
26	GND	Ground Level Pin		
27	GND	Ground Level Pin		

Corresponded connector: 0.3mm pitch, ZIF Connector (HRS FH23-27S-0.3SHW)

Signals connecting to LCD module. Symbol correspondable to Circuit diagram



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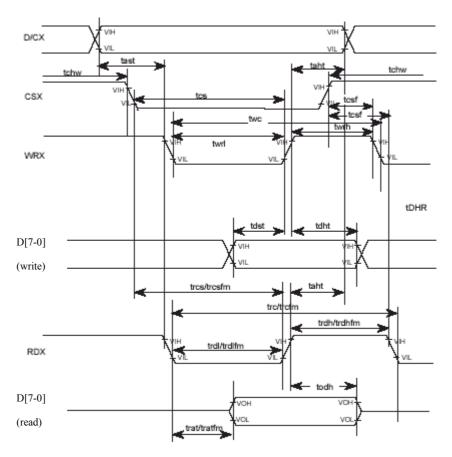
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(5-4) Host Interface Timing Diagrams (80-family MPU access) for R69406



Notes: 1. The logic High and Low levels are defined by 70 and 30 percent of the IOVcc level, respectively

2. Fix unused pins of D(15:0) to either IOVcc or IOGND.

 $V_{Ci} = 2.600 \text{ V} \sim 2.950 \text{ V}$, $IOVec = 1.650 \text{ V} \sim 1.950 \text{ V}$, $Ta = -30^{\circ}\text{C} \sim +75^{\circ}\text{C}$)

Item	Sym	nbol	unit	Timing diagram	Min.	Max.
Address setup time	D/CX	tast	ns		10	-
Address hold time (Write/Read)	D/CX	taht	ns		10	-
CSX"H" pulse width		tchw	ns		0	-
Chip select setup time (Write)		tes	ns		35	-
Chip select setup time (Read ID)	CSX	trcs	ns		45	-
Chip select setup time (Read FM)		trosfm	ns		355	-
Chip select setup time (Write/Read)		tesf	ns		10	-
Write cycle time		two	ns		100	-
Control pulse "High" period	WRX	twrh	ns		35	-
Control pulse "Low" period		twrl	ns		35	-
Read cycle time (ID)		trc	ns	ID data read	160	-
Control pulse "High" period (ID)	RDX(ID)	trdh	ns	7	90	-
Control pulse "Low" period (ID)		trdl	ns	7	45	-
Read cycle time (FM)		trcfm	ns	Read from frame	450	-
Control pulse "High" period (FM)	RDX(FM)	trdhfm	ns	memory	90	-
Control pulse "Low" period (FM)		trdifm	ns		355	-
Data setup time		tdst	ns	CL	10	-
Data hold time		tdht	ns	Max. 30 pF Min. 8 pF	10	-
Read access time (ID)	D[150]	trat	ns		-	40
Read access time (FM)		tratfm	ns	7	-	340
Output disable time		todh	ns		20	80

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(5-6) Schematic of LCD module system

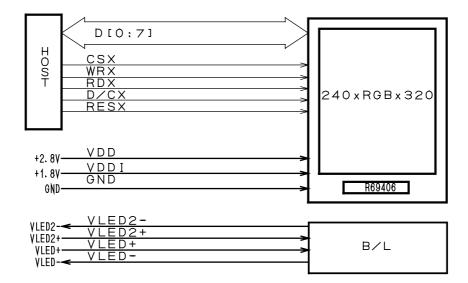


fig. 1 Schematic of LCD module system

(5-7) Schematics of LCD

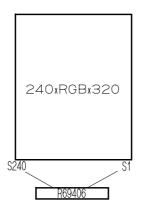


Fig.2 Schematic of Main-LCD

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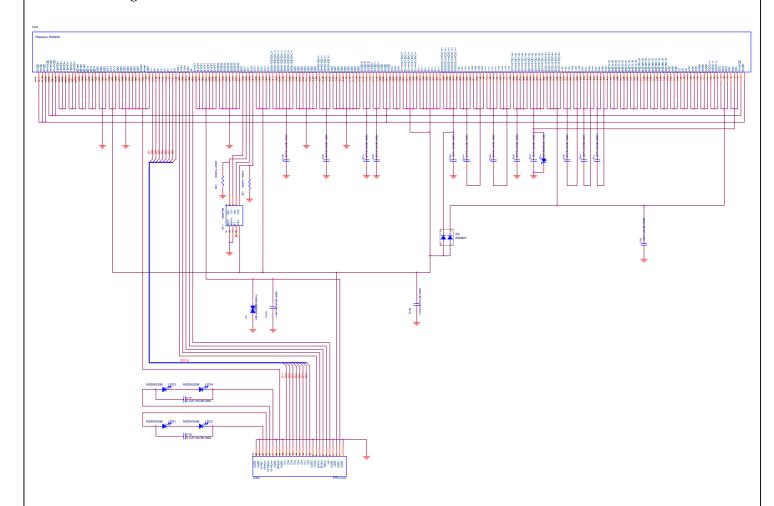
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(5-8) Circuit diagram



(5-9) Parts Layout

(T.B.D.)

(5-10) Parts List

(T.B.D.)

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6. Optical Characteristics

VDD=2.8[V],VDDI=1.8[V],Ta=25[]

Table 10

					1010 10				
	Param	neter	svmbo	Condition	MIN	TYP	MAX	Unit	Remark
	Brightne	SS	В	θ=0°	T.B.D	(300)	-	cd/m²	Note1,2,5
	Contrast		Cot	θ=0°	T.B.D	(350)	-		Note1,3
	Flicker ra	atio	F	*1	-	-	(7.0)	%	
	NTSC rat	tio	Nrt	θ=0°	-	(80)	-	%	(u',v')
	Viewing A	Angle	Θ11	Co > 5	T.B.D	(80)	-	Deg	Note1
Trar			Θ12		T.B.D	(80)	-		
msr			Θ21		T.B.D	(80)	-		
issi			Θ22		T.B.D	(80)	-		
Transmissive mode	White ch	romaticity	u′	θ=0°	-	(0.196)	-		Note1
ode			v′		-	(0.467)	-		
	Red chro	maticity	u		-	(0.433)	-		
			v′		-	(0.518)	-		
	Green ch	romaticity	u		-	(0.127)	-		
			v′		-	(0.562)	-		
	Blue chro	omaticity	u		-	(0.157)	-		
			v′		-	(0.170)	-		
Re	Reflectar	nce	R	θ=0°	T.B.D	(4)	-	%	Note6
flect	Contrast		Cor	θ=0°	T.B.D	(45)	-		Note3,6
ive	NTSC rat	tio	Nrr	θ=0°	-	0	-	%	
Reflective mode	White ch	romaticity	u	θ=0°	-	(0.194)	-		Note.1
'n			v′		-	(0.490)	-		
	esponse	Rise	r	θ=0°	-	(25)	T.B.D	ms	Note1,4
	Time	Decay	d		-	(15)	T.B.D	ms	

*1: Measuring condition

- Measuring systems: YOKOGAWA 3298_01 + 3298_11
- Temperature = 25 (± 3), Frame Frequency = 60Hz (-0/+5Hz), LED back-light: ON, Environment brightness < 150 lx
- Measuring pattern : Horizontal stripe pattern < black (V0) / gray(V32) / black (V0) / gray (V32)...>
- Measured sample : New sample before a long term aging.
- Flicker ratio is very sensitive to measuring condition.

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Note 1) Definition of range of visual angle

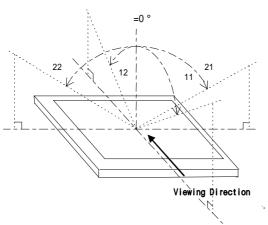


Fig .3 Definition of viewing angle

Note 2) Brightness is measured as shown in Fig.8, and is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

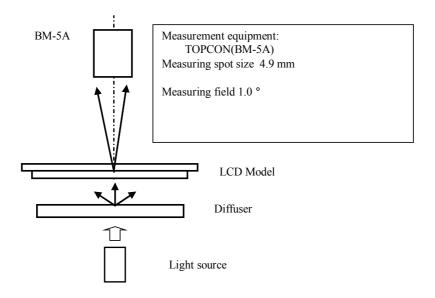


Fig4. Optical characteristics Test Method (Brightness)

Note 3) Contrast ratio is defined as follows:

Co= Luminance(brightness) all pixcels "White"
Luminance(brightness) all pixcels "Black"

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Note 4) Response time is defined as follows:

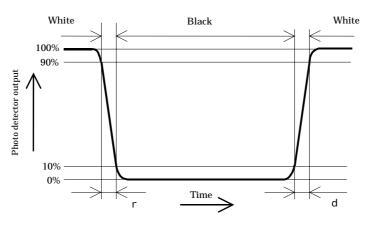


Fig.5 Response time

Note 5) $I_{LED1} = 20[mA]$, $I_{LED2} = 20[mA]$

Note 6) Reflectance is defined as follows:

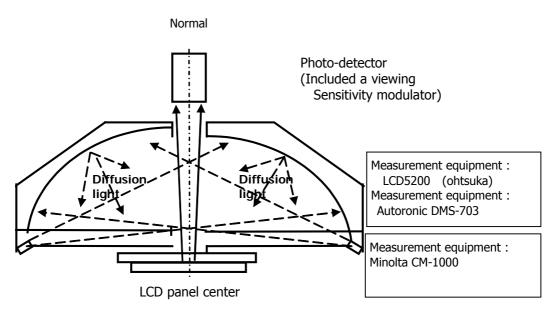


Fig. 8 Optical Characteristics Test Method

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7. Reliability			
(T.B.D.)			
8. Packaging specifications			
(T.B.D.)			



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- 9. Initial Sequence
- 9-1. Power On/Off Sequence

PowerOn

	oweron			•		
No.	Instruction	Setting Value	ADS (RS)	Register	Parameter	Remarks
1	Power ON (VDD 2.8[V], VDDI 1.8[V])					
2	Power will be stable					
3	Hardware Reset	RESX="H"->"L"				
	wait 1ms					
		RESX="L"->"H"				
	wait 5ms					
3	Software Reset					
		Software Reset	L	01		
	wait 5ms					
4	Sleep Out					
		Sleep Out	L	11		
	wait 120ms					
5	TE On				•	
		TE On	L	35		
			Н	00		
6	Display data write to VRAM					
		Display memory write	<u> </u>	2C		
<u> </u>			1	VRAN	1 write	
7	Display On	<u> </u>			••••••	
		Display On	L	29		

PowerOff

No.	Instruction	Setting Value	ADS (RS)	Register	Parameter	Remarks
1	Display Off					
		Display Off	L	28		
		Sleep IN	L	10		
	wait 120ms					
2	Hardware Reset	RESX="H"->"L"				
	wait 5ms					
3	Power Off (VDD 2.8[V],VDDI 1.8[V])					



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9-2. Partial On/Off Sequence

Example for Low Power Partial Mode On

No.	ltem	Setting Value	ADS (RS)	Register	Parameter	Remarks
1	Partial mode ON					
		Partial mode ON	L	12		
		Partial Area setting	L	30		
		Area Start line	Н		(00)	*example for 48 line partial
			Н		(91)	
		Area End line	Н		(00)	
			Н		(BF)	
2	Idle mode ON					
		ldle mode ON	L	39		for 8 color mode
3	Display data write to VRAM					
		Display memory write	L	2C		
				VRAN	l write	

Example for Low Power Partial Mode Off

No.	ltem	Setting Value	ADS (RS)	Register	Parameter	Remarks
1	Idle mode Off					
		ldle mode Off	L	38		for normal color mode
2	Partial mode Off					
		Partial mode Off	L	13		

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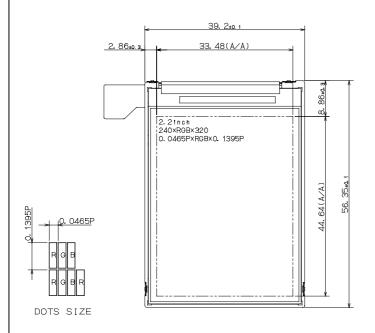
10. Serial Number Label identification

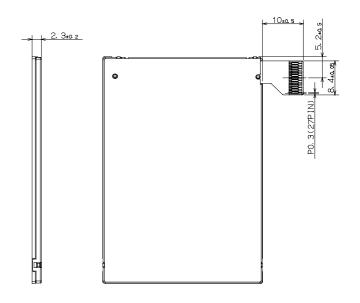
(T.B.D)

11. LCD Module Code Rule.

(T.B.D)

12. Module Outline





			ISSUE	
	SHA	DD	File No.	
	SHA		Page	11 pages
	Mobile Liquid Crystal Di	splav Group		
	SHARP CORPOR			
	Incoming Inspection	Standards		
		for CC SiliconTT	T-10D	\
Inco		tor CG-SiliconTF	T-LCD	1
	ming Inspection Standards	TOT CC CITICOTTT		
	ming inspection Standards	TOT GG GIIIGGITT		
	S022Q8			
L				
Customer's Receipt		BUXO		
L		BUXO		
Customer's Receipt		PRESENTED BY	5	
Customer's Receipt Date		PRESENTED BY	Crystal Dis	play Group II

				First issue		
	RECOR	DS OF REVI	SION	First File No.		
				Model	LS022	Q8UX05
DATE	REVISED		SUMMARY			Check & APPROVAL

INCOMING INSPECTION STANDARDS FOR CG-silicon TFT-LCD MODULES

1. Scope

These incoming inspection	standards shall apply to CG-silicon TFT-LCD modules
(hereinafter called "MODULE")	supplied by Sharp Corporation (hereinafter called the "Seller")
to	(hereinafter called the "Buyer").

2. Incoming inspection

The Buyer shall have the right to conduct at its own cost and expense, an incoming inspection of the Module's at the destination specified in the relevant bills of lading in accordance with the Module's specifications separately agreed upon and the inspection standard set forth in this Article.

The Buyer shall notify the Seller writing of a result of such inspection judgment (acceptance or rejection) in accordance with the said inspection standard within 40 days after the date of the bills of lading.

Should the Buyer fail to so notify the seller within the said 40 days period, the Buyer's right to reject the Module's shall then lapse, and the said Module's shall be deemed to have been accepted by the Buyer.

3. Method of incoming inspection

Unless otherwise agreed in writing, the method of incoming inspection shall be in Accordance with a sampling inspection based on ISO 2859-1.

a) Lot size : Quantity per shipment lot per modelb) Sampling type : Normal inspection, Single sampling

c) Inspection level: II

d) Sampling table : Table in ISO 2859-1

4. Acceptable quality level ("AQL")

The AQL for major and minor defects shall be respectively set forth below.

a) Major defects: AQL 0.4

b) Minor defects: AQL 1.0 Based on overall evaluation

5. Classification of defects

Defects are classified as major defect and a minor defect according to the degree of defect defined herein.

a) Major defect

A major defect is a defect that is likely to result in failure, or to reduce materially the usability of the product for its intended purpose.

Function defect

Abnormal operation including distinct R,G,B line defects and /or white line defect.

b) Minor defect

A minor defect either is a defect that is not likely to reduce materially the usability of the product for its intended purpose, or is a departure from an established having little bearing on the effective use or operation of the product.

Dot Defect
 Display non-uniformity
 Afterimage
 Scratches
 Dents
 Contrast ratio

4. Extraneous substances 8. Current dissipation

6. Determination of acceptability and subsequent disposal

If the number of defects found in the sample Module's from the lot is equal to or less Than the applicable acceptance level, the lot shall be accepted.

If the number of defects is greater than the applicable acceptance level, the lot shall be rejected. The Buyer shall inform the Seller of a detailed result of such inspection within the time period stipulated in Article 2.

The disposal is as follows:

a) Accepted lot

An acceptance under the above incoming inspection shall constitute an acceptance by the Buyer of such lot of the Module's in terms of the landed quality thereof.

b) Rejected lot

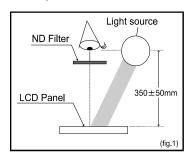
If a lot of PRODUCTS is rejected under the above incoming inspection due to any defects for which the Seller is responsible and such a fact is clearly confirmed by the Seller, the Seller shall exercise one of the following three options. This must be determined with mutual consent and shall be confirmed by the Seller. The best choice of the options shall be left to the Seller's discretion and the Seller shall advise the Buyer of its choice not later than two weeks of receipt of the Buyer's advice:

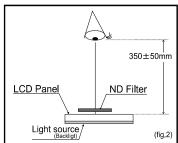
- 1. The Buyer shall return the defective lot to the place to be designated by the Seller and the Seller shall screen all of the PRODUCTS in the lot and repair defective PRODUCTS.
- 2. The Seller shall screen all of the PRODUCTS in the lot and repair defective products within a reasonable time period at the Buyer's facility.
- 3. The Buyer shall screen the entire lot for the good modules at the expense of the Seller to be separately agreed upon. The rejected PRODUCTS shall be returned to the place to be designated by the Seller

7. Inspection conditions

lto m	Inspection co	onditions
Item	Reflection inspection	Back light inspection
Panel surface	2500 ± 500 lx	Back light *
illumination	(uniform lighting on the panel surface)	
Light source	Florescent tube	LED (Back light)
Ambient illumination	300 ~ 700 lx	←
Ambient temperature	20 ~ 25 °C	←
Ambient Humidity	65 ± 5%RH	←
Viewing distance	350 mm ± 50 mm	←
Direction of lighting	Set light tube without	
Direction of lighting	reflection on the panel surface	
Viewing angle	The surface of the Module and the eyes of the inspector shall be 90 ± 5 degrees.	←
How to use ND filter	Use ND filter close to eyes (fig.1)	Use ND filter open to eyes (fig.2)
Check pattern (Bright dot)	Black picture position	<u></u>
Check pattern (Black dot)	RGB picture position	←

^{*} Please refer to the panel surface brightness of the specifications



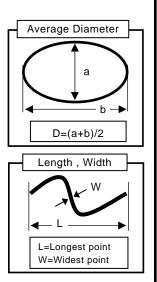


8. External inspection

8-1 Extraneous Substances, Polarizer bubble, Scratch

 $Width: W(mm) \;, \, Length: L(mm) \;, \, Average \; diameter: D(mm)$

Item	Inspection criteria	Allowable	note
	D<=0.15	ignore	
Black or white spots	0.15 <d<=0.25< td=""><td>2</td><td>A,B</td></d<=0.25<>	2	A,B
Black of write spots	D>0.25	0	А,Б
	Defect distance : 5r	nm or more	
	L<=0.15	ignore	
Lints*1	0.15 <l<=2.0< td=""><td>2</td><td>Α</td></l<=2.0<>	2	Α
LINIS	L>2.0	0	A
	Defect distance : 5r	nm or more	
	L<=2.0	ignore	
Scratch	2.0< L< =3 and W<=0.1	1	A,B
	L>3.0	0	



Item	Inspection criteria	Allowable	note
Polarizer	D<=0.15	ignore	
DentPolarizer Bubble	0.15 <d<=0.3< td=""><td>3</td><td>Α</td></d<=0.3<>	3	Α
	<0.3	0	

^{*1} Extraneous substances

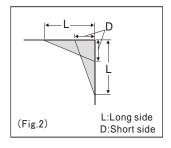
Note:inspection condition; judgement in each screen

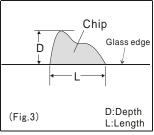
Item	condition A condition B	
Panel surface illumination	2500±500lx (external lighting source) Use Back light *2	
Ambient illumination	300 to 700lx	
Viewing distance	350mm	±50mm
Check pattern	Module non operation	White or Black picture position

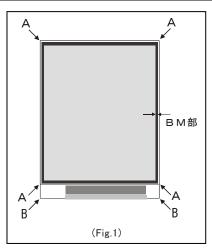
^{*2} Please refer to the panel surface brightness of the description specifications.

8-2 Glass edge crack / chip

Items	Inspection criteria (Acceptable level)	note
Chip on glass corner (Part A)	L <= 5mm , D <= 1mm L + D <= 5mm	Fig.1-A fig.2
	*BM (black mask) is not affected.	
Chip on the terminal glass	L <= 3mm , D <= 3mm	fig.1-B
(Part B)	*FPC and patterns are not affected	fig.2
Chip on glass edge	L <= 10mm , D <= 1mm	fig.3
	*BM (black mask) is not affected	





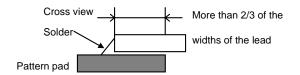


^{*}Please refer to specifications for the inspection area of the externals inspection.

8-3 Parts assembly

8-3-1 Parts alignment

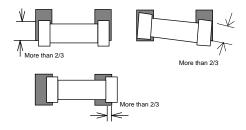
(a) Flat packaged LSI, IC Locate 2/3 or more of the widths of the lead on the pattern pad.



(b) Chip component

Locate 2/3 or more of the widths of the electrode on the pattern pad.

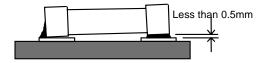
Locate the entire electrode on the pattern pad, If the width of pattern pad is narrower than component electrode.



8-3-2 Height of components

The installation floatages of the chip components must be less than 0.5mm from the FPC pad.

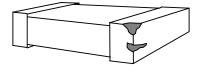
Individual regulations give priority when individual regulations exist on specified drawings



8-3-3 Damaged electrode of chip components

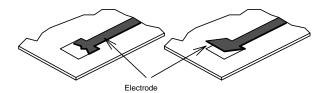
Do not expose the inside. Do not allow the crack.

Peeling off of the electrode plating must be less than 10% of the area of the electrode.



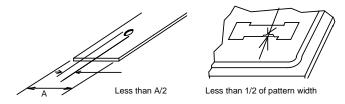
8-3-4 FPC electrode peeling off (floatage)

The electrode (FPC pattern) must not peel off from the FPC substrate.



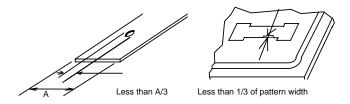
8-3-5 Damaged FPC pattern

The width of pinhole and/or loss of FPC pattern must be less than 1/2 of pattern width.



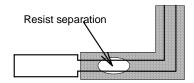
8-3-6 Damaged plating of FPC

The width of pinhole and/or loss of FPC pattern must be less than 1/3 of pattern width



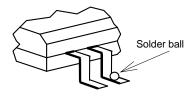
8-3-7 FPC resist separation

FPC pattern which not soldered must be coated by resist.



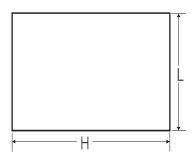
8-3-8 Conductive foreign material

Conductive foreign material of length which exceeds $0.30 \, \text{mm}$ must not adhere on the module even if the length of foreign materials is less than $0.30 \, \text{mm}$, adhering on leads of IC and LSI is not acceptable



9. Visual inspection

9-1 Zone



* Please refer to the effective display area (active area)

of specification about H,L

9-2 Definition

No	Item		Definition	
_	D. I	Pixel	3 sub-pixels (R+G+B)	
а	Dot	Dot	1 sub-pixel (R or G or B)	
		When the Module lig	ghts, dot appear bright in display	
b	Bright dot *	at Black picture position.		
	(caused by TFT failure)	Count	Visible through 5% ND filter	
		Ignore	Not visible through 5% ND filter	
	Black dot *	When the Module lights, dot appear black in display at		
С	(caused by TFT failure)	white picture position		
١.,	Scratch on the	Count as bright dot	Visible over the half of a dot	
d	color filter	Ignore	Visible under the half of a dot	
	Scratch on the	Count as bright dot Visible over ø50 µm	Visible over ø50 µm	
е	Cr mask	Ignore	Visible under ø50 µm	

^{*} Regarding Black dot caused by Extraneous Substances, Polarizer bubble and/ or Scratch,

9-3 Number of Dot Defects(Bright dot+Black dot)

Item	Not of dot defects
Bright dots	1
Black dots	3
Total(Bright dots+Black dots)	3

9-4 Defect distance &join

		•	
	Iten	n	Inspection criteria
Defect distance	Bright dots	5 mm or more	
	Defect distance	Black dots	5 mm or more
		Bright dots	Not allowed
	Joined dots	Black dots	Connection of a black dot is permitted to two dots
	3 dots or more	Not allowed	

^{*}It is considered that the joined black dot is one black dot.

10. Display non-uniformity

There should be no distinct non-uniformity visible through 2% ND filter.

[&]quot;External inspection criteria" should be applied to them. (Please see section 8-1)

If e	ome problems arise about mentioned items in this document and other items,
the	user of the TFT-LCD module and Sharp will cooperate and make efforts to solve problems with mutual respect and good will.