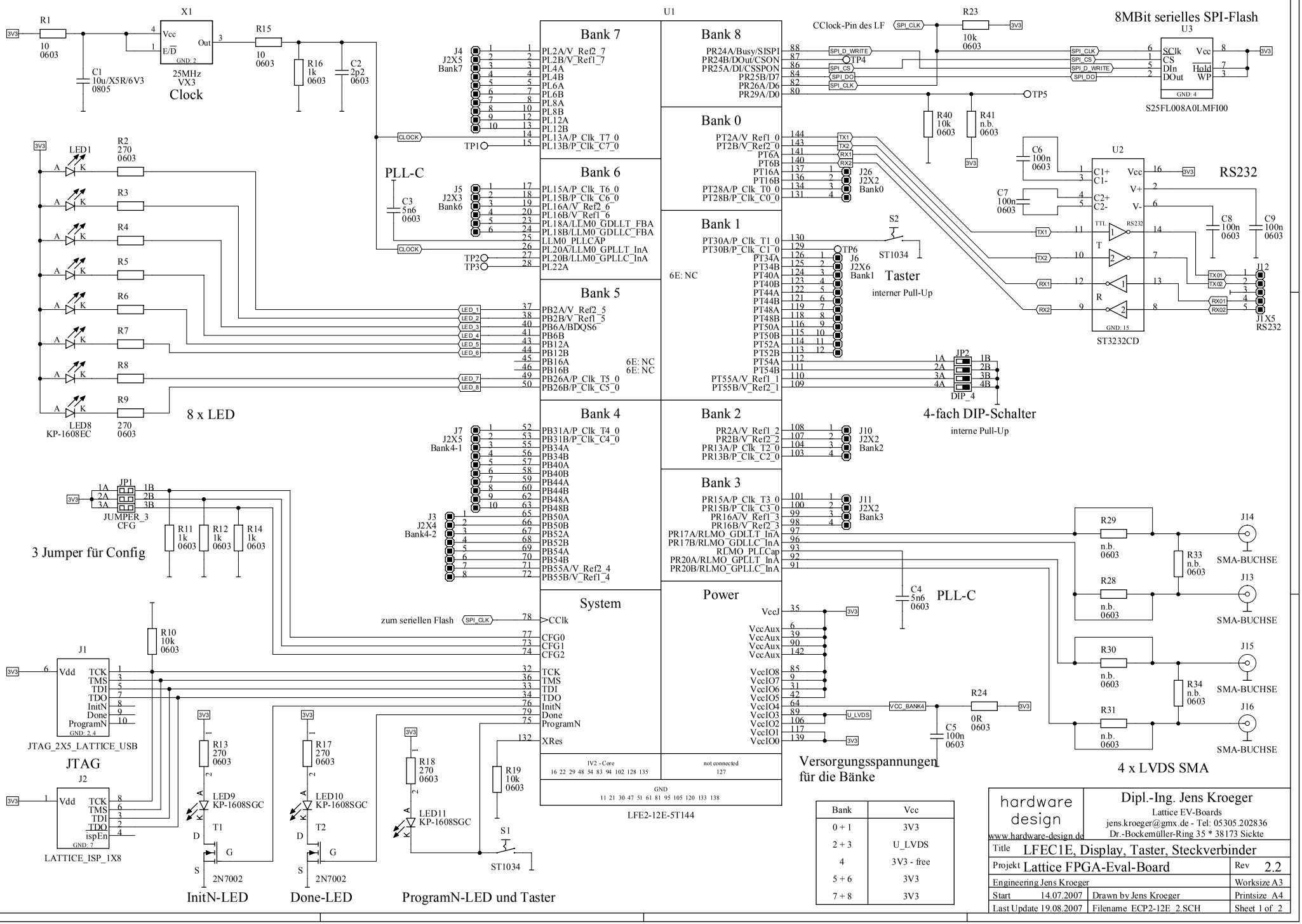
U1
Bank 7
Bank 8
Bank 0
Bank 6
Bank 1
Bank 5
Bank 4
Bank 2
Bank 3
System
Power
LFE2-12E-5T144
X1
25MHz
VX3
Clock
C1
10u/X5R/6V3
0805
R1
10
0603
R15
10
0603
R16
1k
0603
C2
2p2
0603
CLOCK
TP1
PLL-C
C3
5n6
0603
J4
J2X5
Bank7
J5
J2X3
Bank6
TP2
TP3
J3
J2X4
Bank4-2
J7
J2X5
Bank4-1
zum seriellen Flash
SPI_CLK
CCLK-Pin des LF
R23
10k
0603
8MBit serielles SPI-Flash
U3
S25FL008A0LMFI00
SPI_D_WRITE
SPI_CS
SPI_DO
TP4
TP5
R40
10k
0603
R41
n.b.
0603
U2
ST3232CD
RS232
C6
100n
0603
C7
100n
0603
C8
100n
0603
C9
100n
0603
J12
J1X5
RS232
TX1
TX2
RX1
RX2
S2
ST1034
Taster
interner Pull-Up
6E: NC
J6
J2X6
Bank1
J26
J2X2
Bank0
JP2
DIP_4
4-fach DIP-Schalter
interne Pull-Up
LED1
LED8
KP-1608EC
R2
R3
R4
R5
R6
R7
R8
R9
270
0603
8 x LED
JP1
JUMPER_3
CFG
3 Jumper für Config
R11
R12
R14
1k
0603
R10
10k
0603
J1
JTAG_2X5_LATTICE_USB
JTAG
J2
LATTICE_ISP_1X8
R13
R17
R18
270
0603
LED9
LED10
LED11
KP-1608SGC
T1
T2
2N7002
InitN-LED
Done-LED
ProgramN-LED und Taster
R19
10k
0603
S1
ST1034
R29
R28
R30
R31
n.b.
0603
R33
R34
n.b.
0603
J14
J13
J15
J16
SMA-BUCHSE
4 x LVDS SMA
C4
5n6
0603
PLL-C
C5
100n
0603
R24
0R
0603
VCC_BANK4
U_LVDS
Versorgungsspannungen
für die Bänke
IV2 - Core
not connected
GND
Bank | Vcc
0 + 1 | 3V3
2 + 3 | U_LVDS
4 | 3V3 - free
5 + 6 | 3V3
7 + 8 | 3V3
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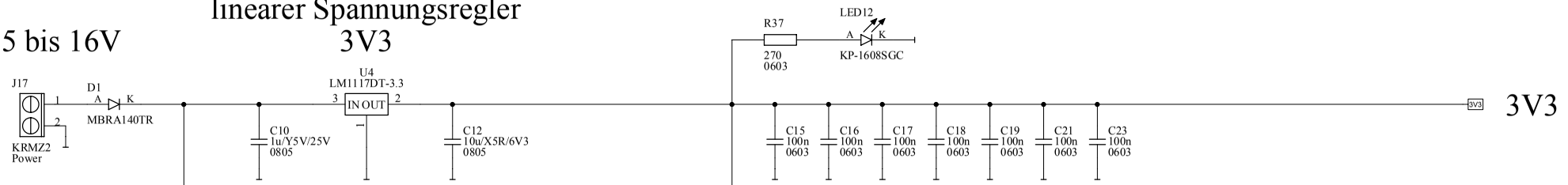
Title LFEC1E, Display, Taster, Steckverbinder
Projekt Lattice FPGA-Eval-Board
Rev 2.2
Engineering Jens Kroeger
Worksize A3
Start 14.07.2007
Drawn by Jens Kroeger
Printsize A4
Last Update 19.08.2007
Filename ECP2-12E_2.SCH
Sheet 1 of 2

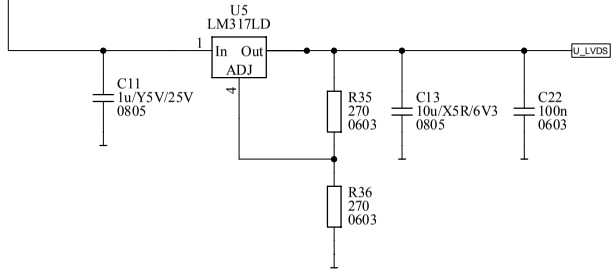
Power - In

5 bis 16V

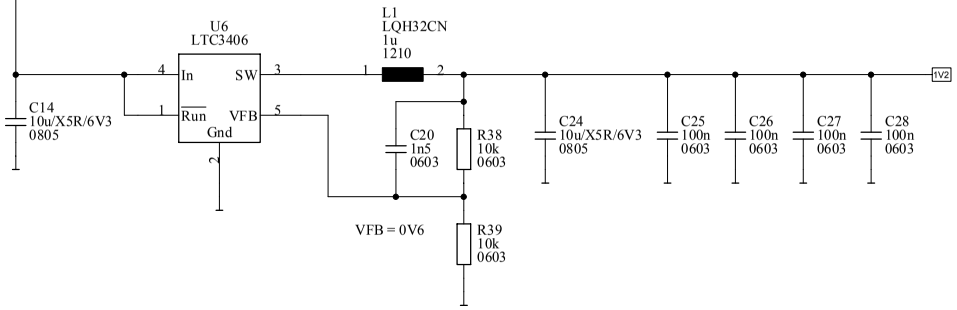
linearer Spannungsregler 3V3



linearer Spannungsregler U_LVDS



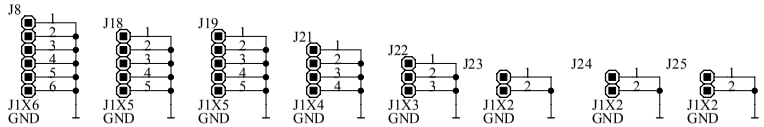
Step-Down-Converter 1V2 - 600mA



2V5 für die LVDS-Verbindung (Bank 2, 3 und wahlweise 4)

Vout = 1,25V (1 + R35/R36) + 0,1mA * R25
R35 = 1,25V * R36 / (Vout - 1,25V - 0,1mA * R36)

I max = 100mA



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Last Update 19.08.2007	Filename ECP2-12E_2.SCH	Sheet 2 of 2