4.0 Register Description

The 82C930 uses the base addresses shown in Table 4-1.

Table 4-1 82C930 I/O Base Addresses

Function	Base	Address Selections
Configuration Registers	MCBase	F8F; E0E,F/FFE,F
Digital Audio Processor	DABase	220/240
Windows Sound System	WSBase	530/640/E80/F40
Proprietary CD ROM	CDBase	320/330/340/360
IDE CD ROM	IDEBase	170 & 370
AdLib	ALBase	388
OPL4	OPL4Base	380
MPU-401	MIDIBase	300/310/320/330

Table 4-2 82C930 Register Map

I/O Address	Description	R/W
SBBase + 0 ALBase + 0	Left FM Status Port	R only
SBBase + 0 ALBase + 0	Left FM Register Address Port	W only
SBBase + 1 ALBase + 1	Left FM Data Port	W only
SBBase + 2 ALBase + 2	Right FM Register Address Port	W only
SBBase + 3 ALBase + 3	Right FM Data Port	W only
SBBase + 4	Mixer Address Port	W only
SBBase + 5	Mixer Data Port	R/W
SBBase + 6	Digital Audio Processor Software Reset	W only
SBBase + 8	FM Status Port	R only
SBBase + 8	FM Register Address Port	W only
SBBase + 9	FM Data Port	W only
SBBase + A	Digital Audio Processor Read Data	R only, Digital Audio Processor AO = 0
SBBase + C	Digital Audio Processor Write Data/ Cmd	W only, Digital Audio Processor AO = 1
SBBase + C	Digital Audio Processor Write Buffer Status	R only, Digital Audio Processor AO = 1
SBBase + E	Digital Audio Processor Output Buffer Status Reg	R only, Digital Audio Processor AO = 1
WSBase + 0-3	Configuration	W only

I/O Address	Description	R/W
WSBase + 0-3	Version	R only
WSBase + 4	Codec Index Reg	R/W, exists in Codec and shadowed in 82C930
WSBase + 5	Codec Indexed Data Reg	R/W, exists in Codec only
WSBase + 6	Codec Status Reg	R/W, exists in Codec only
WSBase + 7	Codec Direct Data	R/W, exists in Codec only
200-201	Game Port	R/W
CDBase + 0-3	CD ROM Reg	R/W
F8F	Password Register/MCBase	W only
MCBase+1	MC1	R/W
MCBase+2	MC2	R/W
MCBase+3	MC3	R/W
MCBase+4	MC4	R/W
MCBase+5	MC5	R/W
MCBase+6	MC6	R/W
MCBase+7	MC7	R/W
MCBase+8	MC8	R/W
MCBase+9	MC9	R/W
MCBase+10	MC10	R/W
MCBase+11	MC11	R/W
MCBase+12	MC12	R/W
380-383/388-38B	OPL4	R/W
388-38F	OPL5	R/W

4.1 82C930 Register Definition

Note (1) All Registers are set to '0' after reset.
(2) The default software setting is highlighted with **BOLD** characters.

4.1.1 Direct MC Register

MCBase Write Only Port = F8F							
7	6	5	4	3	2	1	0
PassWD = E4							
PASS EN#			MCA4	MCA3	MCA2	MCA1	MCAD0

MCBase is the indirect MC address register that controls the access of other MC registers. To access MC1 to MC12. MCBase must be written with the index address first. This register is always protected by the password. Pass Word is "E4".

Pass En#: Pass word protection enable control for the MC registers. '0' enables protection.

MCIdx Port Address = b"111[MCA4] - [MCA3:0] - 1110"							
7	6	5	4	3	2	1	0
Index							

MCData Port Address = b" 111[MCAD4] - [MCA3:0] - 1111"							
7	6	5	4	3	2	1	0
Data							

4.1.2 Indirect MC Registers

MC1 Base/Type configuration Register							
7	6	5	4	3	2	1	0
SB BASE		WSS BASE[1:0]		CDTYPE[2:0]			GPEN#
SB Base Address 0 = 220 1 = 240		WSS Base Address: 00 = WSBase = 530 01 = WSBase = E80 10 = WSBase = F40 11 = WSBase = 604		000 = CD is disabled 001 = reserved 010 = reserved 011 = reserved 100 = Secondary IDE 101 = Primary IDE 110 = reserved 111 = reserved			Game Port Enable 0 = enabled 1 = disabled

SB Base: SB I/O Base Address.

Sound Base: Wss I/O Base Address. MC[5:4] selects the I/O base address among the four specified addresses.

CD Type: Type of CD ROM Interface
This field selects one of the three CD ROM interfaces supported by 82C930.

Game Port Enable:

MC2 CD Configuration Register							
7	6	5	4	3	2	1	0
CDSEL[1:0]		IDE DEN	Reserved				
CD Base Address Select 00 = CDBase = 340 01 = CDBase = 330 10 = CDBase = 360 11 = CDBase = 320		IDE DMA enable 0 = disable 1 = enable					

CDSEL: CD ROM Base Address
The Base I/O address for CD ROM interface.

CDIRQ: CD ROM Interrupt Select
This field selects the interrupt channel for CD ROM interface. When users change IRQ selection through software, false IRQ's will be generated due to the open-drain drivers employed on the IRQ outputs. During this time, interrupt needs to be disabled temporarily.

CDDRQ: CD ROM DMA Select

MC3 SB/WSS Configuration Register							
7	6	5	4	3	2	1	0
CNFG7	ISS	SBISEL[2:0]			SBDSEL[2:0]		
Reserved Must be '0'	Reserved Must be '0' for normal operation in WSS	DAP IRQ SELECT: 000 = IRQ Disable 001 = IRQ7 010 = IRQ9 011 = IRQ10 100 = IRQ11 101 = IRQ5 110 = Reserved 111 = Reserved			DAP DMA SELECT: 000 = Disable 001 = DRQ0 010 = DRQ1 011 = DRQ3 100 = Disable DRQ1 * 101 = DRQ0 DRQ1 * 110 = DRQ1 DRQ0 * 111 = DRQ3 DRQ0 *		

* These should be the DMA channel selection when running MEC operation in DMA mode. SDC should be set to '0'.

MC4 User Programmable General Purpose Register							
7	6	5	4	3	2	1	0
FCC[1:0]		OPL[1:0]		DACZ	SILENCE	SBVER	
Playback FIFO: 00 = Empty 01 = Full-2 10 = Full-4 11 = Not Full		OPL Select: 00 = OPL2 01 = OPL3 10 = OPL4 11 = OPL5		DAC Zero: 0 = Hold 1 = Clear	0 = Audio 1 = Clear	00 = 2.1 01 = 1.5 10 = 3.2 11 = 4.4	

GPOUT[1:0]: General Purpose Outputs

OPL[1:0]: Yamaha Synthesis Chip type selection

SILENCE: Disable host access to FM, SB/WSS

SBVER: Sound Blaster version.

MC5 Option Register							
7	6	5	4	3	2	1	0
Reserved		MODE2	ADPCM EN	CFIFO	EP EN	Reserved	Reserved
PEN RST Enable: 0 = Disable Must be 0		CS4231: 0 = Mode 1 1 = Mode 2	ADPCM Enable: 0 = Disable 1 = Enable	C-FIFO Enable: 0 = Disable 1 = Enable	EP Enable: 0 = Enable 1 = Disable	DRQ TM Enable: 0 = Disable Must be 0	FSMUTE Enable: 0 = Disable Must be '0'

MODE2: To enable Codec's Extended Mode (mode2).

ADPCMEN: To enable SB ADPCM.

CFIFO: To enable command FIFO in Sound Blaster mode.

EPEN: To enable Volume Effect for Sound Blaster Pro mixer voice volume emulation.