## Forum Frage Xilinx: warum kein **xgmii\_rx** 10G Ethernet MAC Core 10GMAC+XAUI clk156 out 10GMAC Testbench xgmii txd[63:0] gmii\_txd[63:0] Using: BIST MODE xgmii\_txd[7:0] xgmii\_txc[7:0] Test Bench **DEMO MODE** xamii rxd[63:0] Dclk= 50MHz xamii rxd[7:0] xamii rxc[7:0] DUT Refclk p/n= 156 MHz Togglin config vector until aligned mdio\_i Signal detect= 1111 mdio ou mdio out Reset 1 → 0 after 700 ns mdio tr nternal/XGMI AXI-S Clk156 out is coming Monitor Xilinx: Xaui testbench Stimulus clk156 lock is coming Figure 3-61: 10G Ethernet MAC Core Integrated with XAUI Core 10G DEMO Ethernet BIST demo\_tb Xaui MAC lanes Xaui lanes are translated into Internal/XGMI AXI-S xamii and Transceivers Stimulus Monitor compared with original frame Clock Clock Support Control and Data structures Generation Management Testbench with xaui Stimulus 4 Original frames AXI-S config Stimulus 10G XAUI loopback Ethernet Figure 6-1: st Bench MAC AXI-S Monitor No xgmii\_rx Here xgmii\_rx data are present: data coming... It begins with 0100009c and when xaui is ready it goes to 0x0707 which means idle. Why? Then 4 Frames can be seen and then again 0x0707 4ever Doesn't make sense! Clock Management Even status and debug vector are Figure 6-1: Test Bench correct like they should be! Value 23.02.22 21

No RXD? WHY?