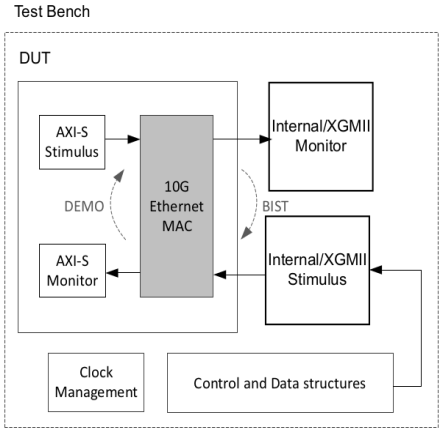
Forum Frage
warum kein **xgmii_rx**

10GMAC Testbench
Using:**BIST MODE**
DEMO MODE



- Dclk= 50MHz
- Refclk_p/n= 156 MHz
- Togglin config vector until aligned
- Signal_detect= 1111
- Reset 1→ 0 after 700 ns
- Clk156_out is coming
- clk156_lock is coming

Xilinx:
10GMAC+XAUI

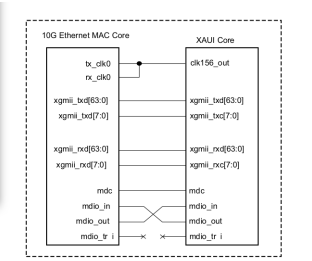
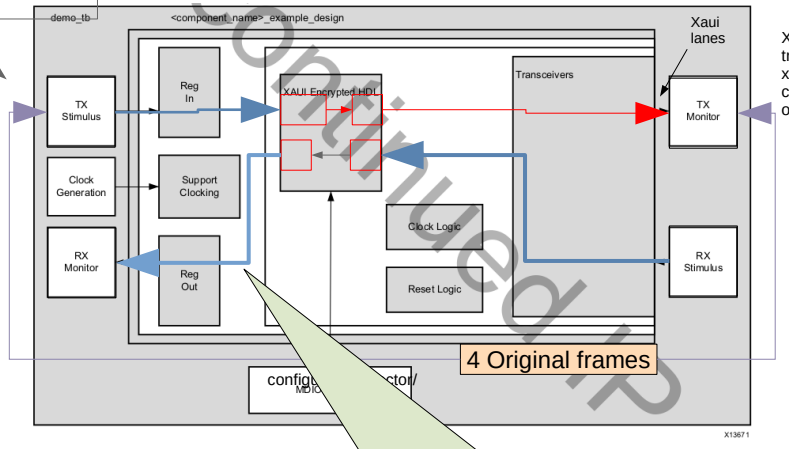


Figure 3-61: **10G Ethernet MAC Core Integrated with XAUI Core**

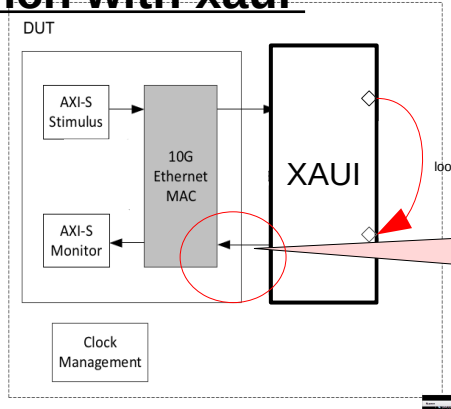
Xilinx: Xaui testbench



Xaui lanes are translated into xgmii and compared with original frame

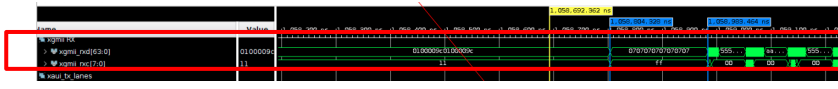
Figure 6-1: **D… …st Bench**

Testbench with xaui



No xgmii_rx
data coming…
Why?
Doesn‘t make sense!

Here **xgmii_rx** data are present:
It begins with 0100009c and when
xaui is ready it goes to 0x0707 which means idle.
Then 4 Frames can be seen and then again 0x0707 4ever



Even status and debug vector are correct like they should be!

Figure 6-1: **Test Bench**