# HD66100F

(LCD Driver with 80-Channel Outputs)

HITACHI

## Description

The HD66100F description segment driver with 80 LCD drive circuits is the improved version of the no longer current HD44100H LCD driver with 40 circuits.

It is composed of a shift register, an 80-bit latch circuit, and 80 LCD drive circuits. Its interface is compatible with the HD44100H. It reduces the number of LSI's and lowers the cost of an LCD module.

## Features

- LCD driver with serial/parallel converting function
- Interface compatible with the HD44100H; connectable with HD43160AH, HD61830, HD61830B, LCD-II (HD44780), LCD-III (HD44790)
- Internal output circuits for LCD drive: 80
- Internal serial/parallel converting circuits
  - 80-bit bidirectional shift register
  - 80-bit latch circuit
- Power supply
  - Internal logic circuit: +5V ±10%
  - LCD drive circuit: 3.0V to 6.0V
- CMOS process

## Comparison with HD44100H

Table 1 shows the main differences between HD66100F and HD44100H.

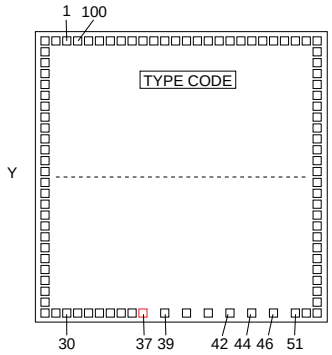
**Table 1 Difference between Products HD66100F and HD44100H**

| | HD66100F | HD44100H |
|---|---|---|
| LCD drive outputs | 80 × 1 channel | 20 × 2 channels |
| Supply voltage for LCD drive circuits | 3 to 6V | 4.5 to 11V |
| Multiplexing duty ratio | Static to 1/16 duty | Static to 1/32 duty |
| Package | 100-pin plastic QFP | 60-pin plastic QFP |

## Ordering Information

| Type No. | Package |
|---|---|
| HD66100F | 100-pin plastic QFP (FP-100) |
| HD66100FH | 100-pin plastic QFP (FP-100B) |
| HD66100D | Chip |

## Pad Coordinate

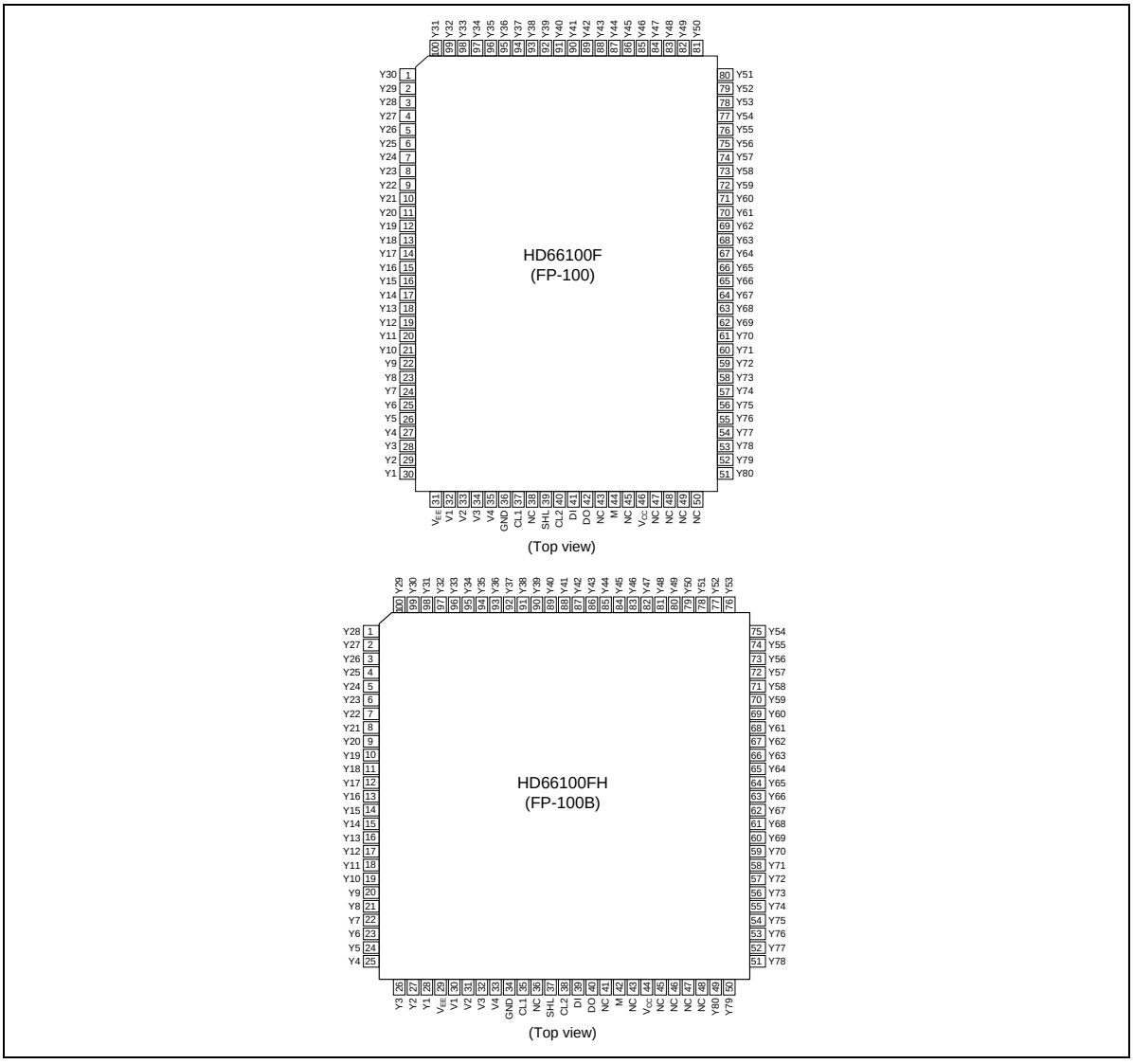



Chip size (X × Y) : 4.50mm × 4.50mm
Coordinate : Pad Center
Origin : Chip Center
Pad size (X × Y) : 100µm × 100µm

Unit : µ m

| Pad No. | Function | Coordinate X | Coordinate Y |
|---|---|---|---|
| 1 | Y30 | –1725 | 2100 |
| 2 | Y29 | –1925 | 2100 |
| 3 | Y28 | –2100 | 2060 |
| 4 | Y27 | –2100 | 1865 |
| 5 | Y26 | –2100 | 1690 |
| 6 | Y25 | –2100 | 1520 |
| 7 | Y24 | –2100 | 1360 |
| 8 | Y23 | –2100 | 1200 |
| 9 | Y22 | –2100 | 1040 |
| 10 | Y21 | –2100 | 880 |
| 11 | Y20 | –2100 | 720 |
| 12 | Y19 | –2100 | 560 |
| 13 | Y18 | –2100 | 400 |
| 14 | Y17 | –2100 | 240 |
| 15 | Y16 | –2100 | 80 |
| 16 | Y15 | –2100 | –80 |
| 17 | Y14 | –2100 | –240 |
| 18 | Y13 | –2100 | –400 |
| 19 | Y12 | –2100 | –560 |
| 20 | Y11 | –2100 | –720 |
| 21 | Y10 | –2100 | –880 |
| 22 | Y9 | –2100 | –1040 |
| 23 | Y8 | –2100 | –1200 |
| 24 | Y7 | –2100 | –1360 |
| 25 | Y6 | –2100 | –1520 |
| 26 | Y5 | –2100 | –1690 |
| 27 | Y4 | –2100 | –1865 |
| 28 | Y3 | –2100 | –2060 |
| 29 | Y2 | –1925 | –2100 |
| 30 | Y1 | –1725 | –2100 |
| 31 | $V_{EE}$ | –1520 | –2100 |
| 32 | V1 | –1360 | –2100 |
| 33 | V2 | –1200 | –2100 |
| 34 | V3 | –1040 | –2100 |
| 35 | V4 | –880 | –2100 |
| 36 | GND | –720 | –2100 |
| 37 | CL1 | –470 | –2100 |
| 38 | | | |
| 39 | SHL | –270 | –2100 |
| 40 | CL2 | –70 | –2100 |
| 41 | DI | 130 | –2100 |
| 42 | DO | 350 | –2100 |
| 43 | | | |
| 44 | M | 620 | –2100 |
| 45 | | | |
| 46 | $V_{CC}$ | 980 | –2100 |
| 47 | | | |
| 48 | | | |
| 49 | | | |
| 50 | | | |
| 51 | Y80 | 1725 | –2100 |
| 52 | Y79 | 1925 | –2100 |
| 53 | Y78 | 2100 | –2060 |
| 54 | Y77 | 2100 | –1865 |
| 55 | Y76 | 2100 | –1690 |
| 56 | Y75 | 2100 | –1520 |
| 57 | Y74 | 2100 | –1360 |
| 58 | Y73 | 2100 | –1200 |
| 59 | Y72 | 2100 | –1040 |
| 60 | Y71 | 2100 | –880 |
| 61 | Y70 | 2100 | –720 |
| 62 | Y69 | 2100 | –560 |
| 63 | Y68 | 2100 | –400 |
| 64 | Y67 | 2100 | –240 |
| 65 | Y66 | 2100 | –80 |
| 66 | Y65 | 2100 | 80 |
| 67 | Y64 | 2100 | 240 |
| 68 | Y63 | 2100 | 400 |
| 69 | Y62 | 2100 | 560 |
| 70 | Y61 | 2100 | 720 |
| 71 | Y60 | 2100 | 880 |
| 72 | Y59 | 2100 | 1040 |
| 73 | Y58 | 2100 | 1200 |
| 74 | Y57 | 2100 | 1360 |
| 75 | Y56 | 2100 | 1520 |
| 76 | Y55 | 2100 | 1690 |
| 77 | Y54 | 2100 | 1865 |
| 78 | Y53 | 2100 | 2060 |
| 79 | Y52 | 1925 | 2100 |
| 80 | Y51 | 1725 | 2100 |
| 81 | Y50 | 1520 | 2100 |
| 82 | Y49 | 1360 | 2100 |
| 83 | Y48 | 1200 | 2100 |
| 84 | Y47 | 1040 | 2100 |
| 85 | Y46 | 880 | 2100 |
| 86 | Y45 | 720 | 2100 |
| 87 | Y44 | 560 | 2100 |
| 88 | Y43 | 400 | 2100 |
| 89 | Y42 | 240 | 2100 |
| 90 | Y41 | 80 | 2100 |
| 91 | Y40 | –80 | 2100 |
| 92 | Y39 | –240 | 2100 |
| 93 | Y38 | –400 | 2100 |
| 94 | Y37 | –560 | 2100 |
| 95 | Y36 | –720 | 2100 |
| 96 | Y35 | –880 | 2100 |
| 97 | Y34 | –1040 | 2100 |
| 98 | Y33 | –1200 | 2100 |
| 99 | Y32 | –1360 | 2100 |
| 100 | Y31 | –1520 | 2100 |

## Pin Arrangement



## Pin Description

**$V_{CC}$, GND, $V_{EE}$:** $V_{CC}$ supplies power to the internal logic circuit. GND is the logic and drive ground. $V_{EE}$ supplies power to the LCD drive circuit.

**V1, V2, V3, and V4:** V1 to V4 supply power for driving an LCD (Figure 2).

**CL1:** HD66100F latches data at the negative edge of CL1.

**CL2:** HD66100F receives shift data at the negative edge of CL2.

**M:** Changes LCD drive outputs to AC.

**DI:** Inputs data to the shift register.

**DO:** Output data from the shift register.

**SHL:** Selects a shift direction of serial data. When the serial data is input in order of D1, D2, ..., D79, D80, the relation between the data and the output Y is shown in Table 3.

**Y1–Y80:** Each Y outputs one of the four voltage levels—V1, V2, V3, or V4—according to the combination of M and display data (Figure 2).

**NC:** Do not connect any wire to these terminals.

**Table 2 Pin Function**

| Symbol | Pin No. | Pin Name | I/O |
|---|---|---|---|
| $V_{CC}$ | 46 | $V_{CC}$ | — |
| GND | 36 | Ground | — |
| $V_{EE}$ | 31 | $V_{EE}$ | — |
| V1 | 32 | V1 | — |
| V2 | 33 | V2 | — |
| V3 | 34 | V3 | — |
| V4 | 35 | V4 | — |
| CL1 | 37 | Clock 1 | I |
| CL2 | 40 | Clock 2 | I |
| M | 44 | M | I |
| DI | 41 | Data in | I |
| DO | 42 | Data out | O |
| SHL | 39 | Shift left | I |
| Y1–Y80 | 1–30, 51–100 | Y1–Y80 | O |
| NC | 38, 43, 45, 47–50 | No connection | — |

**Table 3 Relation between SHL and Data Output**

| SHL | Y1 | Y2 | Y3..... | Y79 | Y80 |
|---|---|---|---|---|---|
| High | D1 | D2 | D3..... | D79 | D80 |
| Low | D80 | D79 | D78..... | D2 | D1 |

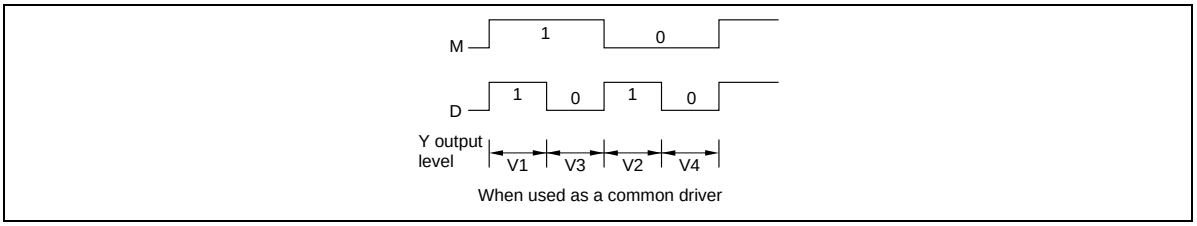



**Figure 1 Selection of LCD Drive Output**

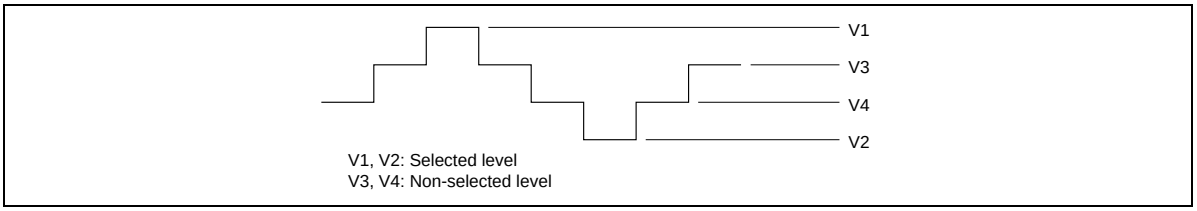



**Figure 2 Power Supply for Driving an LCD**

## Block Functions

### LCD Drive Circuits

Select one of four levels of voltage V1, V2, V3, and V4 for driving a LCD and transfer it to the output terminals according to the combination of M and the data in the latch circuit.

### Latch Circuit

Latches the data input from the bidirectional shift register at the fall of CL1 and transfer its outputs to the LCD drive circuits.

### Bidirectional Shift Register

Shifts the serial data at the fall of CL2 and transfers the output of each bit of the register to the latch circuit. When SHL = GND, the data input from DI shifts from bit 1 to bit 80 in order of entry. On the other hand, when SHL = $V_{CC}$, the data shifts from bit 80 to bit-1. In both cases, the data of the last bit of the register is latched to be output from DO at the rise of CL2.

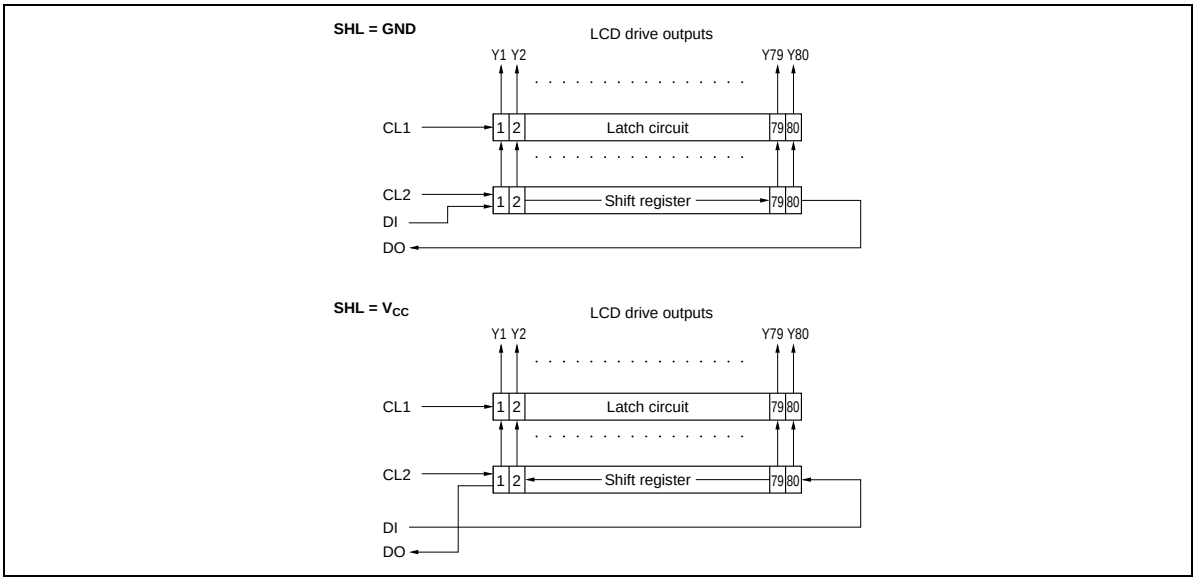



**Figure 3 Relation between SHL and the Shift Direction**

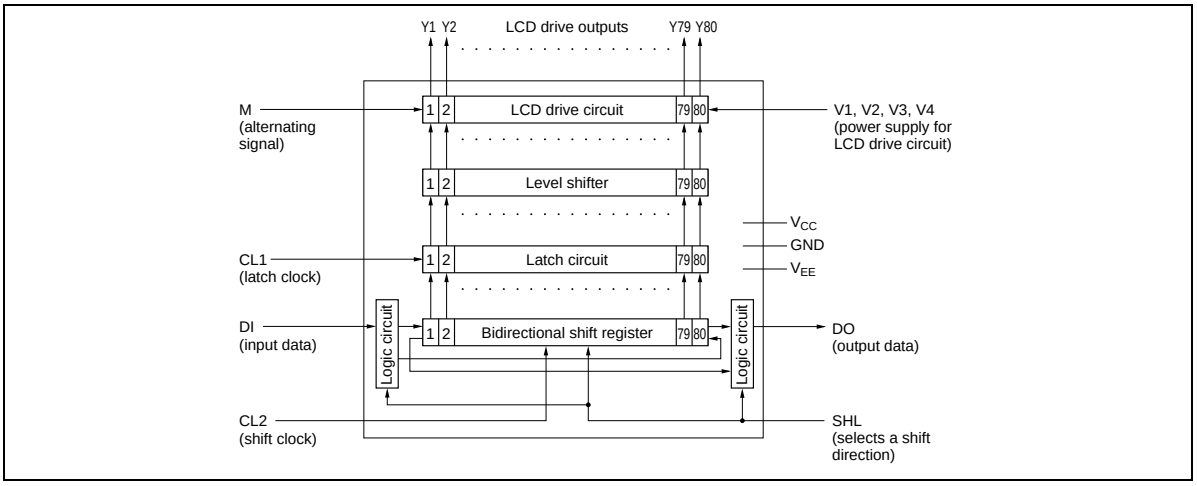



**Figure 4 Block Diagram**

## Primary Operations

### Shifting Data

The input data DI shifts at the fall of CL2 and the data delayed 80 bits by the shift register is output from the DO terminal. The output of DO changes synchronously with the rise of CL2. This operation is completely unaffected by the latch clock CL1.

### Latching Data

The data of the shift register is latched at the negative edge of the latch clock CL1. Thus, the outputs Y1–Y80 change synchronously with the fall of CL1.

### Switching Data Shift Direction

When the shift direction switching signal SHL is connected with GND, the data D80, immediately before the negative edge of CL1, is output from the output terminal Y1. When SHL is connected with $V_{CC}$, it is output from Y80.

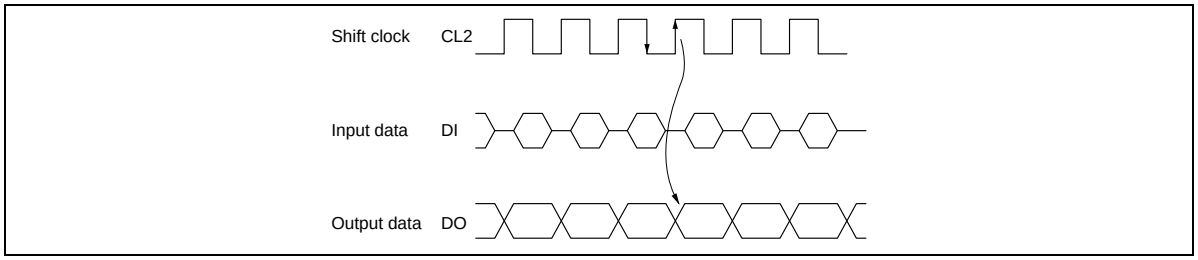



**Figure 5 Timing of Receiving and Outputting Data**

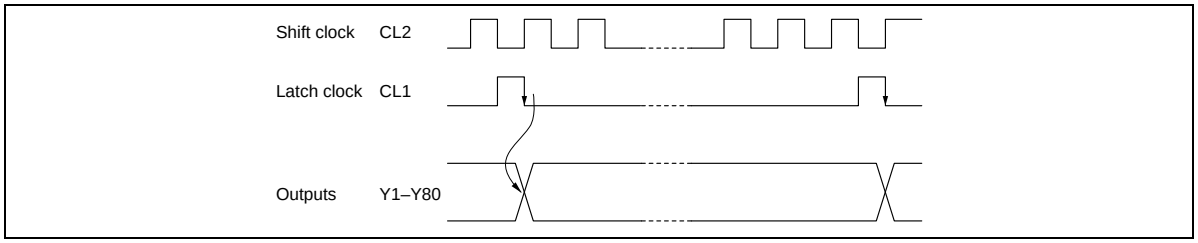



**Figure 6 Timing of Latching Data**

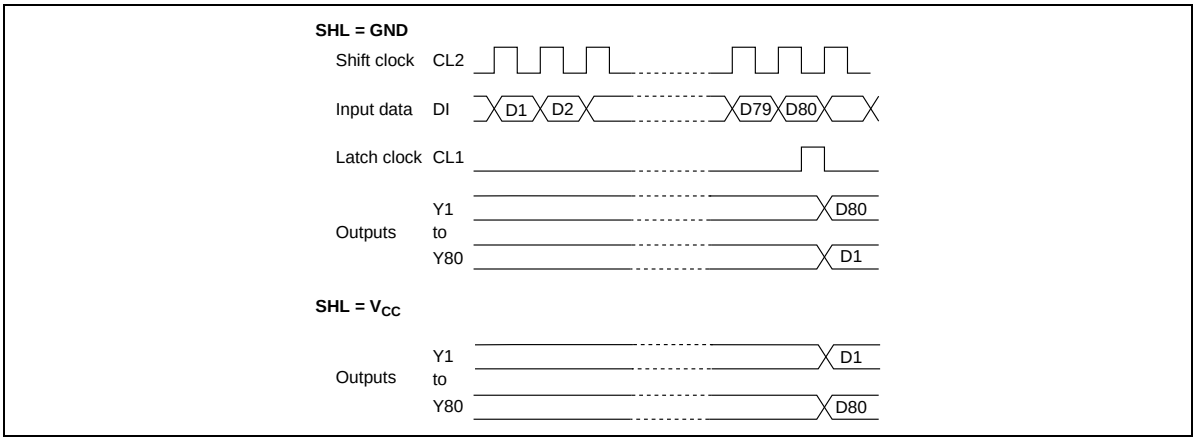



**Figure 7 SHL and Waveforms of Data Shift**

## Absolute Maximum Ratings

| Item | | Symbol | Ratings | Unit | Note |
|---|---|---|---|---|---|
| Supply voltage | Logic circuits | $V_{CC}$ | –0.3 to +7.0 | V | 1 |
| | LCD drive circuits | $V_{CC}$–$V_{EE}$ | –0.3 to +7.0 | V | |
| Input voltage (1) | | VT1 | –0.3 to $V_{CC}$ + 0.3 | V | 1 |
| Input voltage (2) | | VT2 | $V_{CC}$ + 0.3 to $V_{EE}$ – 0.3 | V | 2 |
| Operation temperature | | $T_{opr}$ | –20 to +75 | °C | |
| Storage temperature | | $T_{stg}$ | –55 to +125 | °C | |

Notes: 1. A reference point is GND (= 0V)
2. Applies to V1–V4.

Note: If used beyond the absolute maximum ratings, LSIs may be permanently destroyed. It is best to use them at the electrical characteristics for normal operations. If they are not used at these conditions, it may affect the reliability of the device.

## Electrical Characteristics

**DC Characteristics ($V_{CC}$ = 5V ± 10%, $V_{CC} – V_{EE}$ = 3.0 to 6.0V, GND = 0V, Ta = –20 to +75°C)**

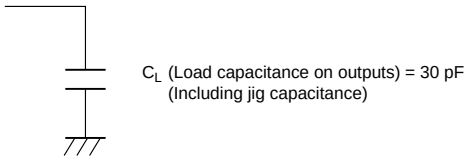
| Item | Symbol | Terminals | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | VIH | CL1, CL2, M, DI, SHL | $0.8 \times V_{CC}$ | — | $V_{CC}$ | V | | |
| Input low voltage | VIL | | 0 | — | $0.2 \times V_{CC}$ | V | | |
| Output high voltage | VOH | DO | $V_{CC} – 0.4$ | — | — | V | $I_{OH}$ = –0.4 mA | |
| Output low voltage | VOL | | — | — | 0.4 | V | $I_{OL}$ = +0.4 mA | |
| On resistance Vi–Vj | $R_{ON1}$ | Y1–Y80 V1–V4 | — | — | 11 | kΩ | $I_{ON}$ = 0.1 mA to one Y terminal | |
| | $R_{ON2}$ | | — | — | 30 | kΩ | $I_{ON}$ = 0.05 mA to each Y terminal | |
| Input leakage current | $I_{IL}$ | CL1, CL2, M, DI, SHL | –5.0 | — | 5.0 | µA | Vin = 0V to $V_{CC}$ | |
| Vi leakage current | $I_{VL}$ | V1–V4 | –5.0 | — | 5.0 | µA | Output Y1–Y80 open<br>Vin = $V_{CC}$ to $V_{EE}$ | |
| Current dissipation | $I_{GND}$ | | — | — | 2.0 | mA | $f_{CL2}$ = 1.0 MHz<br>$f_{CL1}$ = 2.5 kHz | 1 |
| | $I_{EE}$ | | — | — | 0.1 | mA | | |

Note: 1. Input/output currents are excluded; when an input is at the intermediate level in CMOS, excessive current flows from the power supply through the input circuit.
To avoid this, VIH and VIL must be fixed at $V_{CC}$ and GND level respectively.

**AC Characteristics ($V_{CC}$ = 5V ± 10%, $V_{CC}$ – $V_{EE}$ = 3.0 to 6.0V, GND = 0V, Ta = –20 to +75°C)**

| Item | Symbol | Terminals | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Data shift frequency | $f_{CL}$ | CL2 | — | — | 1 | MHz | |
| Clock high level width | $t_{CWH}$ | CL1, CL2 | 450 | — | — | ns | |
| Clock low level width | $t_{CWL}$ | CL2 | 450 | — | — | ns | |
| Data set–up time | $f_{SU}$ | DI | 100 | — | — | ns | |
| Clock set–up time (1) | $t_{SL}$ | CL2 | 200 | — | — | ns | 1 |
| Clock set–up time (2) | $t_{LS}$ | CL1 | 200 | — | — | ns | 2 |
| Output delay time | $t_{pd}$ | DO | — | — | 250 | ns | 3 |
| Data hold time | $t_{DH}$ | DI | 100 | — | — | ns | |
| Clock rise/fall time | $f_{CT}$ | CL1, CL2 | — | — | 50 | ns | |

Notes: 1. Set-up time from the fall of CL2 to that of CL1.
2. Set-up time from the fall CL1 to that of CL2.
3. Test terminal



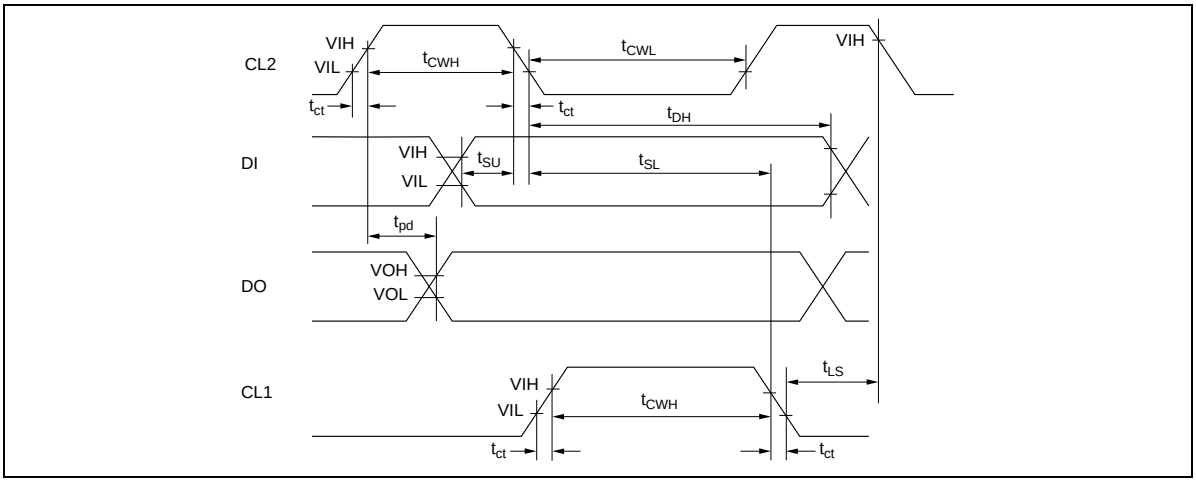




**Figure 8 Timing Chart of HD66100F**

## Typical Applications

### Connection with the LCD Controller HD44780

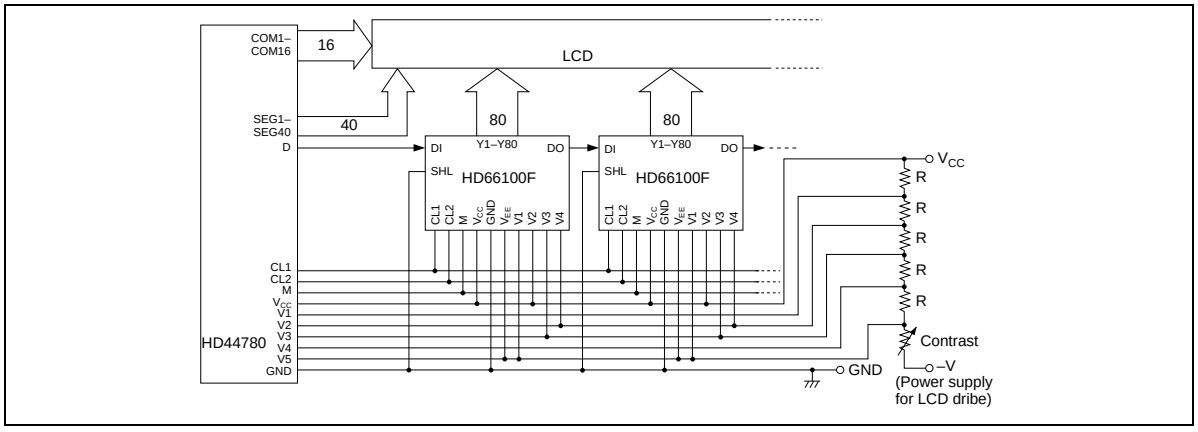



**Figure 9 Example of Connection (1/16 Duty Cycle, 1/5 Bias)**

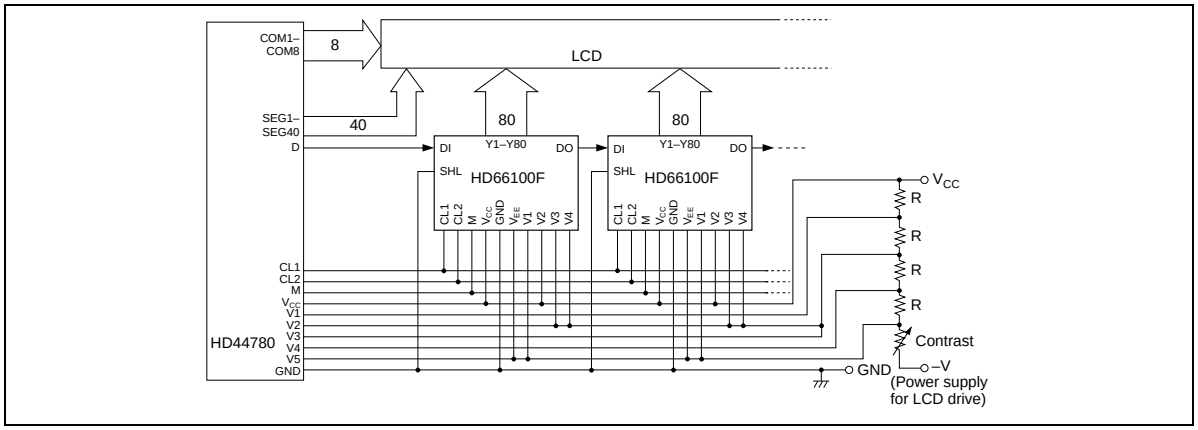



**Figure 10 Example of Connection (1/8 Duty Cycle, 1/4 Bias)**

**Connection with LCD III (HD44790)**

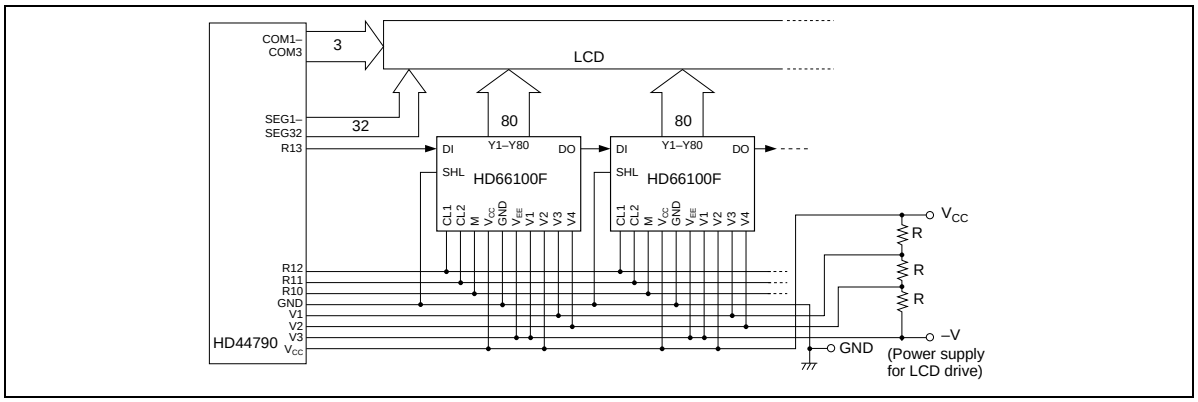



**Figure 11 Example of Connection (1/3 Duty Cycle, 1/3 Bias)**

**Static Drive**

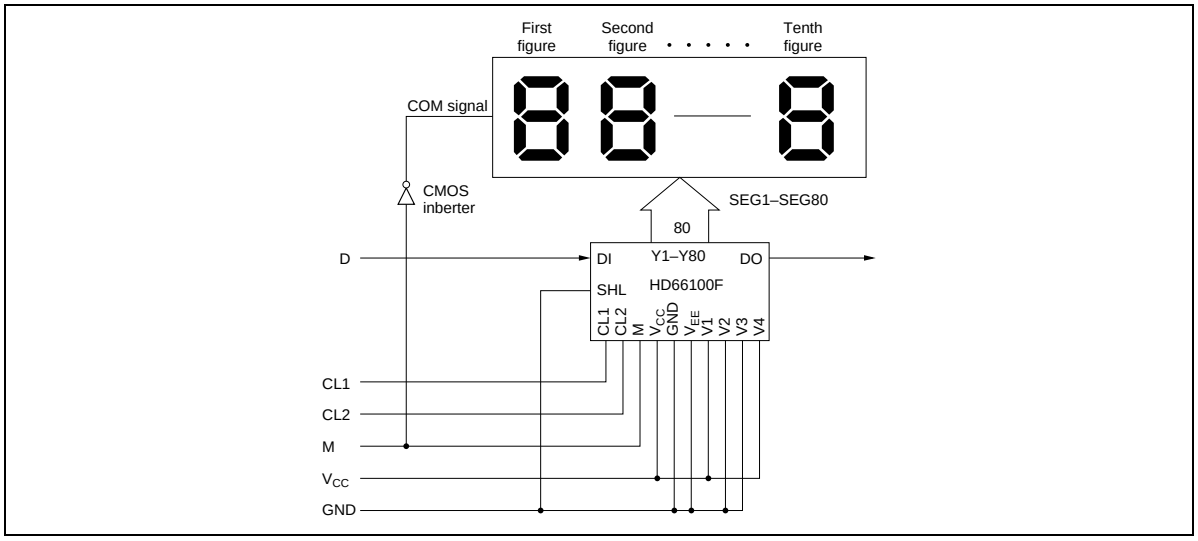



**Figure 12 Example of Connection (80–Segment Display)**

**Timing Chart of Input Waveforms**

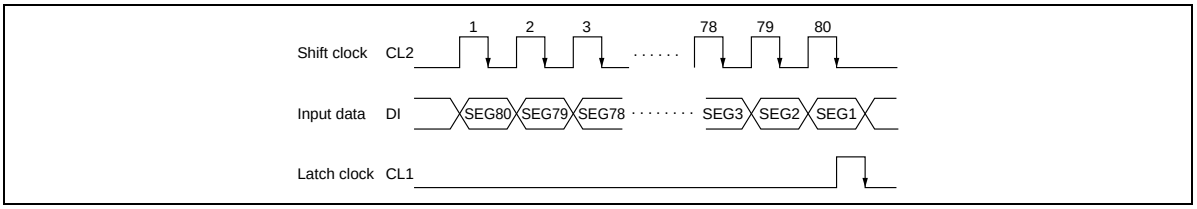



**Figure 13 Timing Chart of Input Waveforms**

Notes: 1. Input square waves of 50% duty cycle (about 30–500 Hz) to M. The frequency depends on the specifications of LCD panels.

2. The drive waveforms corresponding to the new displayed data are output at the fall of CL1. Therefore, when the alternating signal M and CL1 do not fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g. display of hours, minutes, and seconds of a clock). To avoid this, make CL1 fall synchronously with the one edge of M.

3. In this example, the CMOS inverter is used as a COM signal driver in consideration of the large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)

   Usually, one of the HD66100F outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.

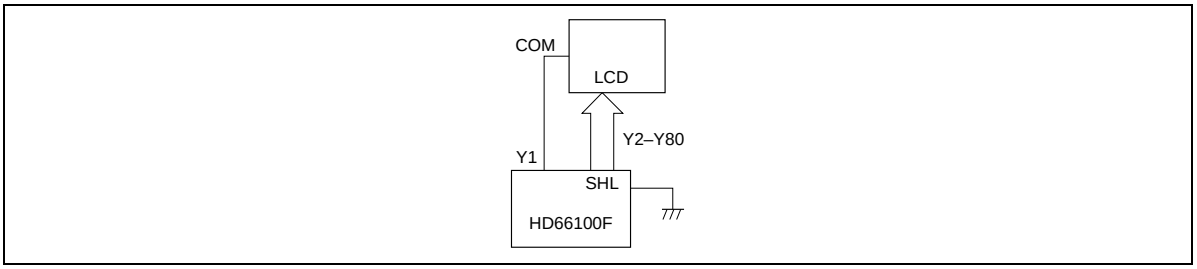



**Figure 14 Example of Connection**

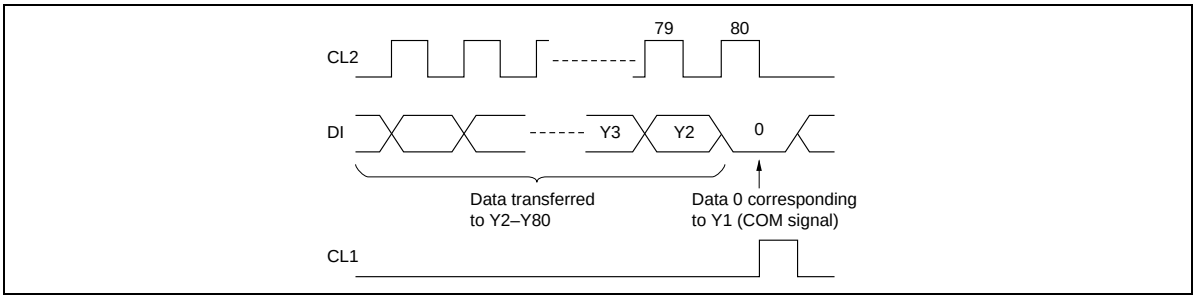



**Figure 15 Timing Chart (when Y1 is Used as a COM Signal)**