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Microcontroller

EMC Design Guidelines for Microcontroller Board Layout

Microcontrollers

Infineon technologies

Never stop thinking.

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all	General update

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1 Overview

The topic of electromagnetic compatibility is important for the functionality and security of electronic devices. Today's designers have to deal with permanently increasing system frequencies, changing power limits, high density layouts by more complex systems and the steady need of low manufacturing cost. Therefore it is necessary to look after EMC.

In this EMC design guideline we are concentrating on some rules, examples, simulations and measurements for printed circuit board (PCB) layout. By using these rules, it is possible to prevent high electromagnetic emission already through a good PCB design. This design guide is made for various applications with their different purpose. Therefore, each application will show different reaction on the realised EMC design improvements. The rules are faced mainly to the problem of electromagnetic emission (EME). Due to the fact that an EME optimised board layout is not so sensitive to interference, using these rules will also decrease the susceptibility (EMS). This guideline is structured in order to fit the needs of a PCB designer. Basics, PCB considerations, design measures, board stack and trace design are followed by various rules for decoupling.

Electromagnetic Compatibility is the quality of a subsystem or circuit to not affect or become not affected in the system where it is used. It has to be seen, that measures to realise a good EMC-behaviour of an application have to be started and implemented already into the first steps of development. In other words, EMC measures have to be considered as a system or circuit specification. Measures and actions taken later on, at an already manufactured printed-circuit board (PCB), are not as effective and additionally will lead to higher costs.

Electromagnetic disturbance is the interference to the normal function of an electric circuit, by coupling in an additional voltage. There are various paths to couple into a circuit and various ways to avoid these interferences.

The EM disturbance needs three steps:

The source: This is the place where the noise or disturbance is created. Reason for this can be e.g. switching noise of a circuit with high current (high di/dt), fast signals, fast rise time, resonance, antenna structures, wrong termination, reflections and electric potential differences. **Major goal must be the RF noise suppression at the source.**

The coupling path: The path or medium where the disturbance is distributed from the 'source' to the 'victim'. **Goal: the 'coupling path' has to be made inefficient.**

The victim: The electrical circuit which becomes influenced by the disturbance coming from the 'source'. This disturbance can lead to some imperceptible noise added on a

signal. But this disturbance can also have some major impact on the functionality of a signal or the whole application.

Goal: Low susceptibility to emission at the 'victim'.

At all three steps it is possible to damp or even eliminate the electromagnetic disturbance by various measures.

1.1 Noise Sources

This is the place where the noise or disturbance is created. There are a lot of sources which can cause RF noise. The most important sources are microcontrollers, oscillator circuits, digital IC´s, switching regulators, ESD, transmitters and the lightning.

Major goal must be the RF noise suppression at the source.

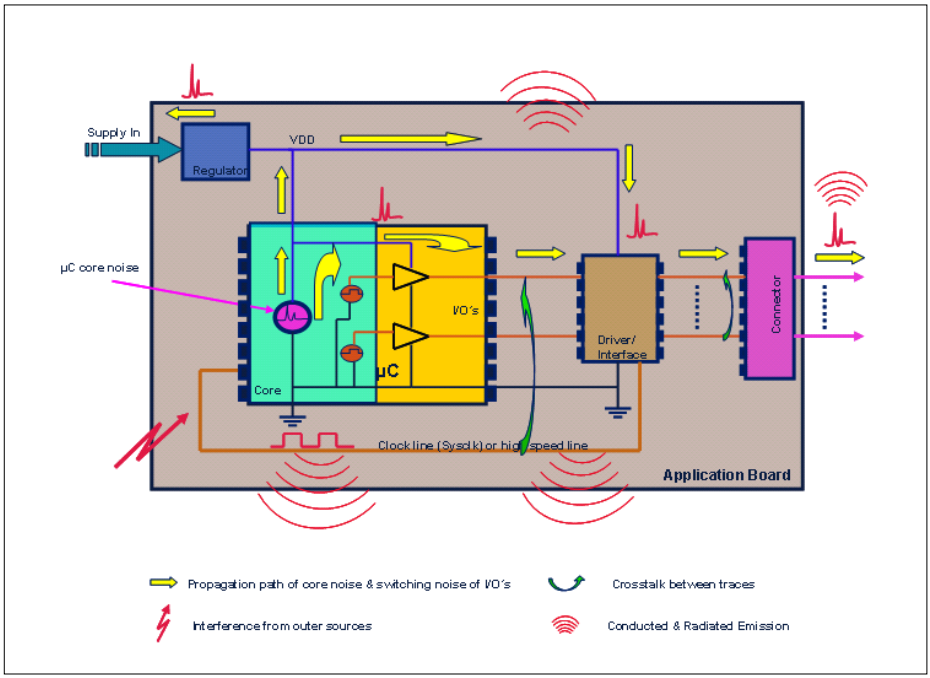


Figure 1 Typical application board and Noise Source paths

From the sight of the PCB design is the most common radiation can be caused from the supply network due to the switching noise of the core activity and toggling I/O ports

of the microcontrollers or other ICs which have driving I/O ports. Generally the drivers outputs are connected to long traces on the board, which are also connected to the cables. These cables are running to the other system components. The nature of the traces and cables are very close to the antenna behavior and the radiation of the energy through these antennas can cause very serious problems. The emission (radiated and conducted) of the switching noise through the power pins and the connected planes are a significant portion of the EMC behavior of the microcontrollers. The capacitive and inductive coupling between the neighbour traces can provide a path to distribute the noise on the board.

The oscillator circuits are producing a trapezoid wave which have a fundamental frequency and harmonics. If a careful placement of the board is not realized, then a coupling to the nearest components and traces is probable.

In digital systems the radiation behavior of a switching circuit depends of the form of the digital signal. As it can be seen in figure 2, the emission spectrum is related to the duty cycle and rise/fall times of the switching signals. The high time determines the point where the spectrum begins to fall with 20 dB/decade, and rise time gives the second point where it begins to fall with 40 dB/decade.

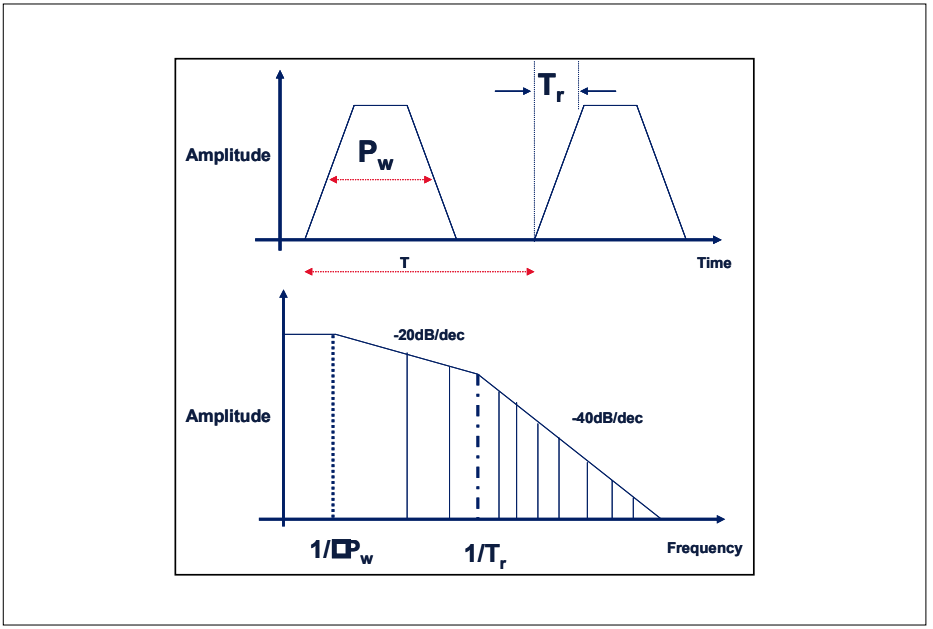


Figure 2 Spectrum of a trapezoidal signal

Next figure 3 shows calculation results, which depict the spectrum of a periodic pulse for different pulse widths and changes in spectrum. The magnitude in spectrum increases as the pulse width increases.

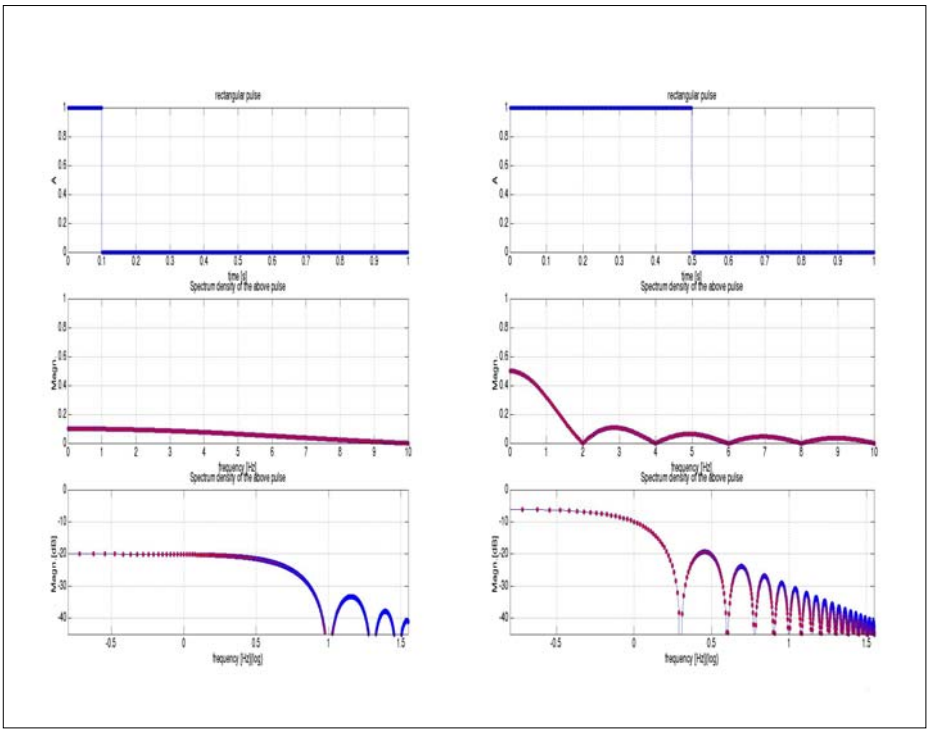


Figure 3 Relation of spectrum and pulse width

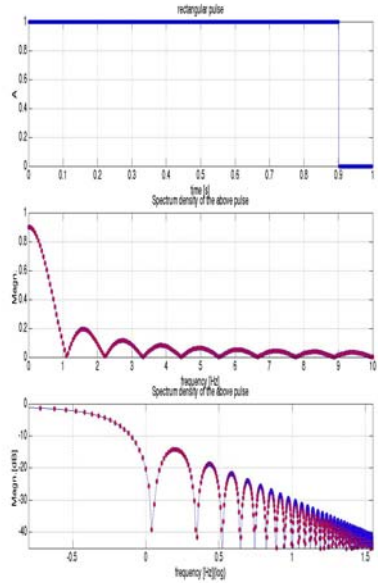


Figure 3 Relation of spectrum and pulse width (continued)

For the high speed design of the PCBs, it is important to decide how to handle the traces if they carry high speed signals and under which circumstances the line length is critical. Generally we can say, if the one half rise/fall time of the signal is smaller than the propagation delay of the PCB trace, the trace should be treated as transmission line and should be routed with additional measures and terminated with its characteristic impedance (see also Chapter “3.2.1. Layout Structures”).

Next important point is the design of the integrated circuits. Most of the designs of the microcontrollers are synchronous clock systems, which cause some EMC problems on the power supply network of the ICs due to the synchronous construction of the logic circuits. A careful design of the IC´s power supply network is also required.

1.2 Coupling Paths

The path or medium where the noise is distributed from the 'source' to the 'victim'. **The goal is to make 'the coupling path' inefficient.** The coupling can be effective in two ways: Radiated and Conducted.

The radiated coupling paths are electromagnetic fields and crosstalk (inductive or capacitive). The radiation path of the signals less then 30MHz are conducted and for the signals above the 30MHz the noise will radiate.

The conducted coupling paths are galvanic coupling, supply network (power & ground). Interference current and voltage of an electrical system can be described as common-mode (CM) or differential-mode (DM).

Common-mode: interference is an asymmetrical disturbance. It often occurs between a cable system and their electrical reference potential. Signal and noise current have the same (a common) direction in the loop. The cables radiate the energy caused by the ground system noise. The common-mode radiation can be reduced by reducing the impedance of the ground system.

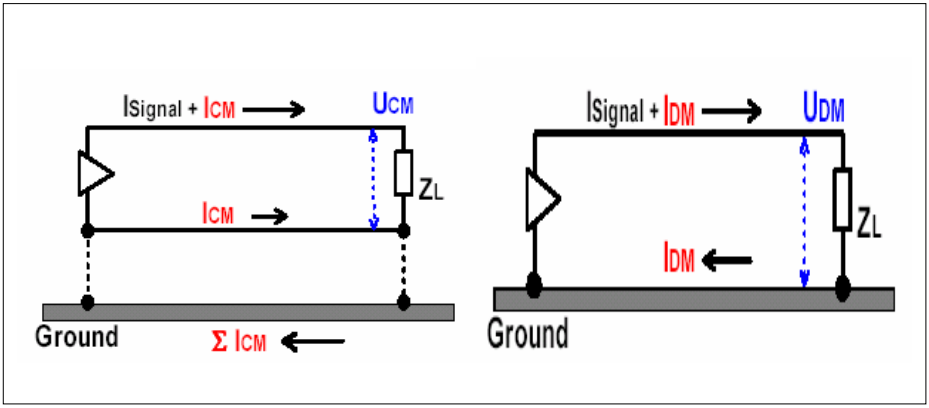


Figure 4 Common Mode and Differential Mode

Differential-mode: interference is a symmetrical disturbance which occurs between two traces or lines. One of these lines can also be the ground path. Signal and noise current have a different direction in the electrical loop. If the loop area of the signal and return path increases then the differential-mode radiation is also increasing.

Switching of a signal produces a current transition , that goes through the trace, receiving device and returns over the power system (VDD or VSS) to the transmitting device. This path builds a current loop.

The current loops have inductance and can be modeled as a coil of a transformer. The inductance of the loop depends on the loop size and increases with it. Usually on a PCB there are many such loops, which interact with eachother. As Figure 5 depicts, if any changes occure in loop current A it induce a proportional voltage in loop B, because a part of the total flux from loop A goes through the loop B and induces the voltage v(t). To minimize the inductive coupling between the loops, the loop inductance has to be reduced. This can be done with reducing the loop size. Using power planes gives a very low impedance connection possibility for VDD and VSS power bus.

Due to the fact, that the low frequency signals follow the least resistance path and the high frequency signals follow the least impedance path, the signal return paths have to be designed so that the loop inductance is as low as possible. In case of the power plane design, the power plane must show no break or discontinuity in the signal return path, so that least impedance path can be used.

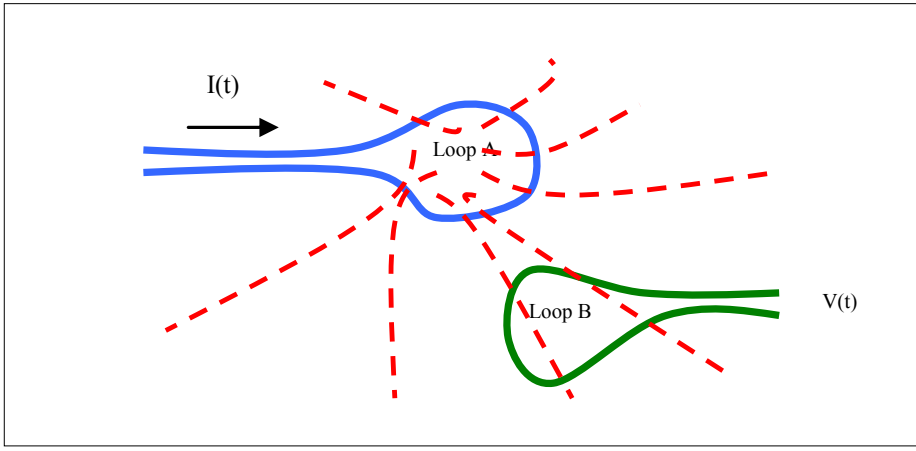


Figure 5 Interaction of two loops

Crosstalk is the coupling between two adjacent traces. The crosstalk effectiveness depends on two parameters : capacitance and inductance between adjacent traces.

In case of the inductive crosstalk, both of the traces form a loop which act like the two windings of a transformer. The loops are the traces on the PCB with their signal and return path. The distance and loop area determine the crosstalk. To reduce the inductive crosstalk the loop area should be reduced.

The circuit in Figure 6 shows two adjacent traces, one trace acting as source and one trace acting as receiver. Because of the capacitance between the lines, the noise

generated by the source can couple to the other trace. The noise generates a current which is coupled through the capacitance to the next signal line.

The dV/dt of a signal source produces a current depending on the coupling capacitance between the two traces.

$$I = C\frac{dV}{dt}$$

The di/dt of a signal source produce a voltage depending on the mutual inductance between the two loops.

$$V = L\frac{di}{dt}$$

The capacitive crosstalk can be reduced by separating the traces/loops. More distance between traces leads to less crosstalk. But in many applications is the PCB area is limited so that a separation of the traces is not always possible. In this case the placement of a guard trace between the traces can help. The guard trace can be an approach for two layer boards, but for the multilayer boards is the benefit not so high because of the ability to place a solid ground plane into the PCB. The most effective measure is the proper termination of the signal lines.

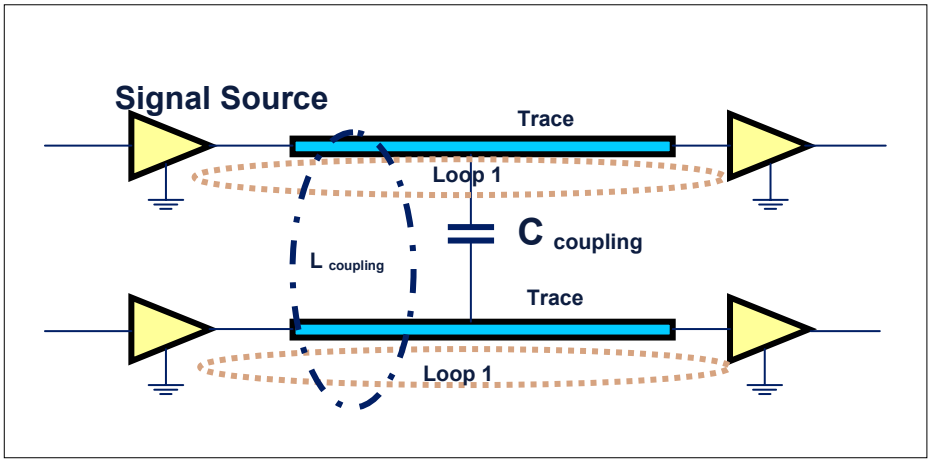


Figure 6 Capacitive and Inductive Coupling

2 PCB Considerations

A good EMC optimized PCB design includes three design stages; component selection/placement, design of the grounding concept (power supply system) and decoupling concept. Before the placement, the critical paths and circuits have to be identified, so that a functional grouping can be made. The analog circuits should be isolated from the source of noisy signals. The high speed ground and analog ground must be sparated from each other. The ground areas of different circuits should not overlap.

For reason of EMS and signal integrity, external logic with high input threshold (Vih) should be choosen. E.g. prefer HC (High Speed CMOS) or AC (Advanced CMOS) standard IC's due to higher Vih. Select optimum (i.e. not unnecessarily fast) rise-/fall times to decrease di/dt noise. Use the criterion of low cross currents for the selection of other ICs.

Supply Voltage

When a higher supply voltage is used, more power is inside the electrical system. That involves, that a higher voltage fluctuation happens and therefore a higher emission will be created. That means, for the reason of electromagnetic emission, use the lowest possible supply voltage. If susceptibility is a matter of concern, the supply voltage level should not be too low. A low voltage level implies a small signal-to-noise ratio.

Oscillator

Use lowest speed for oscillator and crystal. Adjust to the demands of the application hardware and software. Use PLL for higher frequencies. An isolated ground plane under the oscillator circuit can be used to reduce the propagation of the clock noise to the board. This ground isle should be connected (high impedant) at one point to the board ground.

Attaching Cables to a PCB

Group connectors by function. E.g. separate analogue cables from high speed signals. Provide decoupling measures (capacitors, ferrites, optical systems, etc.). Note: Do not let any noise go from the PCB on the cables since this increases emission dramatically. Do not let any noise go from the cables to the PCB since this may cause functional instabilities.

Provide enough GND pins for a cable transferring critical signals. Avoid cables if possible. If they are necessary, make them as short as possible. Fix them so they will not move - otherwise their EMC behaviour is unpredictable.

Twist power or signal cables with the corresponding GND cable. Thus, the flow of current and the back current will be close together. Both electromagnetic fields will neutralise each other.

Two-Layer / Multilayer Boards

The multilayer boards provide many advantages compared to two-layer boards in related EMC behavior. But in some cases two layer boards are prefered because of their low costs. Multilayer boards cost more then two-layer boards.

With multilayer boards it is possible to design low impedance power supply and ground connections using power/gnd planes, which covers one layer or a part of one layer. Realizing EMC related measures is easier with a multilayer board as with a two-layer board.

Traces

In high speed designs the reference (ground) for the traces is very important. The design of the trace can effect the emission and/or signal integrity behavior of the trace. Two types of traces can be used: microstrip and stripline (more information in 3.2.1. Layout structures , Figure 43). The stripline has the reference plane on both sides which results in lower impedance than with the microstrip.

To avoid EMC disturbances of adjacent traces, try to keep the distance between sensitive traces as big as possible. For high speed signals even guard traces might be necessary. That means, that between two signal traces a ground trace should be designed.

In general, sensitive traces should not be designed in parallel to high speed or noisy traces. If you cannot avoid such a design, make the parallel paths as short as possible.

Vias

For reason of EMC it can be of advantage to use different kinds of vias on a high speed signal application.

Microvias: They have a hole diameter from about 100µm and can be designed into the pads of discrete components. Because of the small diameter much space can be saved on the PCB and therefore the power plane structures are not cut as much as by bigger vias. Because of the same reasons, multiple microvias can be designed instead of one big via. That lowers the inductance of the connection since one can calculate it like inductors in parallel.

Buried vias: This kind of via can be used at a multilayer design. They are connecting some signals or power traces at the inner layers of the PCB (e.g. from the 3^{th} to the 4^{th} layer) . They are not drilled from top- to bottom layer but just through the inner layers. With buried vias, some layers of a multilayer board can be made high-frequency sealed, while not cutting the outer planes. Additionally to that, space for trace design can be spared.

Blind vias: They are drilled from an outer layer to one of the inner layers. Because of that, not all layers of a PCB are cut for a signal or power trace connection with the first or last few layers. Blind vias are most efficient if used in combination with 'buried vias'.

High impedance traces

By using traces with higher impedance (smaller or narrower traces), disturbances can be kept local. (E.g. traces to the voltage regulator)

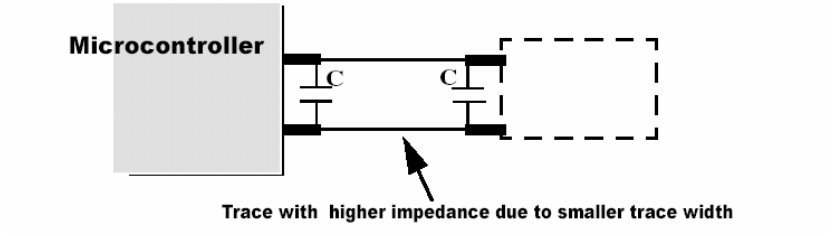


Figure 7 High Impedance Traces

Package

For packages of BGA type, most Vss pins are grouped in the center of the controller. In general the corresponding Vdd pins are located on the inner row of the outer circle. This pinning allows a short connection to the decoupling capacitors, when placed on the opposite side of the PCB. For normal flat packages the decap can be placed between VDD and GND. The connection to the supply and ground has to be made by vias placed on opposite side of the trace to the IC.

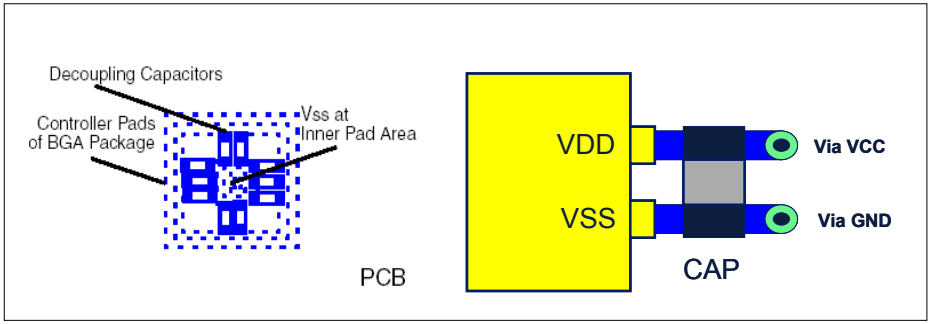


Figure 8 Decoupling of a typical BGA package

PCB Material

The dielectric permittivity 'ε_r' is an important parameter for calculating the wave impedance of a trace or a plane. For the PCB material this constant, at the frequency of 1MHz, can be provided from the board manufacturer. For fast signals it has to be considered that the dielectric permittivity is frequency dependent. (E.g. The material 'FR4' has a ε_r at 1kHz = 4,7 ; At 1MHz = 4,5 ; At 16MHz = 4,35).

In high-speed systems above 4GHz it is recommended to use other materials than the typical 'FR4'. This can be e.g. Teflon or 'BT'-material.

The effect of the dielectric permittivity ε_r on the PCB impedance is shown by a simulation with different ε_r boards (ε_r = 4, 10, 100). For the simulation a board with 10X10 cm dimensions and a PCB thickness of 20mil was used. Figure 9 shows that if the ε_r value increases, the impedance of the board will be lower. The resonance frequency is shifting to the higher frequencies with the lower ε_r value.

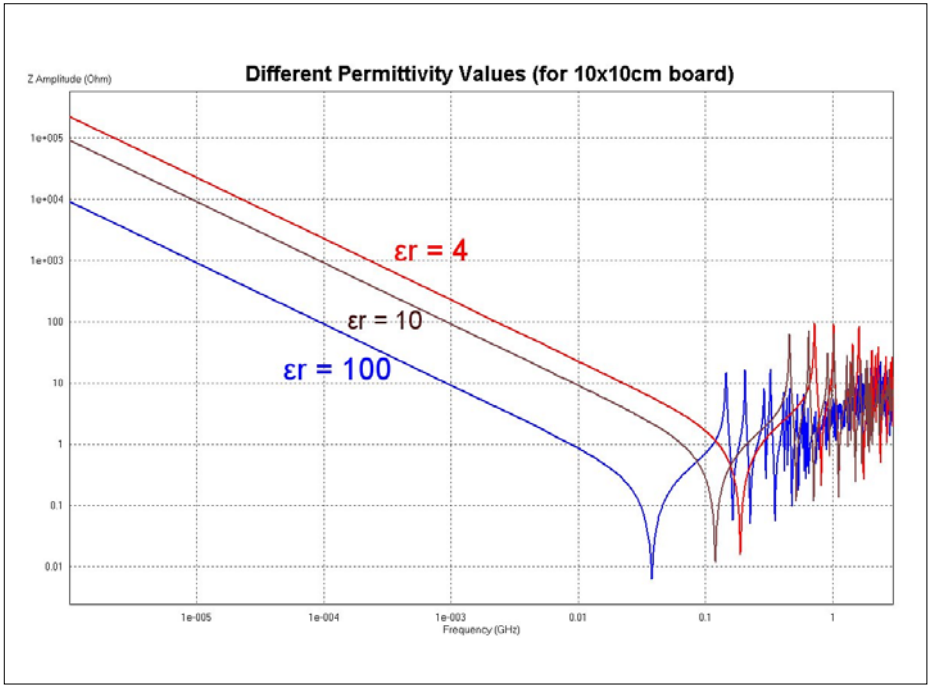


Figure 9 Impedance of PCB for different ε_r values

3 Design Measures

The following guidelines are recommended, however each measure described here must be evaluated for each application. The realisation of all measures can be very difficult, particularly in complex applications, so that a trade off has to be made.

For more complex structures it is not possible to determine general design rules. These structures have to be handled by SPICE simulation in conjunction with 2D- or 3D-Field Solver for establishing design rules.

General design recommandations :

- Define functional units. Classify also by speed: Analogue sensor, digital low speed, digital high speed, power elements. Place all components working with same clock together.
- Keep elements of same functional unit in close distance to keep critical signal traces as short as possible. Provide enough space for decoupling capacitors close to the IC and spread over the whole PCB.
- High speed traces should be placed near the center of the board far from the edge of the board.
- Keep the lead length of the decoupling capacitors as short as possible and locate the capacitors as close as possible to the VCC pin of the component.
- Before beginning the routing, identify critical signals according to highest carrying frequency and shortest rise/fall time of the signal.
- Place high current carrying lines as close as possible to the voltage regulator´s output.
- Provide connections for series resistors within high speed traces close to the driver. But take care that the signal timing will still meet the specification.
- Place oscillators adjacent to the clock driver. If an asymmetrical board stack design is used, place the crystal oscillator on the side of the PCB which has the largest distance from the reference ground layer. This can prevent a direct coupling from the crystal oscillator package into the ground system of the PCB. To reduce the radiation / coupling from oscillator circuit, a separated ground isle on the GND layer should be made. This ground isle can be connected at one point to the GND layer. This helps to keep noise generated by oscillator circuit locally on this separated isle. The ground connections of the load capacitors and oscillator should also be connected to this isle.
- For two layer boards: Keep a “distance” between functional units by geometry (see figures 19 and 20).
- Separate parallel running traces by not less than 2x trace widths.
- The changing of the layers changes also the the impedance, which causes reflections at these points.
- Remove 20*H of metal from edge of VCC supply plane to reduce edge radiation. H is board layer height or thickness (figure 10).

- Place I/O connectors carrying external signals on one edge of the PCB.
- Prefer manuall routing to the auto router of the layout tools for critical signals.
- Do not place the connectors close to high speed circuits.
- Place crystals, oscillators and clock generators away from I/O ports and board edges.

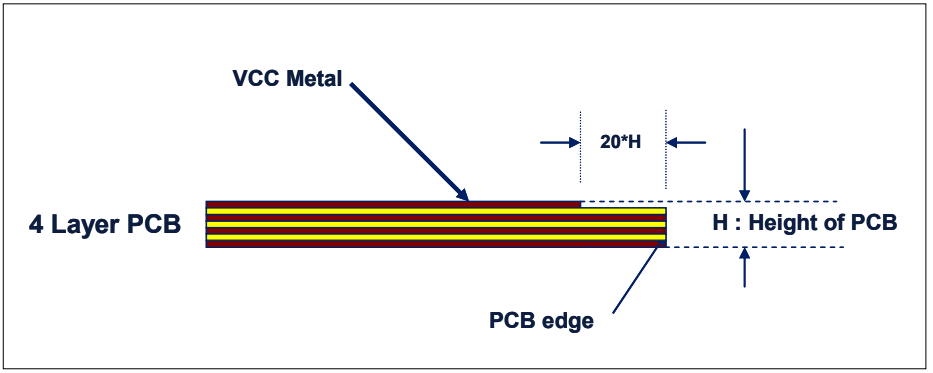


Figure 10 Removing metal of power plane from the edge of PCB (20*H-method)

3.1 Power Supply

In the first step of the PCB layout, the power supply system should be designed. A proper power bus and grounding design is the basic requirement for voltage stability and reduced electromagnetic emission. Decide for PCB technology: two layers or multilayer board layers. For the multilayer boards a proper stack-up of the PCB should be designed (See also part 3.1.1.2. Multilayer Boards).

Note: Concerning EMC, a good design of two layer boards is more difficult to realise than four or more layer boards.

Depending on the PCB technology, different grounding systems can be used. For the power systems, the mostly used distribution method is single or star connection type (see also 3.1.1.1. Two Layer Boards). But in high speed systems the star grounding is not the best solution. Because of the high frequency path of the noise, an increase in radiation can be the result.

In case of multilayer PCB, the use of power layers is a good solution. Covering one layer with metal provides much less impedance for the connection to the decoupling components.

Voltage regulator: Canalising of HF Current

To heat transformed or otherwise canalised energy cannot radiate anymore. See an example to position capacitors to isolate and disturb reflected (high frequency) energy. In fact, the high frequency current is created inside the IC. By using blocking capacitors, this HF energy will not leave the circuit via this supply line. But be aware, that energy can couple out via other paths which are connected to the µC.

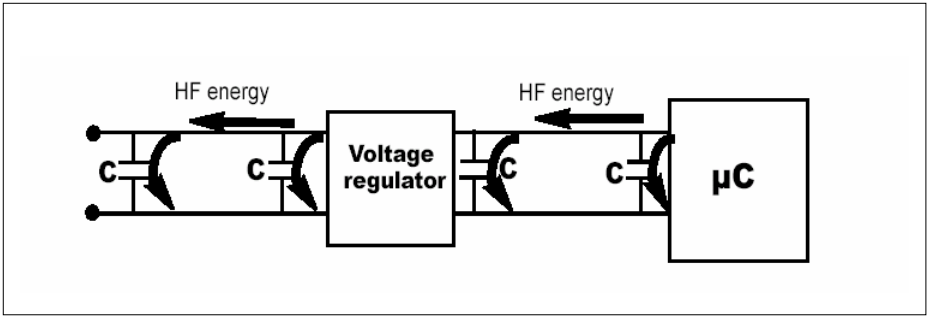


Figure 11 Flow of the Canalised Energy

Separate the digital and the analogue supply system. Use at the output of the voltage regulator decoupling capacitors and inductors to reduce the noise propagated over the powerlines. For the decoupling at the supply level, tantalum capacitors are prefered.

Since supply systems themselves have their parallel resonance frequency it has to be thought about shifting this resonance out of the range of critical frequencies.This can be done by shortening the length of the supply trace. In a normal PCB that is not always possible, since board geometries are given from the application functionality. In this case a capacitor in the range of 100nF can be implemented into the current path. This has the effect of shifting the electrical length of the system with the resulting parallel resonance frequency becoming higher.

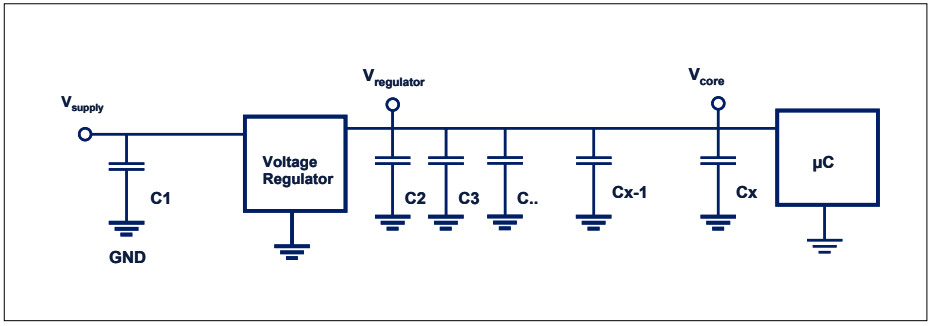


Figure 12 Decoupling of the Power Circuit

3.1.1 Layout Structures

Keep power and ground nets (which belong to each other) close together in order to reduce impedance. The GND trace should be as close to the VDD trace as possible. Best choice is to design them in parallel. If the current and the corresponding ground trace have to go different ways, there will be different potentials and common mode problems. Figure 13 shows GND-trace and VDD-trace on different sides of the PCB.

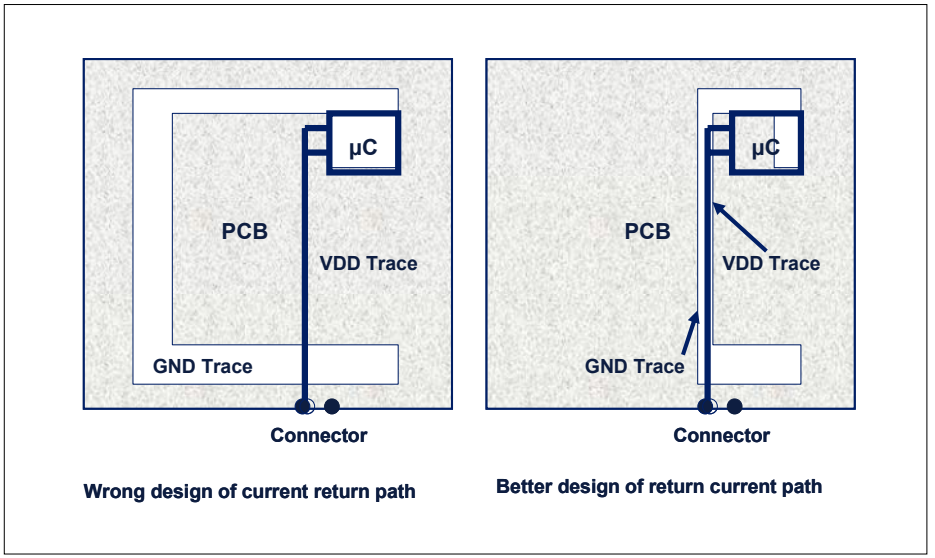


Figure 13 Design of Ground Traces

In general, power and ground traces should lead directly from the supply connector to each component / functional unit. If possible, use one side as a complete ground plane for an optimised current flow. Ground area fills have to be handled with care. Otherwise emission may increase, because of resonance structures and antenna effects. Connect them by several vias or wide traces to the reference ground of the board. Since there are various effects which influence the radiation and susceptibility of the PCB, each application has to be handled specially.

Signal currents use both power plane and ground plane as return path. Keep supply planes as “clean” as possible: Avoid areas of high impedance (groups of vias, gaps). Avoid segments in the ground planes. This measure keeps the current return path short. The supply planes should also be as small as possible to reduce the coupling/radiation of the noise to the power system and it should use enough area to deliver power to all the components which are connected to power system.

Example for placements of vias are shown in figure 14. In the upper-left case the return current is forced to flow around the group of vias. In the upper-right case the current can flow nearly directly from one side to the other. The best solution for a current return path is shown in the lower-left configuration.

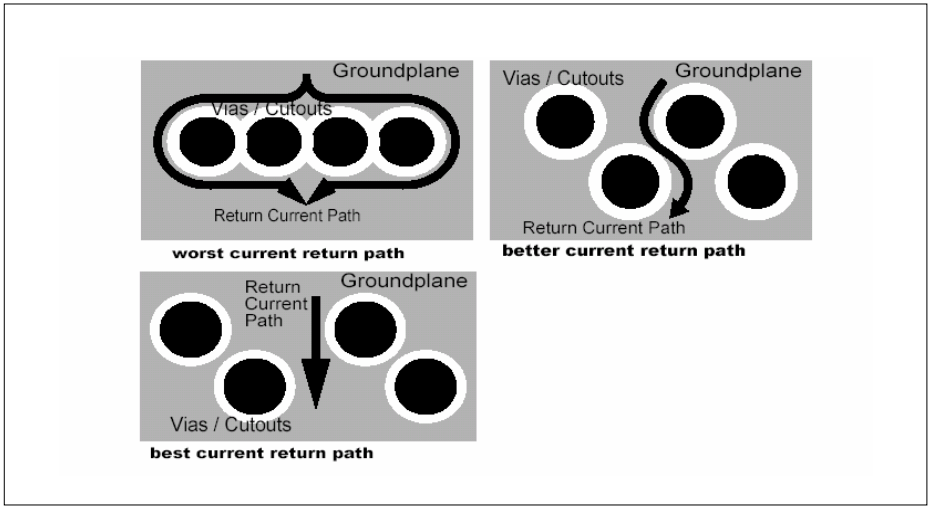


Figure 14 No Blocking of Current Return Path

In some cases, splitting power or ground planes can bring a big improvement to the EMC behaviour and for signal integrity. This splitting has to be done under several considerations of the signal and current flow. A separation of very sensitive parts from

noisy areas of a PCB keeps the disturbance low and minimises the possibility of galvanic coupling. If the VDD plane is to be divided into segments, provide one area for every functional unit. These zones (if they have the same supply) should be still connected together. That influences the way and the impedance of the current flow. For the ground plane a path with low impedance has to be guaranteed. The separated zones should be connected together again at a common supply starpoint, which should be close to the power supply connector or voltage regulator on the PCB.

A functional unit can contain all RF-components, all analogue components, etc. Another way of building functional units is to distinguish by supply voltage (5.0V, 2.5V, etc.)

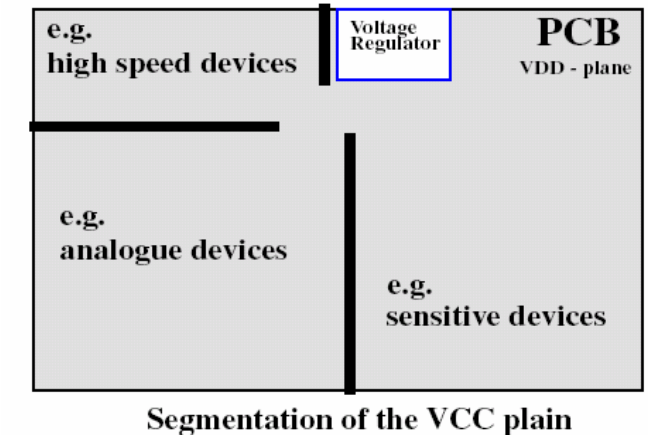


Figure 15 Example: Segmentation of the Supply Plane with Voltage Regulator as Common 'Supply Star-Point'.

Resonances of the board structures influence the EMC behaviour in a direct way. If the harmonics of the work frequencies have the same frequency as the parallel resonances, a significant high amplitude can be produced. These harmonics can then couple to the other supply paths and traces. The board structures should be selected so that no parallel resonances are in the interested range. As it can be seen in the simulations results in Figure 17 the smaller the board structures the higher is the resonances. These parallel resonance frequencies can be seen on the emission spectra and can be critical for signal integrity.

Since board resonance is mainly caused between two planes, one option is to realise the VDD power by traces (i.e. power-star point, separate traces for different board sections, distance to ground plane).

Traces have a higher impedance compared to a plane structure. Using VDD traces, local disturbances on the PCB can be prevented from spreading over the whole board. To provide the necessary current potential for switching operations, locally decoupled 'power islands' should be realised directly underneath the microcontroller and logic devices. From these islands the noise has a path of high impedance to other devices and will be kept locally.

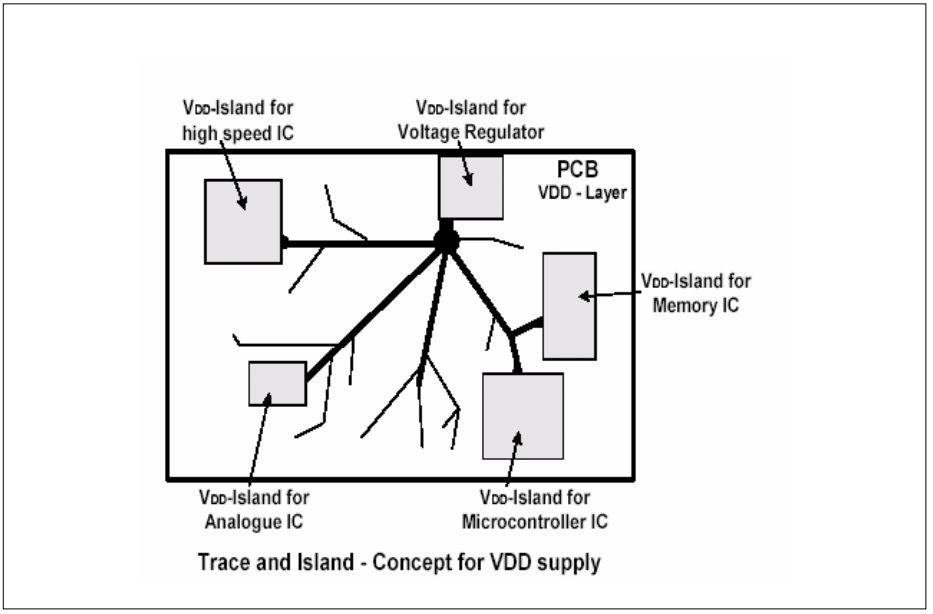


Figure 16 Example: Using VDD Islands and Traces over Ground Plane.

The capacitance and inductance of the planes cause a resonance in high frequencies depending on their values.

In some high-speed applications, the power plane capacitance can be used as a distributed capacitance to reach an attenuation of the total impedance of the power network on the PCB in high frequency range. In this case it is important to calculate the impedance and determine the dimension of the power plane to reach an adequate decoupling effect. The capacitance of a plane structure depends on the board thickness, dimensions and dielectric permittivity of the board.

Figure 17 shows the change in impedance of power planes if the thickness of the board varies and the change of the board impedance if the dimensions of the power plane varies.

The first board resonance shifts to higher frequencies if the plane area gets smaller.

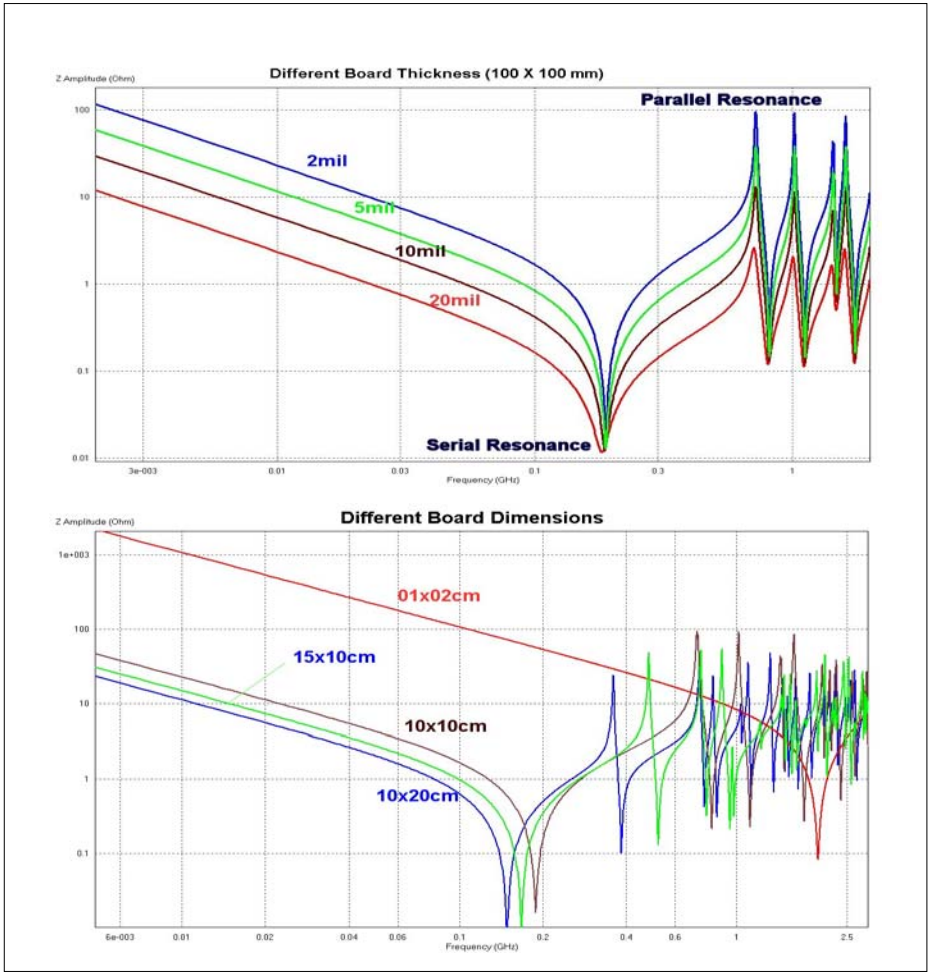


Figure 17 Board impedance for different board thickness and different plane dimension

In some cases the grounds can be separated to reduce propagation of noise. This is possible only in low speed systems. In high speed systems, a cut in the ground plane can affect the high frequency noise path because the high frequency signals require a homogenous ground reference.

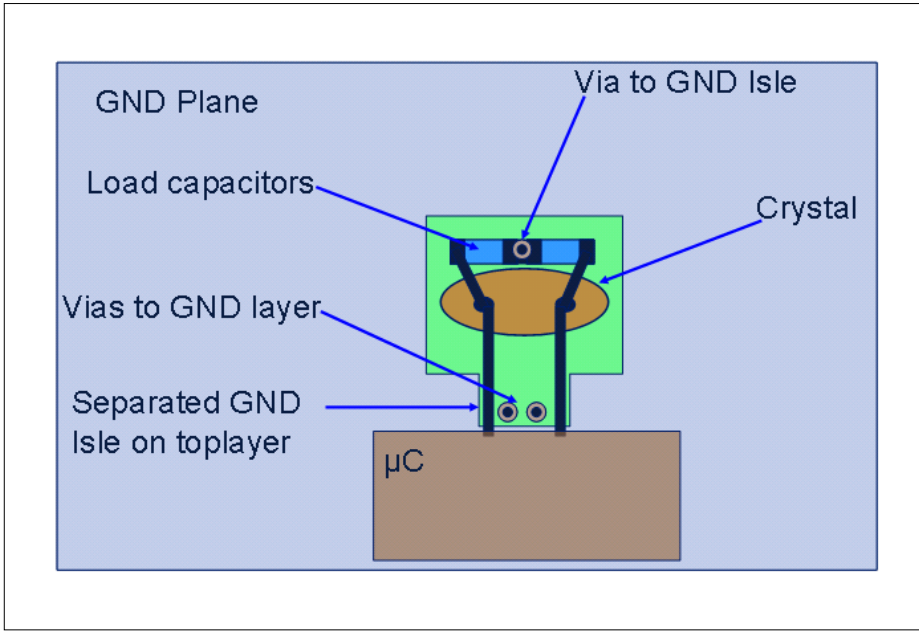


Figure 18 Layout example for Crystal oscillator circuit

3.1.1.1 Two Layer Boards

Each component should have its own power/ground system. It is not easy to realize this in two layer boards. Generally there are two concepts to design a power distribution on two layer boards (see Figure 19).

The power connections over the whole board can be made as star connection. The distribution of the power to each component can be made from the output of the regulator with traces. A power island at the regulator output can be placed to realize the star point. It is also important that all supply traces have ground as reference.

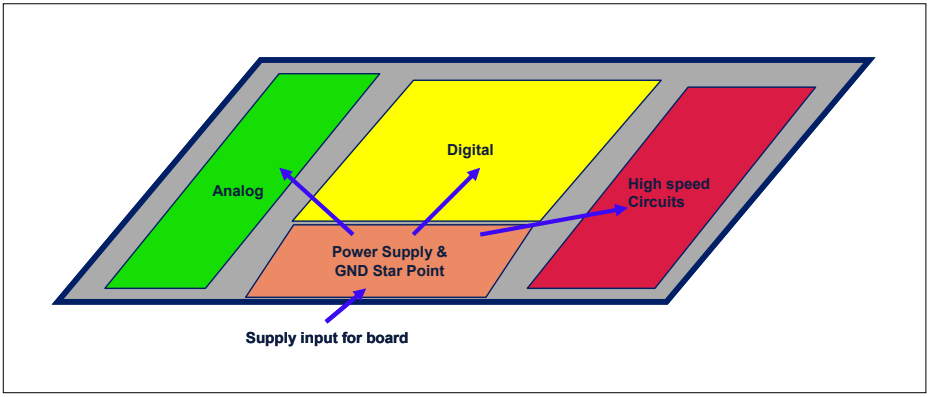


Figure 19 Power / Ground distribution example with star connection system.

Another good solution for the power network in two-layer boards is to build a grid system (see example in Figure 20) with ground and supply nets. The ground and supply nets are routed over the whole board on each layer. The traces of each power system (GND/VDD) on each layer are connected through vias together. With this grid it is possible to provide a low impedant connection of the power system to each point of the board. In general traces on the toplayer of the board are routed in vertical and on bottom layer in horizontal direction so that it will be easy to realize the grid system. But this solution requires a tradeoff with signal traces changing layers which causes impedance changes of the traces.

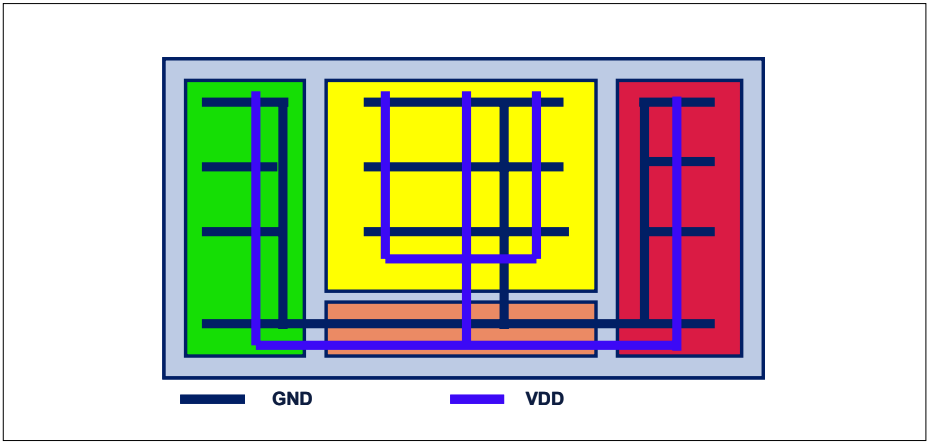


Figure 20 An example for grid power system for the PCB shown in Figure 19

3.1.1.2 Multilayer Boards

For the design of the multilayer board the selection of the construction plan is very important. This construction plan, called stack-up, can be built with the technological data of the manufacturer. It depends also on the requirements of the high speed design. Following some samples of 4-layer and 6-layer board stack-ups are shown.

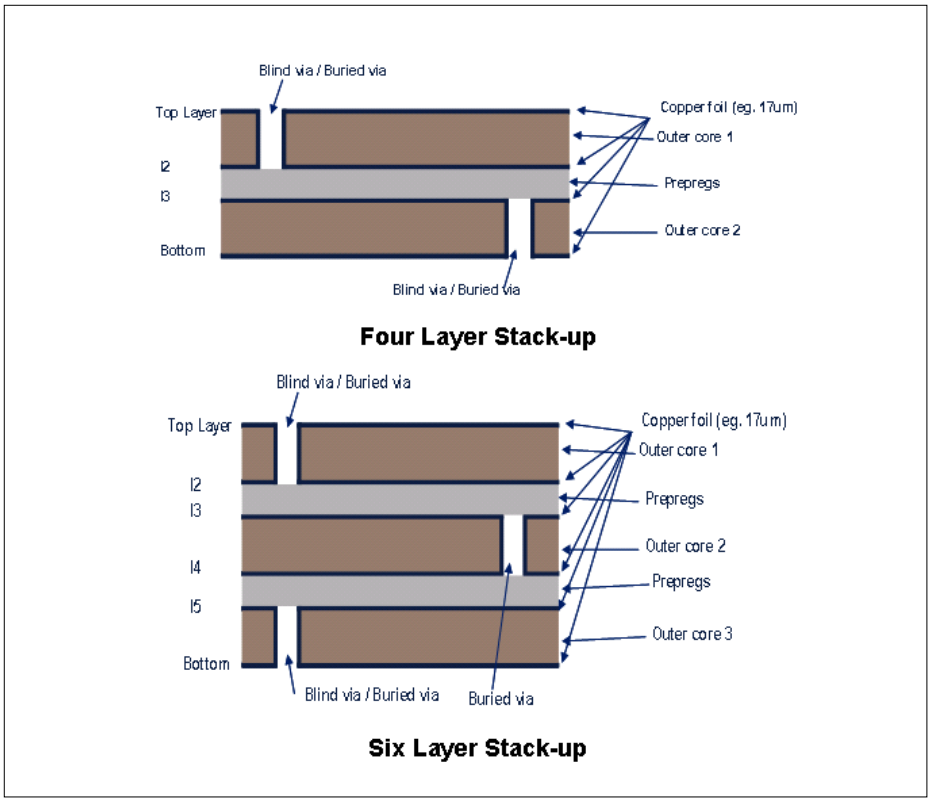


Figure 21 Stack-up examples for four / six layer PCBs

Design at least one power/ground layer-pair. Realize power and ground planes on adjacent layers. The smaller the distance between power and ground layer, the lower becomes the impedance of the power supply. The distance between the layers can be reached with substrate and prepregs with different thicknesses.

Use the shielding effects of supply planes to reduce electromagnetic emission. If you have more than four layers, you may route a signal layer for critical traces between two continuos ground/power layers. That provides a good current return path which is not interfering with other signals. As well, it is effective as a shield against radiation to the outside of the PCB. If there is enough space, implement more extra ground planes in your layer stack, so that each signal layer has its own corresponding ground layer. To have an extra ground plane for a signal layer makes it possible to keep the determined characteristic wave impedance.

Different stack-ups for the VDD and GND layers can also be considered for an EMC optimized board design. The simulation results show a comparison of the effect of three different stack-ups (figure 22), where in first case the signal layer is placed between the VDD/GND layers, in second case the signal layer is placed on toplayer and at third case the signal layer is placed between two GND layers. The current flowing through the decoupling capacitor is displayed in figure 23. The stack-ups, where the signal layer is embedded between the GND/GND or VDD/GND layers delivers best results. But it must be also taken into account that increasing distance between the VDD and GND layers decreases the plane capacitance of the board. The plane capacitance supports the decoupling effect of the board at high frequencies.

Placing noisy signals (clock traces) between two ground layers can prevent a lot of problems.

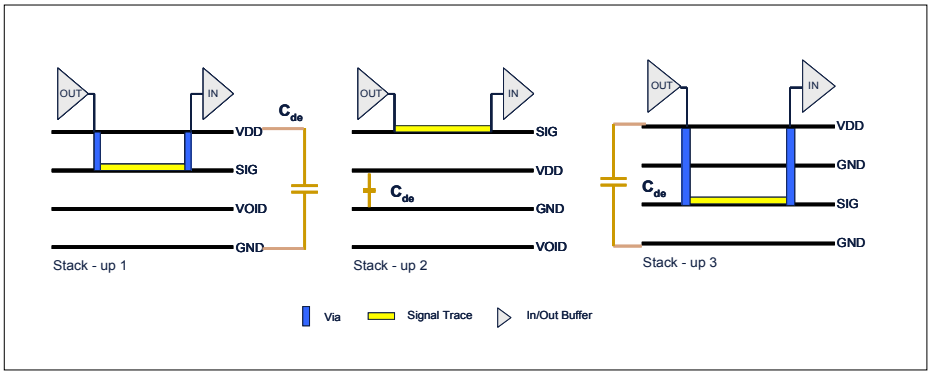


Figure 22 Different stack-ups for reference plane

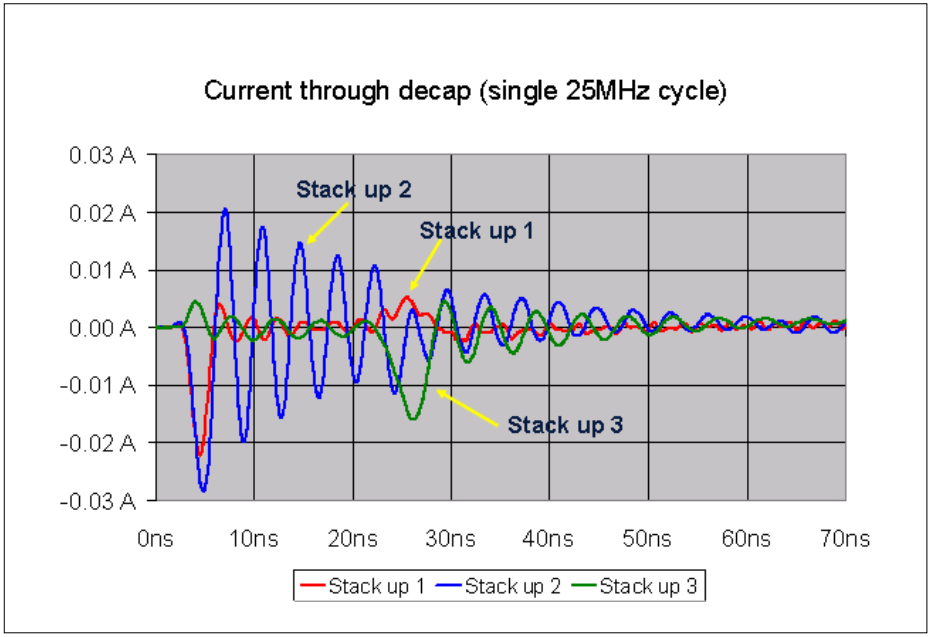


Figure 23 Current through decap for different stack-ups

It is also important to select the right layer for critical signals. Designing critical signals as stripline can reduce the switching noise on the power network (VDD). Figure 24 shows a comparison of noise level on VDD in cases of different layer routing of a signal trace (stripline vs. microstrip). The advantage of a stripline layout can be seen clearly up to 500Mhz. For construction of stripline and microstrip see figure 43.

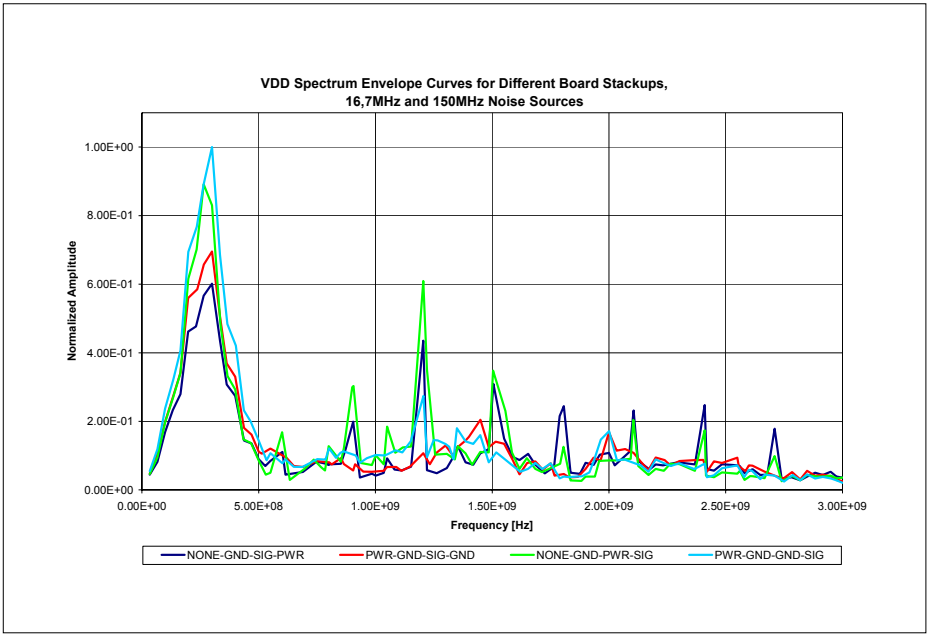


Figure 24 Noise level on power network with different stackup configuration for the signal line.

The connection of the decoupling capacitors is important in the high frequency range. While the connection on two-layer PCB´s are made with traces, on multilayer PCB´s the connection can be made through vias to the VDD/GND layers. Depending on the length and width of the traces can the parasitic inductance takes effect on the impedance and also on the decoupling efficiency. A comparison of the via and trace connection of a decoupling capacitor shows, that a via connection has lower impedance above 400Mhz. Additionally it can be seen that the trace thickness (1mm -> 1.5mm) plays also a role as the impedance decreases with increasing trace thickness.

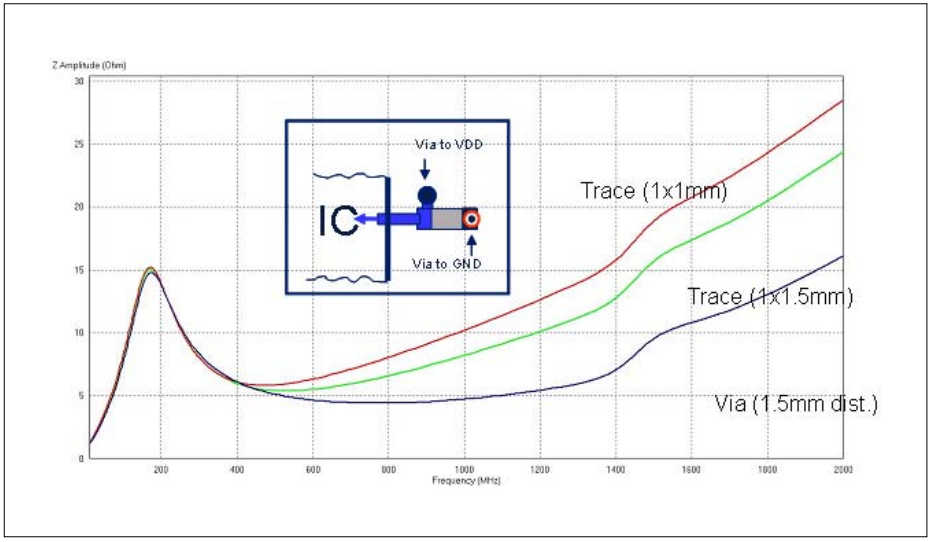


Figure 25 Impedance comparison of different connection types (via- vs. trace-connection of decoupling caps)

3.1.2 Components

Passive components are used to reduce the EMI in circuits. For optimum usage of these components, their behaviour has to be understood.

3.1.2.1 Capacitor

Capacitors are used to deliver required energy locally while circuits are switching. They reduce the power supply radiation loops.

There are two types of common capacitors: Aluminum/Tantalum and Ceramic capacitors.

- Aluminum / Tantalum capacitors: They are used mainly for bulk decoupling at supply lines. The capacitance value decreases with increasing frequency. But Tantalum/Aluminum capacitors have a very stable temperature and bias behavior. For the applications where high values are required, tantalum capacitors preferred.
- Ceramic Capacitors: Due to the low ESR they are preferred for the decoupling at ICs. They are more stable in the high frequency range. For filtering both tantalum and ceramic work well. The impedance at interesting frequencies is very important for the decision of capacitor type and value.

Figure 26 shows the equivalent RF circuit of a capacitor: Besides the pure capacitance there is an Equivalent Series Inductance ESL and an Equivalent Series Resistance ESR as parasitics of the capacitor.

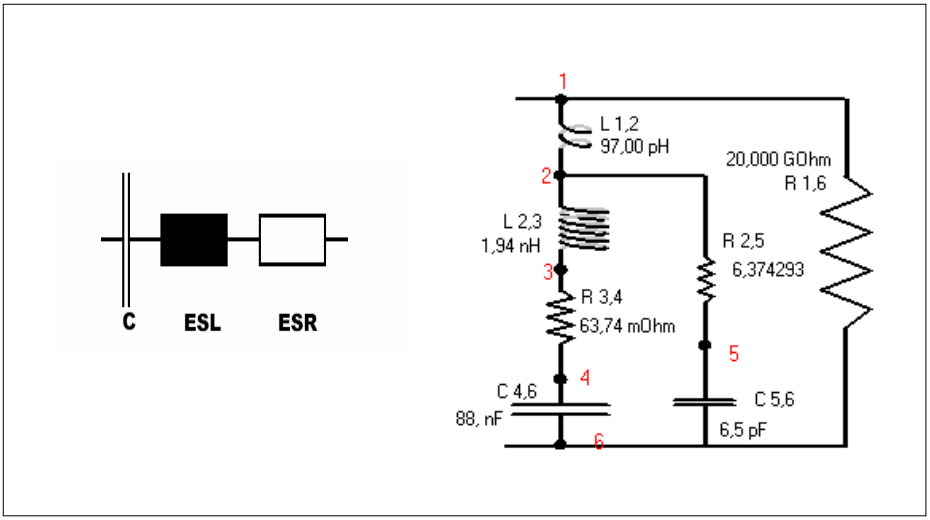


Figure 26 Equivalent Circuit of Capacitor (simplified and a model from the manufacturer)

A capacitor shows capacitive behaviour in the lower frequency range; for frequencies higher than the series resonance frequency the behaviour becomes inductive. Optimum decoupling effect is found at series resonant frequency. This information should be available in capacitor data sheets. Figure 27 shows the impedance curves of different capacitor values (1nF, 10nF, 100nF, 470nF). One impedance curve in Figure 27 shows the effect of the parallel connection of two capacitors. A positive resonance (increasing of the impedance at 100Mhz) occurs due to the resonance of inductance of the 100nF and capacitance of the 1nF. Between the resonance peaks of each capacitor, there is an increase in impedance. This is caused by the L of 100nF and C of 1nF. The 100nF is inductive in this range and the 1nF is still capacitive, so that a resonance is formed. The parallel combination of these parameters gives an parallel resonance which inreases the impedance. To avoid or reduce this effect, connect capacitors parallel with one decade value difference.

For the supply lines, the main target is to reach an impedance as low as possible and in very wide frequency range. The lower impedance of the supply system the higher is the ability of the system to response to switching current demands. A low impedance supply system can deliver this high frequency current and prevent the RF energy to

propagate. With the parallel connection of capacitors, the impedance can be reduced in a wide frequency range. But one important rule has to be taken into the care: the parallel connected capacitors should have value difference of ~ 10 (e.g. 100nF and 10nF parallel connection) to prevent higher peaks on the impedance curve due to the parallel resonance.

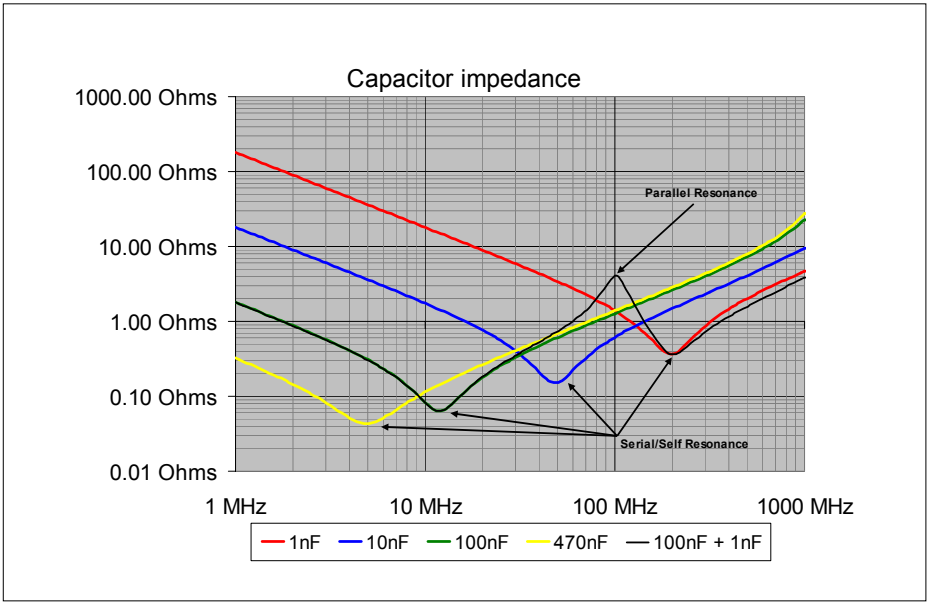


Figure 27 Impedance Characteristics of different Capacitors

Selection of decoupling capacitors:

For the selection of the decoupling capacitors, the working frequencies of the application have to be taken into account. The self resonance frequency of the capacitor has to be in the range of the clock or working frequency of the application. The total decoupling concept has to cover few harmonics of the fundamental frequency. The self resonance frequency can be calculated by the Equation:

$$X_c = \frac{1}{2\pi f C}$$

Where: X_c=capacitance reactance, F= frequency, C= Capacitance value

Take care of additional resonance frequencies caused by decoupling. Figure 28 shows an equivalent circuit of a decoupled power bus which consists of the capacity of the planes Cboard on the one side, on the other side there is the equivalent circuit of the decoupling capacitor. This structure is an oscillator with certain resonance frequencies (if one decoupling C is used, then there is just one resonance frequency). If you use two or more values of capacitors, check for additional resonance frequencies.

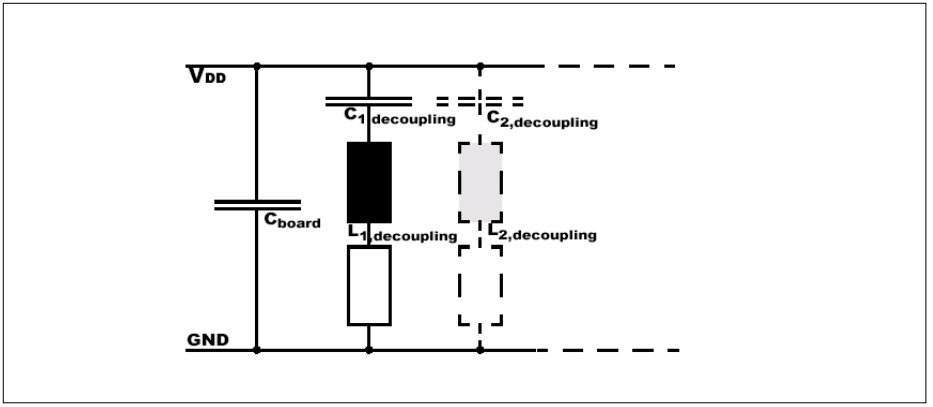


Figure 28 Additional Resonance Frequencies

Using Surface Mounted Device (SMD) capacitors reduces additional lead inductance. The inductance causes the increase of the impedance curve. To get an optimum decoupling effect, the total inductance along the connection path of decoupling capacitors has to be reduced.

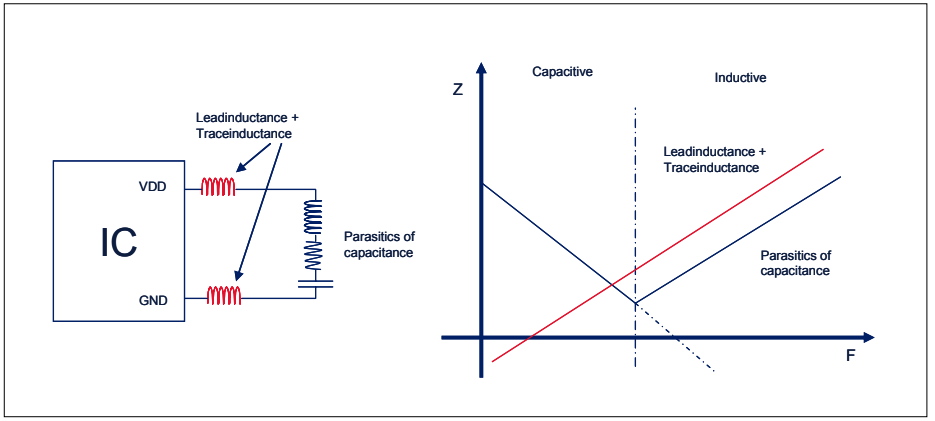


Figure 29 Effect of the inductance on impedance characteristics

Figure 30 clarifies the effect of lead inductance. The effect is mainly visible in high frequency range. This means that the decoupling is less effective in high frequencies with increasing inductance along the decoupling path.

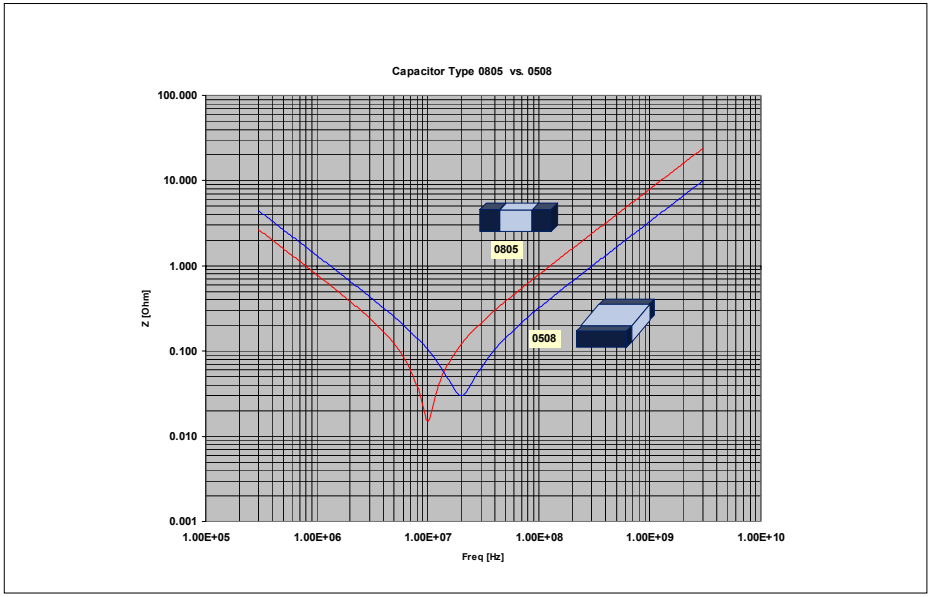


Figure 30 Low ESL package 0508 vs. Standard package 0805

The low ESL type of capacitors have optimized packages with a reduced inductance value and provide further reduction of the inductance.

The development of new technologies allow to manufacture also high value multilayer ceramic capacitors which have values up to 10-22µF. Using these capacitors, lower impedance values can be reached and total decoupling capacitor count can be reduced (costs saving). But as it can be seen in figure 31, the capacitors are effective up to ~100Mhz.

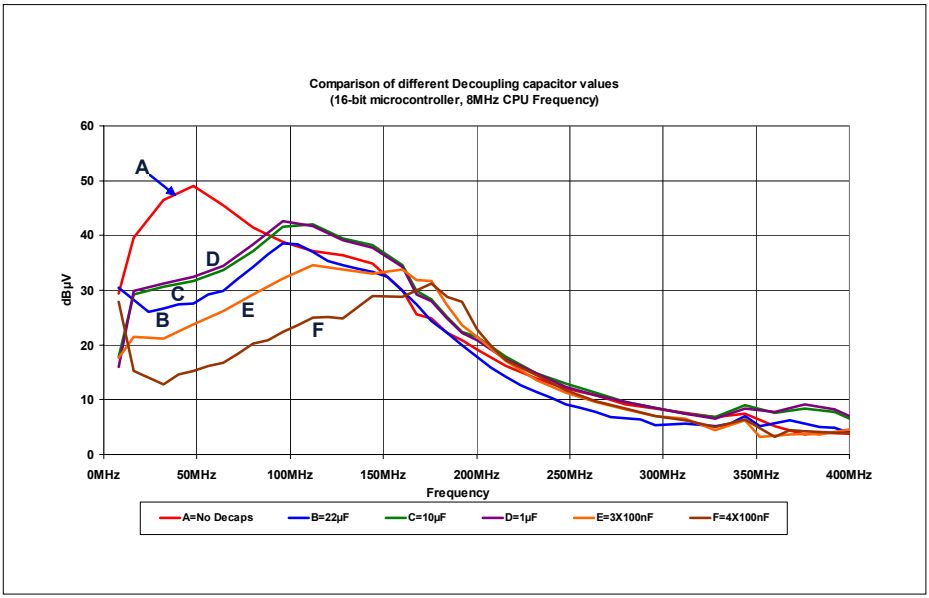


Figure 31 Comparison of different high value decoupling capacitors

In general, the suggested value for ceramic capacitors to decouple the power pins of the microcontroller is in the range from 10nF to 100nF. Capacitors have a limited frequency response, which keeps them from delivering power at all the frequencies. Therefore other values of capacitors have to be chosen if special frequencies are of interest. For global decoupling of the power system, single capacitors in the value range of 10nF up to 100nF are typical. It is efficient to place different values in parallel (while considering the antiresonance on impedance). Decoupling at the connectors and the power supply star point (e.g. voltage regulator) should be realised with additional tantalum-electrolyte capacitors.

Beside the capacitive effect of the ground plane under the microcontroller, the fast current has to be delivered from the discrete decoupling capacitors. Decide for pin-decoupling or/and global decoupling.

Layout Measures for decoupling Capacitors:

By pin-decoupling each pair of VDD-GND pads is first contacted to the capacitor(s) and then to the supply layers/nets. Advantage: Optimised decoupling for every pin possible. Disadvantage: High number of capacitors required.

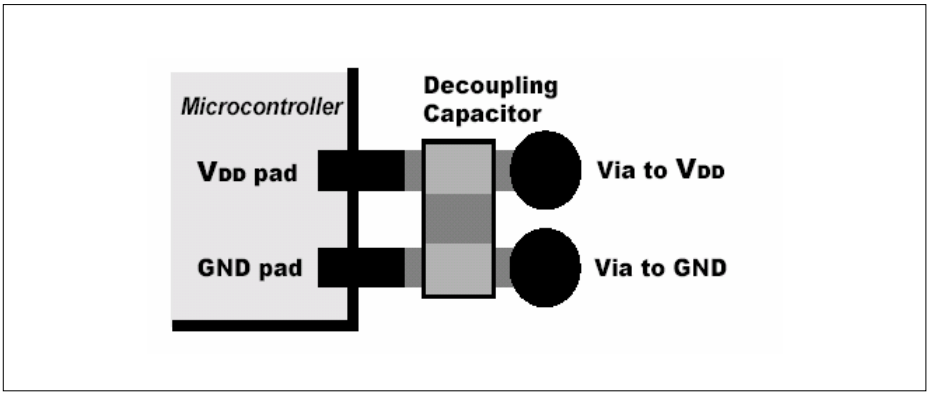


Figure 32 Placing of Blocking Capacitor

Place capacitor-pad as close as possible to the microcontroller's VDD/GND pins. First contact the capacitor, then contact the vias to GND and VDD plane (see figure 32). The connection from the decoupling capacitor to the ground plane can also be realised by several microvias inside the outline of the capacitor pad. That guarantees a low impedant and low inductive connection to ground.

If possible, keep decoupling capacitor on the same side as the microcontroller. Remember that vias cause as additional inductance. Design traces between pads and capacitor as wide as possible.

If you have to place the capacitors on the bottom side of the board, provide two or more vias in parallel and think about using microvias if possible. Keep GND-vias and VDD-vias as closely together as possible.

Figure 33 shows four different connection types of decoupling capacitors to the VDD/VSS planes. The impedance curve of the connections shows a reduction in the impedance if two vias are connected in parallel and further reduction in case of placing the vias directly on the pads of the capacitors.

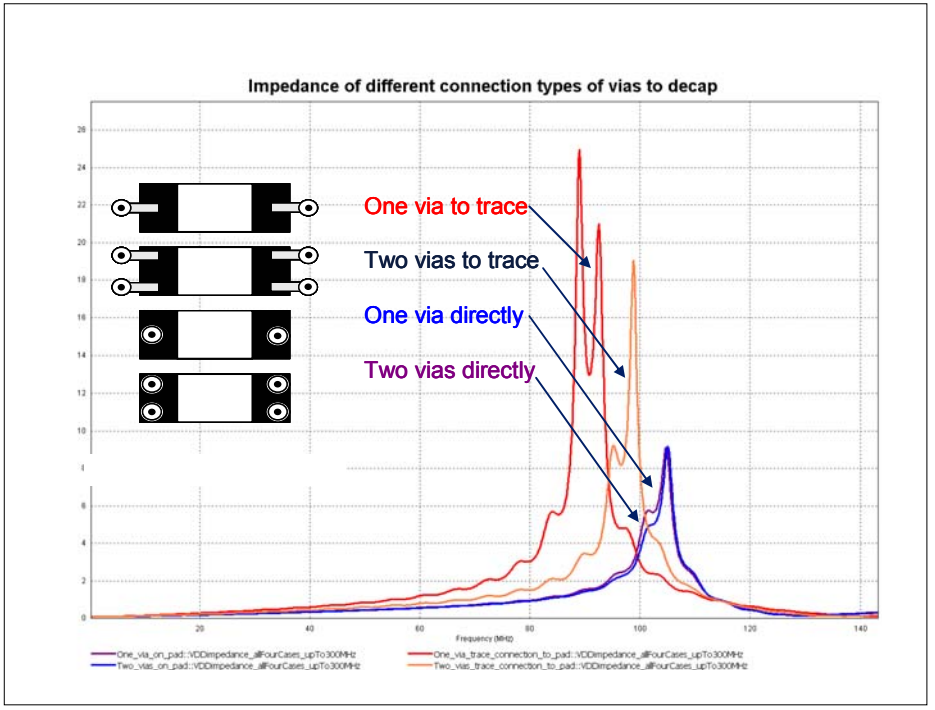


Figure 33 Impedance change caused by different types of connections to decap

By global decoupling each pair of VDD-GND pad is first contacted to the supply layers. The capacitors are placed around the microcontroller, directly contacted to the supply plane. Advantage: Lower number of capacitors required since some VDD-GND pairs can share one capacitor. Disadvantage: Larger current loops compared to pin-decoupling.

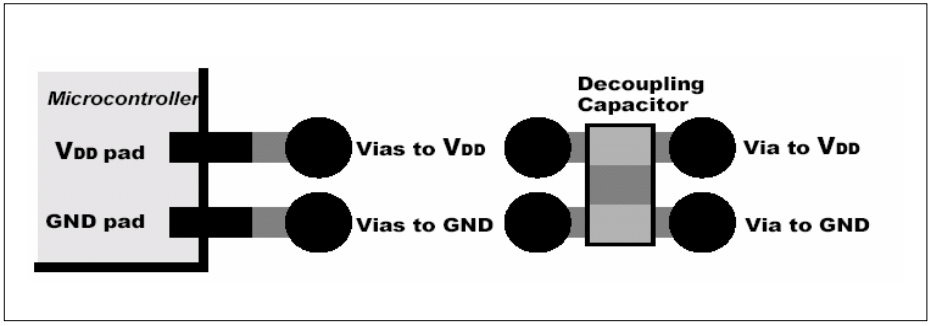


Figure 34 Global Decoupling on Multilayer PCB

Provide at least half as many capacitors of the same value as there are supply pairs at your microcontroller.

Avoid long traces between µC pad and via to supply plane (additional inductance).

Provide two vias in parallel if possible.

Keep GND-vias and VDD-vias as closely together as possible.

Note: Global decoupling cannot be used on two layer boards

Best decoupling concept is a combination of local and global decoupling. This will bring some more costs for discrete components, but can save much development time and redesign activities at critical applications.

Calculation of Decoupling Capacitors

To determine the requirements of optimum decoupling capacitors, the capacitive and inductive values must be calculated. The capacitive value has to be large enough to support local switching current and the inductive value has to be small enough to get low impedant path to the capacitors.

The steps of calculation of decoupling capacitors:

1. Determine the tolerable noise level on the power supply.
   Example: ΔV = %5 if VDD=5V ➔ ΔV= ±75mV

2. Average current at application: ΔI
   Determine the maximum impedance:

$$Z = \frac{\Delta V}{\Delta I}$$

3. On board required minimum capacitance:

$$C = \frac{1}{2\pi F_{tran} Z}$$

   F_{tran} ~ 1Mhz (up to this frequency the current changes will be delivered from voltage regulator)

4. Calculation of maximum board inductance for power supply connection to capacitors:

$$F_{tran,\max} = \frac{1}{2\pi C_{on} Z}$$

   $F_{tran,max}$ = frequency where the on chip capacitance is effective
   C_{on} = on-chip capacitance (from specification of chip or from manufacturer)

$$L_{\max} = \frac{1}{2\pi F_{tran,\max}}$$

   L_{max} = maximum inductance on supply connection path (trace + via + package)

3.1.2.2 Inductor and ferrite bead

The next important components for lower EMI are inductors and ferrite beads. If the current produced by the microcontroller cannot be supplied from the decoupling loop, the noise will couple to the power supply line. The ferrite prevents the noise from spreading out over the power supply line. Even though the ferrite beads were not so popular in the past because of place requirement on board and cost issues, with new technologies it is possible to manufacture multilayer ferrite chip beads, which have very good impedance characteristics. They are available in standard SMD packages.

As shown in figure 35, the equivalent circuit of the ferrite contains some parasitics and builds a parallel resonance.

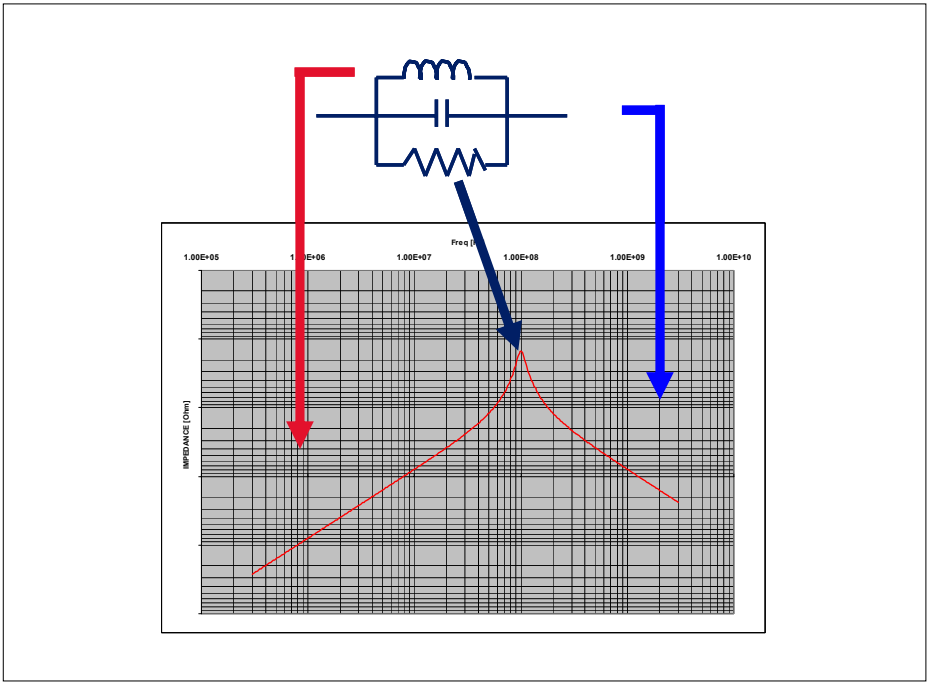


Figure 35 Typical impedance characteristics of an inductor

The ferrites have to be placed on the supply line. The current consumption of the supply path must be also considered with the selection of the ferrite beads. A high current ferrite bead can cause a voltage drop on the supply line.

The suppression mechanism is shown in figure 36. The decoupling capacitor has a series resonance in lower frequency range and the ferrite has a parallel resonance in higher frequency range. The total frequency behavior of the circuit (seen from the IC side) is drawn in the diagram on the right side.

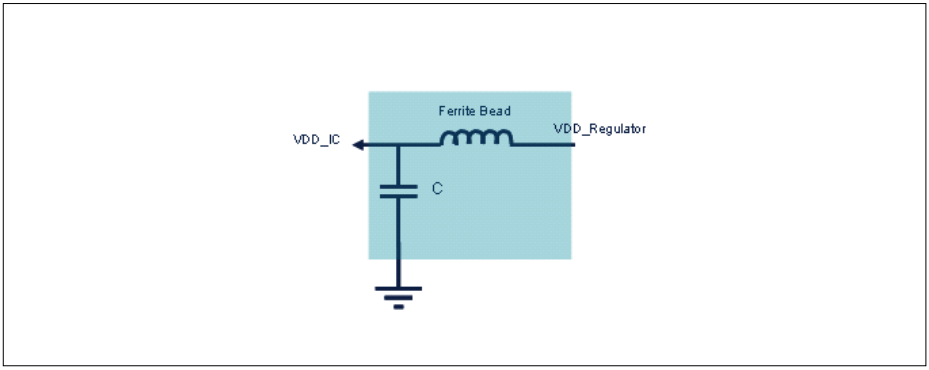


Figure 36 Placement of ferrite beads

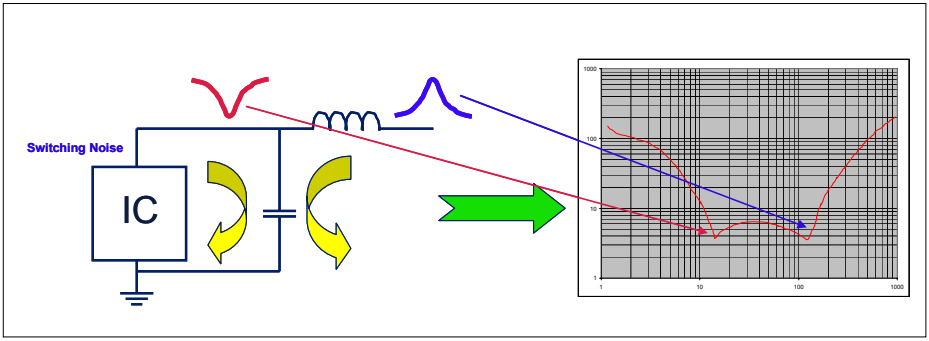


Figure 37 Total impedance of the noise filter circuit with capacitor and chip ferrite bead.

Some measurement results of a 16-bit microcontroller are shown in figure 38 with a ferrite in the supply line (no decaps used). The ferrite blocks the noise on regulator side but the noise on IC side is as much as without ferrite. The maximum improvement of the ferrite on regulator side ist about 30dBµV.

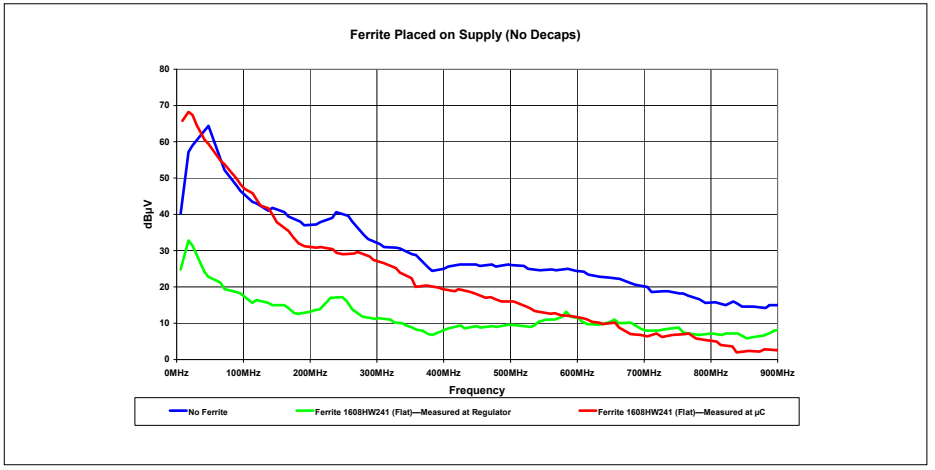


Figure 38 Measurement with ferrite on different points on board (no decaps)

Figure 39 shows the same measurements with using decoupling capacitors. The additionally reduction of the capacitors delivers an emission level on regulator side of 10 dBµV.

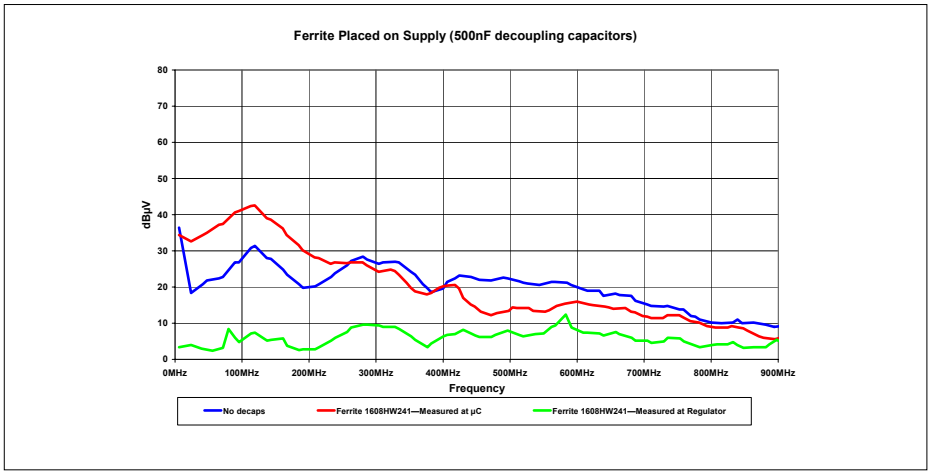


Figure 39 Measurement with ferrite beads on different points on board (with 500nF decoupling capacitors)

3.2 Signals

Before routing, determine critical nets by their rise and fall times, and driver strength. The shorter the rise and fall times become the more high-frequency components are contained in the spectrum. The higher the signal frequency becomes, the higher the corresponding harmonic frequencies are.

Figure 40 shows the spectra of signals with different rise times (worst case setting)

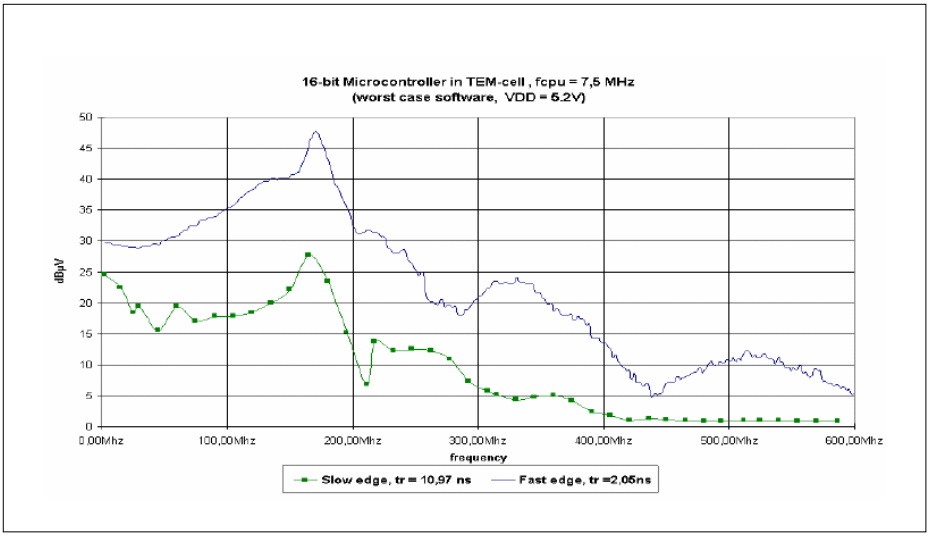


Figure 40 Effect of Rise Time on the Spectrum

Typical critical nets (if available):

Most critical signals at single chip applications: Clock out, SSC(Synchronous Serial Channel). Most critical signals at other applications: Clock out, ALE, Read, Data bus, Address bus, SSC (Synchronous Serial Channel).

3.2.1 Layout Structures for Two and Multilayer Boards

During the routing some important rules have to be considered:

- It should be avoided to put traces with high speed signals along edges of a PCB. Disturbances can be coupled easily into a metal case/shielding of the application.
- Route high speed signals as short as possible and without vias.
- For high speed signals route traces with a corner angle of 45° .

- Sensitive signals should not be placed close to of high current switching signals.
- Route critical signals with a low impedance trace (trace width) and if neccesary with guard traces.

A simulation result in figure 41 shows the improvement with the guard traces which is approximately 10dB.

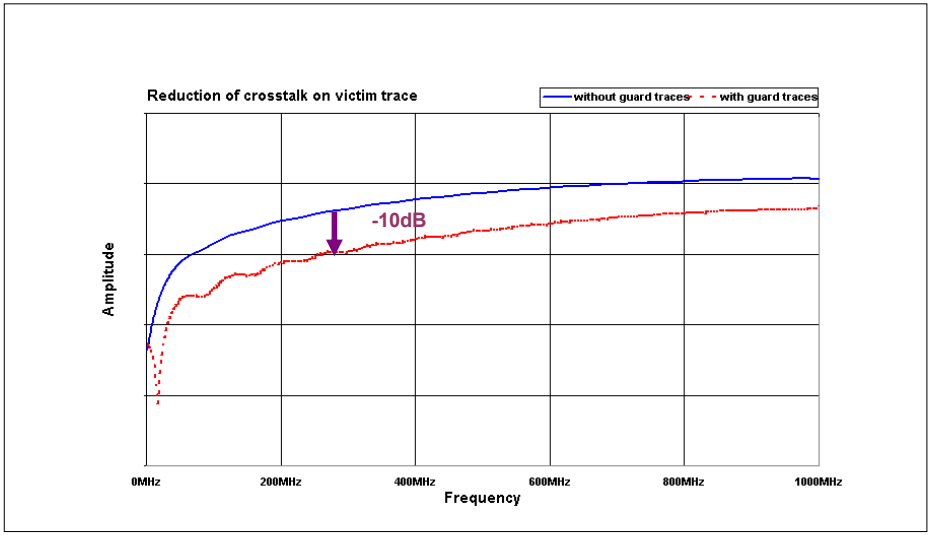


Figure 41 Effect of the guard trace

- Critical signals should be routed away from the signals/traces which lead to the connectors.
- Very critical signals (Interrupt Request and Reset) should be filtered properly. Any noise on these signals can cause malfunction of the whole circuit.
- Low frequency signal return path is along least resistance. High frequency (above 1MHz) signal return path is along least inductance.

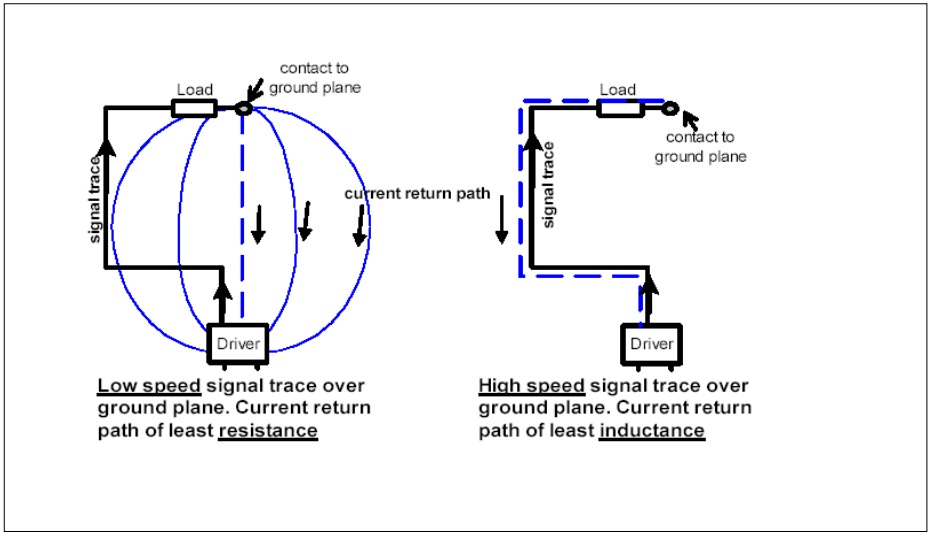


Figure 42 Return Current of High Speed Signals

- If possible, do not design any signal traces across the separation areas. Due to the slot in the power plane the loop size can be increased. Especially, avoid high speed nets leading from one zone over to the other one. Design short traces.
- To limit crosstalk (XTalk): Determine a maximum overshoot on XTalk. Determine a minimum distance / maximum parallel length between high speed nets in order to limit a minimum crosstalk (use simulation).
- To ensure Signal Integrity (SI) and radiation: Take care of characteristic wave impedance of traces when using more than one layer. The possible types of signal lines are microstrip and stripline. Microstrip can be designed when the trace is routed over a ground plane and stripline can be designed when the trace is placed on a layer between two ground planes.

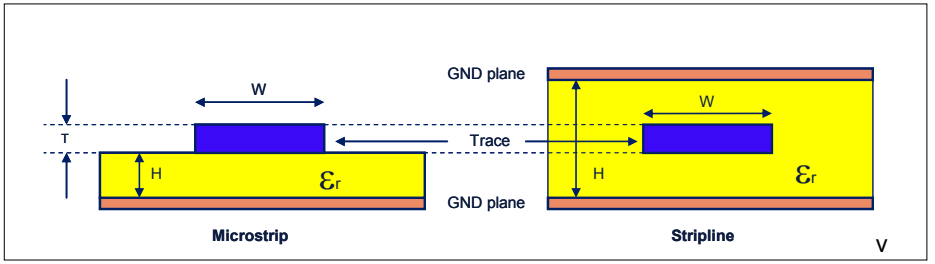


Figure 43 Construction of Microstrip and Stripline

- Determine widths of traces to guarantee the same characteristic wave impedance over the whole PCB.

Figure 44 shows the changes in characteristic wave impedance due to a smaller distance trace to groundplane or due to a wider trace.

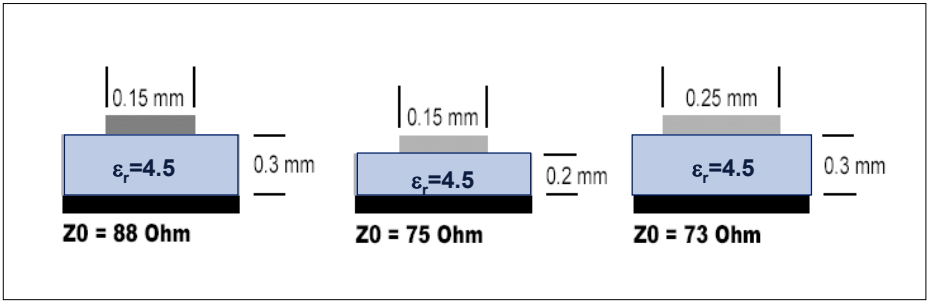


Figure 44 Wave Impedance

- If the one half rise/fall time of the signal is smaller than the propagation delay of the PCB trace, the trace should be treated as a transmission line. These traces should be terminated with their characteristic impedance. This means that if the critical length is exceeded then the trace should be terminated. The critical length of the traces can be calculated as follows:

$$L = \frac{T_r}{2T_{pd}}$$

$$T_{pd} = \frac{\sqrt{\varepsilon_r}}{c}$$

T_r: rise / falltime; T_{pd}: propagation delay; c: speed of light

The charachteristic impedance of the Stripline can be calculated with:
(valid when 0.1<W/H<2.0 and 1< ε_{rel} <15)

$$\frac{Z}{\Omega} = \frac{87}{\sqrt{\varepsilon_{rel} + 1.41}} \left[\ln\left(\frac{5.98H}{0.8W + T} \right) \right]$$

For the Microstripline following formula can be used:
(valid when W/H<0.35 and T/H<0.25)

$$\frac{Z}{\Omega} = \frac{60}{\sqrt{\varepsilon_{rel}}}\left[\ln\left(\frac{4H}{0.67\pi(T+0.8W)}\right)\right]$$

H: height of dielectrica between trace and ground plane; W: width of trace; T: height of trace.

Termination Methods:

A mismatch between the output impedance of the driver and the line impedance causes reflections on the line. These reflections influence the performance of the circuits. Most popular measure against the reflections is to use terminations. There are different methods to realize the terminations.

If the characteristic impedance of the line is matched on the source side, the line is ***source*** *(Figure 45a)* terminated. In this case the reflections will be cancelled at the source because of the matching and zero reflection coefficient. The output impedance of the driver should be subtracted from the ideal value of the source termination.

If the termination is placed at the end of the line, the line is ***load*** (*Figure 45b*) terminated. The reflections will be cancelled at the end of the line. The received voltage is equal to the transmitted voltage. A variation of the load termination is the DC biasing termination, with a resistance connected to the supply in additional to the resistance to the ground. The parallel combination of both resistances must be equal to the characteristic impedance Z_0. The source termination results in a slower rise time of the signal and smaller reflections than ***load*** terminations. Because of the DC current consumption in case of load termination, two other types of termination can be used: DC-load termination (*Figure 45c*) and AC-load termination (*Figure 45d)*.

There are three goals for termination: minimising reflection, voltage swing and emission. To minimise reflection match the driver's Ri to Z0 by a series resistor Rx close to the driver. A matching termination of a high speed signal trace on both sides is very important, especially when the rise time of the driver signal is short in comparison to the signal propagation delay.

For optimising the voltage swing determine a series resistor Rx, that cuts half of the voltage swing on a two-point-net (with a characteristic wave impedance Z0) while regarding the non-linear Ri.

For minimising electromagnetic emission, provide resistors (20-200 Ohms) and adjust for a smooth rising edge. If provided in the microcontroller, use software settings for edge control.

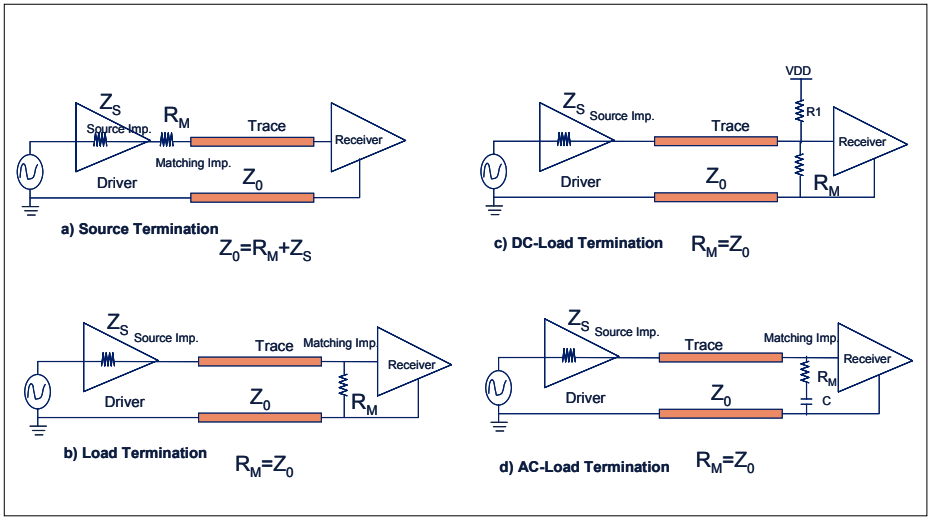
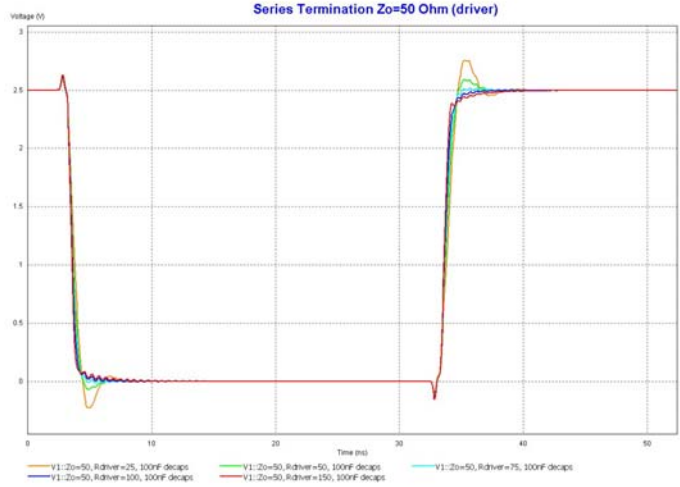


Figure 45 Source, Load, DC-Load and AC-Load Terminations

To ensure SI and reduce electromagnetic emission (EME): Provide series resistors close to the drivers. Optimise their values by simulation or by approximate calculation from VI-table of the driver and the trace's impedance.

The simulation results in figures 46-47 show that both series and parallel terminations deliver best signal integrity behaviour if the source or load termination matches with the driver´s output or trace impedance.



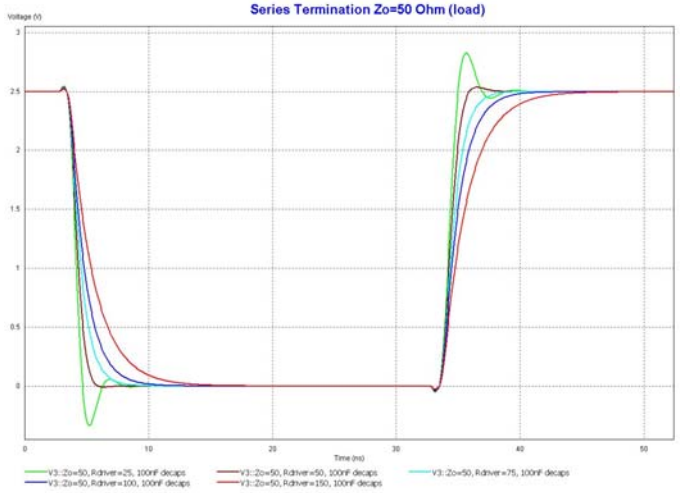


Figure 46 Series Source Termination of a 50Ohm Trace with 25 / 50 / 75 / 100 / 150 Ohm Impedances (signals at source and load)

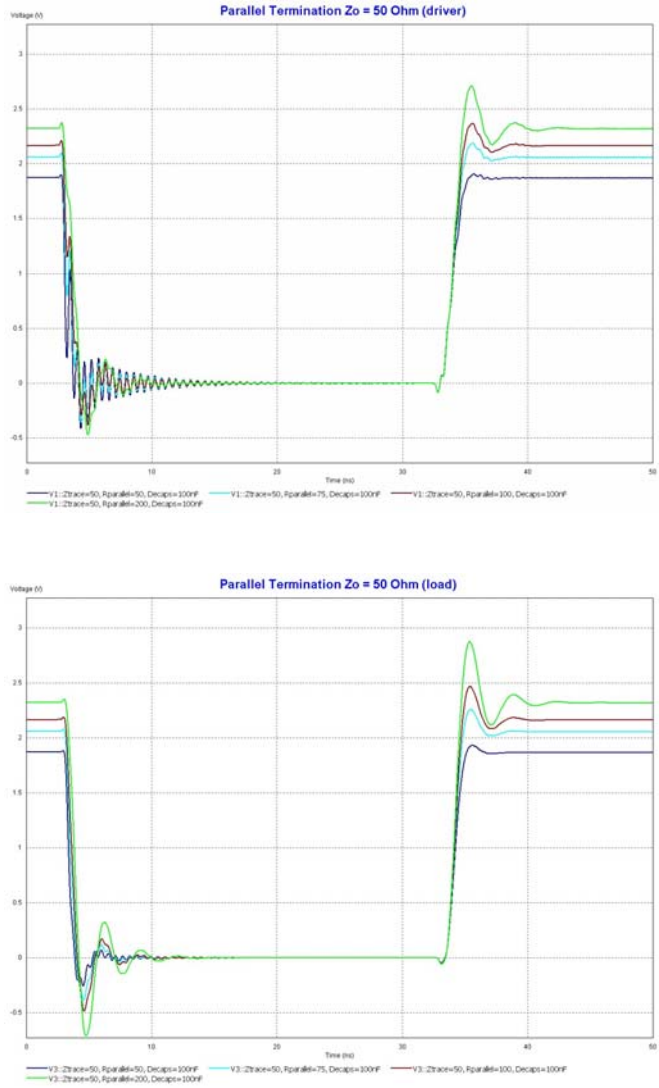


Figure 47 Load Termination of a 50Ohm Trace with 50 / 75 / 100 / 200 Ohm Impedances (signals at source and load)

Use controlled impedance for critical signals. To reach the termination targets (as explained above) calculate the impedance of the trace from the technological and geometrical data of the PCB.
Critical signals should be routed with a ground reference, if possible as a strip line on a power layer surrounded with ground.
Avoid overlapping power planes in multilayer boards. The noise can couple in this way over the different supply domains.

Keep the return current path as short as possible at the high-speed trace. In four or more layer boards, avoid gaps or batteries of vias within a ground plane in order to keep the loop of the current return path small. On two layer boards provide power and ground nets close to the high-speed trace.

The smaller the return current loop the lower the electromagnetic emission. Keep in mind that return currents can also use the VDD system!

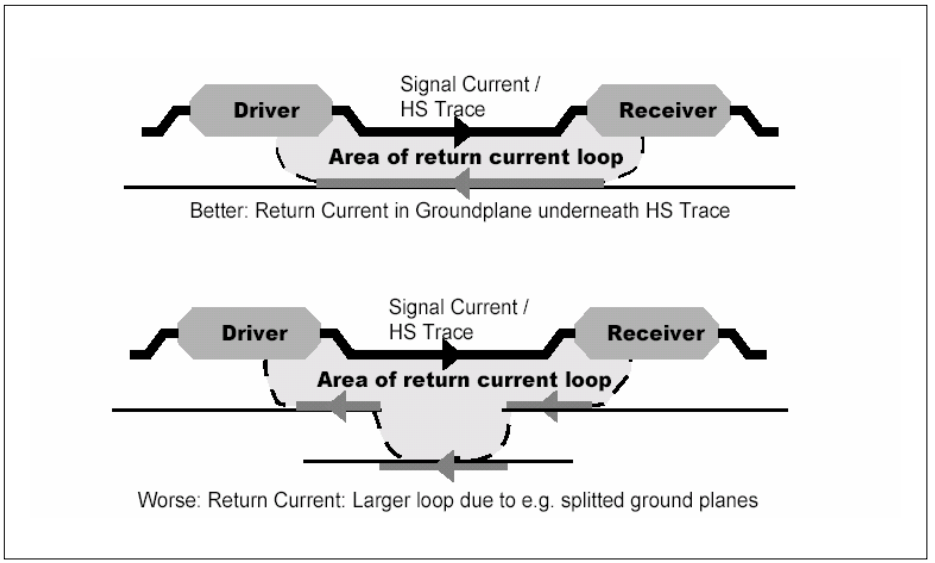


Figure 48 Return Current Loop Area for Multilayer Boards

If fast signals are provided on the PCB, design a ground ring around each layer of your board. This ground ring should be connected by several vias on the edge of the board together to the reference ground plane. The distance from one via to the next should be not longer than 5mm. This builds a reference ground ring around the board, which helps to decrease radiation from the inner layers. Additionally it avoids that current at the edges of the PCB can build antenna structures and radiate to the outside. If very

high frequencies are transferred, the distance between the connecting vias has to be even smaller. The efficiency of this measure is increasing if you have more ground planes. Then this construction forms a faraday cage for the middle signal layers.

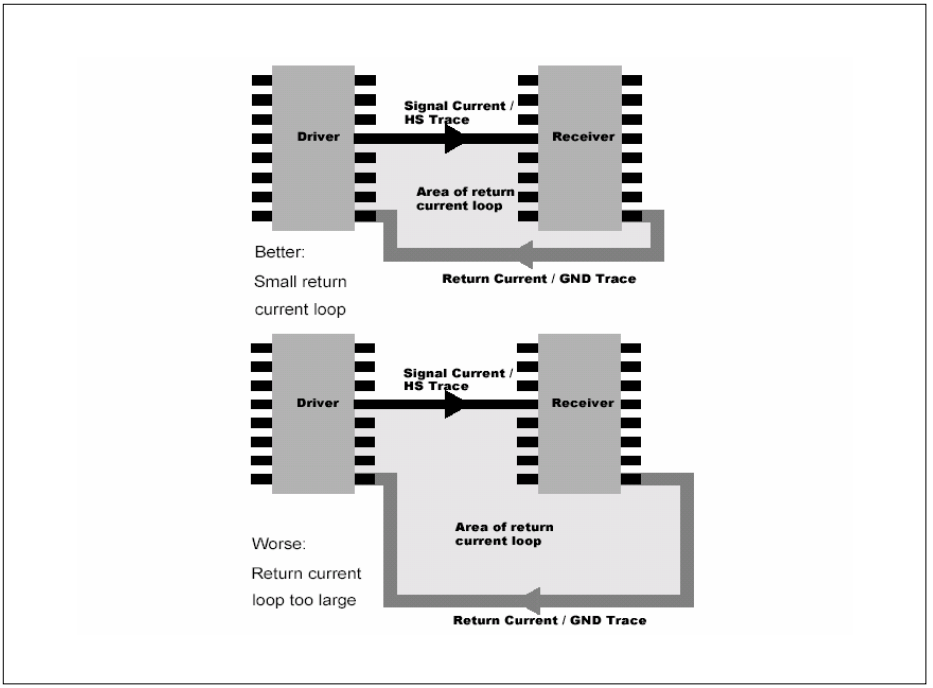


Figure 49 Return Current Loop Area for Two-Layer Boards

Avoid vias in high speed traces and through the power planes. Vias through the power planes can cause coupling of the signal to the power supply network. Vias have an additional inductance of ca. 0.5nH – 1nH.

Avoid turns in high speed traces. Turns mean a change in the characteristic wave impedance of a trace. Better use 45 degree turns (or even less!) instead of 90 degree turns. 90 degree turns cause a change in the trace's width. Changes in the trace's width cause changes in the characteristic wave impedance which will result in unwanted reflections.

Provide room for a series resistor close to the driving component. If you have not set up a specific design rule yet, optimise the resistor value.

If you have two adjacent signal layers, realise x-y-tracing to reduce crosstalk. Place and layout decoupling capacitors.

Finally design all other traces. This chapter should be kept in mind there as well.

3.2.2 Components

3.2.2.1 Resistors:

As mentioned in the paragraph “Termination” the resistors are used for the impedance matching, biasing and pull-up / pull-down circuits. Resistors are commonly used in surface mount packages (SMD). This package type has low parasitic elements compared to the lead packages. Figure 50 shows the equivalent circuit of a resistor and impedance of the 1 Ohm resistors. Increasing of the impedance at higher frequencies is because of the parasitic inductance. The inductance begins to be dominant at 30Mhz.

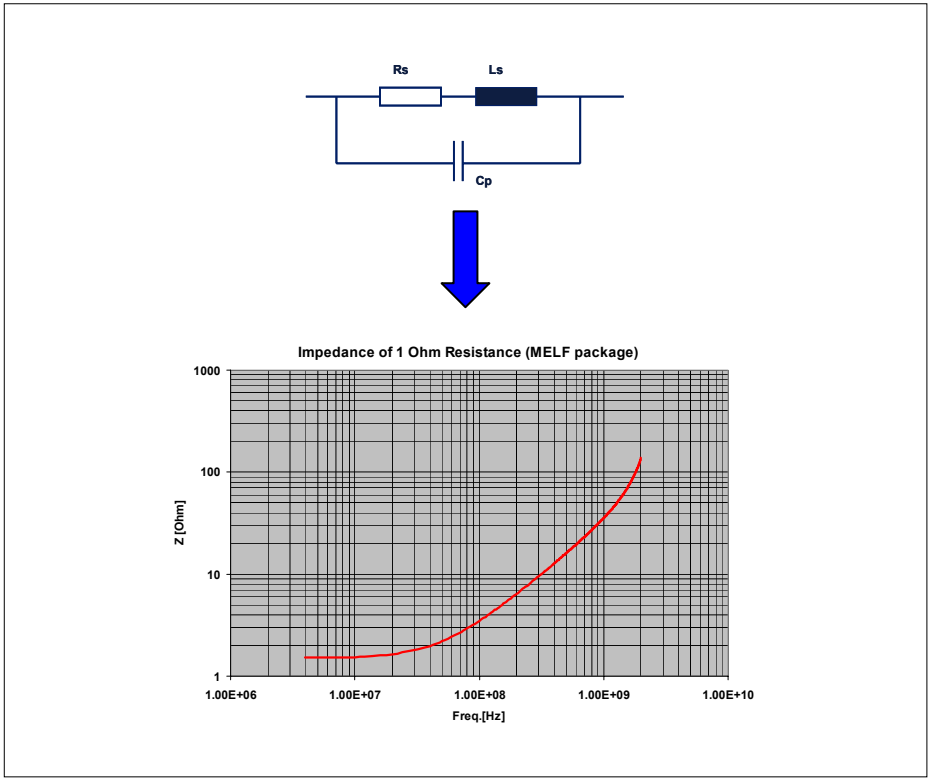


Figure 50 Equivalent circuit of a resistor and Impedance of 1 Ohm Resistance

3.2.2.2 EMI Filters:

Filters are commonly used for the power lines, but they are also very effective in signal lines. Especially on clock and bus lines which are paths for the propagation of the noise in applications.

The filters consist of L and C elements. Depending on the required insertion loss of the filter they are configured as π-, L- and T-filter. If the source and load impedance is high then a π-type filter is the best solution. The π-type filter has an inductor surrounded with two capacitors so that the capacitances are lowering the impedance on both sides (according their selected frequency characteristics).

Figure 51 shows the equivalent circuits of different types of EMI filters together with their optimum application cases.

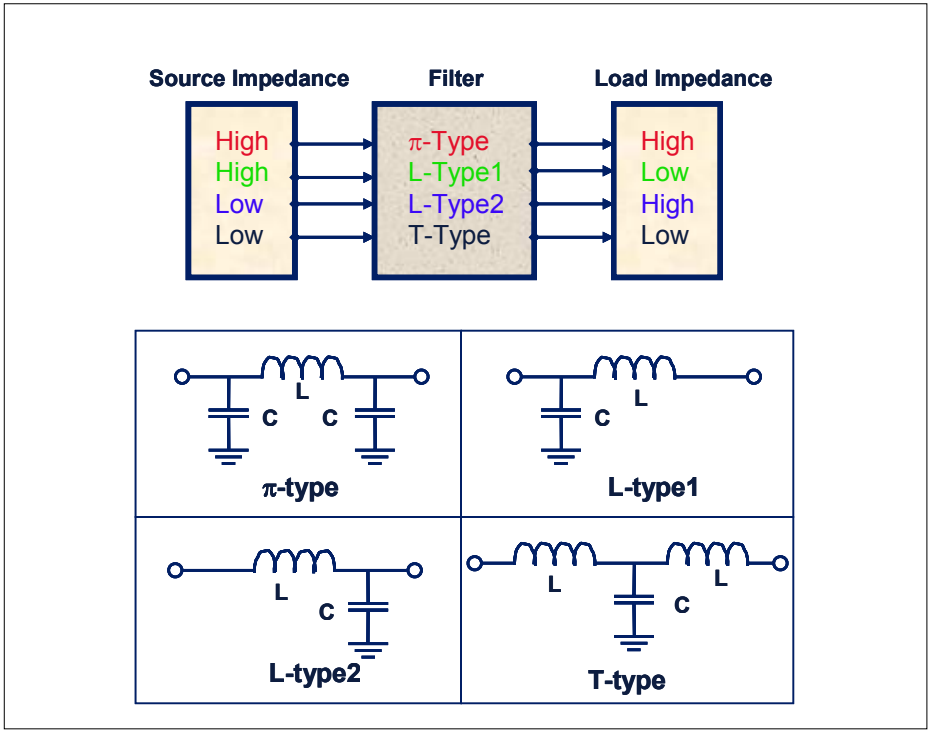


Figure 51 Different types of EMI- filters and usage conditions.

4 Simulations

An additional way to improve the design of an application is to test certain structures in the layout by simulation. Find below a description of the most common tools (which are offered by several software manufacturers) and techniques. By simulation of EMC relevant parameters (like emission, susceptibility and signal integrity) of electrical systems, an assessment of the necessary effort and the most effective measures can be made. Electrical systems can be: module, printed circuit board (PCB), electrical circuit, sub-circuits and even integrated devices. More and better simulation models are provided from the different manufacturers or distributors.

In the last few years, there are some efforts to get accurate models for the power supply network of the microcontrollers, which are missing in IBIS models. This model called ICEM (Integrated Circuit Emission Model), is a IEC standard proposal, (project number 62014-3, October 2001). The model describes the high frequency behavior of power supply network of core and I/Os of Integrated Circuits. The models can today be used with all all SPICE based simulators. An IBIS4 integration is planned.

For the 16bit and 32bit microcontrollers from Infineon Technologies, IBIS-models are provided and ICEM models under construction.

SPICE

Simulation Program with Integrated Circuit Emphasis. SPICE allows the analysis of electrical circuits; for EMI/SI items it allows the analysis of electrical systems (e.g. a bus system) regarding parasitic effects (couplings to neighbouring nets, reflections, etc.). The parasitics themselves are calculated by using a 2-D- or 3-D-Field-solver. The driver and receiver models are supplied by the manufacturers as transistor based models or in the IBIS format. There are plenty of SPICE-like programs.

Generation of SPICE Models

To achieve good results from SPICE simulations, modelling know-how is a basic requirement. The better SPICE models (subcircuits) are, the more efficient analysis becomes. For the analysis of e.g. a bus system, IBIS models (mostly provided by the chip manufacturer) and transmission line models (generation by 2D- and 3D- field solver) are necessary.

2D-Field-solver

A 2D-field solver is needed for the determination of the parasitics (capacitance, inductance and resistance values) for (in the 3rd dimension geometrically uniform)

transmission lines or transmission line systems, i.e. traces or trace structures. These values can be used to model SPICE subcircuits for the analysis of e.g. bus systems.

3D-field solver

For more complex structures like vias and rectangular traces, or structures in integrated circuits like packages, wirebonds and leadframe etc., a 3D-field solver is needed to determine the parasitics. Again these values can be used to model SPICE subcircuits.

The electric or magnetic field in any given point in the space around a conducting 3Dstructure (especially a PCB) is calculated by adding the corresponding field vectors caused by all current-vectors of this structure for a given moment in time and given frequency.

Pre-Layout Analysis

Pre-layout analysis means investigation on certain design decisions (even in the specification phase) in order to find an early optimum solution. Pre-layout analysis also means the set-up of a bundle of design rules for subsequent design stages (i.e. minimum distance of traces to keep crosstalk low, etc.).

Post-Layout Analysis

Post-layout analysis means the investigation (partially/fully) of designed devices (PCBs) in order to detect design hazards, e.g. areas of high EME, before any hardware prototype is built.

5 Formula Appendix

Calculation of Decibel

Decibel [dB] is a dimensionless ratio of levels. EMC measurement results are expressed in spectrum or limit curves with the unit [dBµV].

Power [dB] = 10 log(P1/P0), P[dBmW or dBm] = 10 log(P1/1mW);

dBm is defined for a 50Ohm system with P1 being the measured power and P0 being the reference power.

Voltage [dB] = 20 log (V1/V0), V[dBµV] = 20 log(V1/1µV);

with V1 being the measured voltage, V0 being the reference voltage.

(e.g. harmonic of 100µV amplitude = 20 log(100) = 40 dBµV)

6 Glossary

2D Field Solver	Simulation tool for analysis (couplings, characteristic wave impedance, etc.) of two-dimensional trace structures.
3D Field Solver	Simulation tool for analysis (couplings, characteristic wave impedance, etc.) of three-dimensional trace structures like via holes.
Cross (bar) current	Current which flows across two or more transistors connected in line, if they are conducting at the same time.
DUT	Device Under Test.
EMC	Electromagnetic Compatibility (Compatibility regarding emission and susceptibility of electromagnetic disturbances between DUT and environment).
EMI	Electromagnetic Interference (Undesired or illegal generation of electromagnetic signals; bandwidth DC to daylight).
EMS	Electromagnetic Susceptibility (An adverse reaction of electronic equipment to radiated or conducted signals).
EME	Electromagnetic Emission (Radiated or conducted emission of electromagnetic noise by an electronic device).
ESR	Equivalent Series Resistor of capacitors at high frequency.
ESL	Equivalent Series Inductance of capacitors at high frequency.
GND	Board ground net.
IBIS	Input/Output Buffer Information Specification (An established standard for electrical behavioural specifications of digital integrated circuit input/output analogue characteristics).
ICEM	Integrated Circuit Emission Model
Microvia	Via with a diameter of about 100µm.
PCB	Printed circuit board.
RF	Radio Frequency (High Frequency).
SPICE	Name of a common simulation tool.
SI	Signal Integrity (Reflection, Timing, Crosstalk).
VI - Table	Static behavioural driver description Voltage vs. Current.
Vih	Input threshold voltage.
VCC	Board supply net.
VDD	IC supply pin.
VSS	IC ground pin.
XTK	Crosstalk (Interference between two neighbouring traces).
x-y-tracing	On adjacent signal layers keep traces orthogonal to avoid crosstalk.
Z0	Characteristic wave impedance.

7 Literature

For more detailed information and physical explanations, it might be useful to have a book or lecture about the subject of EMC. The following list is a selection of literature, which includes the various subjects of EMC, like emission, susceptibility and electrostatic discharge.

- A.Schwab, **Elektromagnetische Verträglichkeit**, 3.Ausgabe, Springer Verlag, 1994 Berlin-Heidelberg. (German language). [Comment: Good book for wide basic knowledge of EMC] ISBN: 3-540-57658-4

- Michael Mardiguian, **Controlling Radiated Emission by Design**, Chapman & Hall, 1992 New York, [comment: detailed and special for radiation] ISBN: 0-442-00949-6

- Howard Johnson, Martin Graham, **High-Speed Digital Design - A Handbook of Black Magic**, 1993 by Prentice Hall PTR. [comment: very detailed and mathematical] ISBN: 0-13-395724-1

- Mark Montrose: **EMC and the Printed Circuit Board: Design, Theory and Layout Made Simple**, IEEE Electromagnetic Compatibility Society, [Contents: EMC Fundamentals; EMC inside the PCB; Components and EMC; Image Planes; bypassing and Decoupling; Transmission Lines; Signal Integrity and Crosstalk; Grounding Concept.] ISBN 0-7803-4703-X

- **EMC KOMPENDIUM 1999 - 2005**, publish-industry Verlag GmbH, Munich, (in German)

- **Paper to the workshop "Optimized Decoupling Concepts for Digital VLSI Circuits"**, Joachim Held, Siemens AG Munich; Prof. Thomas Wolf, University of Applied Sciences, Landshut; IEEE - EMC seminar 2001

- **Paper to the seminar "EMV auf Leiterplatten 1999"**, Prof. Chr. Dirks, published by Nils Dirks Corporate Consulting, Donaueschingen. (German language)

- **Paper to the workshop "EMV auf Leiterplattenebene"**, Werner John, published by MESAGO GmbH Stuttgart. (German language)

- **Paper to the workshop "Techniques for PCB and Circuit Level Radiation Reduction"**, David A. Weston, published by MESAGO GmbH Stuttgart.

- **High-Speed Digital System Design "A Handbook of Interconnect Theory and Design Practices",** Stephen H. Hall, Garret W. Hall, James A. McCall, 2000 by John Wiley & Sons , Inc. ISBN:0-471-36090-2

Literature

- **Paper to the EMC COMPO 2004, "IC Emission Models from Measurement and from Netlist**", Mehmet Gökcen, Thomas Steinecke., Angers, France
- **Taiyo-Yuden "The Fundamental Technical Knowledge of passive Components" Appl. Notes.** www.taiyo-yuden.com
- **Ilfa GmbH, "Layoutstrategien und Leiterplattentechnik**", Arnold Wiemers. www.ilfa.de
- **Murata , Technical Specification of Murata Capacitors**. www.murata.com
- **Kemet , Technical Specification of Kemet Capacitors**. www.kemet.com

http://www.infineon.com

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