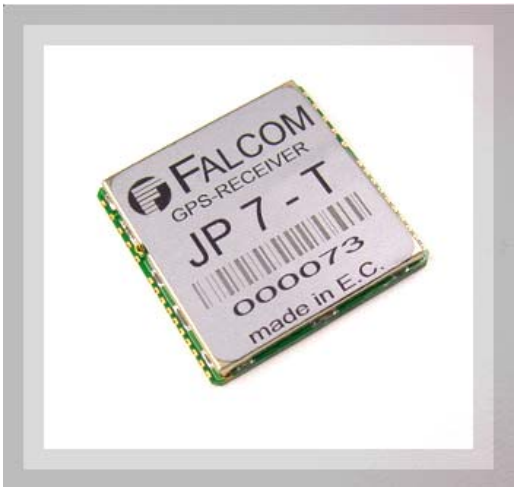
JP7-T Family

GPS-Receiver

Hardware description



Version 1.02

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Version history

Version number	Author	Changes
1.00	Fadil Beqiri	Initial version
1.01	Fadil Beqiri	- The signal names of serial ports updated - New section 11.4 "XTrac software description" added. - **CheckSum** calculation added - A complete update implemented.
1.02	Fadil Beqiri	- Chapter 11.3 updated.

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0 Introduction

0.1 General

This description is focussed on the GPS receiver of the FALCOM JP7-T family from FALCOM GmbH. The JP7-T family is an excellent device designed and supports a wide variety of solutions regarding to the customer fulfilment, the wide variety of the JP7-T family offers easy integration in the various way on the user independent application platform. Regarding to the JP7-T family (which contains JP7-T, JP7-TB, JP7-TC-1(-2)) concept, there are three different GPS receiver with different options. This manual contains information about purpose and use of the GPS receivers included into the FALCOM JP7-T family. Please read this manual very carefully to avoid any mistakes and to secure an optimal use of the devices. Each GPS receiver into the JP7-T family is a single-board 12 parallel channel receiver intended as a component for OEM products. The FALCOM JP7-T family is based and advanced on the Falcom JP7 GPS receiver which delivers major advancement in GPS performance, accuracy, integration, computing power and flexibility without modification regarding to the receiver form factor and pin-out. Each GPS receiver of the FALCOM JP7-T family has an integrated temperature compensated crystal oscillators (TCXO). Due to the higher stability of frequency it offers a high improved performance. Additionally, a TCXO accept the condition for use the SiRFXTrac2 firmware. The JP7- T family using SiRFXTrac2 firmware is able to track the GPS signals an extremely small level by 16 dBHz. In addition, higher sensitivity allows it more flexibility on the its design, the placement of the antenna and the selection of the kind of antenna. The GPS receiver continuously tracks all satellites in view, thus providing accurate satellite position data. The highly integrated digital receiver uses the SiRFstarII-Low Power chipset. The internal GPS software completes the package providing flexible system architecture for standalone GPS based products.
In order to save space on the application platform, the Falcom JP7-T family comes as an extremely slim and compact module. This makes it ideally suited for a broad range of mobile computing devices, and particularly offers easy integration with smart phones, PDAs, and other handhelds.
The FALCOM JP7-T family is also designed to be an entire product such as an AVL tracking unit, handheld GPS.
Please consult SiRF (www.sirf.com) for special information about the SiRFstarII-Low Power chipset.

Figure 1: The FALCOM JP7-T family GPS receiver (top, side and bottom view)

Users are advised to proceed quickly to the chapter "Security" and read the hints carefully to secure its optimal use.

0.2 Scope of the user's manual

This document describes the hardware interface and the technical specifications of the JP7-T.
It is also the preliminary data sheet for the electrical and mechanical device application design.
As far as JP7-T family concept is concerned, there are three different JP7-T GPS Receiver Modules available. The difference between these receivers can be recognised by looking on the bottom side of the module (see attached picture on the chapter 0.5 "**Order option**").
To choose a unit it depends on the customer requirements:

	JP7-T	**JP7-TB**	**JP7-TC-1**	**JP7-TC-2**
RF Part				
TCXO	25.5535 MHz	25.5535 MHz	25.5535 MHz	25.5535 MHz
Active antenna power control	built in	built in	built in	built in
RF connector	Not available	Not available	U.FL-R-SMT – plug antenna connector from Hirose.	No RF connector. Solder pads, only
Digital Part				
Connector	Not available	Not available	50-pin, Hirose DF12C, Board-To-Board connector	50-pin, Hirose DF12C, Board-To-Board connector
Balls	Not available	48-Balls are available	Not available	Not available

In this manual user will not find separately description for each option of devices. The interfaces, pin-out and some application's example are the same for all devices.

0.3 Used abbreviations

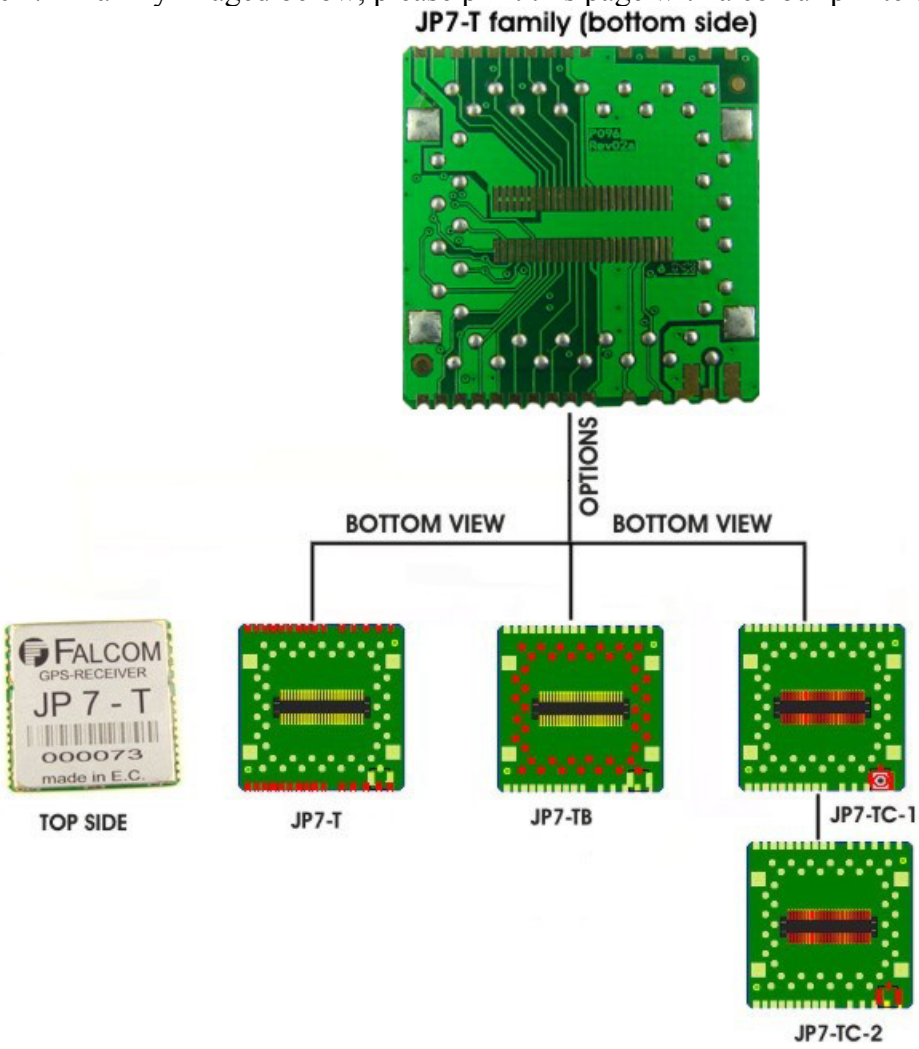
Abbreviation	Description
DGPS	Differential GPS
DOP	Dilution of Precision
GPS	Global Positioning System
GGA	GPS Fixed Data
LNA	Low Noise Amplifier
NMEA	National Maritime Electronics Association
PRN	Pseudo - Random Noise Number – The Identity of GPS satellites
RF	Radio Frequency
RP	Receive Protocol
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime Services
SDI	Data input
SDO	Data output
SA	Selective Availability
WAAS	Wide Area Augmentation System
MSK	Minimum Shift Keying
PCB	Printed Circuit Board
PRN	Pseudo-random noise
IF	Intermediate Frequency
A/D	Analog/Digital

0.4 Related documents

[1.] SiRF binary and NMEA protocol specification;
http://www.falcom.de/service/downloads/manual/SiRF/SiRFmessages.pdf
[2.] SiRF-demo software and manual;
http://www.falcom.de/service/downloads/manual/SiRF/SiRFdemo.pdf
http://www.falcom.de/service/downloads/manual/SiRF/SiRFdemo.zip

0.5 Order options

Before you start up the receiver, make sure that your package includes the following items. If any item is missing or damaged, please contact your vendor immediately. According to your requirements you can choose the desired unit. In the figure below the available components are marked with red colour. (In order to have a clearly view and to detect the required option of JP7-T family imaged below, please print this page with a colour printer.)



The table below contains the order options of JP7-T family.

Name	Options	
JP7-T	30-pin out on the left and right side of JP7-T are available for use	
JP7-TB	48 Balls are available for use	
JP7-TC	JP7-TC-1	A 50-pin connector and a RF connector are available for use
	JP7-TC-2	A 50-pin connector and solder pads for an antenna cable are available for use. There is no antenna cable included in the delivery package.

1 Security

This chapter contains important information for the safe and reliable use of the GPS receiver. Please read this chapter carefully before starting to use the GPS receiver.

1.1 General information

The Global Positioning System uses satellite navigation, an entirely new concept in navigation. GPS has become established in many areas, for example, in civil aviation or deep-sea shipping. It is making deep inroads in vehicle manufacturing and before long everyone of us will use it this way or another.
The GPS system is operated by the government of the United States of America, which also has sole responsibility for the accuracy and maintenance of the system. The system is constantly being improved and may entail modifications effecting the accuracy and performance of the GPS equipment.

1.2 Restricted use

Certain restrictions on the use of the GPS receiver may have to be observed on board a plane, in hospitals, public places or government institutions, laboratories etc. Follow these instructions.

1.3 Children

Do not allow children to play with the GPS receiver. It is not a toy and children could hurt themselves or others. The GPS receiver consists of many small parts which can come loose and could be swallowed by small children. Thoughtless handling can damage the GPS receiver.

1.4 Operation/antenna

Operate the GPS receiver with an antenna connected to it and with no obstruction between the receiver and the satellite.
Make absolutely sure that the antenna socket or antenna cable is not shorted as this would render the GPS receiver disfunctional.
Do not use the receiver with a damaged antenna. Replace a damaged antenna without delay. Use only a manufacturer-approved antenna. Use only the supplied or an approved antenna with your GPS receiver. Antennas from other manufacturers which are not authorized by the supplier can damage the GPS receiver.
Technical modifications and additions may contravene local radio-frequency emission regulations or invalidate the type approval.

Authorized GPS antennas:
FAL-ANT-3 (active antenna)

1.5 Electrostatic Discharge (ESD)

The JP7-T family GPS receiver contains class 1 devices. The following Electrostatic Discharge (ESD) precautions are recommended:

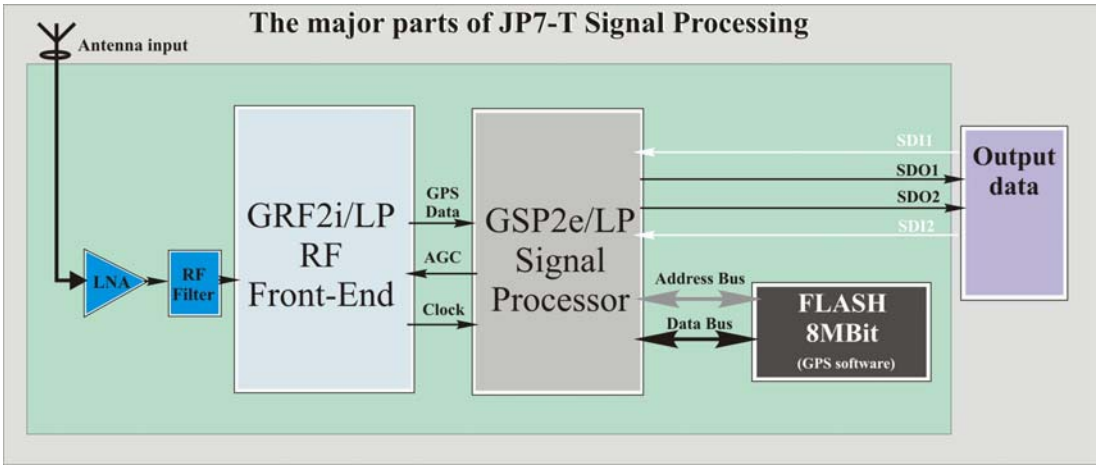
- Protective outer garments.
- Handle device in ESD safeguarded work area.
- Transport device in ESD shielded containers.
- Monitor and test all ESD protection equipment.
- Treat the JP7-T family GPS receiver as extremely sensitive to ESD.

2 Safety standards

The GPS receiver meets the safety standards for RF receivers and the standards and recommendations for the protection of public exposure to RF electromagnetic energy established by government bodies and professional organizations, such as directives of the European Community, Directorate General V in matters of radio frequency electromagnetic energy.

3 GPS basics principle

3.1 Signal Processing Operation



The JP7-T family is designed to use L1 Frequency (C/A Code). The module is separated into four major parts: **RF frequency down-converter**, **digital baseband demodulation**, **embedded ARM microprocessor** and **internal GPS software** stored on-board (8 MBits) Flash-Memory. The RF frequency conversion and the baseband demodulation are executed by hardware while the embedded ARM processor computes the GPS Position, Velocity and Time solution employing the internal GPS software.

- The purpose of the RF circuitry is to reinforce the very weak (-130dBm nominal) GPS signal, filters it and down-converts it to an Intermediate Frequency (IF) of 9.45MHz for digital processing. The JP7-T family architecture relies on the high level of integration in the RF part to significantly reduce part count and circuit complexity. The IF filter is built-in as well.
- The digital baseband demodulator takes the quantified GPS signal and detects the individual satellites serial data bit stream, along with the associated pseudo range. This action consists of removing spread spectrum and Doppler frequency components of the signal to obtain the serial data messages.
- The embedded ARM processor monitors channel allocation, extracts the raw satellite tracking data, computes the position and time solution and sends it on a serial port for high level applications to use or process it locally. Support functions for the microprocessor include real-time clock and reset pulse generator circuits.
- The internal GPS software monitors and allocate channels, computes the Position, Velocity and Time using the pseudo-range of the satellites and reformat the data to be output at the serial interface or used locally. The internal GPS software is a tasking based architecture driven by the 100ms interrupt generated by GSP2e internal hardware.

4 Technical data

FEATURES

- OEM single board 12 channel GPS receiver
- size: **JP7-T : 25,4 x 25,4 x 3 mm (L x B x H)**
  JP7-TB : 25,4 x 25,4 x 3.3 mm (L x B x H)
  JP7-TC-1 : 25,4 x 25,4 x 5.2 mm (L x B x H)
  JP7-TC-2 : 25,4 x 25,4 x 5.2 mm (L x B x H)
- weight: **JP7-T : 2,5 g (without shielding)**
  JP7-TB : 2,5 g (without shielding)
  JP7-TC-1 : 2,5 g (without shielding)
  JP7-TC-2 : 2,5 g (without shielding)
- Casing: Fully shielded
- TCXO
- 8Mbit FLASH memory
- operating voltage: +3.3 V DC ±5 %
- power consumption: 220 mW (continuous mode with Low Power chipset)
- temperature range: -40 to +85 °C (operation, transportation and storage)
- protocol: SDI1/ SDO1:
  NMEA 9600 baud, Msg.: GLL, GGA, RMC, VTG, GSV, GSA
  8 data bits, no parity, 1 stop bit
  SDI2/ SDO2:
  RTCM, 9600 baud
- trickle power mode: The default Mode of FALCOM JP7-T is continuous Mode, but the user can set FALCOM JP7-T into the Trickle Power Mode via input command message. The FALCOM JP7-T family enters the trickle power mode corresponding to figure 2 (**800 ms OFF Time and 200 ms ON Time**) as soon as valid GPS data are available. As a result the average power consumption is reduced by approximately 80 % (approximately 150 mW). The settings for the trickle power mode can be modified by using the SiRFstar demo software. For example if the FALCOM JP7-T is configured to enter the OnTime mode each 10 s for a duration of 200 ms the

average power consumption can be reduced up to approx. 95 % (approx. 15 mW, ca. 4,8 mA at Vcc=3.3 V).
For more details see chapter 4 “Operating modes”.

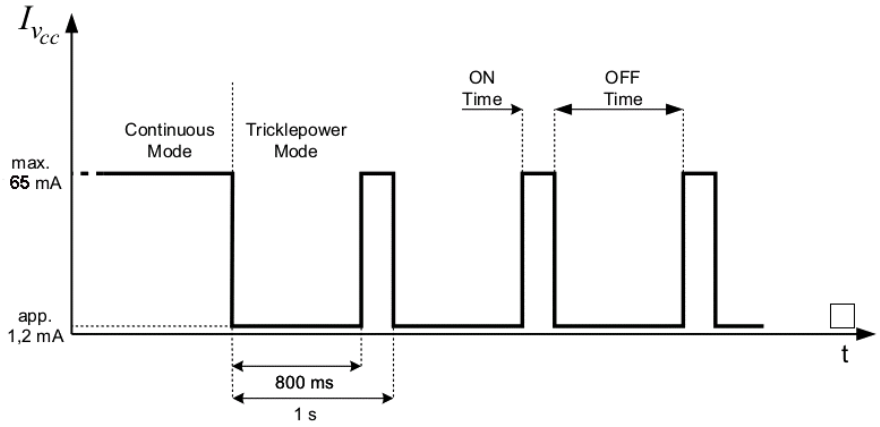


Figure 2: Example for the trickle power mode of FALCOM JP7-T family

5 Description of operating modes

There are three basic operating in which the JP7-T family operates during use. Each mode is used to accomplish a different task during the process of acquiring and maintaining the GPS information. The Falcom JP7-T family designs include all the functionality necessary to implement the three different modes of operation. The default mode of JP7-T family is normal mode (continuous mode). Three different operating modes are described below. Additionally, two of them are designed as low-power mode consumption such as the Trickle Power mode and Push-To-Fix mode.

5.1 Normal Operation

In this default implementation of normal mode the JP7-T family is fully powered and performs the function of signal search, acquisition, measurement and satellite tracking. The amount of time spent in the initial full power is dependent on the start condition that applies the number of satellites for which the ephemeris must be collected and the time to calibrate the RTC as well as the location of the GPS antenna (which it must have an unobstructed view to the sky in order to receive the satellite radio transmissions). When the JP7-T family has been locked-on to at least four satellites, the receiver is able to calculate its current positions. In this mode the JP7-T family is fully powered and satellite searching, initial acquisition, initial position calculation and tracking measurements functions are always performed. In order to reduce the start up time of the receiver it is preferable to be connected to an external back up battery, so that the RTC is running during the power interrupt. The backup power is required for retention of SRAM memory and maintaining the Real-Time-Clock. The validity of data stored in SRAM is kept due to RTC keeps running and these data will be needed on the next power up scenario.

5.2 Trickle Power Operation

In the Trickle Power mode, power is still applied to the JP7-T family, but the GPS engine is shut off and RF circuits are powered down. The Trickle Power mode provides a method of operating the JP7-T family in a user programmable duty cycle, consisting of a receiver measurement on time tracking and an interval of position update, thereby reducing the average power consumption over a period of time. The transition into the Trickle Power mode of JP7-T family can be implemented and configured by using the **Set Operating Mode** command in SiRFdemo. Between two on time tracking periods the JP7-T family sets itself in the sleep phase in other word into the low power consumption. The transition from sleep mode of JP7-T family back to the on time tracking is generated through the internal RTC which transmits a wakeup signal to the GPS engine to switch it on as well the RF circuit is powered on. The JP7-T is waked up and begins to acquire the on view satellites. In order to reduce the start up time of the receiver for the next power up is preferable to connect an external back up battery, so that the RTC is running during the power interrupt and the required data and the Trickle Mode configuration are kept from previous operation. If the

receiver fails to acquire satellites within a given period of time (approx. 150 sec), the receiver sets itself into the sleep phase. The duration of this sleep phase is approx. 30 sec. After that, the receiver wakes up, reset itself and tries to acquire satellites which are in view. This procedure repeats itself until the initial position computation of GPS receiver is completed.

Hint: After initial turn on or system reset, the JP7-T will remain in the full power tracking until a series of Kalman filter navigation solution is obtained, all ephemeris data is collected and the RTC is calibrated prior to transitioning to the low power duty cycle mode.

5.3 Push-to-Fix Mode

The Push-to-Fix mode puts the FALCOM JP7-T family into a background duty cycle which provides a periodic refresh of position, receiver time, ephemeris data and RTC calibration every 30 minutes. The Push-to-Fix mode is similar but executive from Trickle Power mode, meaning that only one mode can be set at a time. In this mode the receiver sets itself into the sleep phase for 29.5 minutes and a full tracking phase for 30 seconds. During the tracking phase the JP7-T family acquires satellites, computes position and updates ephemeris data as well the RTC is being calibrated.
The transition into the Push-to-Fix mode of JP7-T family can be implemented and configured by using the **Set Operating Mode** command in SiRFdemo. During the subsequent background cycles or when a user requests a position update (the RESET_N has to be used) a reset is generated and a hot start will be typically performed which may take up to a maximum of 8 seconds. The receiver wakes up, computes its position fix and goes back to the previous sleep phase again.

5.4 NMEA input message for Trickle Power Mode

The input command message below sets the FALCOM JP7-T family into the Trickle Power Mode or Push-To-Fix Mode. Details to configure Trickle Power Mode and Push-To-Fix Modes are described below.

The receiver accepts the input message with following format:

$PSRF107,<parameter>, <parameter> ,<parameter><* Checksum><CR> <LF>.

COMAND SYNTAX	DESCRIPTION
$PSRF107, ptf, dc, msot *XX <CR><LF>	**Parameters description:** **ptf** *// numeric, performs the receiver in one of two pre-defined modes* **Possible values:** **0: Set the receiver in Trickle Power mode** **1: Set the receiver in Push-To-Fix mode** **dc** *// numeric, Duty Cycle in percent (%)* **Possible value:** **max 1000: Set the time which will be spent for tracking (dc% / 10)** **msot** *// numeric, the on Time in milliseconds* **Possible value** **200.. 900: Set the time duration of each tracking period** ***XX** *// Checksum has to be calculated in hexadecimal.*

	Example: `$PSRF107,0,200,200*3D` *The receiver will be set in Trickle Power mode where 20% of time it will spend for tracking and the tracking period will takes 200 msec.*

Table 1: Example of Trickle Power Mode Control.

Note:

If the receiver is set into the Trickle Power Mode, the high data rate transmission is recommend as suitable.

Computation of Duty Cycle and On Time

The Duty Cycle is the desired time, which will be spent for tracking. The On Time is the duration of each tracking period (range is 200 - 900 msec.) To calculate the Trickle Power update rate as a function of Duty Cycle and On Time, use the following formula:

$$\text{Off Time} = \frac{\text{On Time} - (\text{Duty Cycle} * \text{On Time})}{\text{Duty Cycle}}$$

Update rate = Off Time + On Time

Hint:

It is not possible to enter an On Time > 900 msec.

Following are some examples of selections:

Mode	On Time (msec)	Duty Cycle (%)	Update Rate (1/Hz)
Continuous	1000	100	1
Trickle Power	200	20	1
Trickle Power	200	10	2
Trickle Power	300	10	3
Trickle Power	500	5	10

Table 2: Example of Selections for Trickle Power Mode of Operation.

	Update Rates (seconds)									
On Time (msec)	1	2	3	4	5	6	7	8	9	10
200	√	√	√	√	√	√	√	√	√	√
300	√	√	√	√	√	√	√	√	√	√
400	√	√	√	√	√	√	√	√	√	√
500	√	√	√	√	√	√	√	√	√	√
600	√	√	√	√	√	√	√	√	√	√
700		√	√	√	√	√	√	√	√	√
800		√	√	√	√	√	√	√	√	√
900		√	√	√	√	√	√	√	√	√

Table 3: Trickle Power supported Modes.

Push-To-Fix

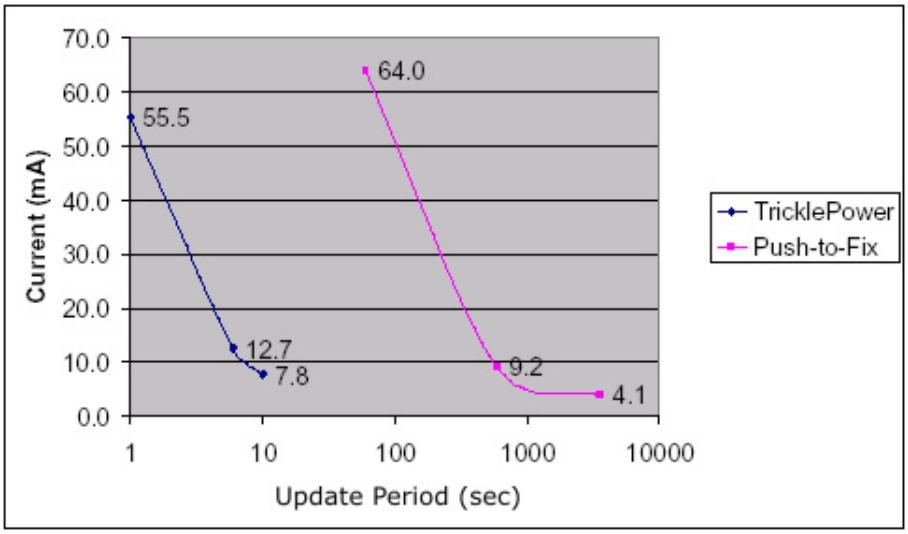
In this mode the receiver will turn on every 30 minutes to perform a system update consisting of a RTC calibration and satellite ephemeris data collection if required (i.e., a new satellite has become visible) as well as all software tasks to support SnapStart in the event of an NMEA. Ephemeris collection time in general takes 18 to 30 seconds If ephemeris data is not required then the system will re-calibrate and shut down. In either case, the amount of time the receiver remains off will be in proportion to how long it stayed on:

$$\text{Off period} = \frac{\text{On Period} * (1 - \text{Duty Cycle})}{\text{Duty Cycle}}$$

The off period has a possible range between 10 and 7200 seconds. The default is 1800 seconds.

Comparison

A comparison of the Trickle Power and Push-to-Fix modes is shown in Figure below. This diagram shows that for position update intervals less than approximately 600 seconds (i.e. rates faster than one fix per 10 minutes), the Trickle Power mode at an update interval of 10 seconds offers a lower power solution. The user would then be required to filter the output position data to use only the data points corresponding to the desired update interval. For example, if the desired position output is at 60 second intervals, then the user would only need one out of every six position outputs at a 10 second Trickle Power update interval. Alternatively, the user could perform smoothing or averaging of the position data and provide an output at the desired rate.



6 Technical Description

6.1 Receiver Architecture

The JP7-T family OEM GPS receiver from FALCOM is new OEM GPS receiver product that features the SiRFstarII-Low Power chipset. This completes 12 channel, WAAS-enabled GPS receiver provides a vastly superior position accuracy performance in a much smaller package. The SiRFstarII architecture builds on the high-performance SiRFstarI core, adding an acquisition accelerator, differential GPS processor, multipath mitigation hardware and satellite-tracking engine. The JP7-T family delivers major advancements in GPS performance, accuracy, integration, computing power and flexibility.

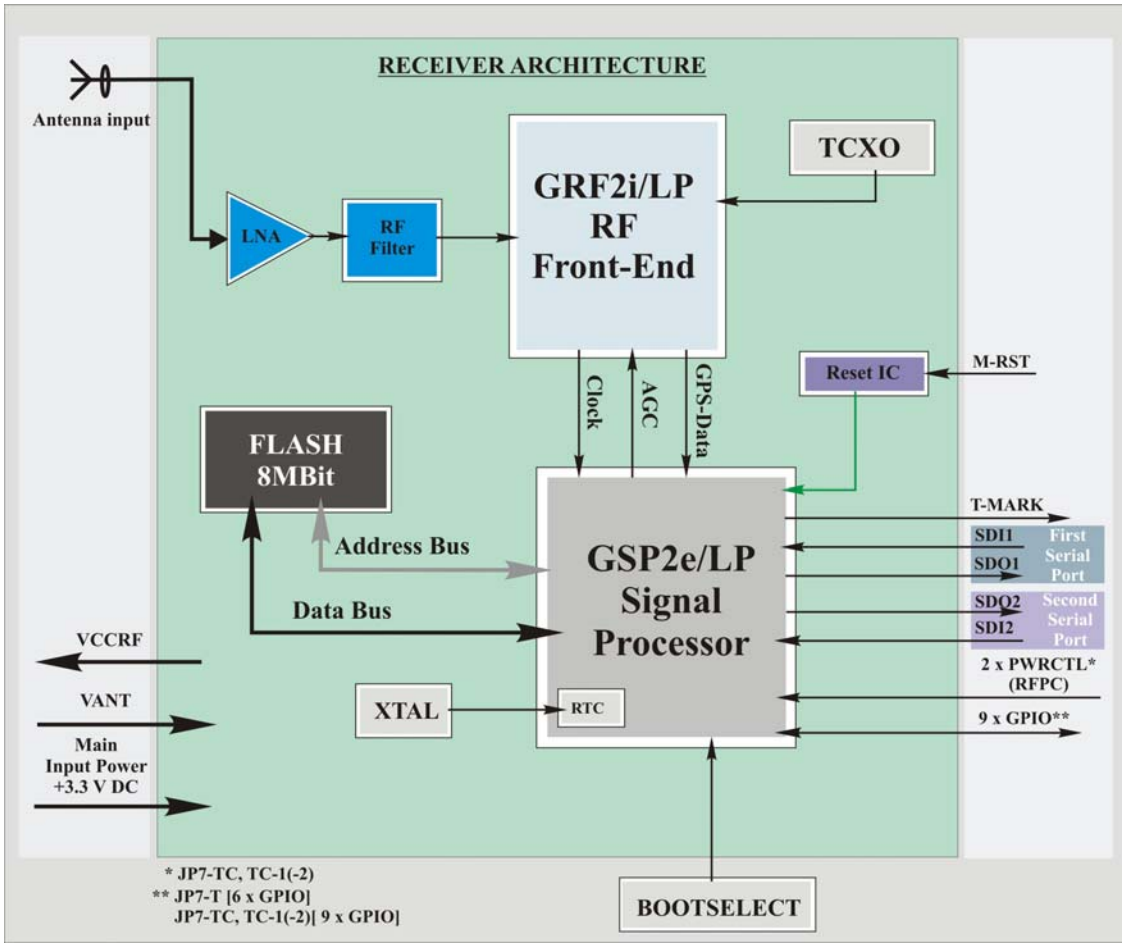


Figure 3: Receiver architecture of the JP7-T family GPS receiver.

Figure 3 above shows the block diagram of the JP7-T family architecture.

6.2 Description of GPS receiving signals

When the GPS receiver is initially turned on, it begins to determinate its current positions, velocity and time. In order to perform a successful start it must have a current almanac, a reasonable expectation of its current location and a reasonable idea of the current time. When the Ephemeris data are completely collected, then satellite signals are tracked continuously and the position is calculated from time to time.
While the receiver trying to obtain a position fix, it needs to be locked-on to at least four satellites. In order to calculate quickly its current location, the receiver uses the current received signals, together with data from its memory (SRAM).
The initial state of the receiver refers to the last status of the receiver in memory (SRAM). This essentially determines the length of time it will take for the receiver to obtain a GPS fix. Position can be quickly fixed within 8 seconds from a "hot-start" state, and typically 45 seconds from a "cold-start" state.
The receiver uses the satellite signals to calculate its exact current location by calculating the receiver distance from the satellites. The position data within the receiver is then converted into latitude and longitude coordinates, which are usually provided in the geodetic datum on which the GPS is based (WGS84).

6.3 Start-Up Modes

The start-up modes of the JP7-T family depend on the last stored position in the SRAM memory, such as the current time and ephemeris data. So that the JP7-T family can be initiated to one of three different start up procedures, but note that only one can be initiated at a time. In order to perform a Warm and Hot start, a backup battery has to be connected to the JP7-T family.
Without an external backup battery the receiver will perform a cold start after every turn on. To achieve the faster start-up offered by a hot or warm start, a backup battery must be connected. To maximize battery lifetime, the battery voltage should not exceed the maximal supply voltage and should be between 2.85 V and 3.15 V.

6.3.1 Cold start

The unit stores data about where the satellites are located at any given time. The data is called almanac. Occasionally, when the JP7-T family has been turned off for a long time, the almanac can get out-dated or “cold”. The cold start takes place when the receiver does not know its last position or time. In this start-up mode, the receiver either does not operate under back-up power conditions or it is the first start-up time (i.e. no idea about ephemeris or almanac data). At this time, the Ephemeris data has yet to be completely collected. Once the ephemeris data is collected from in view satellites, then the data from these satellites is considered valid and available for navigation. This start up scenario is one of the longest time which the receiver will take to obtain a GPS fix.

6.3.2 Warm start

This start-up procedure so called Warm start is performed when the time and position are known to within some limits, as well the almanac data are known and at least 3 Satellites Ephemeris are valid from previous operation. The validity of this data is dedicated if the receiver is switched off for more than 2 hours. If the receiver has been moved for more than 100 miles or the accurate time is currently not available then the Ephemeris data can be invalid. In such case the receiver will have to acquire the satellites and to collect the Ephemeris data which are in this scenario required.

6.3.3 Hot start

This start-up procedure so called Hot start is performed when the time and position are accurate known, as well the almanac data are also valid. The validity of this data is dedicated if the receiver has been switched off for less than 2 hours and the real-time clock (RTC) has been operating during that switch off time. This start-up procedure performs computing of valid positions, only.

The problems which may be met while start-up modes:
The validity of the Real-time Clock (RTC) during start-up is determined in part through a checksum of the SRAM to see if it has been corrupted. If the SRAM checksum shows the memory has been corrupted, the RTC is also assumed to be invalid and the system ignores the RTC value. In this case, the system will not perform a hot start, but will fall back to a cold start mode with a longer time to first fix (TTFF), on the order of less than 45 seconds typical. These problems may happens in case of the RTC randomly drop counts under minimal supply voltage conditions which is supplied from external connected backup battery and supports the RTC operation (+3.0 VDC –5%).

6.4 Product applications

- Handheld GPS receiver applications
- Automotive applications
- Marine navigation applications
- Aviation applications
- Timing applications

6.5 Technical specifications

6.5.1 Electrical Characteristics

6.5.1.1 General

Frequency	L1, 1575.42 MHz
C/A code	1.023 MHz chip rate
Channels	12

6.5.1.2 Accuracy

Position	10 meters CEP without SA
Velocity	0.1 meters/second, without SA
Time	1 microsecond synchronized to GPS time

6.5.1.3 DGPS Accuracy

Position	1 to 5 meters, typical
Velocity	0.05 meters/second, typical

6.5.1.4 Datum

WGS-84

*6.5.1.5 Time to First Position**

Hot start	< 4 sec., average
Warm start	< 35 sec., average
Cold start	< 45 sec., average

* The values listed above are available by using the SiRFXTrac2 firmware, only.

*6.5.1.6 Sensitivity **

Tracking	16 dBHz
Hot Start	23 dBHz
Warm Start	28 dBHz
Cold Start	32 dBHz

* The sensitivity value is specified at the correlator. On a JP7-T Evaluation Receiver using SiRFXTrac2 firmware with the supplied antenna, 32 dBHz is equivalent to -142 dBm or -172 dBW. Other board and antenna characteristics will vary.

6.5.1.7 Acquisition Rate

Snap start	< 3 sec., average
Hot start	< 8 sec., average
Warm start	< 38 sec., average
Cold start	< 45 sec., average

6.5.1.8 Dynamic Conditions

Altitude	18,000 meters (60,000 feet) max.
Velocity	<515 meters/second (1000 knots) max.
Acceleration	4 g, max.
Jerk	20 meters/second³, max.

6.5.1.9 DC Power

Main power	+ 3.3 V DC ±5 %
Continuous mode	65 mA at 3.3 V DC
Backup battery power	+3 V DC ±5%

6.5.1.10 Serial Port

Electrical interface	Two full duplex serial communication, CMOS.
Protocol messages	SiRF binary and NMEA-0183, version 2.32 with a baud rate selection SiRF binary – position, velocity, altitude, status and control NMEA – GGA, GLL, GSA, GSV, RMC and VTG
DGPS protocol	RTCM SC-104, version 2.32, type 1, 5 and 9

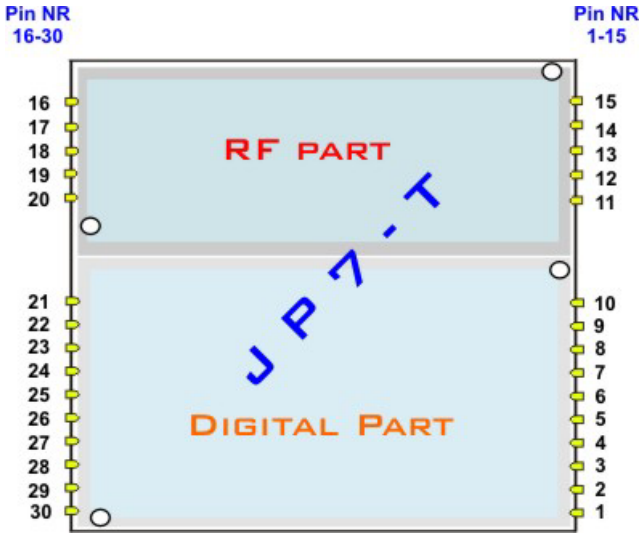
6.5.1.11 Time – 1PPS Pulse

Level	CMOS
Pulse duration	100 ms
Time reference	At the pulse positive edge
Measurements	Aligned to GPS second, ± microsecond

6.5.1.12 TCXO-Specification

Typical phase noise density	1 Hz offset	-57.0 dBc/Hz
Typical phase noise density	10 Hz offset	-88.0 dBc/Hz
Typical phase noise density	100 Hz offset	-112.0 dBc/Hz
Typical phase noise density	1 kHz offset	-130.0 dBc/Hz
Typical phase noise density	10 kHz offset	-140.0 dBc/Hz
Load sensitivity	± 10% load change	0.2 ± ppm
Long term stability	Frequency drift over 1 year	0.5 to 2.0 ± ppm

6.6 Hardware interface



Pin	Name	I/O	Description	Level
1	VCC	I	Supply voltage	3.3 V DC±5 %
2	GND		Digital ground	
3	BOOT_SELECT	I	Boots in update mode, if high	CMOS
4	SDI1	I	Serial Data Input A	CMOS
5	SDO1	O	Serial Data Output A	CMOS
6	SDO2	O	Serial Data Output B	CMOS
7	SDI2	I	Serial Data Input B	CMOS
8	GPIO3	I/O	See chapter 6.8.4	
9	RF_ON	O	High if RF part on RF chip is on	CMOS
10	GND		Digital ground	
11	RF_GND		Analog ground	
12	RF_GND		Analog ground	
13	RF_GND		Analog ground	
14	RF_GND		Analog ground	
15	RF_GND		Analog ground	
16	RF_GND		Analog ground	
17	RF_IN	I	GPS signal from connected antenna	50 Ohms @ 1.575 GHz

Pin	Name	I/O	Description	Level
18	RF_GND		Analog ground	
19	V_ANT	I	Power supply for active antenna	upto +12 V DC
20	VC3.0	O	Supply voltage of RF section	+3.0 V DC
21	V_BAT	I	Power for RTC and SRAM	+3 V DC ±5%
22	RESET_N	I	Resets the unit if active LOW	CMOS
23	GPIO10	I/O	See chapter 6.8.4	CMOS
24	GPIO6	I/O	See chapter 6.8.4	CMOS
25	GPIO5	I/O	See chapter 6.8.4	CMOS
26	GPIO7	I/O	See chapter 6.8.4	CMOS
27	GPIO0	I/O	See chapter 6.8.4	CMOS
28	GPIO1	I/O	See chapter 6.8.4	CMOS
29	T-MARK	O	One pulse per second	CMOS
30	GND		Digital ground	

Table 4: Pin assignment of the JP7-T

6.7 Balls assignment of the JP7-TB

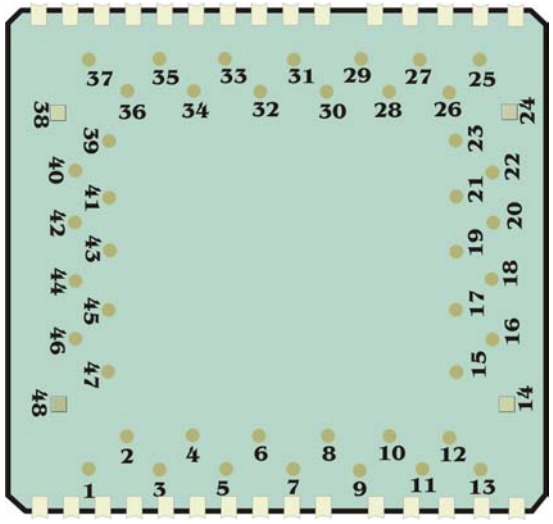


Figure 4: Balls assignment of the JP7-TB

Ball	Name	I/O	Description	Level
1	GPIO1	I/O	See chapter 6.8.4	CMOS
2	GPIO0	I/O	See chapter 6.8.4	CMOS
3	GPIO7	I/O	See chapter 6.8.4	CMOS
4	GPIO5	I/O	See chapter 6.8.4	CMOS
5	GPIO6	I/O	See chapter 6.8.4	CMOS
6	GPIO10	I/O	See chapter 6.8.4	CMOS
7	RESET_N	I	Reset the unit, if Active Low	CMOS
8	V_BAT	I	Power for RTC and SRAM	+3 V DC ±5%
9	VC3.0	O	Supply voltage of RF section	+ 3.0 V DC / max. 25 mA
10	V_ANT	I	Power supply for an active antenna	Up to +12 V DC / max. 25 mA
11	RF_GND		Analog ground	
12	RF_GND		Analog ground	
13	RF_IN	I	GPS signal from connected antenna	50 Ohms @ 1.575 GHz
14	GND		Digital ground	
15	GND		Digital ground	
16	GND		Digital ground	
17	GND		Digital ground	
18	GND		Digital ground	
19	GND		Digital ground	
20	GND		Digital ground	
21	GND		Digital ground	
22	GND		Digital ground	
23	GND		Digital ground	
24	GND		Digital ground	
25	GND		Digital ground	
26	GND		Digital ground	

Ball	Name	I/O	Description	Level
27	GND		Digital ground	
28	GND		Digital ground	
29	GND		Digital ground	
30	GND		Digital ground	
31	Vcca	O	Control output for RF part	+ 2.85 V DC / max. 25 mA
32	GPIO3	I/O	See chapter 6.8.4	CMOS
33	SDI2	I	Serial Data Input B	CMOS
34	SDO2	O	Serial Data Output B	CMOS
35	SDO1	O	Serial Data Output A	CMOS
36	SDI1	I	Serial Data Input A	CMOS
37	BOOT_SELECT	I	Boots in update mode, if high	CMOS
38	GND		Digital ground	
39	VCC	I	Main power supply	+ 3.3 V DC ±5 %
30	VCC	I	Main power supply	+ 3.3 V DC ±5 %
41	GND		Digital ground	
42	RFPC1	O	Control output for Trickle-Power Mode	+ 2.85 V DC / max. 25 mA
43	RFPC0	O	Control output for Trickle-Power Mode	+ 2.85 V DC / max. 25 mA
44	GPIO15	I/O	See chapter 6.8.4	CMOS
45	GPIO14	I/O	See chapter 6.8.4	CMOS
46	GPIO13	I/O	See chapter 6.8.4	CMOS
47	T-MARK	O	1 PPS Time Mark Output	CMOS
48	GND		Digital ground	

Table 5: Pin assignment of the JP7-TB

6.8 Pin assignment of the 50-pin connector

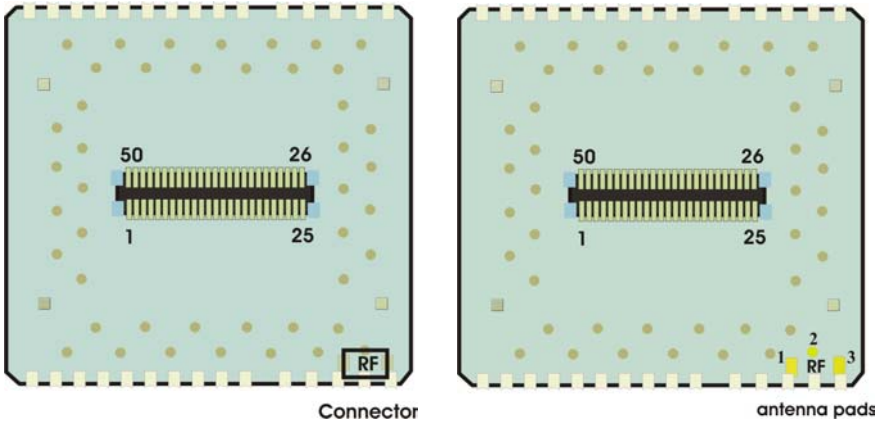


Figure 5: Pin out of the interface connector on the JP7-TC-1(-2)

Please note that, the JP7-TC-2 is without RF connector, and there is no antenna cable included in the delivery package. The pin assignment of 50-pin connector described in the table below is the same as JP7-TC-1.

PIN	Name	I/O	Description	Level
1	RFPC1	O	Control output for Trickle-Power Mode	+ 2.85 V DC / max. 25 mA
2	RFPC0	O	Control output for Trickle-Power Mode	+ 2.85 V DC / max. 25 mA
3	GPIO15	I/O	See chapter 6.8.4	CMOS
4	GPIO14	I/O	See chapter 6.8.4	CMOS
5	GPIO13	I/O	See chapter 6.8.4	CMOS
6	T-MARK	O	1 PPS Time Mark Output	CMOS
7	GPIO1	I/O	See chapter 6.8.4	CMOS
8	GPIO0	I/O	See chapter 6.8.4	CMOS
9	GPIO7	I/O	See chapter 6.8.4	CMOS
10	GPIO5	I/O	See chapter 6.8.4	CMOS
11	GPIO6	I/O	See chapter 6.8.4	CMOS
12	GPIO10	I/O	See chapter 6.8.4	CMOS
13	RESET_N	I	Reset the unit if Active Low	CMOS
14	V_BAT	I	Power for RTC and SRAM	+3 V DC ±5%

PIN	Name	I/O	Description	Level
15	V_BAT	I	Power for RTC and SRAM	+3 V DC ±5%
16	GND		Digital ground	
17	GND		Digital ground	
18	GND		Digital ground	
19	GND		Digital ground	
20	VC3.0	O	Supply voltage of RF section	+ 3.0 V DC / max. 25 mA
21	GND		Digital ground	
22	V_ANT	I	Power supply for an active antenna	Up to +12 V DC/ max. 25 mA
23	GND		Digital ground	
24	GND		Digital ground	
25	GND		Digital ground	
26	GND		Digital ground	
27	GND		Digital ground	
28	GND		Digital ground	
29	GND		Digital ground	
30	GND		Digital ground	
31	GND		Digital ground	
32	GND		Digital ground	
33	GND		Digital ground	
34	GND		Digital ground	
35	GND		Digital ground	
36	GND		Digital ground	
37	Vcca	O	Control output for RF part	+ 2.85 V DC / max. 25 mA
38	Vcca	O	Control output for RF part	+ 2.85 V DC / max. 25 mA
39	GPIO3	I/O	See chapter 6.8.4	CMOS

PIN	Name	I/O	Description	Level
40	SDI2	I	Serial Data Input B	CMOS
41	SDO2	O	Serial Data Output B	CMOS
42	SDO1	O	Serial Data Output A	CMOS
43	SDI1	I	Serial Data Input A	CMOS
44	BOOT_SELECT	I	Boots in update mode, if high	CMOS
45	VCC	I	Main power supply	+ 3.3 V DC ±5 %
46	VCC	I	Main power supply	+ 3.3 V DC ±5 %
47	VCC	I	Main power supply	+ 3.3 V DC ±5 %
48	VCC	I	Main power supply	+ 3.3 V DC ±5 %
49	VCC	I	Main power supply	+ 3.3 V DC ±5 %
50	VCC	I	Main power supply	+ 3.3 V DC ±5 %
Antenna pads on the JP7-TC-2, only				
1	RF_GND	-	Analog ground	-
2	RF_IN	I	GPS signal from connected antenna	50 Ohms @ 1.575 GHz
3	RF_GND	-	Analog ground	-

Table 6: Pin assignment of the JP7-TC-1(-2)

6.8.1 Configuration and timing signals

RESET_N — This pin provides an active-low reset input to the board. It causes the board to reset and to start searching for satellites. Reset is an optional input and, if not utilized, it may be left open.

T-MARK — This pin provides 1 pulse per second output from the board, which is synchronized to within 1 microsecond of GPS time. The output is a CMOS level signal.

BOOT_SELECT — Set this Pin to high (+3.3 V DC) for reprogramming the flash of the JP7-T (for instance updating a new firmware for the JP7-T).

RFPC0 — RFPC0 pin is provided to the JP7-TB and JP7-TC module. This pin is a control output for the Trickle-Power Mode. A possible circuit is shown in figure below. If the LED lights permanently the GPS

receiver is searching satellites. Is the GPS receiver in Trickle-Power Mode, the LED flashes in rhythm, i.e. the GPS receiver receives valid positions data (see also figure 6).

Note: By switched off Trickle power the LED will flash permanently. The reception of satellites data can be checked by using the T-Mark, however, can not be evaluated.

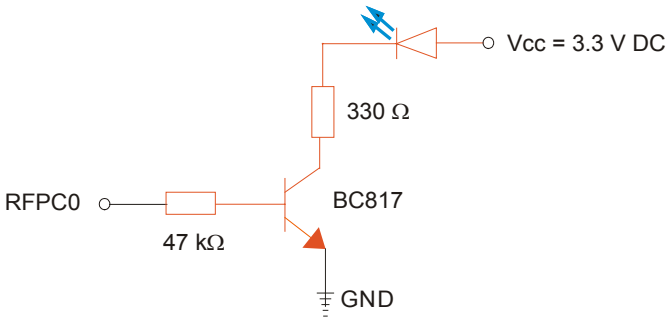


figure 6: The control output for Trickle-Power Mode.

6.8.2 Serial communication signals

The board supports two full duplex serial channels. All serial connections are at CMOS levels. If you need different voltage levels, use appropriate level shifters, (e.g. MAX 3232 from Maxim) in order to obtain RS-232 compatible signal levels (se also chapter 10). All supported variable baud rates and all can be controlled from the appropriate screens in SiRFdemo software. You can directly communicate with a PC serial port.

SDI1	This is the main receiving channel and is used to receive software commands to the board from SiRFdemo software or from user written software.
SDI2	This is the auxiliary receiving channel and is used to input differential corrections to the board to enable DGPS navigation.
SDO1	This is the main transmitting channel and is used to output navigation and measurement data to SiRFdemo or user written software.
SDO2	For user's application.

6.8.3 DC input signals

VCC	This is the main DC power supply for 3,3 V powered board JP7-T family.
RF_IN	Active antennas have an integrated low-noise amplifier. They can be directly connected to this pin (**RF_IN)**. If an active antenna is connected to **RF_IN**, the integrated low-noise amplifier of the antenna needs to be supplied with the correct voltage through pin **V_ANT**. **Caution:** Do not connect or disconnect the antenna when the JP7-T family is running. **Caution:** The RF_IN is always fed from the input voltage on the V_ANT. Do not use any input voltage on this pin
V_ANT	This pin is an input and reserved for an external DC power supply for an active antenna. The antenna bias for an external active antenna can be provided in two way to pin **V_ANT**. In order to use a 5 V or 12 V active GPS antenna, the **V_ANT** has to be connected to 5 V, 12 V external power supply respectively. The other possibility is available when you connect the **VC3.0** output (which provides 3.0 V) to **V_ANT**, so that an antenna with 3.0 V supply voltage can be used. Hint: The input voltage on the **V_ANT** should be chosen in according to the antenna to be used. **Note: The GPS receiver JP7-T family has to be connected with an active 3 V GPS antenna (max. current of 25 mA). The antenna voltage is provided by the internal power management.**
VC3.0	This pin is an output which provides +3.0 V DC, and can be connected to the V_ANT, to supply the connected GPS antenna. In Trickle Operation and Push-To-Fix operation, VC3.0 is switched off when the receiver sets itself into the sleep mode. When the receiver wakes up the VC3.0 is switched on.

6.8.4 General purpose input/output

Several I/O's (GPIO0, GPIO1, GPIO3, GPIO5, GPIO6, GPIO7, GPIO10, GPIO13, GPIO14, GPIO15, please refer to the tables 4, 5, 6) of the CPU are connected to the hardware interface connector of the JP7-T family. They are reserved for customer specific applications.
For example:

- For realization a SPI-Bus
- For realization an Antenna-indication.

These pins are not supported by the current GPS firmware.

7 Software interface

The FALCOM JP7-T family supports NMEA-0183 and SiRF binary protocols. A short description of these protocols are provided herein.
For more detailed information please refer to the SiRFstarII message set specification available in the section "service/downloads/manuals" at FALCOM homepage.

7.1 SiRF binary data message

Table 7 lists the message list for the SiRF output messages.

Hex	ASCII	Name	Description
0 x 02	2	Measured Navigation Data	Position, velocity and time
0 x 03	3	True Tracker Data	Not implemented
0 x 04	4	Measured Tracking Data	Satellite and C/No information
0 x 06	6	SW Version	Receiver software
0 x 07	7	Clock Status	Current clock status
0 x 08	8	50 BPS Subframe Data	Standard ICD format
0 x 09	9	Throughput	Navigation complete data
0 x 0A	10	Error ID	Error coding for message failure
0 x 0B	11	Command Acknowledgement	Successful request
0 x 0C	12	Command No Acknowledgement	Unsuccessful request
0 x 0D	13	Visible List	Auto Output
0 x 0E	14	Almanac Data	Response to Poll
0 x 0F	15	Ephemeris Data	Response to Poll
0 x 10	16	Test Mode 1	For use with SiRFtest (Test Mode 1)
0 x 11	17	Differential Corrections	Received from DGPS broadcast
0 x 12	18	Ok To Send	CPU ON/OFF (Trickle Power)
0 x 13	19	Navigation Parameters	Response to Poll
0 x 14	20	Test Mode 2	Additional test data (Test Mode 2)
0 x 1C	28	Nav. Lib. Measurement Data	Measurement Data

Hex	ASCII	Name	Description
0 x 1D	29	Nav. Lib. DGPS Data	Differential GPS Data
0 x 1E	30	Nav. Lib. SV State Data	Satellite State Data
0 x 1F	31	Nav. Lib. Initialization Data	Initialization Data
0 x FF	255	Development Data	Various status messages

Table 7: SiRF Output Messages

Table 8: lists the message list for the SiRF input messages.

Hex	ASCII	Name	Description
0 x 55	85	Transmit Serial Message	User definable message
0 x 80	128	Initialize Data Source	Receiver initialization and associated parameters
0 x 81	129	Switch to NMEA Protocol	Enable NMEA message, output rate and baud rate
0 x 82	130	Set Almanac (upload)	Sends an existing almanac file to the receiver
0 x 84	132	Software Version (Poll)	Polls for the loaded software version
0 x 85	133	DGPS Source Control	DGPS correction source and beacon receiver information
0 x 86	134	Set Main Serial Port	Baud rate, data bits, stop bits and parity
0 x 87	135	Switch Protocol	Obsolete
0 x 88	136	Mode Control	Navigation mode configuration
0 x 89	137	DOP Mask Control	DOP mask selection and parameters
0 x 8A	138	DGPS Mode	DGPS mode selection and timeout value
0 x 8B	139	Elevation Mask	Elevation tracking and navigation masks
0 x 8C	140	Power Mask	Power tracking and navigation masks
0 x 8D	141	Editing Residual	Not implemented
0 x 8E	142	Steady-State Detection – not used	Not implemented

Hex	ASCII	Name	Description
0 x 8F	143	Static Navigation	Configuration for static operation
0 x 90	144	Poll Clock Status (Poll)	Polls the clock status
0 x 91	145	Set DGPS Serial Port	DGPS port baud rate, data bits, stop bits and parity
0 x 92	146	Poll Almanac	Polls for almanac data
0 x 93	147	Poll Ephemeris	Polls for ephemeris data
0 x 94	148	Flash Update	On the fly software update
0 x 95	149	Set Ephemeris (upload)	Sends an existing ephemeris to the receiver
0 x 96	150	Switch Operating Mode	Test mode selection, SV ID and period
0 x 97	151	Set Trickle Power Parameters	Push to fix mode, duty cycle and on time
0 x 98	152	Poll Navigation Parameters	Polls for the current navigation parameters
0 x A5	165	Set UART Configuration	Protocol selection, baud rate, data bits, stop bits and parity
0 x A6	166	Set Message Rate	SiRF binary message output rate
0 x A7	167	Low Power Acquisition Parameters	Low power configuration parameters
0 x B6	182	Set UART Configuration	Obsolete

Table 8: SiRF Input Messages

7.2 NMEA data message

The SiRFstarIIe evaluation receiver is capable of outputting data in the NMEA-0183 format as defined by the National Marine Electronics Association (NMEA), Standard for Interfacing Marine Electronic Devices, Version 2.20, January 1, 1997.

7.2.1 NMEA output messages

Table 9 lists all NMEA output messages supported by SiRFstarIIe evaluation receiver and a brief description.

Option	Description
GGA	Time, position and fix type data.
GLL	Latitude, longitude, UTC time of position fix and status.
GSA	GPS receiver operating mode, satellites used in the position solution and DOP values.
GSV	The number of GPS satellites in view satellite ID numbers, elevation, azimuth and SNR values.
MSS	(This message can be switched on via SiRFdemo software) Signal-to-noise ratio, signal strength, frequency and bit rate from a radio-beacon receiver.
RMC	Time, date, position, course and speed data.
VTG	Course and speed information relative to the ground.

Table 9: NMEA Output Messages

7.2.2 NMEA input messages

Message	MID[1]	Description
Set Serial Port	100	Set PORT A parameters and protocol
Navigation Initialization	101	Parameters required for start using X/Y/Z[2]
Set DGPS Port	102	Set PORT B parameters for DGPS input
Query/Rate Control	103	Query standard NMEA message and/or set output rate
LLA Navigation Initialization	104	Parameters required for start using Lat/Lon/Alt[3]
Development Data On/Off	105	Development Data messages On/Off
MSK Receiver Interface	MSK	Command message to a MSK radio-beacon receiver.

Table 10: NMEA Input Messages

1. Message Identification (MID).
2. Input co-ordinates must be WGS84.
3. Input co-ordinates must be WGS84.

Note: NMEA input messages 100 to 105 are SiRF proprietary NMEA messages. The MSK NMEA string is as defined by the NMEA 0183 standard.

7.2.3 Transport Message

Start Sequence	Payload	Checksum	End Sequence
$PSRF<MID>[1]	Data[2]	*CKSUM[3]	<CR> <LF>[4]

1. Message Identifier consisting of three numeric characters. Input messages begin at MID 100.
2. Message specific data. Refer to a specific message section for <data>...<data>definition.
3. CHECKSUM is a two-hex character checksum as defined in the NMEA specification. Use of checksums is required on all input messages.
4. Each message is terminated using Carriage Return (CR) Line Feed (LF) which is \r\n which is hex 0D 0A. Because \r\n are not printable ASCII characters, they are omitted from the example strings, but must be sent to terminate the message and cause the receiver to process that input message.

CheckSum

The checksum is 15-bit checksum of the bytes in the payload data. The following pseudo code defines the algorithm used.
Let message to be the array of bytes to be sent by the transport.
Let ***msgLen*** *be the number of bytes in the message array to be transmitted.*
Clearly to say, the string over which the checksum has to be calculated is between the "$" and "*" (without characters "$" and "").*

Index = first
checkSum = 0
while index < msgLen
checkSum = checkSum + message[index]
checkSum = checkSum AND (2^{15}-1).

Note: All fields in all proprietary NMEA messages are required, none are optional. All NMEA messages are comma delimited.

8 Mechanical draw

The following chapters describe the mechanical dimensions of JP7-T family and give recommendations for integrating JP7-T family into the user application. Note that, the absolute maximum dimension for all modules (JP7-T, JP7-TB, JP7-TC-1, JP7-TC-2) is: 25.4 mm x 25.4 mm (L x B).
Figure 7 shows the top view on JP7-T family (without connectors) and provides an overview of the mechanical dimensions of the board.
Please note that, the JP7-T family has a dimension tolerance from ±0.1 mm.

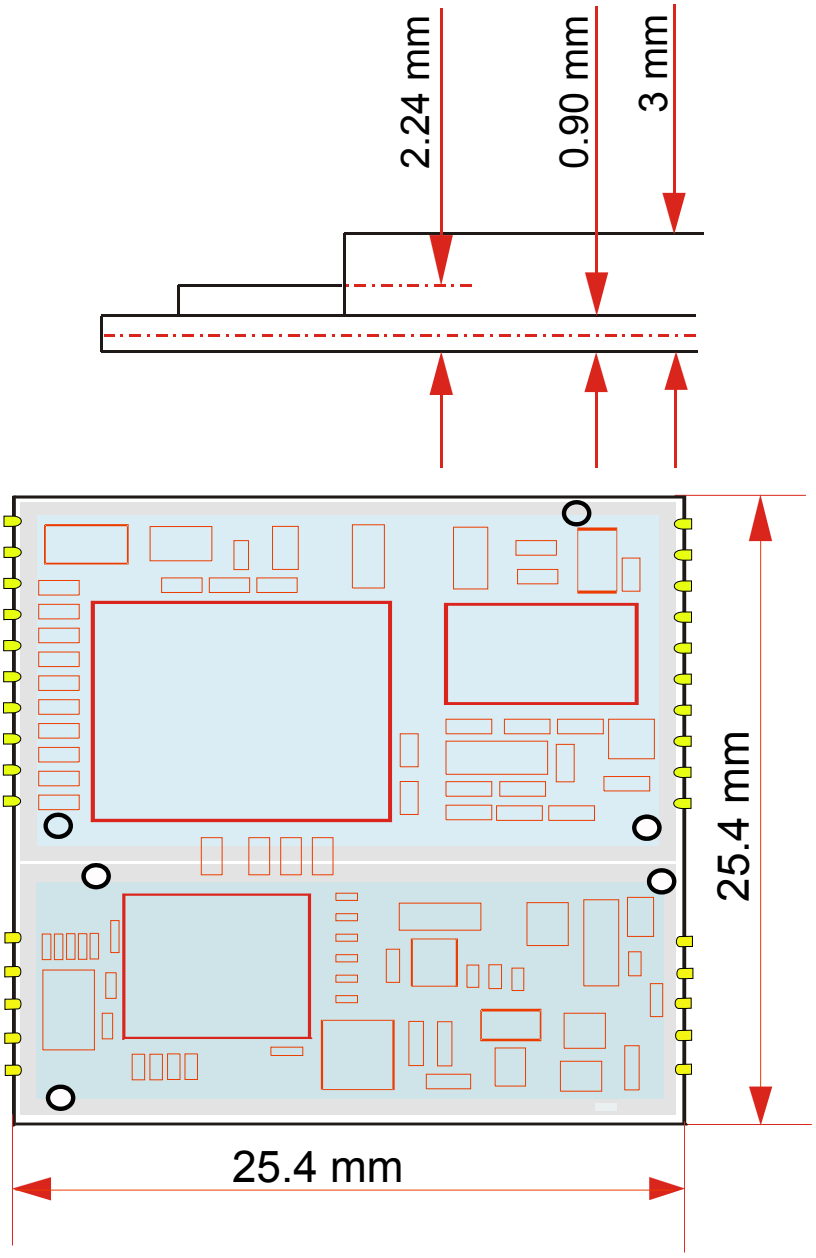


Figure 7: The mechanical draw of the JP7-T family

Figure 8 shows the bottom view on JP7-TB and provides an overview of the mechanical dimensions of the pointed balls.

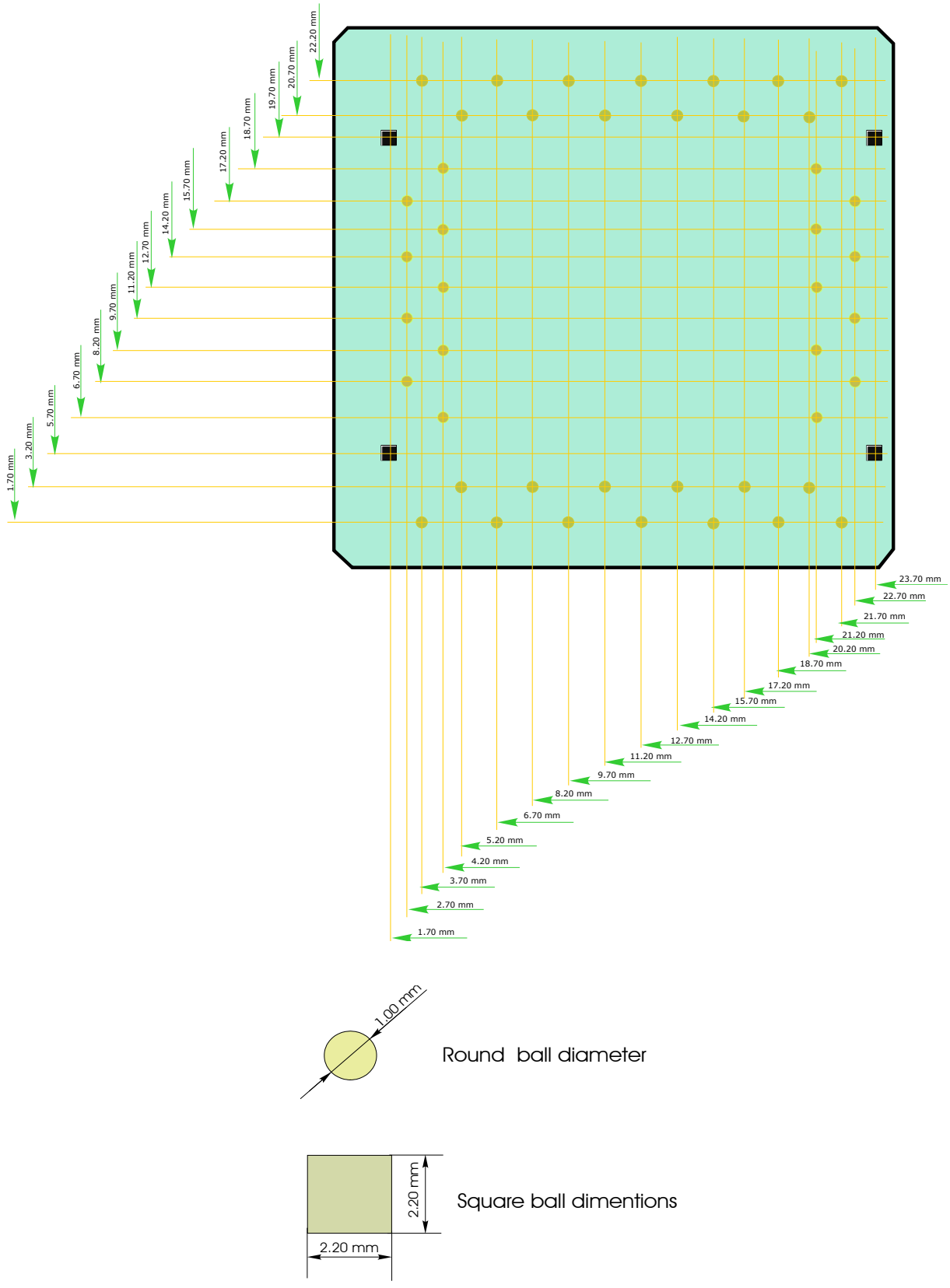


Figure 8: The mechanical draw of the JP7-TB

Figure 9 shows the bottom view on JP7-TC-1(-2) and provides an overview of the mechanical dimensions of the integrated 50-pin connector and RF connector.

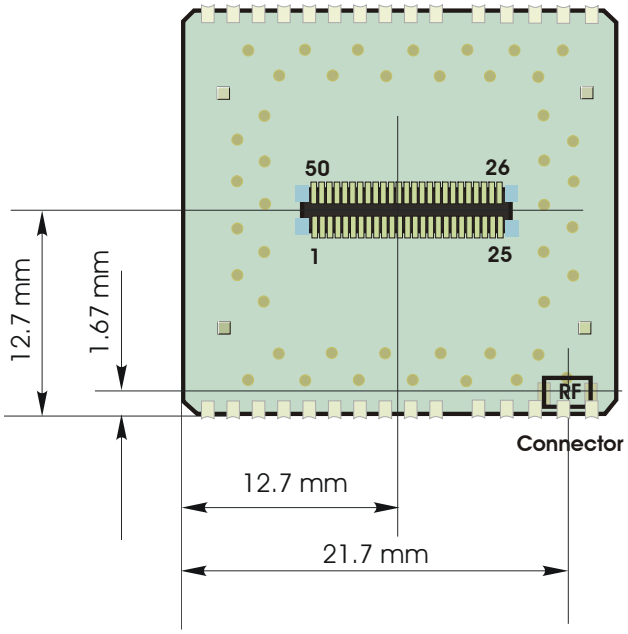


Figure 9: The mechanical draw of the JP7-TC-1

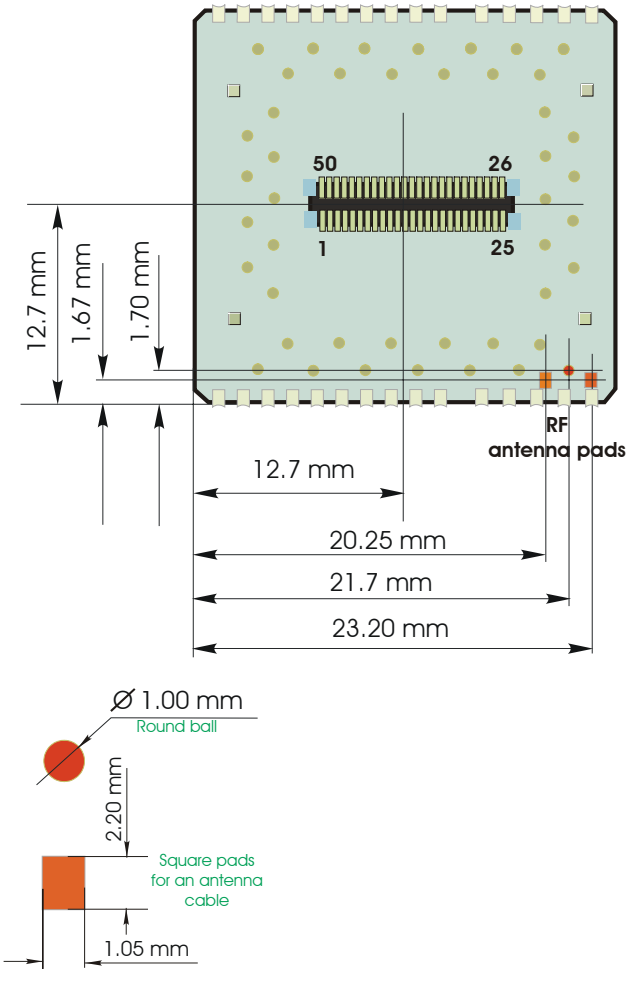


Figure 10: The mechanical draw of the JP7-TC-2

9 Layout recommendation

9.1 Ground planes

JP7-T GPS receiver needs two different ground planes. The pins RF_GND (Pins 11, 12, 13, 14, 15, 16, 18) shall be connected to analog ground, the pins GND (Pins 2, 10, 30) to digital ground.

The two ground planes shall be separated :

- the planes are connected inside the receiver (see Figure 11).

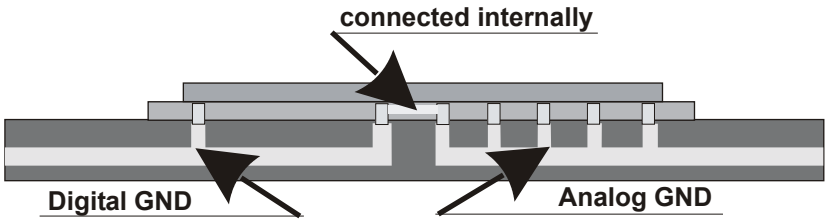


Figure 11: Ground plane of the JP7-T family GPS receiver

9.2 RF connection

The JP7-T family GPS receiver is designed to be functional by using either a passive patch antenna or an antenna connector with standard RF cables. In order to make a RF connection properly, the user has to connect the antenna points or the pins of the connector to the RF pin (pin 17) and RF grounds (GND's of RF part), respectively (see Figure 11)

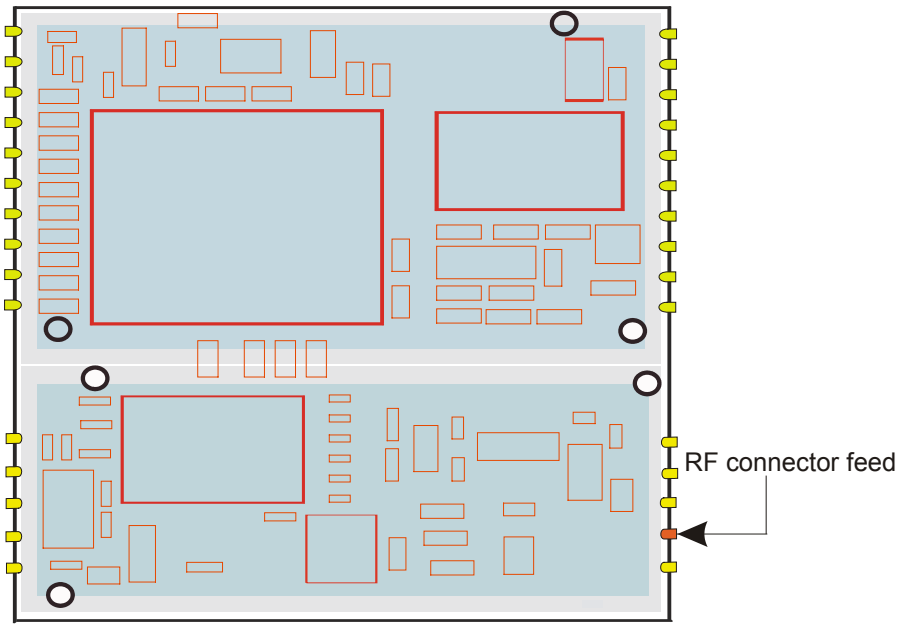


Figure 12: RF connection to antenna feed of the JP7-T GPS receiver.

To make a properly antenna connection to the antenna pads (available on bottom side of JP7-TC-2, only) refer to the figure below which shows their position and pin name (refer also on the table 6).

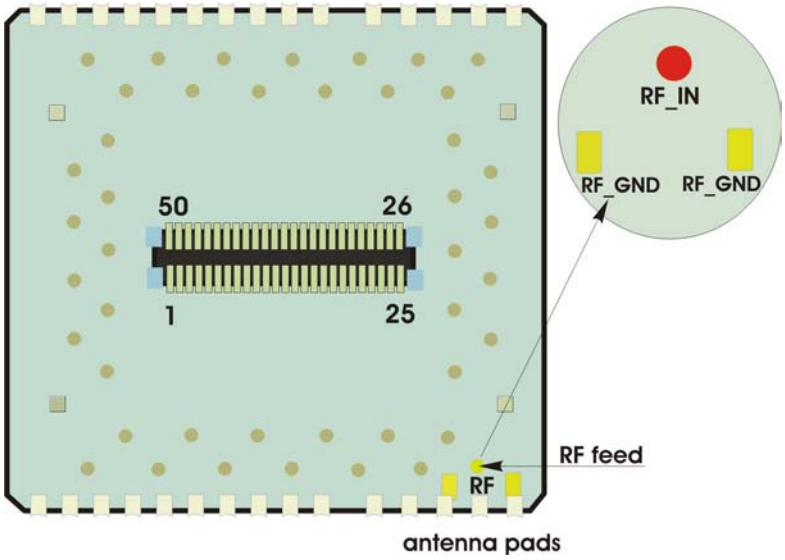


Figure 13: RF connection to antenna feed of the JP7-TC-2 GPS receiver.

Recommendations for layout, and soldering.
Please note that, the dimension tolerance is ±0.1 mm.

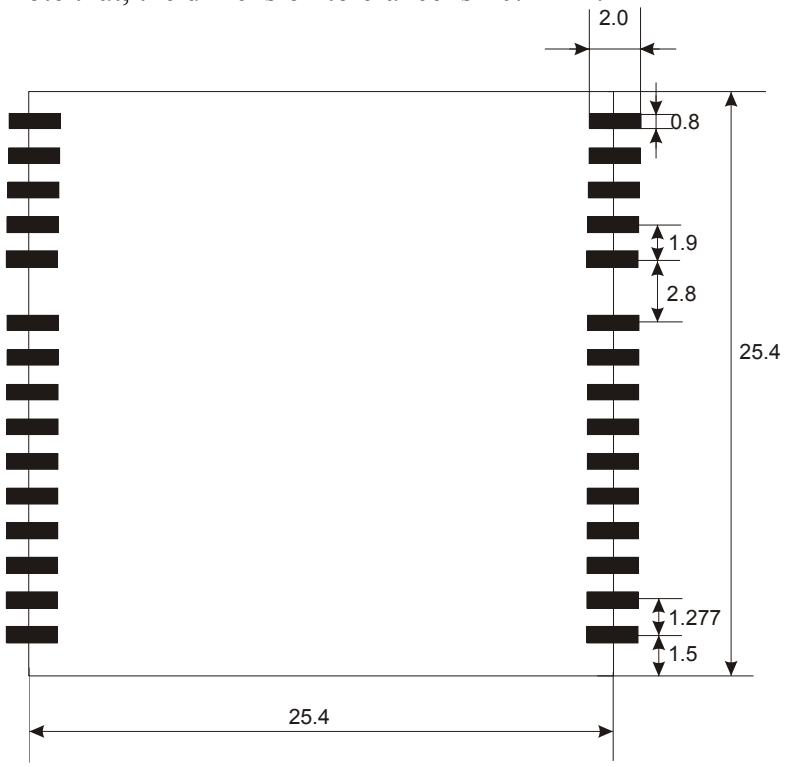


Figure 14: Recommendations for layout.

Recommended soldering reflow profile for JP-T family mounting on PCB

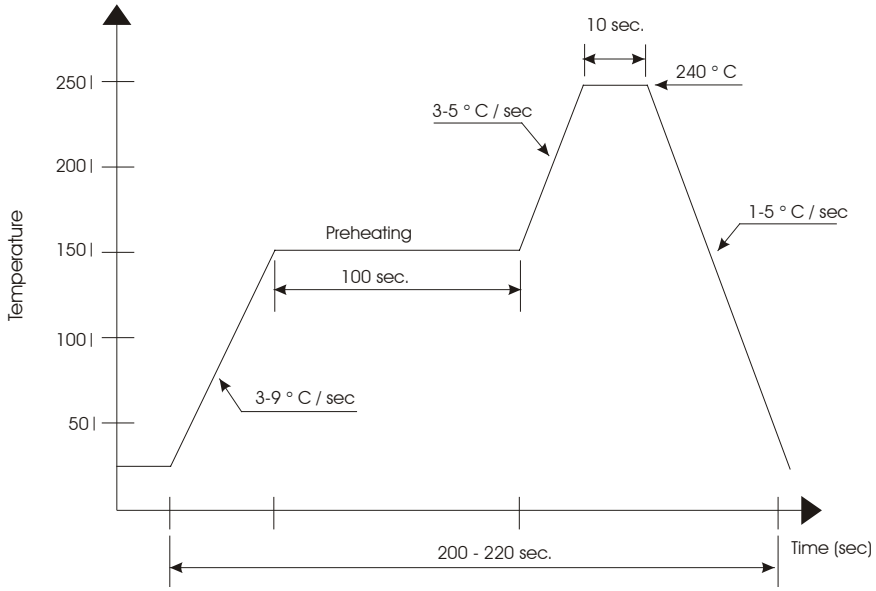


Figure 15: Typical solder conditions (temperature profile, reflow conditions).

Consider for a long time in the soldering zone (with temperature higher than 180°C) has to be kept as short as possible to prevent component and substrate damages. Peak temperature must not exceed 240°C. JP7-T family are able to withstand twice the previous recommended reflow profile in order to be compatible with a double reflow when SMDs are mounted on both sides of the PCB. A maximum of two soldering reflows are allowed for these packages. The use of a no clean flux is highly recommended to avoid any cleaning operation. In order to prevent any bump cracks, ultrasonic cleaning methods are not recommended.

10 First steps to make it work

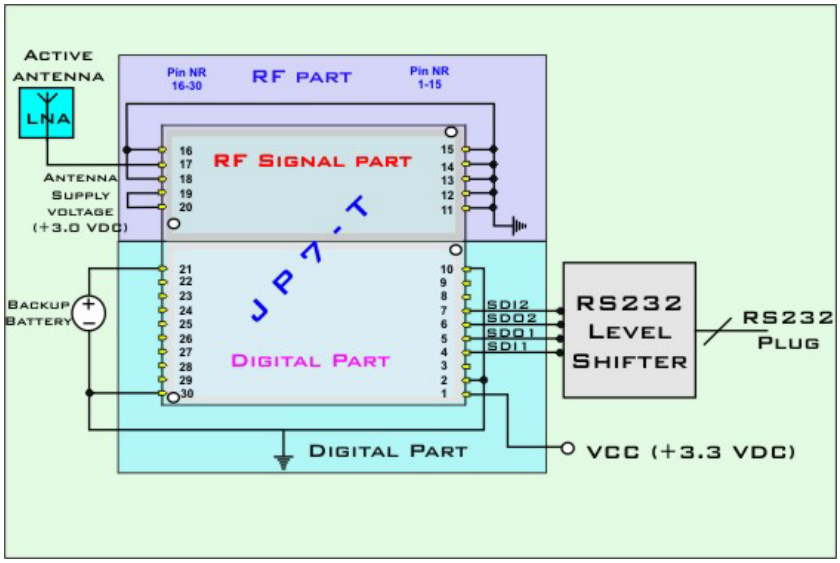


Figure 16 : The minimum hardware interface of JP7-T to get started.

- **Antenna**: The antenna connection is the most critical part of PCB routing. Previously placing the JP7-T on the PCB secure that the connection to the antenna signals is routed. In order to make it properly functional a control impedance line has to connect the RF_IN signal with antenna feed points or antenna connector, respectively. The routing on the PCB depends on your choice.

- **Power:** The input power is also very important as far as the minimum and maximum voltage is concerned. The power supply of JP7-T family has to be a single voltage source of VCC at 3.3 VDC. The power supply has to be able to provide a sufficient current which typically rises to 200 mA. Please, connect GND pins to ground, and connect the line which supply the VCC pin to +3.3 V, properly. If they are correctly connected, a proper RESET signal is internally generated the board is full powered and the unit begins obtaining its position fix.

- **Serial Interface:** The JP7-T family provides two serial interfaces. Each interface is provided with two-wire the SDI1, SDO1 supports line and ground for the first serial interface (port A) and SDI2, SDO2 supports line and ground for the second serial interface (port B). These pins are both 3.3 V CMOS and 5 V TTL compatible. In order to use different voltage levels, a appropriate level shifters has to be used.
  E. g. in order to provide RS232 compatible levels use the 3 V compatible MAX3232 transceiver from Maxim or others based on the required levels. The GPS data will be transmitted through port A (first serial port), if an active antenna is connected, which has a good view to sky (no obstacle). You

can use port B (second serial port) to feed in DGPS correction data. Pull-up (100 kΩ) unused SDI inputs.

- **Active Antenna Bias Voltage:** The output voltage at the antenna cable can be used to power the bias voltage of the antenna, provided can make sure that the antenna runs down to 2.7 V bias voltage and the current does not exceed 20 mA.

- **Backup Battery:** In order to allow the GPS receiver to perform internally the warm and hot start it is advisable to connect the **V_BAT** pin to an external backup battery**.** For more information on cold, warm, and hot-start scenarios, please refer to the Section 6.3 " Start-Up". In case of a power interruption on pin **VCC** the real-time clock and backed-up SRAM are continually supplied through **V_BAT**. The voltage at this pin has to be +3 V DC ±5%. If you do not use a backup battery, connect this pin to GND or leave it open. Do not use a super cap for the battery backup supply (recommended by SiRF).

The quickest way to get first results with the JP7-T is to use the JP7-T Evaluation board together with the program SiRFdemo.

Figure 17: JP7-T Evaluation board

The Evaluation board contains:

- Evaluation Box
- JP7-T sample with soldered antenna cable.
- power supply (AC/DC adapter, Type FW738/05, Output 5VDC 1.3 A)
- active GPS antenna (FAL-ANT-3)
- RS232 level shifter
- RS232 cable to your computer.

The Evaluation board with contained components are not included in the delivery package. In order to have one the users of JP7-T family have to purchase it.

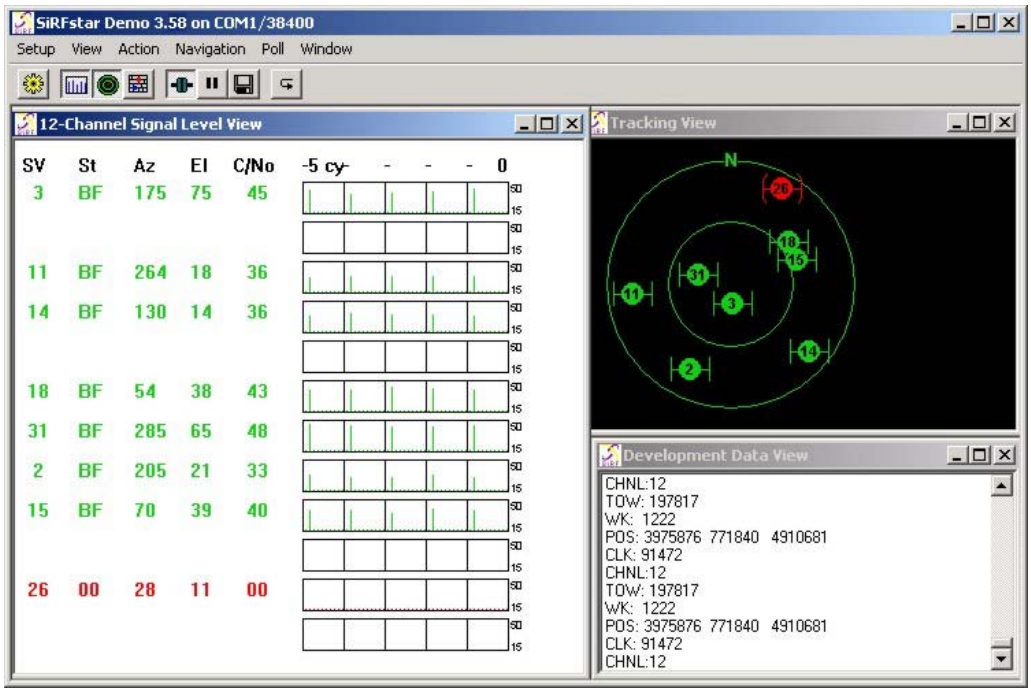


Figure 18: Example of using of the SiRFdemo

The SiRFdemo manual and software are available on the Falcom's Website for free download:

➔ www.falcom.de/service/downloads/manual/SiRF/SiRFdemo.pdf
➔ www.falcom.de/service/downloads/manual/SiRF/SiRFdemo.zip

11 Appendix

11.1 Board-to-board connector

This chapter provides specifications for the 50-pin board-to-board connector which serves as physical interface to the host application. The receptacle assembled on the JP7-TC is type Hirose DF12C. Mating headers from Hirose are available in different stacking heights.

Figure 19.a: Hirose DF12C receptacle on JP7-TC

Figure 19.b: Header Hirose DF12C

11.2 RF connector

The JP7-TC uses an ultra-miniature SMT antenna connector supplied from Hirose Ltd.
The product name is:

- **U.FL-R-SMT**

The position of the antenna connector on the JP7-TC board has to be seen on bottom side on the upper right corner.
Mating plugs and cables can be chosen from the Hirose U.FL Series. Examples are shown in figure below. For latest product information please contact your Hirose dealer or visit the Hirose home page, for example http://www.hirose.com.

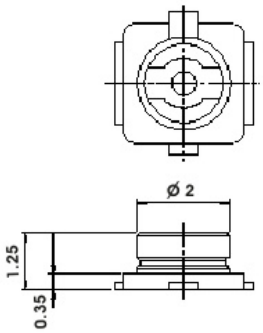


Figure 20: Mechanical dimensions of U.FL-R-SMT connector with U.FL-LP-040 plug

11.3 Firmware Interface

The table below shows supported SiRF firmware versions into the JP7-T family devices.

GPS Receiver	Supported SiRF internal firmware version			
	2.20	2.32	SiRFXTrac2	SiRFDrive
JP7-T	X	X	X	
JP7-TB	X	X	X	X
JP7-TC-1	X	X	X	X
JP7-TC-2	X	X	X	X

11.4 XTrac firmware description

The JP7-T family using SiRFXTrac2 software offers high position accuracy and fast Time-To-First-Fix (TTFF) than is currently possible with other autonomous GPS solution. This means that the JP7-T family will continue to determinate its positions or obtain an initial fix in places where previously not possible. When the GPS receiver loaded with SiRFXTrac2 is initially turned on, it begins to determinate its current positions, velocity and time which will be calculated from tracking the GPS signals an extremely small level by 16 dBHz. While trying to calculate a position fix, the receiver needs to be locked-on to at least four satellites. Your position can be extremely quick fixed within 4 seconds instead of within 8 seconds using other GPS software from a "hot-start" state, and within 45 seconds from a "cold-start" state.
As a general note, the SiRFdemo v3.61 supports the additional functionality and configuration of SiRFXTrac2.
This software is now available on the Falcom's Website for free download:
➔ www.falcom.de/service/downloads/manual/SiRF/SiRFdemo3.61.zip

11.4.1 SiRFXTrac2 firmware default settings

All GPS units which use the SiRFXTrac2 firmware version have the following settings on serial interfaces:

SDI1/SDO1 (first serial port):
NMEA 38400 baud, Msg.: GLL, GGA, RMC, VTG, GSV, GSA
8 data bits, no parity, 1 stop bit

SDI2/SDO2(second serial port):
RTCM, 38400 baud

11.4.2 Order options

As far as the SiRFXTrac2 firmware is concerned the products listed below with specific requirements are also available upon request:

Name		Using firmware version	Options
JP7-TX		SiRFXTrac2	30-pin out on the left and right side of JP7-T are available for use
JP7-TBX		SiRFXTrac2	48 Balls are available for use
JP7-TCX	JP7-TCX-1	SiRFXTrac2	A 50-pin connector and a RF connector are available for use
	JP7-TCX-2	SiRFXTrac2	A 50-pin connector and solder pads for an antenna cable are available for use. There is no antenna cable included in the delivery package.