REGISTER 20-1: ADCON0: A/D CONTROL REGISTER 0 (ACCESS FC2h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VCFG1	VCFG0	CHS3(2)	CHS2(2)	CHS1(2)	CHS0(2)	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **VCFG1:** Voltage Reference Configuration bit (V_{REF-} source)
1 = V_{REF-} (AN2)
0 = AV_{SS}

bit 6 **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)
1 = V_{REF+} (AN3)
0 = AV_{DD}

bit 5-2 **CHS<3:0>:** Analog Channel Select bits(2)
0000 = Channel 00 (AN0)
0001 = Channel 01 (AN1)
0010 = Channel 02 (AN2)
0011 = Channel 03 (AN3)
0100 = Channel 04 (AN4)
0101 = Channel 05 (AN5)(1)
0110 = Channel 06 (AN6)(1)
0111 = Channel 07 (AN7)(1)
1000 = Channel 08 (AN8)
1001 = Channel 09 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12)
1101 = (Reserved)
1110 = V_{DDCORE}
1111 = V_{BG} Absolute Reference (~1.2V)(3)

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit
1 = A/D Converter module is enabled
0 = A/D Converter module is disabled

REGISTER 20-2: ADCON1: A/D CONTROL REGISTER 1 (ACCESS FC1h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCAL	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **ADCAL:** A/D Calibration bit
1 = Calibration is performed on next A/D conversion
0 = Normal A/D Converter operation

bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits
111 = 20 T_{AD}
110 = 16 T_{AD}
101 = 12 T_{AD}
100 = 8 T_{AD}
011 = 6 T_{AD}
010 = 4 T_{AD}
001 = 2 T_{AD}
000 = 0 T_{AD}

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits
110 = $F_{OSC}/64$
101 = $F_{OSC}/16$
100 = $F_{OSC}/4$
011 = F_{RC} (clock derived from A/D RC oscillator)(1)
010 = $F_{OSC}/32$
001 = $F_{OSC}/8$
000 = $F_{OSC}/2$

REGISTER 20-3: ANCON0: A/D PORT CONFIGURATION REGISTER 2 (BANKED F48h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG7(1)	PCFG6(1)	PCFG5(1)	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PCFG<7:0>:** Analog Port Configuration bits (AN<7:0>)
1 = Pin configured as a digital port
0 = Pin configured as an analog channel – digital input disabled and reads '0'

Note 1: These bits are not implemented on 28-pin devices.

REGISTER 20-4: ANCON1: A/D PORT CONFIGURATION REGISTER 1 (BANKED F49h)

R/W-0	r	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VBGEN	—	—	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8
bit 7							bit 0

Legend:	r = Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **VBGEN:** 1.2V Band Gap Reference Enable bit
1 = 1.2V band gap reference is powered on
0 = 1.2V band gap reference is turned off to save power (if no other modules are requesting it)

bit 6 **Reserved:** Always maintain as '0' for lowest power consumption

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **PCFG<12:8>:** Analog Port Configuration bits (AN<12:8>)
1 = Pin configured as a digital port
0 = Pin configured as an analog channel – digital input disabled and reads '0'