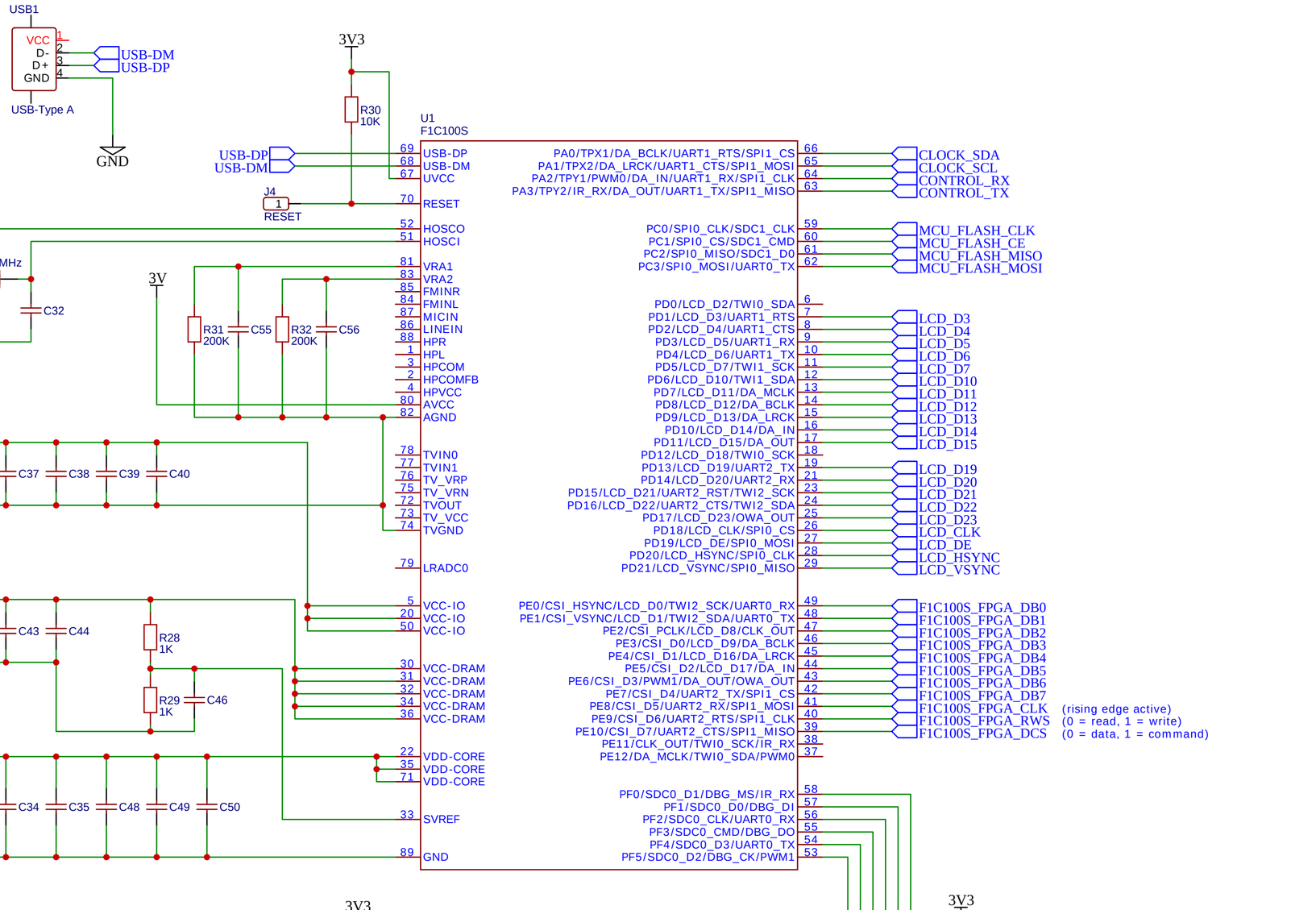
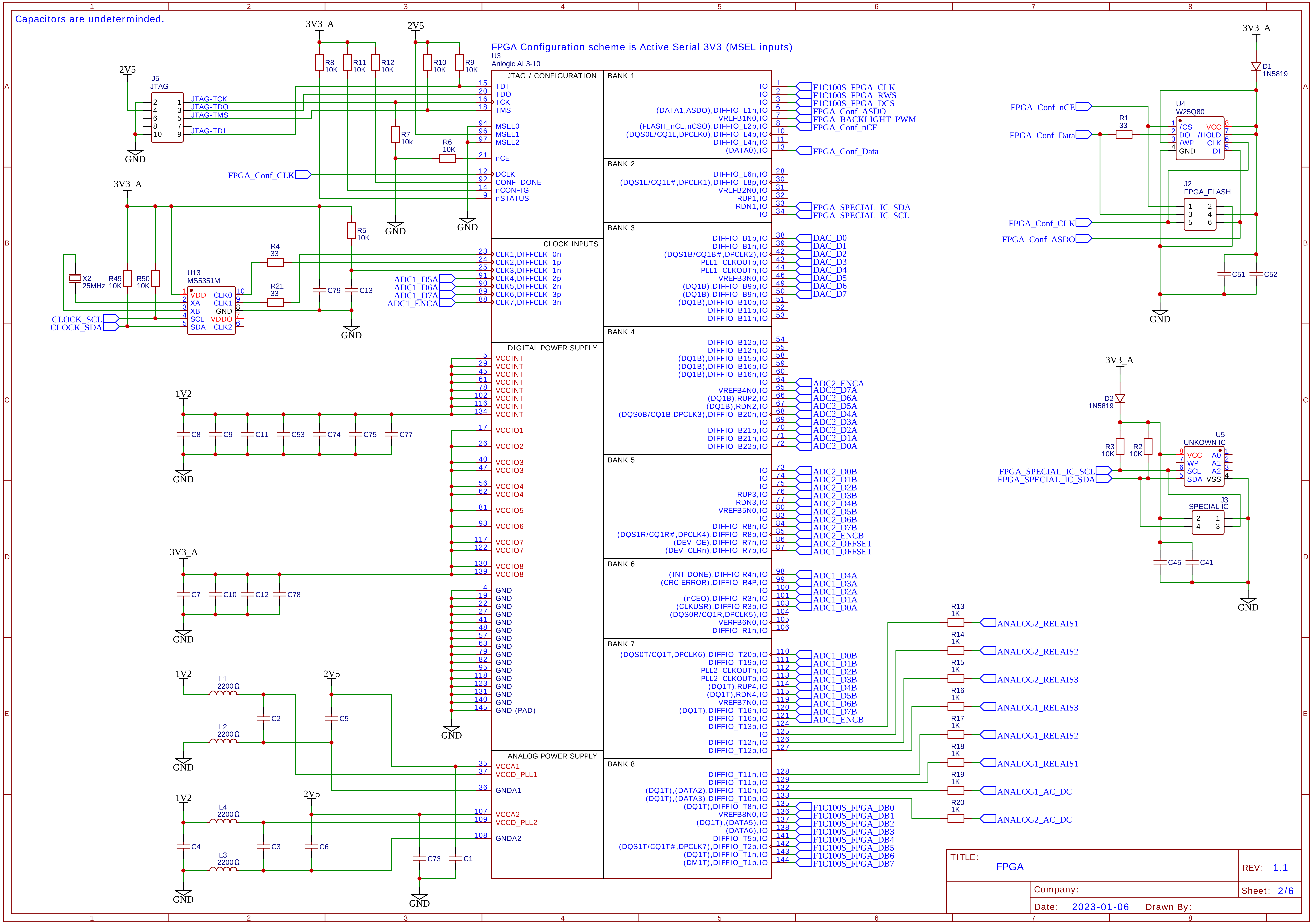
Capacitors are undeterminded.



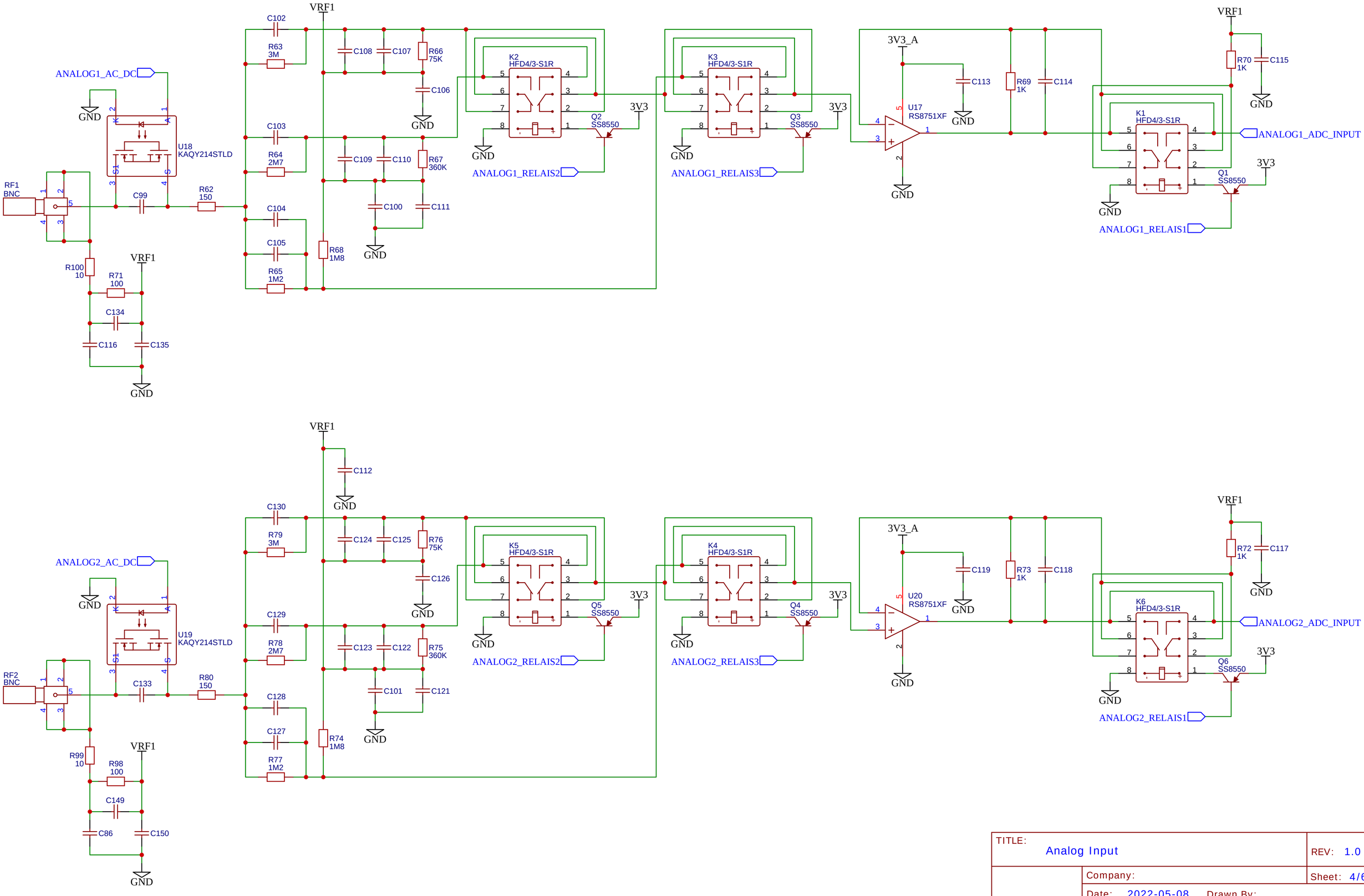
FLASH CONNECTOR PINOUT	
PIN	FUNCTION
1	SPI-CE
2	GND
3	SPI-MISO
4	3V3
5	SPI-CLK
6	SPI-MOSI

TITLE: Processor		REV: 1.0
	Company:	Sheet: 1/6
	Date: 2022-05-08 Drawn By:	



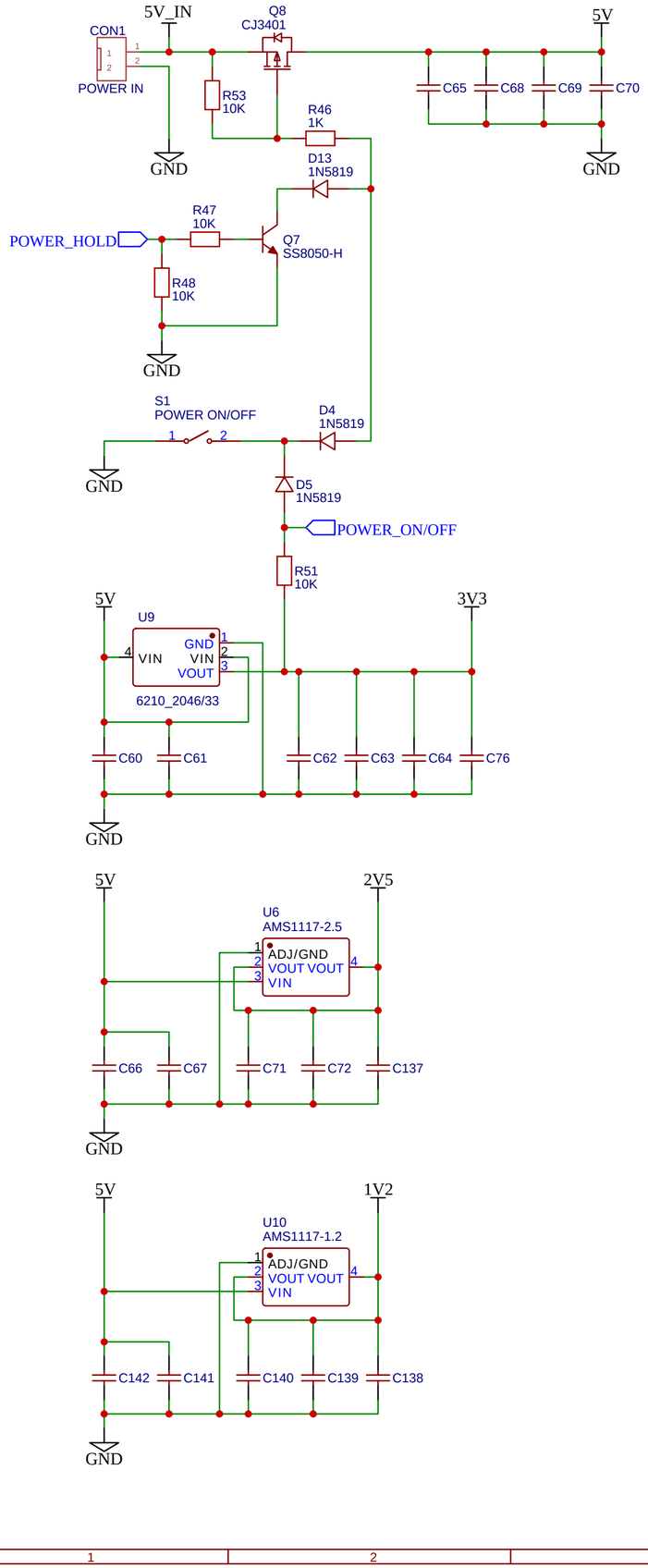
Capacitors are undetermined.
FPGA Configuration scheme is Active Serial 3V3 (MSEL inputs)
U3
Anlogic AL3-10
JTAG / CONFIGURATION
BANK 1
BANK 2
BANK 3
BANK 4
BANK 5
BANK 6
BANK 7
BANK 8
CLOCK INPUTS
DIGITAL POWER SUPPLY
ANALOG POWER SUPPLY
TDI
TDO
TCK
TMS
MSEL0
MSEL1
MSEL2
nCE
DCLK
CONF_DONE
nCONFIG
nSTATUS
CLK1,DIFFCLK_0n
CLK2,DIFFCLK_1p
CLK3,DIFFCLK_1n
CLK4,DIFFCLK_2p
CLK5,DIFFCLK_2n
CLK6,DIFFCLK_3p
CLK7,DIFFCLK_3n
VCCINT
VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO8
GND
GND (PAD)
VCCA1
VCCD_PLL1
GNDA1
VCCA2
VCCD_PLL2
GNDA2
(DATA1,ASDO),DIFFIO_L1n,IO
VREFB1N0,IO
(FLASH_nCE,nCSO),DIFFIO_L2p,IO
(DQS0L/CQ1L,DPCLK0),DIFFIO_L4p,IO
DIFFIO_L4n,IO
(DATA0),IO
DIFFIO_L6n,IO
(DQS1L/CQ1L#,DPCLK1),DIFFIO_L8p,IO
VREFB2N0,IO
RUP1,IO
RDN1,IO
DIFFIO_B1p,IO
DIFFIO_B1n,IO
(DQS1B/CQ1B#,DPCLK2),IO
PLL1_CLKOUTp,IO
PLL1_CLKOUTn,IO
VREFB3N0,IO
(DQ1B),DIFFIO_B9p,IO
(DQ1B),DIFFIO_B9n,IO
(DQ1B),DIFFIO_B10p,IO
DIFFIO_B11p,IO
DIFFIO_B11n,IO
DIFFIO_B12p,IO
DIFFIO_B12n,IO
(DQ1B),DIFFIO_B15p,IO
(DQ1B),DIFFIO_B16p,IO
(DQ1B),DIFFIO_B16n,IO
VREFB4N0,IO
(DQ1B),RUP2,IO
(DQ1B),RDN2,IO
(DQS0B/CQ1B,DPCLK3),DIFFIO_B20n,IO
DIFFIO_B21p,IO
DIFFIO_B21n,IO
DIFFIO_B22p,IO
RUP3,IO
RDN3,IO
VREFB5N0,IO
DIFFIO_R8n,IO
(DQS1R/CQ1R#,DPCLK4),DIFFIO_R8p,IO
(DEV_OE),DIFFIO_R7n,IO
(DEV_CLRn),DIFFIO_R7p,IO
(INT DONE),DIFFIO R4n,IO
(CRC ERROR),DIFFIO_R4P,IO
(nCEO),DIFFIO_R3n,IO
(CLKUSR),DIFFIO R3p,IO
(DQS0R/CQ1R,DPCLK5),IO
VERFB6N0,IO
DIFFIO_R1n,IO
(DQS0T/CQ1T,DPCLK6),DIFFIO_T20p,IO
DIFFIO_T19p,IO
PLL2_CLKOUTn,IO
PLL2_CLKOUTp,IO
(DQ1T),RUP4,IO
(DQ1T),RDN4,IO
VREFB7N0,IO
(DQ1T),DIFFIO_T16n,IO
DIFFIO_T16p,IO
DIFFIO_T13p,IO
DIFFIO_T12n,IO
DIFFIO_T12p,IO
DIFFIO_T11n,IO
DIFFIO_T11p,IO
(DQ1T),(DATA2),DIFFIO_T10n,IO
(DQ1T),(DATA3),DIFFIO_T10p,IO
(DQ1T),DIFFIO_T8n,IO
VREFB8N0,IO
(DQ1T),(DATA5),IO
(DATA6),IO
DIFFIO_T5p,IO
(DQS1T/CQ1T#,DPCLK7),DIFFIO_T2p,IO
(DQ1T),DIFFIO_T1n,IO
(DM1T),DIFFIO_T1p,IO
F1C100S_FPGA_CLK
F1C100S_FPGA_RWS
F1C100S_FPGA_DCS
FPGA_Conf_ASDO
FPGA_BACKLIGHT_PWM
FPGA_Conf_nCE
FPGA_Conf_Data
FPGA_SPECIAL_IC_SDA
FPGA_SPECIAL_IC_SCL
DAC_D0
DAC_D1
DAC_D2
DAC_D3
DAC_D4
DAC_D5
DAC_D6
DAC_D7
ADC2_ENCA
ADC2_D7A
ADC2_D6A
ADC2_D5A
ADC2_D4A
ADC2_D3A
ADC2_D2A
ADC2_D1A
ADC2_D0A
ADC2_D0B
ADC2_D1B
ADC2_D2B
ADC2_D3B
ADC2_D4B
ADC2_D5B
ADC2_D6B
ADC2_D7B
ADC2_ENCB
ADC2_OFFSET
ADC1_OFFSET
ADC1_D4A
ADC1_D3A
ADC1_D2A
ADC1_D1A
ADC1_D0A
ADC1_D0B
ADC1_D1B
ADC1_D2B
ADC1_D3B
ADC1_D4B
ADC1_D5B
ADC1_D6B
ADC1_D7B
ADC1_ENCB
ADC1_D5A
ADC1_D6A
ADC1_D7A
ADC1_ENCA
F1C100S_FPGA_DB0
F1C100S_FPGA_DB1
F1C100S_FPGA_DB2
F1C100S_FPGA_DB3
F1C100S_FPGA_DB4
F1C100S_FPGA_DB5
F1C100S_FPGA_DB6
F1C100S_FPGA_DB7
R13 1K ANALOG2_RELAIS1
R14 1K ANALOG2_RELAIS2
R15 1K ANALOG2_RELAIS3
R16 1K ANALOG1_RELAIS3
R17 1K ANALOG1_RELAIS2
R18 1K ANALOG1_RELAIS1
R19 1K ANALOG1_AC_DC
R20 1K ANALOG2_AC_DC
J5
JTAG
JTAG-TCK
JTAG-TDO
JTAG-TMS
JTAG-TDI
3V3_A
2V5
1V2
GND
R8 10K
R11 10K
R12 10K
R10 10K
R9 10K
R7 10k
R6 10K
R5 10K
R4 33
R21 33
R49 10K
R50 10K
X2 25MHz
U13
MS5351M
VDD XA XB SCL SDA
CLK0 CLK1 GND VDDO CLK2
CLOCK_SCL
CLOCK_SDA
FPGA_Conf_CLK
C79
C13
C8 C9 C11 C53 C74 C75 C77
C7 C10 C12 C78
L1 2200Ω
L2 2200Ω
L3 2200Ω
L4 2200Ω
C2 C5 C4 C3 C6 C73 C1
D1 1N5819
U4
W25Q80
/CS DO /WP GND
VCC /HOLD CLK DI
R1 33
FPGA_Conf_nCE
FPGA_Conf_Data
FPGA_Conf_CLK
FPGA_Conf_ASDO
J2
FPGA_FLASH
C51 C52
D2 1N5819
R3 10K
R2 10K
U5
UNKOWN IC
VCC WP SCL SDA
A0 A1 A2 VSS
FPGA_SPECIAL_IC_SCL
FPGA_SPECIAL_IC_SDA
J3
SPECIAL IC
C45 C41
TITLE: FPGA
REV: 1.1
Company:
Sheet: 2/6
Date: 2023-01-06
Drawn By:

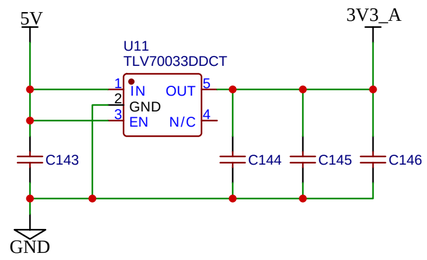
Capacitors are undeterminded.

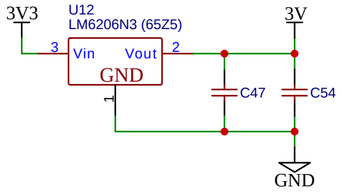


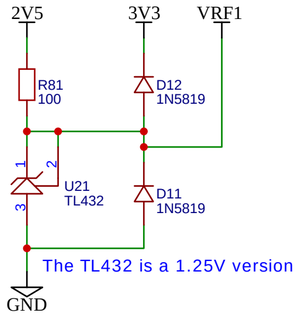
TITLE: Analog Input		REV: 1.0
	Company:	Sheet: 4/6
	Date: 2022-05-08 Drawn By:	

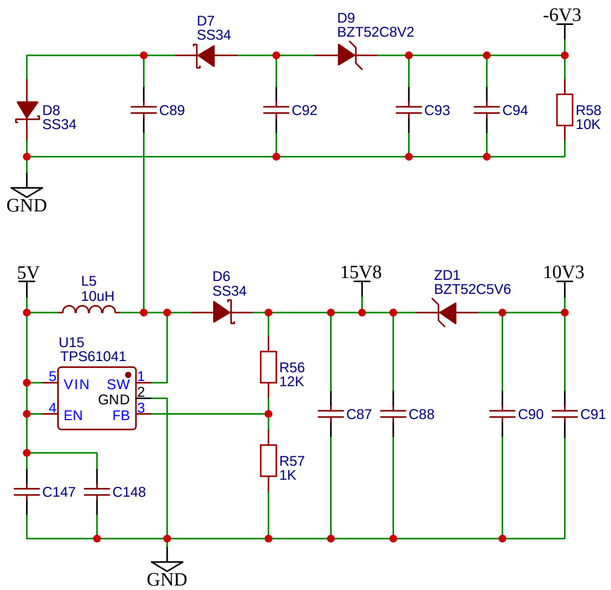
Capacitors are undeterminded.

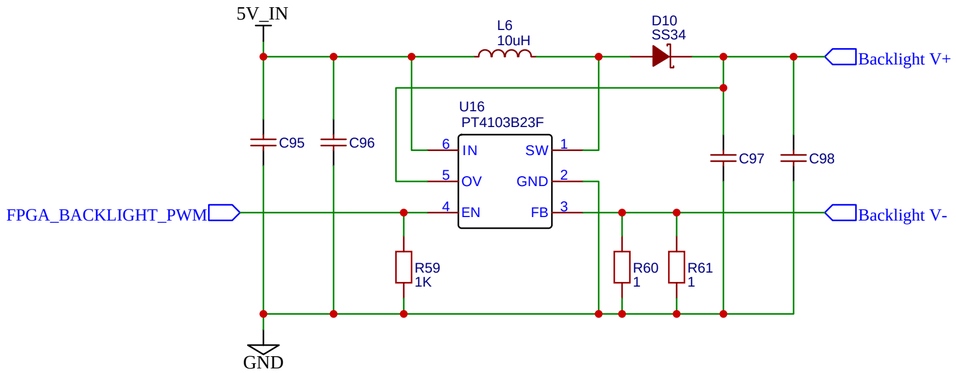








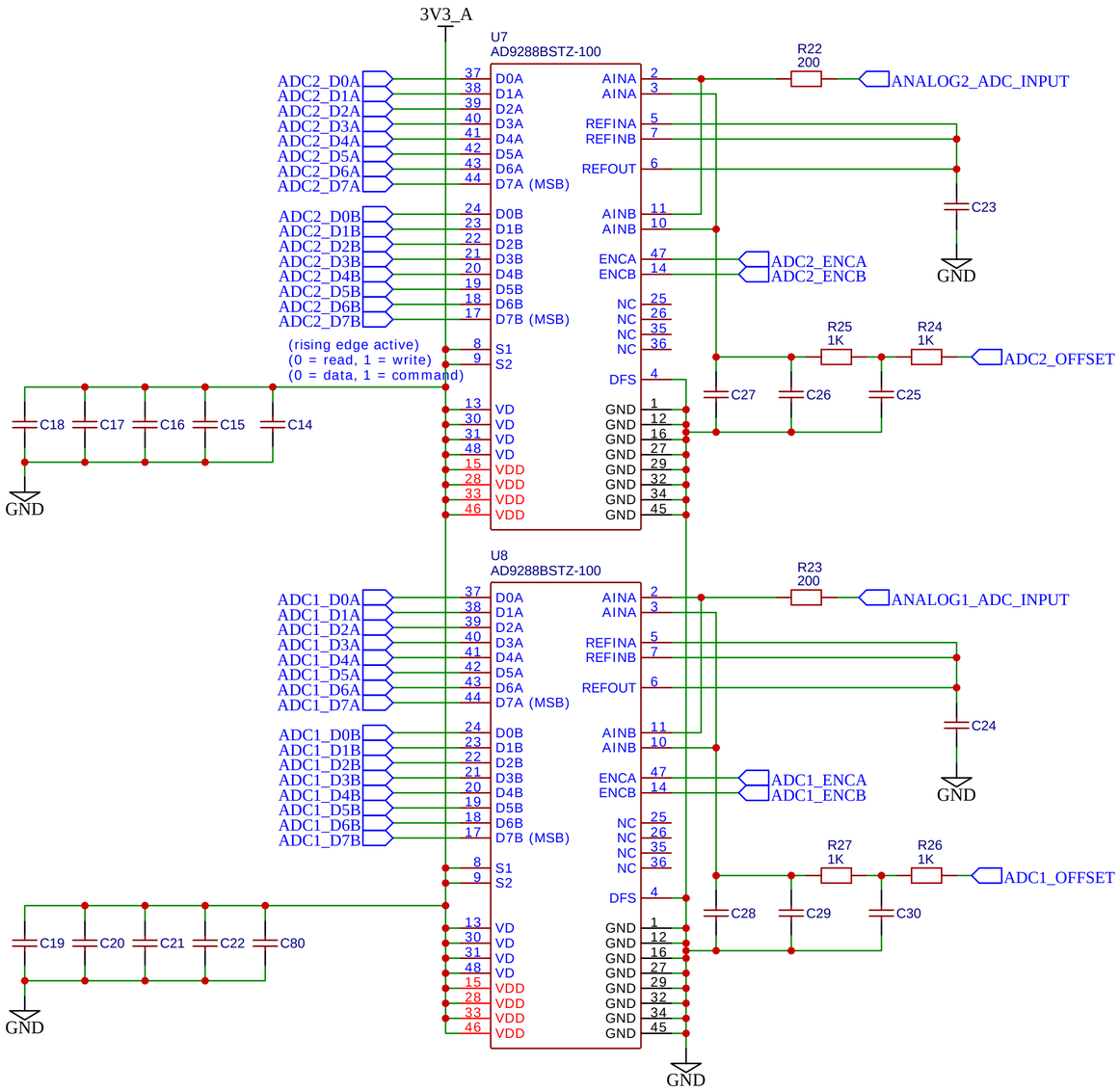


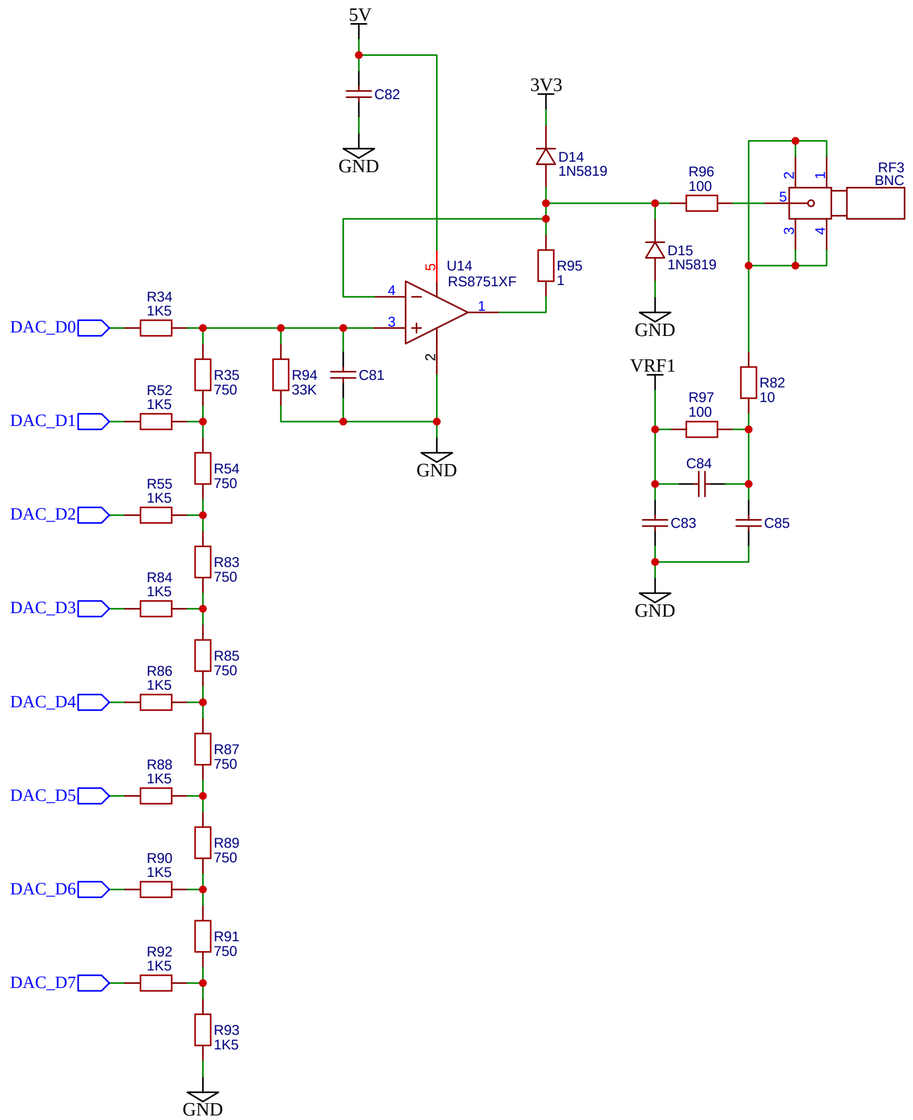


TITLE: Power Supply		REV: 1.0
	Company:	Sheet: 6/6
	Date: 2022-05-08 Drawn By:	

Capacitors are undeterminded.

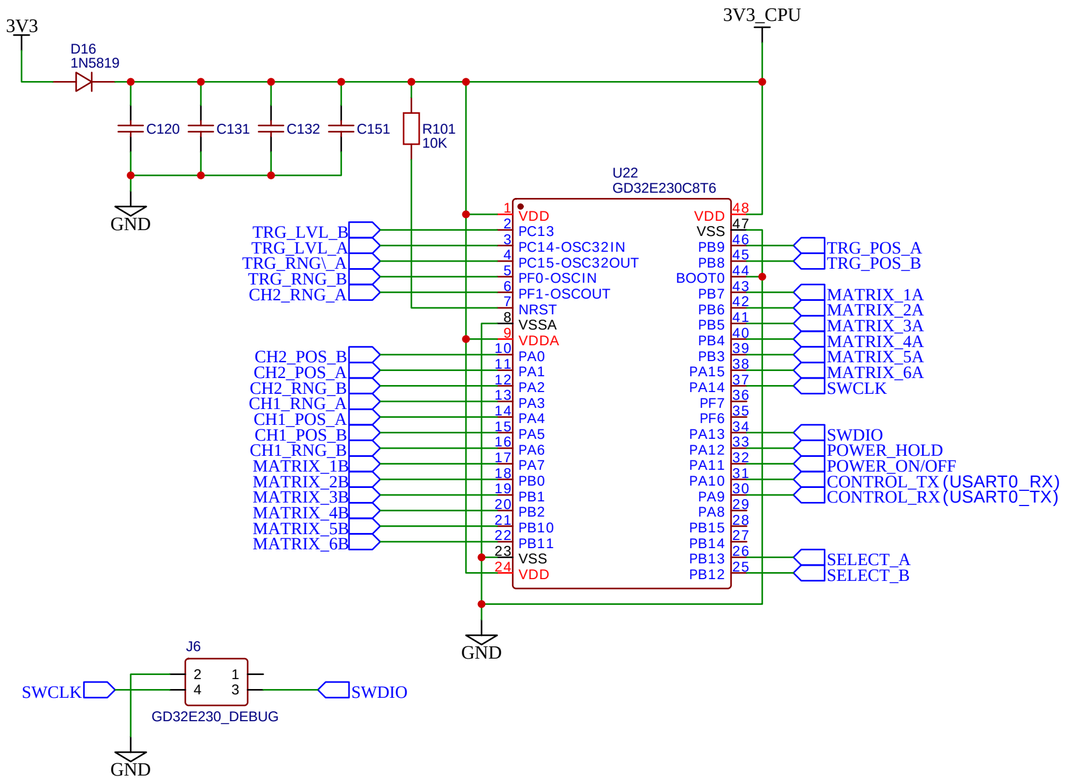
For the ADC's offset binary output is selected (DFS input low)
The data align mode is enabled (S1, S2 inputs high)

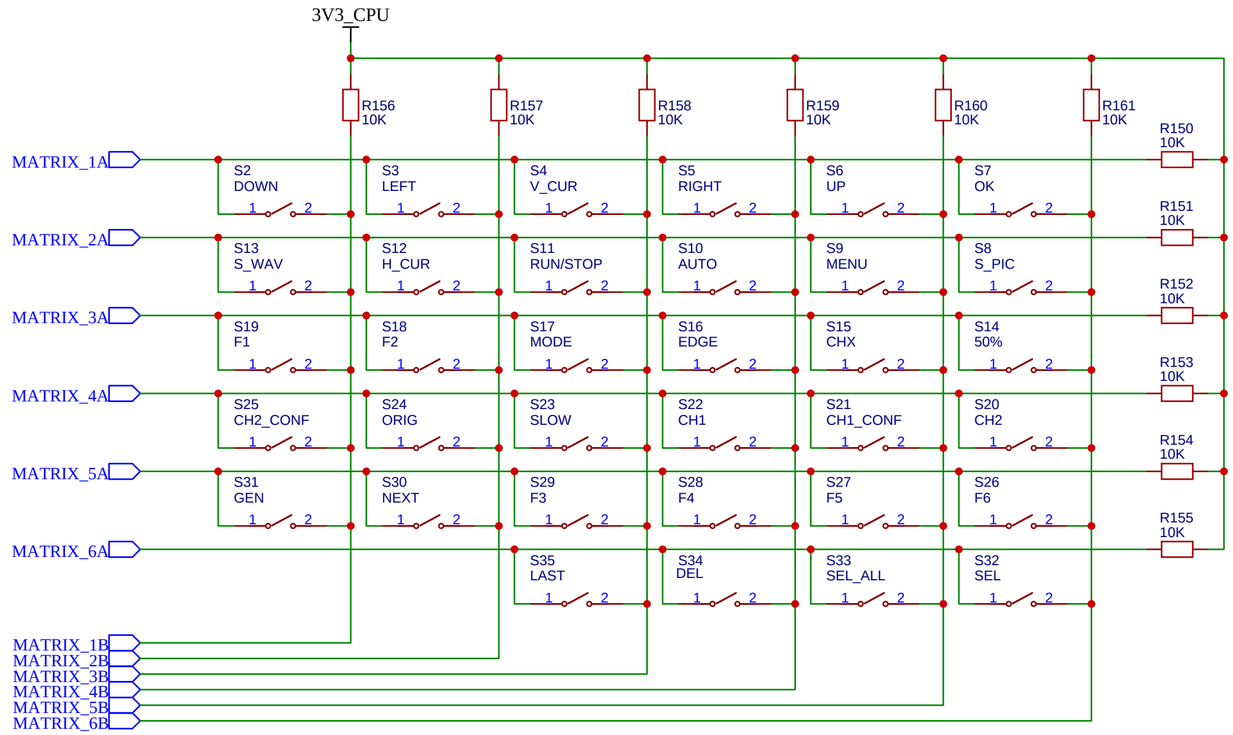


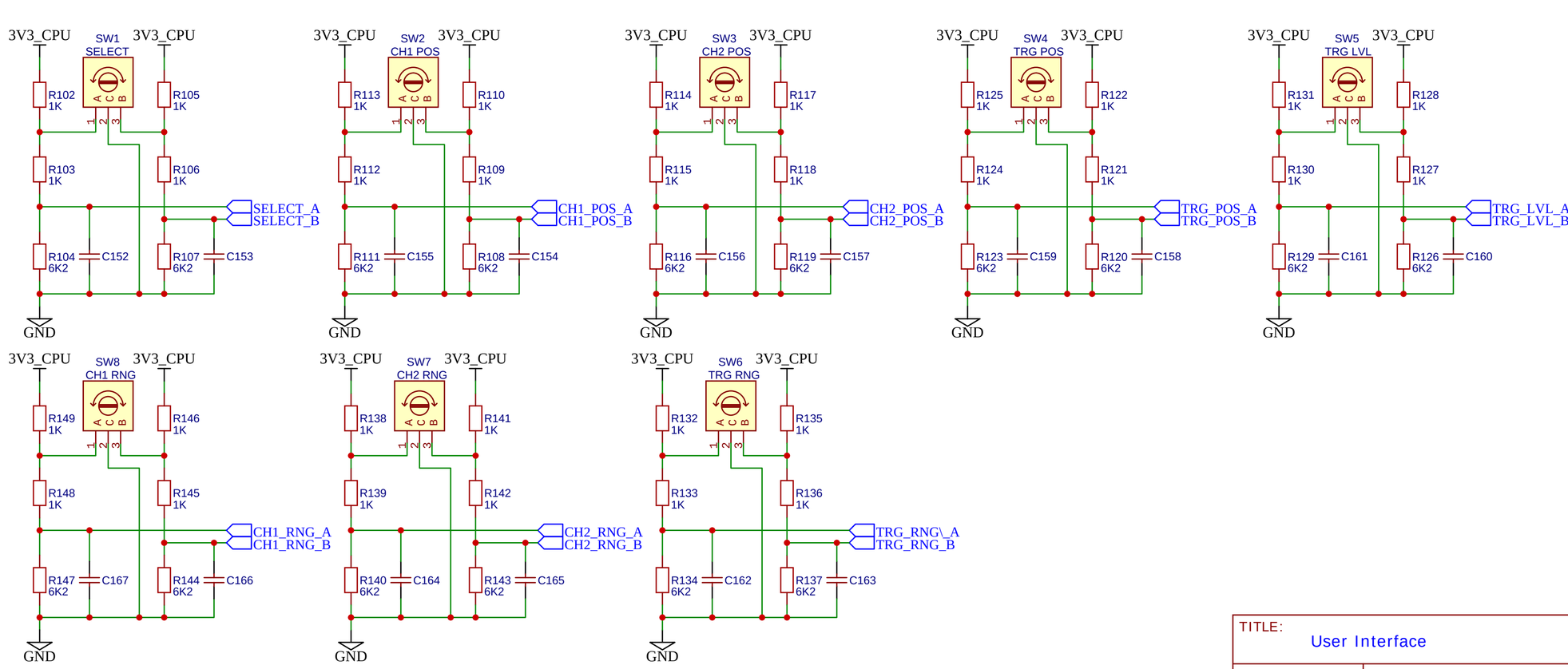


TITLE: ADC's and DAC		REV: 1.0
	Company:	Sheet: 3/6
	Date: 2022-05-08 Drawn By: petercost3	

Capacitors are undeterminded.







TITLE: User Interface		REV: 1.0
	Company:	Sheet: 5/6
	Date: 2022-05-09 Drawn By: petercost3	