SPECIFICATIONS

320*240 Graphic LCD Display with Touch Screen

LEDSEE electronics
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1. GENERAL SPECIFICATIONS:

1-1 SCOPE:
This specification covers the delivery requirements for the liquid crystal display delivered by LEDSEE electronics to Customer.

1-2 PRODUCTS:
Liquid Crystal Display Module (LCM)

1-3 MODULE NAME:
YM320240A-2TS

2. FEATURES:

2-1 MAIN LCD (LARGE)

Item	Standard Value
Display Type	320 *240 dots
LCD Type	☐FSTN, BLUE,Transmissive,Negative,Extened TEMP ☐FSTN, Transflective,Positive,Extened TEMP ■STN, BLUE, Transflective,Negative,Extened TEMP ☐STN, GREY,Transflective,Positive,Extened TEMP ☐STN, Yellow-GREEN,Positive,Normal TEMP
Drive Pattern	1/240Duty, 1/17Bias
Viewing Direction	6 O'clock
Backlight Type	☐YELLOW-GREEN LED BOTTOM BL ■WHITE EDGE LED BL ☐CCFL WHITE BL
Weight	TBD
Interface	8-bit 8080 MPU interface / 6800 series
Driver IC	SED1335

3. MACHANICAL SPECIFICATIONS:

ITEM	STANDARD VALUE	UNIT
DISPLAY FORMAT	320X 240 DOTS	
MODULE DIMENSION	167.0(W) X 109.0(H) X 12.0(T)	mm
EFFECTTVE DISPLAY AREA	122.0(W) X92.0(H)	mm
DOT SIZE	0.33(W) X 0.33(H)	mm
DOT PITCH	0.36W) X 0.36 (H)	mm
LCD TYPE	BLUE, STN	
DUTY AND BIAS	1/240 DUTY; 1/17 BIAS	
VIEWING DIRECTION	6:00	
BACK LIGHT	WHITE EDGE LED BL	

4. ABSOLUTE MAXIMUM RATING

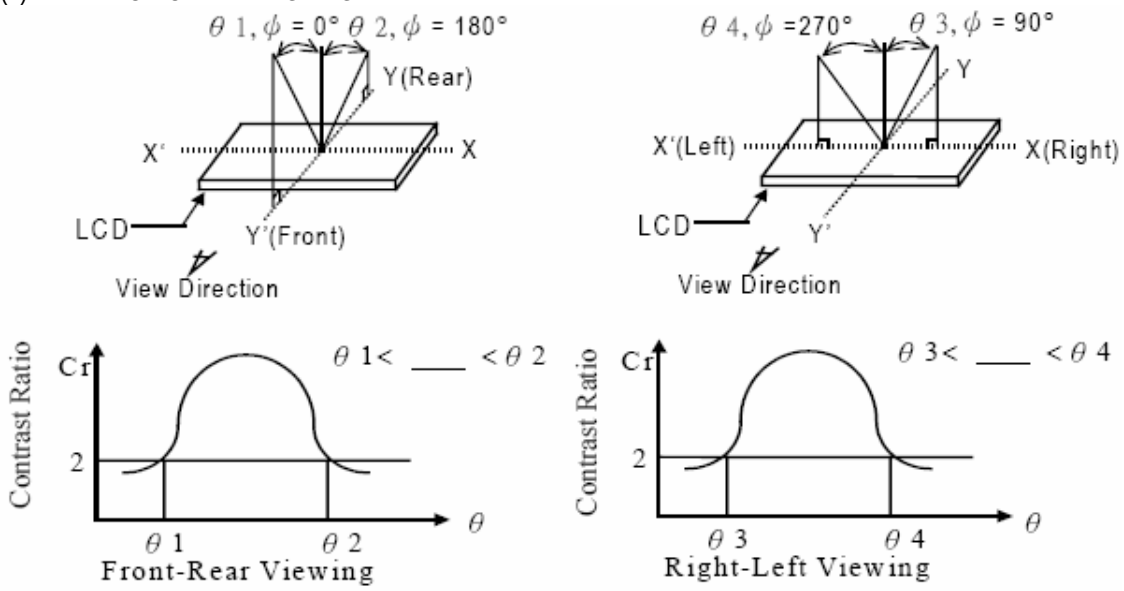
ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
POWER SUPPLY FOR LOGIC	VDD	Ta=25℃	-0.3	—	7.0	V
INPUT VOLTAGE	VIN	Ta=25℃	-0.3	—	VDD+0.3	V
Module OPERATION TEMPERATURE	TOPR	---	-10	—	+60	℃
Module STORAGE TEMPERATURE	TSTG	---	- 20	—	+70	℃
Storage Humidity	HD	Ta < 40 °C	-		90	%RH

5. ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage (logic)	Vdd-Vss	-	4.5	5	5.5	V
Supply Voltage (LCD)	Vlcd	Vdd=5.0(25°C)	20	-	24	V
Input signal voltage	V-ih	“H” level	0.5Vdd	-	Vdd	V
	V-il	“L” level	VSS	-	0.2Vdd	V
Output signal voltage	V-oh	“H” level	2.4	-	-	V
	V-ol	“H” level	vss	-	0.4	V
Supply Current (logic)	Icc	-	-	0.3	0.5	mA
Supply Current (LCD)	Io	-	-	-	-	mA
Supply Voltage (LED)	V-bl		-	5	-	V
Supply Current (LED)	I-bl		400	-	500	mA

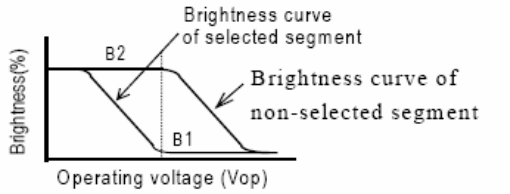
6. OPTICAL CHARACTERISTICS

(1) DEFINITION OF VIEWING ANGLE

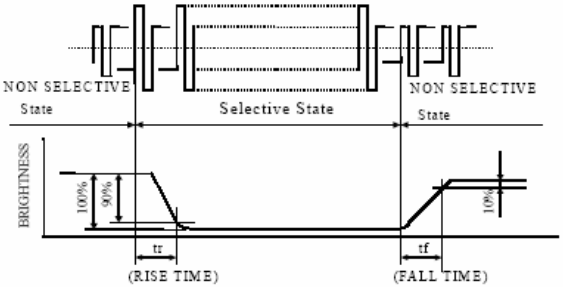


(2) DEFINITION OF CONTRAST

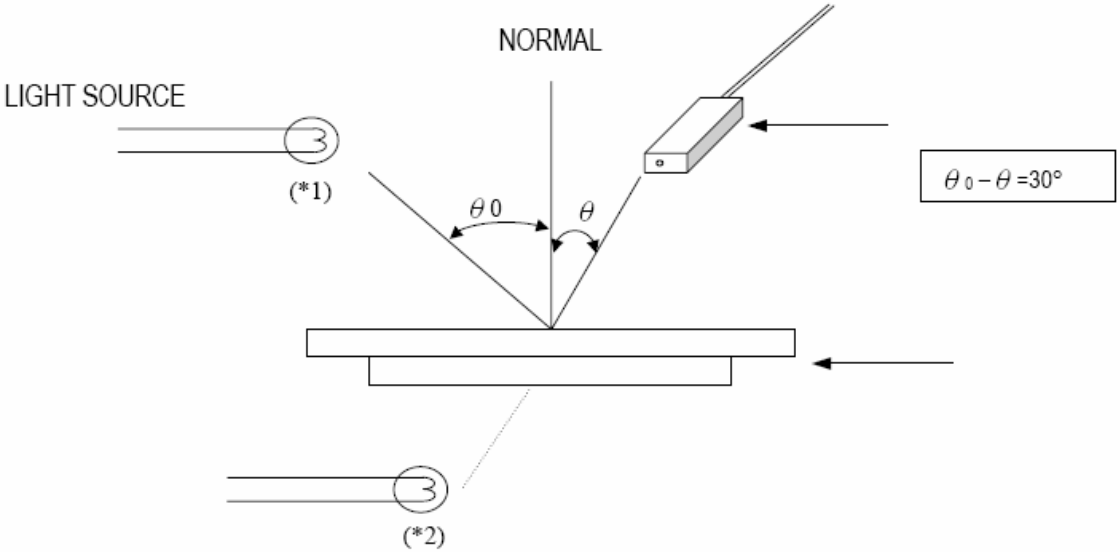
$$C.R = \frac{\text{Brightness of non-selected segment (B2)}}{\text{Brightness of selected segment (B1)}}$$



(3) DEFINITION OF RESPONSE

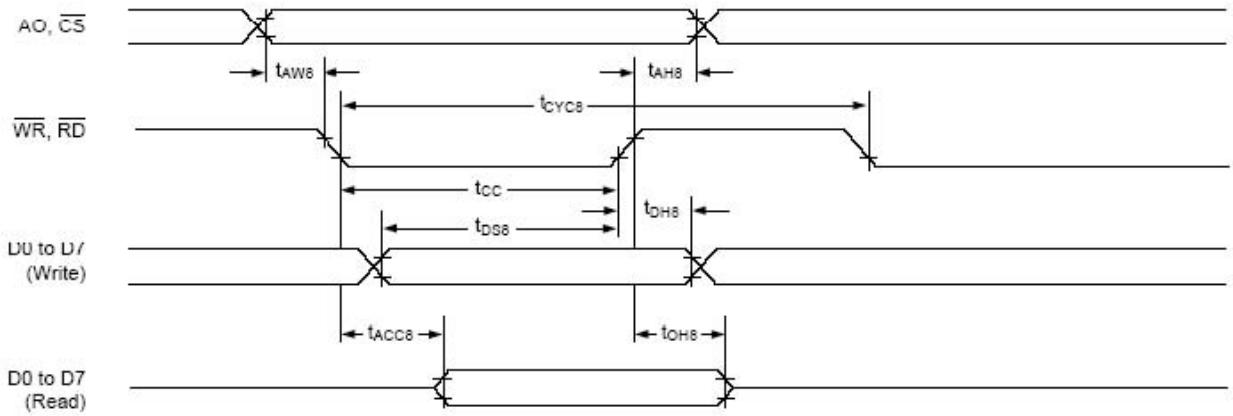


(4) Measuring Instruments For Electro-optical Characteristics



7. TIMING CHARACTERISTICS

8080 family interface timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
A0, CS	tAH8	Address hold time	10	—	10	—	ns	CL = 100pF
	tAW8	Address setup time	0	—	0	—	ns	
WR, RD	tCYC8	System cycle time	See note.	—	See note.	—	ns	
	tCC	Strobe pulsewidth	120	—	150	—	ns	
D0 to D7	tDS8	Data setup time	120	—	120	—	ns	
	tDH0	Data hold time	5	—	5	—	ns	
	tACC8	RD access time	—	50	—	80	ns	
	tOH8	Output disable time	10	50	10	55	ns	

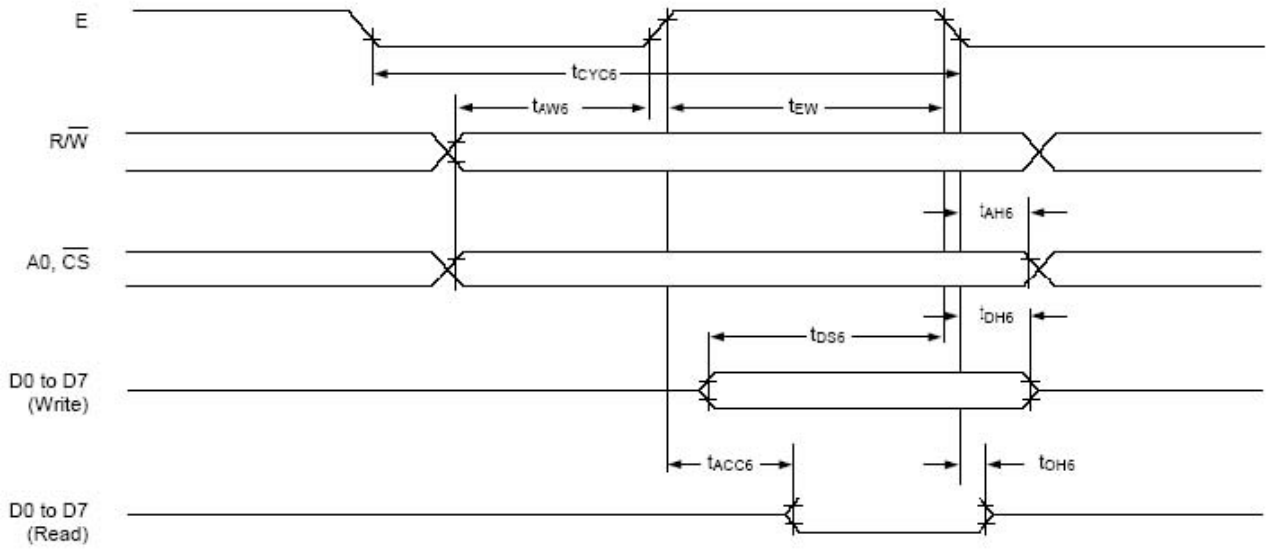
Note: For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

. 6800 family interface timing



Note: tCYC6 indicates the interval during which CS is LOW and E is HIGH.

Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
A0, CS, R/W	tCYC6	System cycle time	See note.	—	See note.	—	ns	CL = 100 pF
	tAW6	Address setup time	0	—	10	—	ns	
	tAH6	Address hold time	0	—	0	—	ns	
D0 to D7	tDS6	Data setup time	100	—	120	—	ns	
	tDH6	Data hold time	0	—	0	—	ns	
	tOH6	Output disable time	10	50	10	75	ns	
	tACC6	Access time	—	85	—	130	ns	
E	tEW	Enable pulsewidth	120	—	150	—	ns	

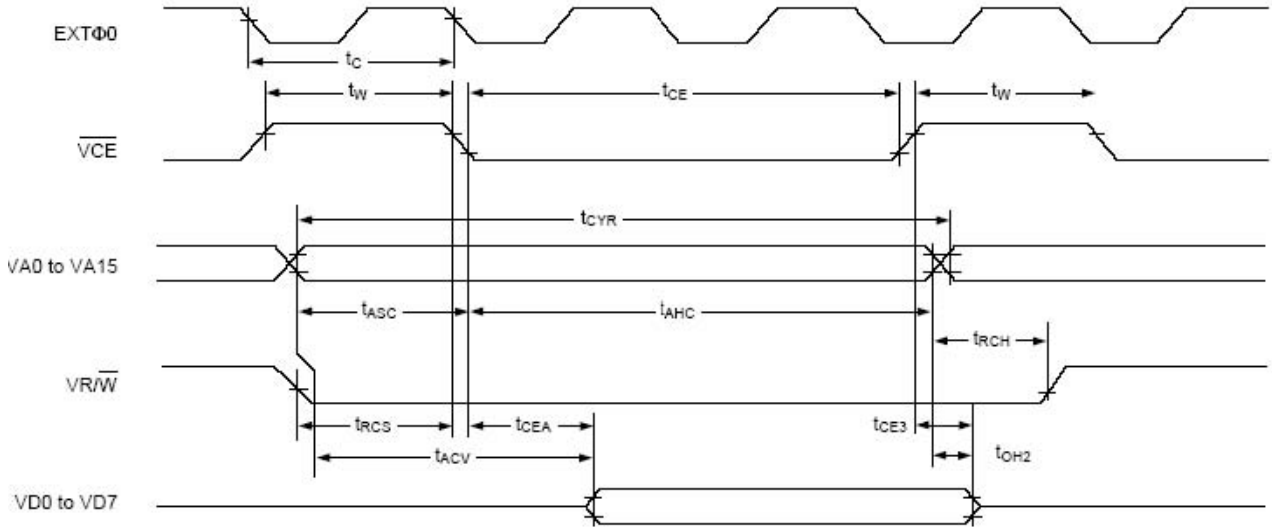
Note: For memory control and system control commands:

$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC6} = 4t_C + t_{EW} + 30$

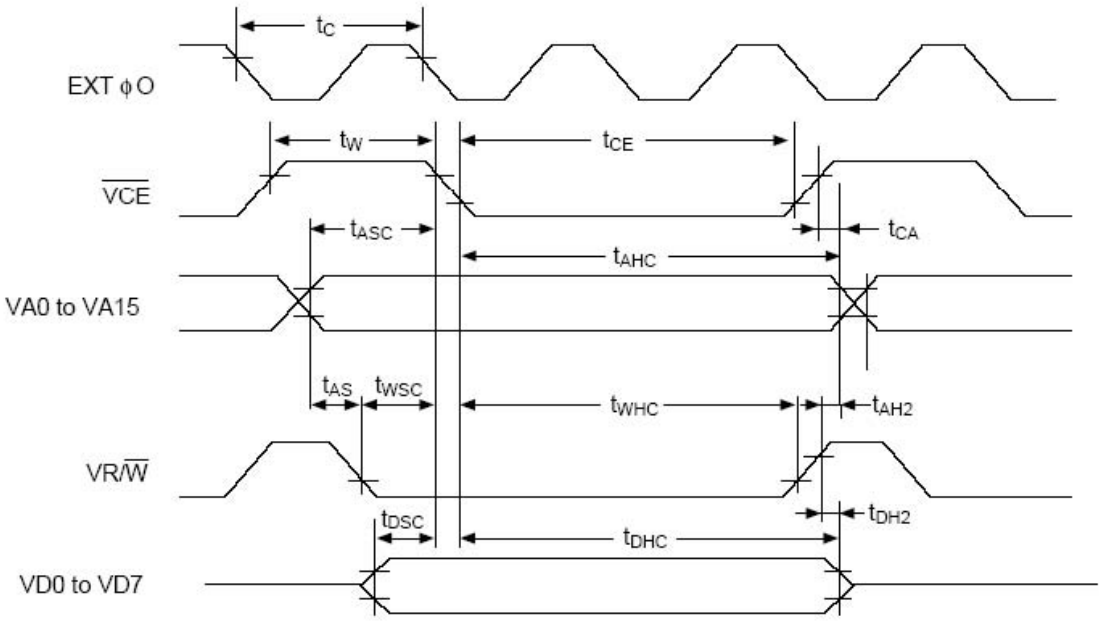
3. Display memory read timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tC	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	tW	$\overline{VCE}$ HIGH-level pulsewidth	tC – 50	—	tC – 50	—	ns	
	tCE	$\overline{VCE}$ LOW-level pulsewidth	2tC – 30	—	2tC – 30	—	ns	
VA0 to VA15	tCYR	Read cycle time	3tC	—	3tC	—	ns	
	tASC	Address setup time to falling edge of $\overline{VCE}$	tC – 70	—	tC – 100	—	ns	
	tAHC	Address hold time from falling edge of $\overline{VCE}$	2tC – 30	—	2tC – 40	—	ns	
$\overline{VRD}$	tRCS	Read cycle setup time to falling edge of $\overline{VCE}$	tC – 45	—	tC – 60	—	ns	
	tRCH	Read cycle hold time from rising edge of $\overline{VCE}$	0.5tC	—	0.5tC	—	ns	
VD0 to VD7	tACV	Address access time	—	3tC – 100	—	3tC – 115	ns	
	tCEA	$\overline{VCE}$ access time	—	2tC – 80	—	2tC – 90	ns	
	tOH2	Output data hold time	0	—	0	—	ns	
	tCE3	$\overline{VCE}$ to data off time	0	—	0	—	ns	

Display memory write timing



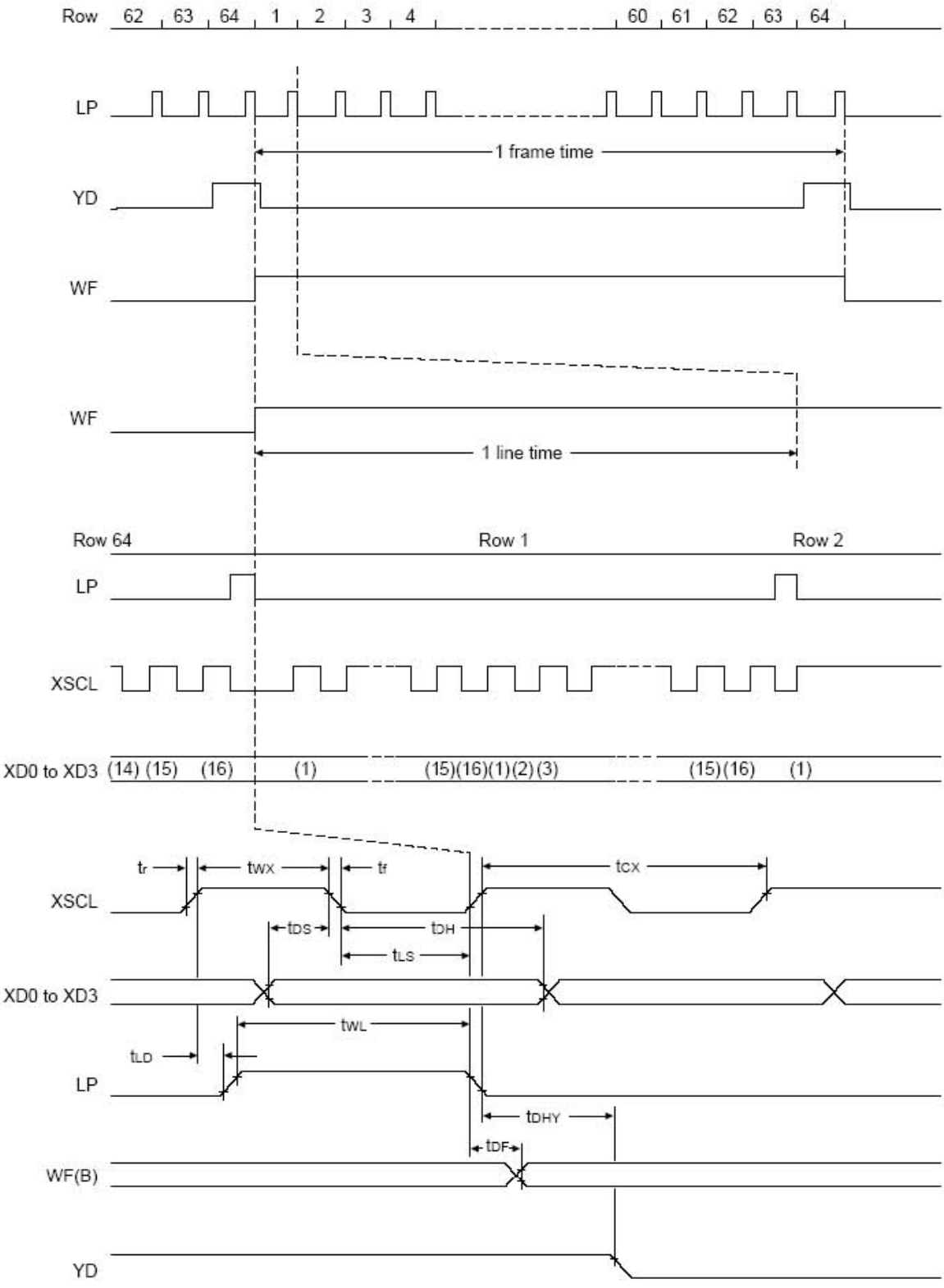
Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tC	Clock period	100	—	125	—	ns	CL = 100 pF
VCE	tW	VCE HIGH-level pulsewidth	tC – 50	—	tC – 50	—	ns	
	tCE	VCE LOW-level pulsewidth	2tC – 30	—	2tC – 30	—	ns	
VA0 to VA15	tCYW	Write cycle time	3tC	—	3tC	—	ns	
	tAHC	Address hold time from falling edge of VCE	2tC – 30	—	2tC – 40	—	ns	
	tASC	Address setup time to falling edge of VCE	tC – 70	—	tC – 110	—	ns	
	tCA	Address hold time from rising edge of VCE	0	—	0	—	ns	
	tAS	Address setup time to falling edge of VWR	0	—	0	—	ns	
	tAH2	Address hold time from rising edge of VWR	10	—	10	—	ns	
VWR	tWSC	Write setup time to falling edge of VCE	tC – 80	—	tC – 115	—	ns	
	tWHC	Write hold time from falling edge of VCE	2tC – 20	—	2tC – 20	—	ns	
VD0 to VD7	tDSC	Data input setup time to falling edge of VCE	tC – 85	—	tC – 125	—	ns	
	tDHC	Data input hold time from falling edge of VCE	2tC – 30	—	2tC – 30	—	ns	
	tDH2	Data hold time from rising edge of VWR	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

LCD output timing

The following characteristics are for a 1/64 duty cycle.



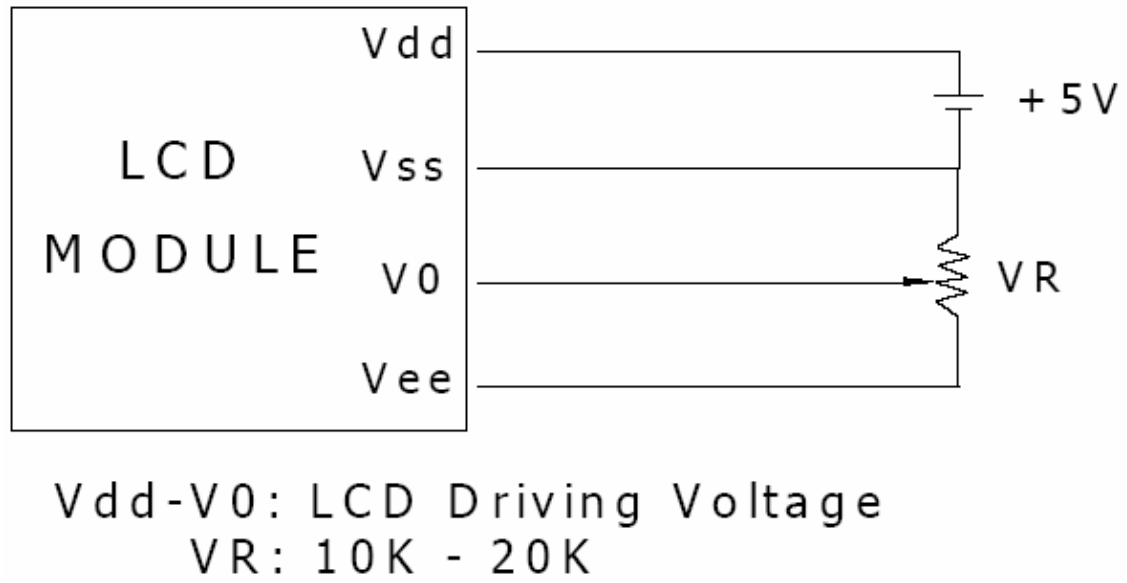
T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
	t_r	Rise time	—	30	—	40	ns	CL = 100 pF
	t_f	Fall time	—	30	—	40	ns	
XSCL	t_{CX}	Shift clock cycle time	4tc	—	4tc	—	ns	
	t_{WX}	XSCL clock pulsewidth	2tc – 60	—	2tc – 60	—	ns	
XD0 to XD3	t_{DH}	X data hold time	2tc – 50	—	2tc – 50	—	ns	
	t_{DS}	X data setup time	2tc – 100	—	2tc – 105	—	ns	
LP	t_{LS}	Latch data setup time	2tc – 50	—	2tc – 50	—	ns	
	t_{WL}	LP pulsewidth	4tc – 80	—	4tc – 120	—	ns	
	t_{LD}	LP delay time from XSCL	0	—	0	—	ns	
WF	t_{DF}	Permitted WF delay	—	50	—	50	ns	
YD	t_{DHY}	Y data hold time	2tc – 20	—	2tc – 20	—	ns	

8. PIN ASSIGNMENT

PIN	SYMBOL	FUNCTION
1	VSS	Ground.
2	VDD	Power supply.
3	V0	Contrast adjust.
4	A0	A0="L": Instruction ; A0="H"; Data.
5	/WR	WR="L": Write.
6	/RD	RD="L": Read
7~14	DB0~DB7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
15	/CS	Chip select for SED1335. 'L" active.
16	/RES	Reset signal.
17	VEE	DC/DC voltage converter.
18	SEL1	"L": 8080 series. "H":6800 series.
19	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.
20	/CS2	Chip select for touch screen.
21	DIN	Serial Data Input. If $\overline{CS}$ is LOW, data is latched on rising edge of DCLK.
22	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{CS}$ is HIGH.
23	/PEN	Pen Interrupt. Open anode output (requires 10kΩ to 100kΩ pull-up resistor externally).
24	BUSY	Busy Output. This output is high impedance when $\overline{CS}$ is HIGH.
25	IN3	Auxiliary Input 1. ADC input Channel 3.
26	IN4	Auxiliary Input 2. ADC input Channel 4.

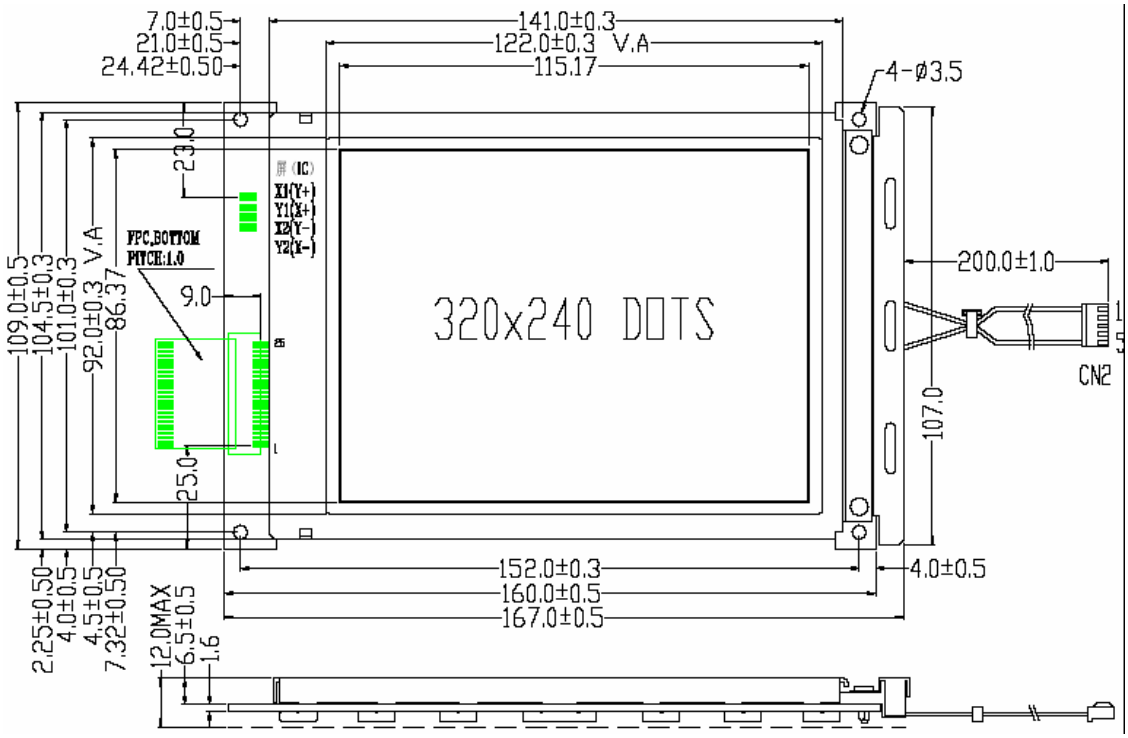
9. BLOCK DIAGRAM

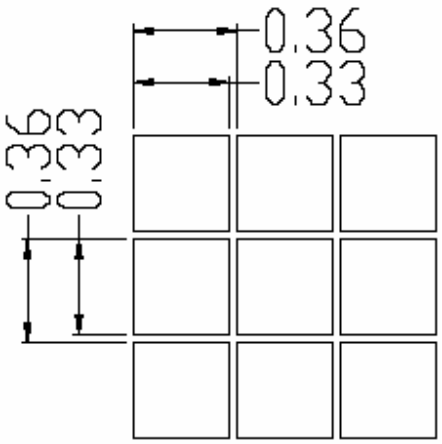


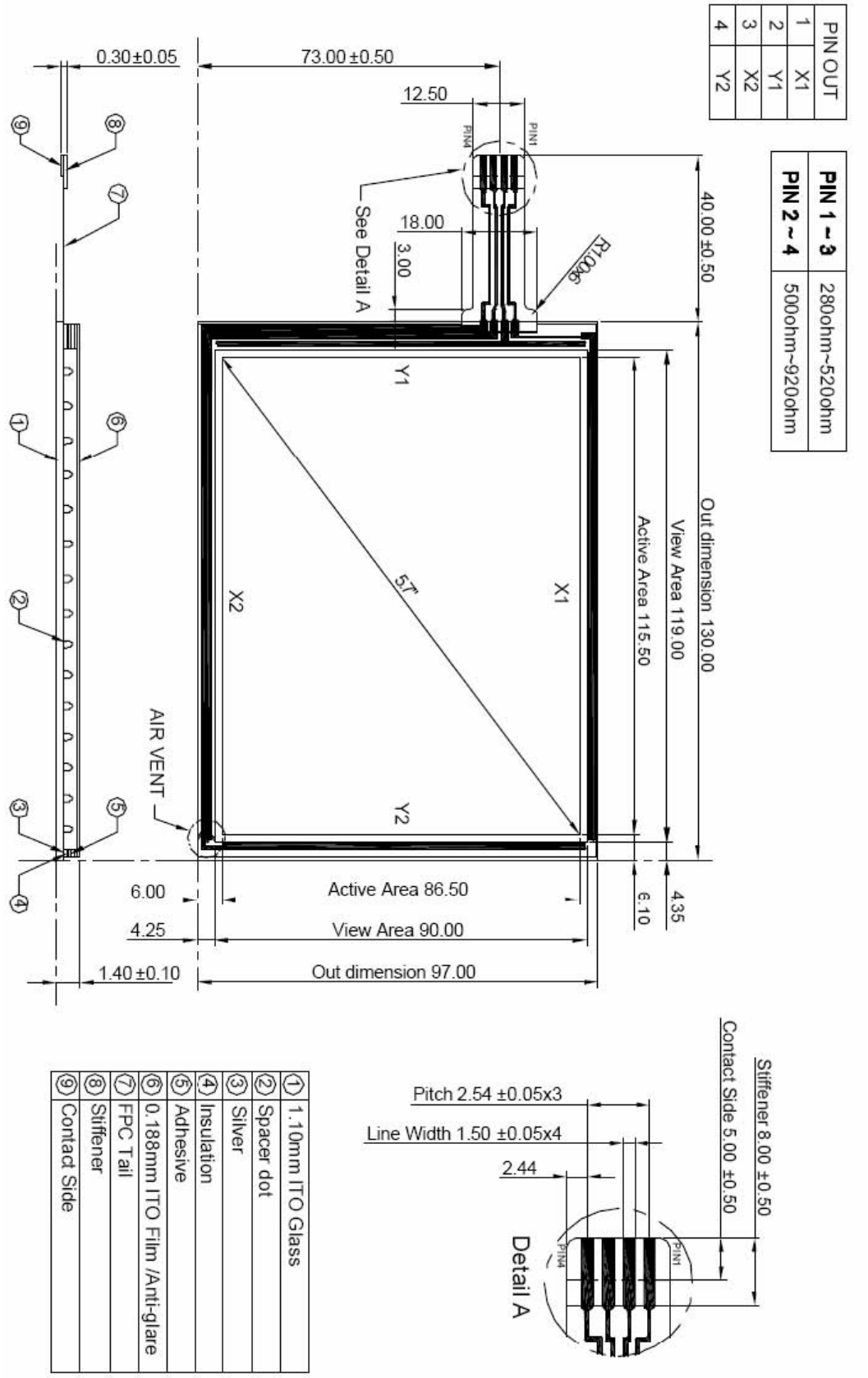
Display Control Instruction:

Please refer to the series of SED1335.

10. OUTLINE DIMENSIONS






PIN OUT
1 X1
2 Y1
3 X2
4 Y2
PIN 1 ~ 3 280ohm~520ohm
PIN 2 ~ 4 500ohm~920ohm
0.30±0.05
73.00±0.50
12.50
18.00
3.00
R1.00
See Detail A
40.00±0.50
Y1
X1
X2
Y2
5T
AIR VENT
Out dimension 130.00
View Area 119.00
Active Area 115.50
6.10
4.35
6.00
Active Area 86.50
4.25
View Area 90.00
1.40±0.10
Out dimension 97.00
① 1.10mm ITO Glass
② Spacer dot
③ Silver
④ Insulation
⑤ Adhesive
⑥ 0.188mm ITO Film /Anti-glare
⑦ FPC Tail
⑧ Stiffener
⑨ Contact Side
Pitch 2.54 ±0.05x3
Line Width 1.50 ±0.05x4
2.44
Detail A
Contact Side 5.00 ±0.50
Stiffener 8.00 ±0.50

11. ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	CONDITIONS	CRITERION
OPERATING TEMPERATURE	TOPR	-20℃～+70℃	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
STORAGE TEMPERATURE	TSTG	-30℃～+80℃	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
HUMIDITY	—	See Note	WITHOUT CONDENSATION

12. RELIABITY

12-1 RELIABILITY TEST

ITEM	CONDITIONS	CRITERION
OPERATING TEMPERATURE	HIGH TEMPERTURE +70℃240HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE -20℃240HRS	
STORAGE TEMPERATURE	HIGH TEMPERTURE +80℃240HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
	LOW TEMPERTURE - 30℃240HRS	
HUMIDITY	40℃90%RH 240HRS	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
VIBRATION	• Operating Time: thirty minutes exposure for each direction (X,Y,Z) Sweep Frequency: • 10～55Hz (1 min) • Amplitude: 1.5mm	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION
THERMAL SHOCK	-20℃(30mins) ⟷ +70℃(30mins) 10 cycles	NO DEFECT IN DISPLAYING AND OPERATIONAL FUNCTION

*NOTE: TEST CONDITION

(1)TEMPERATURE AND HUMIDITY: IF NO SPECIFICATION, TEMP. SET AT 25±2℃, HUMIDITY SET AT 60±5%RH

(2) OPERATING STATE: SAMPLES SUBJECT TO THE TESTS SHALL BE IN " OPERATING" CONDITION

13. PRECAUTION FOR USE

The following precautions should be followed, since this module contains precise parts.

(1) Do not store module for an extended periods of time under the conditions of high temperature and high humidity.

(2) Avoid using or storing the module in areas that expose it to direct sunlight or ultraviolet rays.

(3) Use protective finger covers when handling the module to avoid scratching or staining the module.

(4) Care should be taken not to expose the module to static electricity, because the module contains C-MOS LSI's.

(5) The LSI is sensitive to light.
The user's product should be designed so that LSI is not exposed to any light during operation.

(6) During installation, cover the display area with acrylic protection plates to protect the polarizer plate and LCD cells.

(7) Do not apply any excessive shocks to the module because the module contains sensitive LCD cells. Do not use a module, which has experienced strong mechanical shock.

(8) Care should be taken when the power supply turns on as following.
(a) Do not apply any input signals before the supplying voltage is applied.
(b)Do not turn off the power supply while any input signals are applied.

Caution

(1) Dangerous. Do not shock glass because glass can break.

(2) If module breaks, do not touch it directly.
(Glass could stick or cut skin.)

(3) Do not swallow Liquid Crystal.
(In case of broken LCD panel, do not swallow liquid crystal even if there is no proof that liquid crystal is poisonous.)

(4) If liquid crystal is exposed to skin, wash the area thoroughly with alcohol or soap.

(5) When disposing of the product, please observe industrial waste disposal laws in each country and district.

(6) In case of injury, give immediate treatment and consult with a doctor.

(7) This product is constructed precisely. Don't disassemble or modify.

※ Neglecting this mark can cause injury to humans and damage to materials