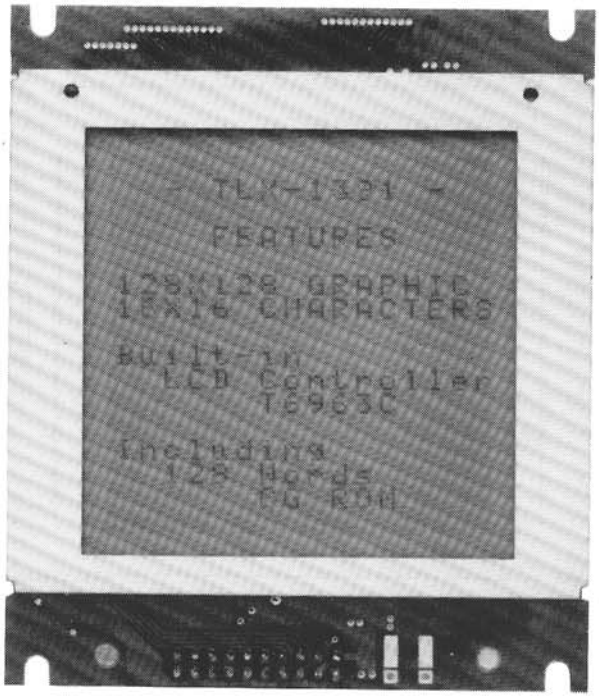
TOSHIBA

Electron Tube, Device & Equipment

TECHNICAL DATA

TOSHIBA DOT MATRIX LCD MODULE TLX-1391 TLX-1391-E0

TLX-1391 and TLX-1391-E0 are 128x128 dots graphic LCD modules including an LCD controller, a display RAM, an EL backlight (TLX-1391-E0) and driver circuit. These module are suitable for copiers, facsimiles, PBXs, marine instruments, and a message display for various instruments.



FEATURES

(1) Excellent readability and high contrast ratio.
(2) 8-bit parallel bus for read/write data from CPU interface.
(3) Built-in LCD controller T6963C and display RAM (8k byte).
(4) Large graphic display for 128x128 dots.
(5) Various attribute functions.
(6) Built-in 128 words character generator ROM and 128 words character generator RAM, or 256 words character generator RAM.
(7) Built-in EL backlight (TLX-1391-E0).
(8) Wide operating temperature range (0 to 50°C).
(9) Compact and easily mountable on any equipment.

CONTENTS

1. Outline of LCD Module

1.1 TLX-1391

TLX-1391 consists of a 128x128 dots LCD panel, LCD drivers, an LCD controller, a display RAM (8k byte) and a print circuit board.

Fig. 1.1 Dimensional Outline

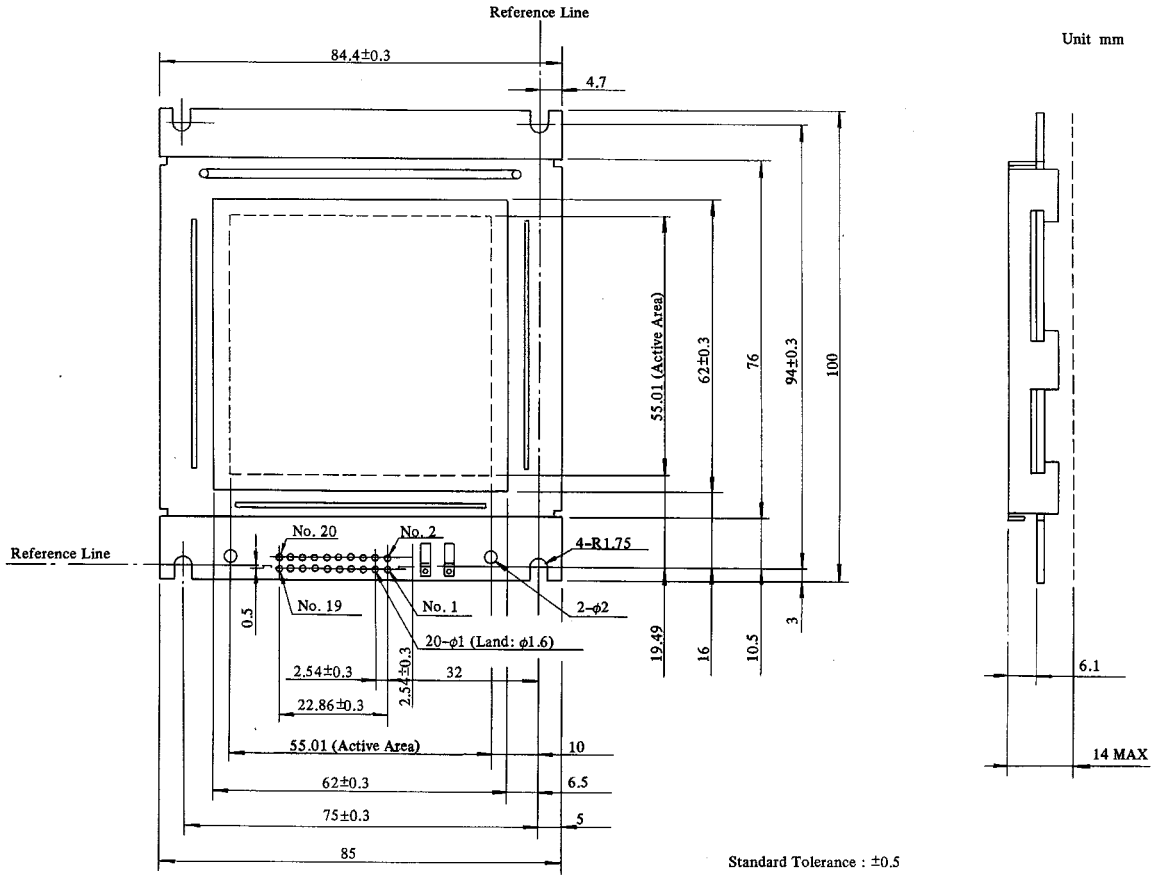
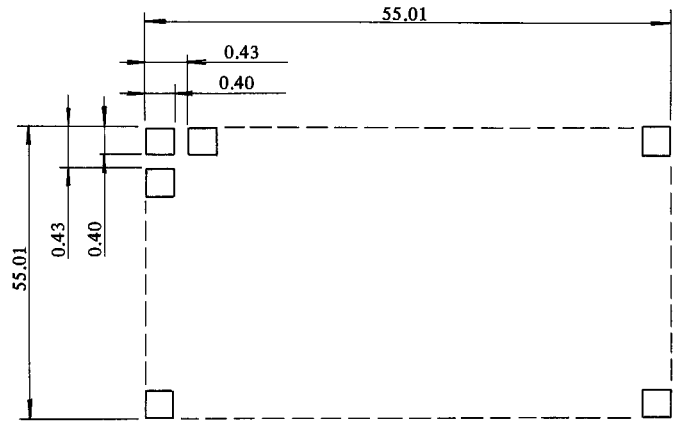


Fig. 1.2 Detail of dot matrix



1.2 TLX-1391-E0

TLX-1391-E0 consists of 128x128 dots LCD panel, LCD drivers, an LCD controller, a display RAM (8k byte), an EL backlight and a print circuit board.

Fig. 1.3 Dimensional Outline

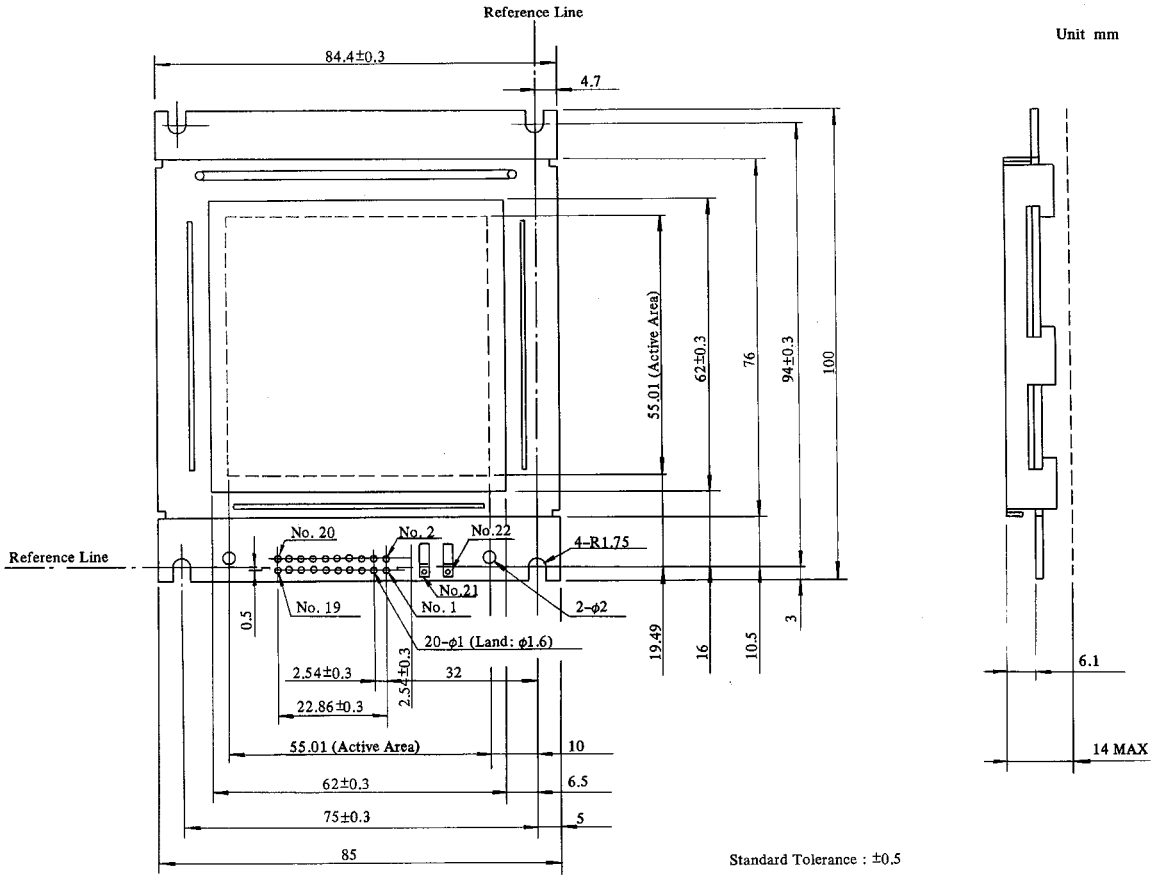
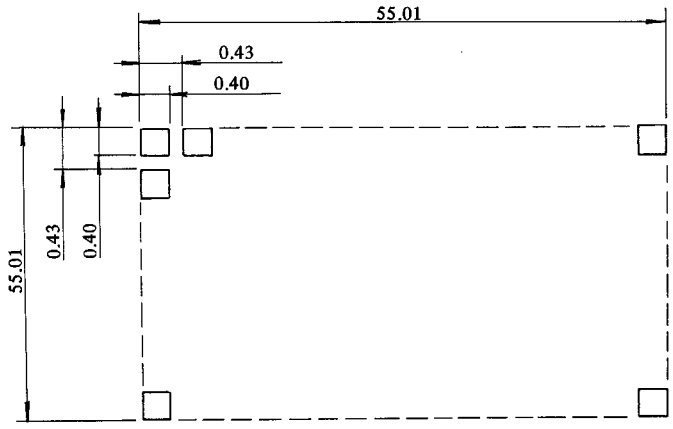


Fig. 1.4 Detail of dot matrix



2. Specifications

2.1 Absolute Maximum Ratings

Make sure not to exceed following maximum rating values under the worst probable conditions.

Item	Symbol	Rating		Unit
		TLX-1391	TLX-1391-E0	
Supply Voltage	V_{DD}	7		V
	V_{DD}-V_{EE}	29		
	V_{EL}	———	130 (AC)	
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3		V
EL Driving Freq.	f_{EL}	———	1	kHz
Operating Temp.	Top	0 to 50		°C
Storage Temp.	Tstg	-20 to 60		°C
Humidity	———	10 to 90 (Note)		%

Note: Wet bulb temperature should be 29°C Max., and no condensation of water.

2.2 Mechanical Characteristics

Item	Specifications	Unit
	TLX-1391 and TLX-1391-E0	
Dimensional Outline	84.4(W) x 100.0(H) x 14.0(D)	mm
Number of Dots	128 x 128 dots	-
Number of Characters	21 x 16(336) in case of 6 x 8 fonts 16 x 16(256) in case of 8 x 8 fonts	-
Viewing Area	62.0 (W) x 62.0 (H)	mm
Bezel Opening	62.0 (W) x 62.0 (H)	mm
Active Area	55.01(W) x 55.01(H)	mm
Dot Pitch	0.43 (W), 0.43 (H)	mm
Dot Size	0.40 (W) x 0.40 (H)	mm
Weight (Approx.)	100 (TLX-1391) 105 (TLX-1391-E0)	g

2.3 Electrical Characteristics (Ta=25°C)

Item	Symbol	Condition	Specifications	Unit	Note
Supply Voltage	V_{DD}	———	5.0±0.25	V	
	V_{EE}	———	-14.5±3.0		
EL Drive Voltage	V_{EL}	f_{EL}=500Hz	110±10	V	2
High Level Input Voltage	V_{IH}	V_{DD}=5±0.25V	V_{DD}-2.2 MIN.	V	
Low Level Input Voltage	V_{IL}	V_{DD}=5±0.25V	0.8 MAX.	V	
High Level Output Voltage	V_{OH}	V_{DD}=5±0.25V	V_{DD}-0.3 MIN.	V	
Low Level Output Voltage	V_{OL}	V_{DD}=5±0.25V	0.3 MAX.	V	
Current Consumption	I_{DD}	V_{DD}=5V V_{EE}=-14.5V	9.0 MAX.	mA	1
	I_{EE}		3.0 MAX.	mA	
	I_{EL}	V_{EL}=110V f_{EL}=500Hz	16.0 (AC)MAX.	mA	2

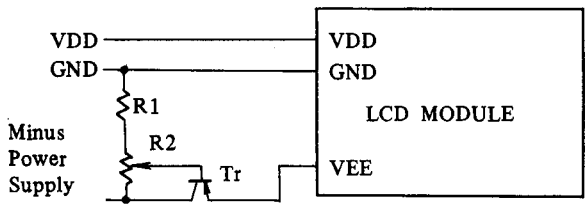
Note 1 : In case of all dots on.
2 : Only for TLX-1391-E0

Table 2.1 Recommended power supply voltage for LCD drive (V_{DD}-V_{EE})

As LCD panel is driven by the voltage of V_{DD}-V_{EE}, adjustable V_{EE} is required for contrast control and temperature compensation.

Temperature (°C)	V_{DD}-V_{EE}(V)	
	TLX-1391	TLX-1391-E0
0	21.0	20.5
25	19.5	19.0
50	18.0	17.5

Example of Variable Negative Voltage Supply Circuit

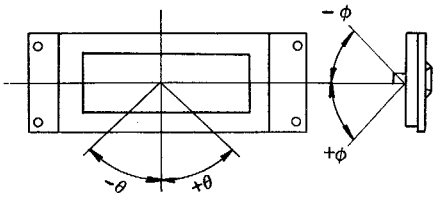


R1 = 10k
R2 = 10k (Variable resister)
Tr : 2SA1162 etc.

2.4 Optical Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Viewing Angle	ϕ	Ta=25°C θ=0° K>1.3	-15	0	40	Degree	1,2
Contrast	K	Ta=25°C ϕ=0° θ=0°	2.5	4	—	——	1,3
Response Time (Rise Time)	τ_r	Ta=25°C ϕ=0° θ=0°	——	200	350	ms	1,4
Response Time (Decay Time)	τ_d	Ta=25°C ϕ=0° θ=0°	——	250	350	ms	1,4
EL Brightness (TLX-1391-E0)	B_{EL}	Ta=25°C ϕ=0°, θ=0° V_{EL}=110V f_{EL}=500Hz	4	6	——	nt	5

Note 1 : Definition of ϕ and θ

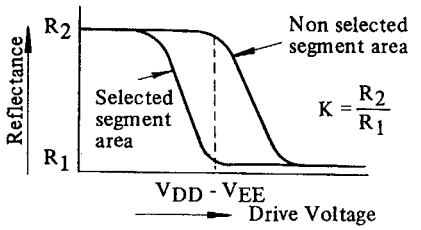


Note 2 : Definition of Viewing Angle

Contrast higher than 1.3 can be obtained by adjusting the V_{EE} Value.

Note 5 : Brightness of the LCD panel surface when the power supply for LCD module are off in the dark room.

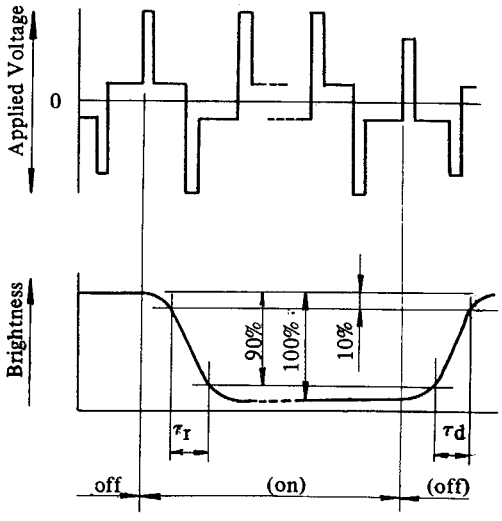
Note 3 : Definition of Contrast



R_1: Reflectance of selected segment area

R_2: Reflectance of non-selected segment area (Group dots measurement)

Note 4 : Definition of Rise time and Decay time



3. Interface

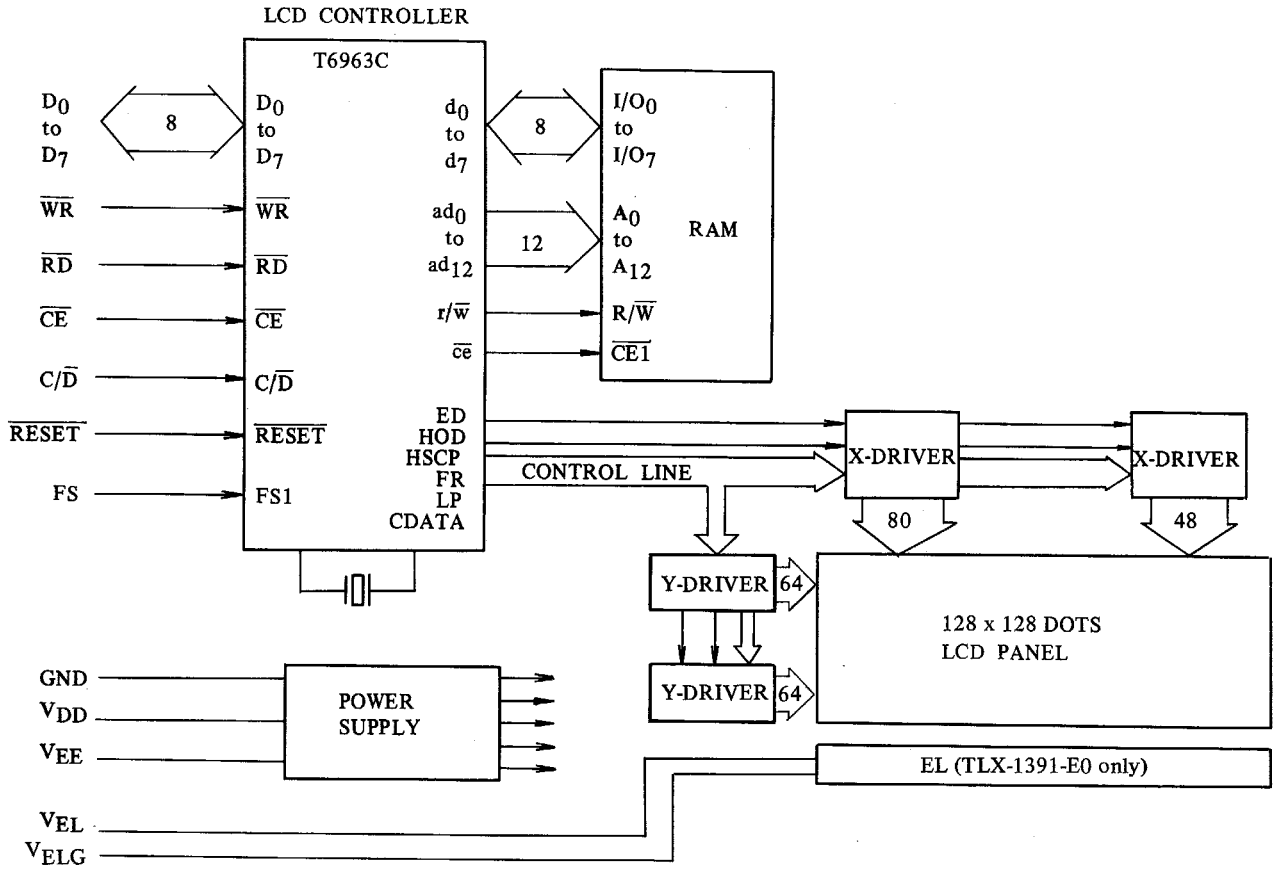
3.1 Interface Connection

Pin No.	Signal	Function
1	FGND	Frame Ground (Connected to Metal Bezel)
2	GND	Ground (Signal Ground)
3	V_{DD}	Power Supply for Logic
4	V_{EE}	Power Supply for LCD Drive (Should be Variable)
5	$\overline{WR}$	Data Write (Write Data to the Module at "L")
6	$\overline{RD}$	Data Read (Read Data from the Module at "L")
7	$\overline{CE}$	Chip Enable for the Module
8	C/$\overline{D}$	$\overline{WR}$="L";C/$\overline{D}$="H":Command Write, C/$\overline{D}$="L":Data Write $\overline{RD}$="L";C/$\overline{D}$="H":Status Read , C/$\overline{D}$="L":Data Read
9	NC	No Connection
10	$\overline{RESET}$	Module Reset (Controller Reset)
11	D0	Data Input/Output (LSB)
12	D1	Data Input/Output
13	D2	Data Input/Output
14	D3	Data Input/Output
15	D4	Data Input/Output
16	D5	Data Input/Output
17	D6	Data Input/Output
18	D7	Data Input/Output (MSB)
19	FS	Font Select; Connect to VDD: 6 x 8 dots fonts Connect to GND: 8 x 8 dots fonts
20	NC	No Connection
21	V_{EL}	Power Supply for EL Drive (only for TLX-1391-E0)
22	V_{ELG}	Power Supply for EL Drive (only for TLX-1391-E0)

3.2 Block Diagram

The block diagram of internal circuit is shown in Fig. 3.1. TLX-1391 and TLX-1391-E0 need two power sources V_{DD} for logic circuit and V_{EE} for LCD drive. TLX-1391-E0 also needs additional power supply for EL Panel (V_{EL}).

Fig. 3.1 Block Diagram



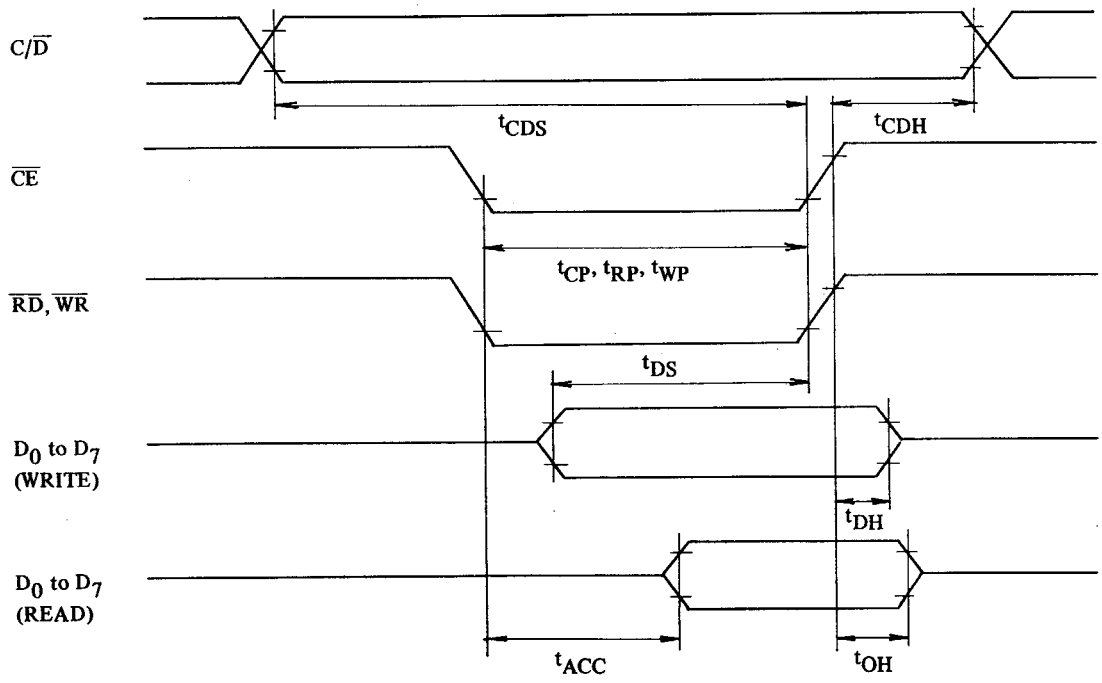
Note : It is necessary to guard all signals from external noise as signal lines are directly connected to C-MOS and are not pull-up or pull-down internally excluding RESET which is pull-up to V_{DD}.

3.3 Signal Timings

Item	Symbol	Min.	Max.	Unit
C/$\overline{D}$ Set Up Time	t_{CDS}	100	-	ns
C/$\overline{D}$ Hold Time	t_{CDH}	10	-	ns
$\overline{CE}$, $\overline{RD}$, $\overline{WR}$ Pulse Width	t_{CP}, t_{RP} t_{WP}	80	-	ns
Data Set Up Time	t_{DS}	80	-	ns
Data Hold Time	t_{DH}	40	-	ns
Access Time	t_{ACC}	-	150	ns
Output Hold Time	t_{OH}	10	50	ns

Conditions : V_{DD}=5±0.25V, GND=0V, Ta=25°C

Fig. 3.2 Bus Timing



3.4 Memory Address and Display Position (In case of 6x8 dots/fonts)

Relationship between display memory address and display position on LCD module is defined in the following maps. Text home address TH, Number of text area TA=16H(HEX.), Graphic home address GH and Number of graphic area GA=16H(HEX.) are defined by "Internal RAM Write" command. TH and GH can be defined in the memory area, but all memory address should be located within 0000H to 1FFFH (8k byte memory area).

3.4.1 Text Display

TH	TH+1H		TH+13H	TH+14H
TH+TA	TH+TA+1H		TH+TA+13H	TH+TA+14H
				16 lines
TH+14TA	TH+14TA+1H		TH+14TA+13H	TH+14TA+13H
TH+15TA	TH+15TA+1H		TH+15TA+13H	TH+15TA+13H

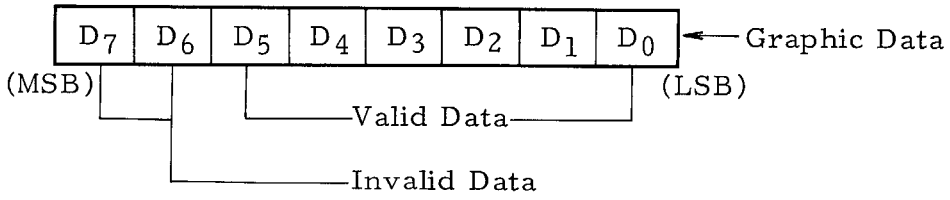
21 character

3.4.2 Graphic Display

GH	GH+1H		GH+13H	GH+14H
GH+GA	GH+GA+1H		GH+GA+13H	GH+GA+14H
				128 dots
GH+126GA	GH+126GA+1H		GH+126GA+13H	GH+126GA+14H
GH+127GA	GH+127GA+1H		GH+127GA+13H	GH+127GA+14H

21 x 6 dots

Note : In case of graphic display,



3.5 Memory Address and Display Position (In case of 8x8 dots/fonts)

Relationship between display memory address and display position on LCD module is defined in the following maps. Text home address TH, Number of text area TA=10H(HEX.), Graphic home address GH and Number of graphic area GA=10H(HEX.) are defined by "Internal RAM Write" command. TH and GH can be defined in the memory area, but all memory address should be located within 0000H to 1FFFH (8k byte memory area).

3.5.1 Text Display

TH	TH+1H		TH+0EH	TH+0FH
TH+TA	TH+TA+1H		TH+TA+0EH	TH+TA+0FH
≈				≈16 lines
TH+14TA	TH+14TA+1H		TH+14TA+0EH	TH+14TA+0FH
TH+15TA	TH+15TA+1H		TH+15TA+0EH	TH+15TA+0FH

16 character

3.5.2 Graphic Display

GH	GH+1H		GH+0EH	GH+0FH
GH+GA	GH+GA+1H		GH+GA+0EH	GH+GA+0FH
≈				≈128 dots
GH+126GA	GH+126GA+1H		GH+126GA+0EH	GH+126GA+0FH
GH+127GA	GH+127GA+1H		GH+127GA+0EH	GA+127GA+0FH

16 x 8 dots

Note : In case of graphic display,

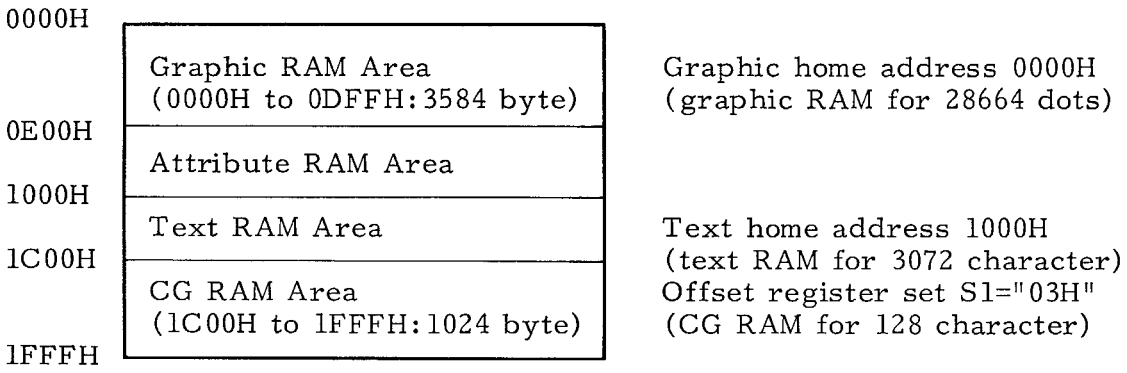
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	← Graphic Data

(MSB) Valid Data (LSB)

3.6 RAM Map

Display RAM is built-in the module, and display data is written to this display RAM. Built-in controller LSI T6963C is automatically read from display RAM, and send data to LCD drivers. "Control word set" command (text home set, text area set, etc.) defines the RAM area which is read by controller LSI, so RAM map can be changed by user's preference.
If more than 1 screen can be stored in the RAM, vertical scrolling and paging is easily performed by resetting text home and/or graphic home address.
These modules have 8k byte built-in RAM located at address 0000H to 1FFFH, and the following is an example of RAM mapping.

*** Example of RAM MAP ***
(In case of 8x8 dots/fonts)



Note 1 : Above example of RAM map is for "CG ROM Mode", in case of "CG RAM Mode" is selected, 2048 byte CG RAM area is necessary. So above RAM map should be relocated.

3.7 Pin Setting of LCD Controller LSI (T6963C)

The pin setting of controller LSI (T6963C) is as follows :

Display Size (Number of rows)	16 lines (128 dots)	MDS="H" MD1="L" MD0="L"
Columns of display	32 columns	MD2="H" MD3="H"
Character font	6x8 dots or 8x8 dots	FS0 ="L"
1/2 screen	1 screen	DUAL="H"

Operating Frequency of controller T6963C(f_{OSC}) is 4.55±0.5 MHz.

Note : Character font can be selected 6x8 dots or 8x8 dots.
Please refer page 8 (Pin No. 19; Font Select).

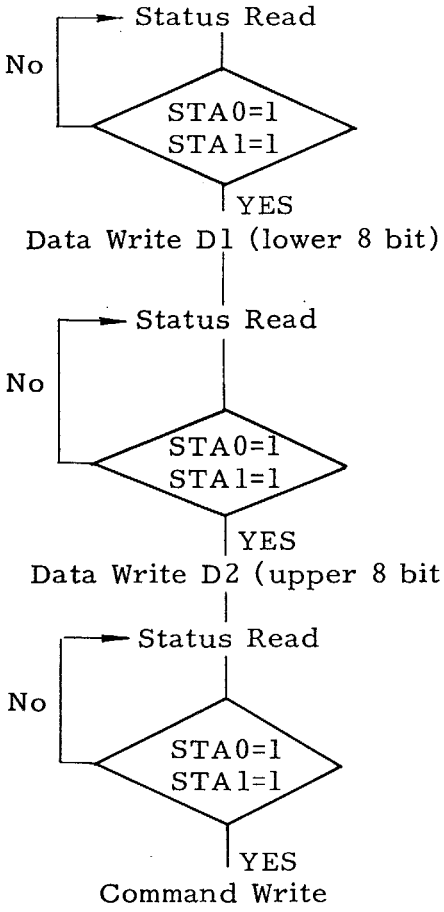
4. Communication between CPU and Module

4.1 Control Sequence

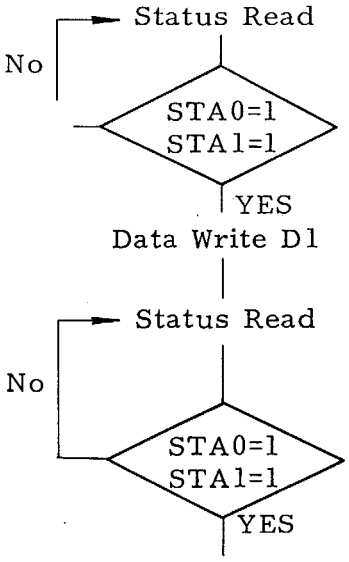
4.1.1 Data Transmission Method

Built-in LCD controller T6963C is operating asynchronously to CPU clock, and following procedure is required for data transmission between module and CPU.

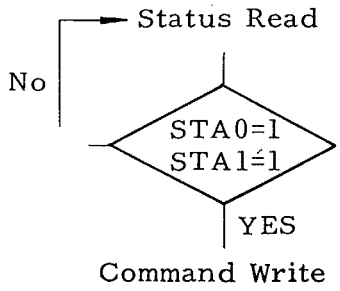
(1) Command with 2 byte data



(2) Command with 1 byte data



(3) Command with no data



(4) Data Auto Write/Data Auto Read

STA2, STA3 should be checked between all data and command.

(Refer 4.2.2.6 "Data Auto Write/Data Auto Read")

(5) Screen Peeking, Screen Copy

STA6 should be checked just after "Screen Peeking"/"Screen Copy".

(Refer 4.2.2.8/9 "Screen Peeking", "Screen Copy")

4.1.2 Status Read

Status of controller LSI should be checked between all command and data in order to complete communication with CPU. Status can be read from 8 bit data lines (D0 to D7) by setting C/$\overline{D}$="H", $\overline{RD}$="L".

STA0 (Busy1)	Check capability of instruction execution	STA0=0 : Disable =1 : Enable
STA1 (Busy2)	Check capability of data read or data write	STA1=0 : Disable =1 : Enable
STA2 (DAV)	Check capability of data read (only effective in auto mode)	STA2=0 : Disable =1=: Enable
STA3 (RDY)	Check capability of data write (only effective in auto mode)	STA3=0 : Disable =1 : Enable
STA4	–	–
STA5 (CLR)	Check posibility of controller operation	STA5=0 : Disable =1 : Enable
STA6 (Error)	Address pointer is out of graphic area on screen peeking and screen copy command	STA6=1 : Out of graphic area
STA7 (Blink)	Check the condition of blink	STA7=0 : Display off =1 : Normal display(on)

(Status Register)

STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0

MSB LSB

4.2 Command

4.2.1 Command List

Command	Command Code								Discription	Execution time (MAX) (Note 1)
	D7	D6	D5	D4	D3	D2	D1	D0		
Pointer Set	0	0	1	0	0	N2	N1	N0	N2 N1 N0 0 0 1 Cursor pointer set 0 1 0 Offset resister set 1 0 0 Address pointer set	Status check
Control word Set	0	1	0	0	0	0	N1	N0	N1 N0 0 0 Text home address set 0 1 Text area set 1 0 Graphic home address set 1 1 Graphic area set	Status check
Mode Set	1	0	0	0	CG	N2	N1	N0	CG=0:CG ROM Mode CG=1:CG RAM Mode N2 N1 N0 (Graphic and Text) 0 0 0 "OR" 0 0 1 "EXOR" 0 1 1 "AND" 1 0 0 Text only (attribute capability)	32x1/fOSC
Display Mode	1	0	0	1	N3	N2	N1	N0	N3=0:Graphic display off 1:Graphic display on N2=0:Text display off 1:Text display on N1=0:Cursor display off 1:Cursor display on N0=0:Cursor blink off 1:Cursor blink on	32x1/fOSC
Cursor Pattern Select	1	0	1	0	0	N2	N1	N0	N2,N1,N0 specify the number of cursor lines (EX) N2 N1 N0 0 0 0 1 line cursor (bottom line) 1 1 1 8 line cursor (8x8 dot cursor)	32x1/fOSC
Data Auto Read/Write	1	0	1	1	0	0	N1	N0	N1 N0 0 0 Data auto write set 0 1 Data auto read set 1 * Auto reset After this command, continuous data can be write or read. (address pointer automatically increment)	32x1/fOSC
Data Read/ Write	1	1	0	0	0	N2	N1	N0	Data read/write command for 1 byte. N2=0:Address pointer up/down =1:Address pointer unchanged N1=0:Address pointer up =1:Address pointer down N0=0:Data write =1:Data read	32x1/fOSC
Screen Peeking	1	1	1	0	0	0	0	0	Transfer display data to data stack for read from CPU.	Status check
Screen Copy	1	1	1	0	1	0	0	0	1 line displayed data which address is indicated by address pointer is copied to graphic RAM area.	Status check
Bit Set/ Reset	1	1	1	1	N3	N2	N1	N0	Set/reset command for a bit in the address pointed by address pointer. N3=0:Bit reset =1:Bit set N2,N1,N0 indicates the bit in the pointed address (000 is LSB, and 111 is MSB.)	Status check

Note 1 : Status check between all commands and data is recommended, though execution time for several commands are specified in above command list. For the commands with "status check" in execution time, execution time does not specified because it is influenced by internal situation of controller LSI.

2 : In case of 2 screen mode, Screen copy command cannot be used.

4.2.2 Description of Command

4.2.2.1 Pointer Set Command

D1, D2,	0	0	1	0	0	N2	N1	N0

Command is selected by setting "1" at selected bit.

N2	N1	N0	Command	D1	D2
0	0	1	Cursor pointer set	column position	row position
0	1	0	Offset register set	address	00H
1	0	0	Address pointer set	address(Lower)	address(upper)

(a) Cursor Pointer Set

The cursor is displayed at the position specified by the D1, D2. The cursor position is shift only by this command, and does not shift by other command like a "data write" command.

D1, D2 are specified as follows.

D1 : Horizontal cursor position counted by "character" (5∿8 dot width/ character specified by hard setting .. refer 3.5 "Pin Setting of LCD controller LSI"). MSB of D1 is neglected, and 127 is the maximum.

D2 : Vertical cursor position counted by "character" (8 dot high character) (1st row of lower half screen is "11H")
Upper 3 bit are neglected and 32 is the Maximum.

Note : Please note that the cursor position should be within actual display area.

(b) Offset Register Set

Offset register set command is used to determine character generator RAM area. The upper 5 bits in start address of CG area is set as the lower 5 bits of D1, and upper 3 bits of D1 is neglected. D2 should be 00H.

Refer 4.4 "Character Generator" for detail of CG RAM.

(c) Address Pointer Set

Address pointer set command is used to indicate the start address for writing data to built-in RAM, or for reading data from built-in RAM. The address should be located in the actual RAM area specified by individual specifications. (refer to 3.4.2 "RAM MAP")

4.2.2.2 Control Word Set Command

D1, D2,	0	1	0	0	0	0	N1	N0

Home address of display RAM (Text, Graphic), and areas are defined by this command.

N1	N0	Command	D1	D2
0	0	Text Home Address Set (TH)	Address(lower)	Address(upper)
0	1	Text Area Set (TA)	No. of column	00H
1	0	Graphic Home Address Set (GH)	Address(lower)	Address(upper)
1	1	Graphic Area Set (GA)	No. of column	00H

(a) Text Home Address Set (TH)

T This command defines the starting address of display RAM for text display. The data in the Text home address(TH) is displayed at the home position of display (left end character on lst row).

(b) Text Area Set (TA)

This command defines the number of column by D1. Text area can be defined independent from character No. fixed by hard setting of controller LSI. Text area is usually defined the same number as the actual character number of LCD display, so address can be continuous in text area in this case.

(c) Graphic Home Address Set (GH)

This command defines the starting address of display RAM for graphic display. The data in the Graphic home address (GH) is displayed at the home position of display (left end 8 bits in 1st line).
When using attribute function, Graphic home address indicates the starting address of attribute RAM area.

(d) Graphic Area Set (GA)

This command defines the number of column by D1. Graphic area can be defined independent from character No. fixed by hard setting of controller LSI. So address in graphic area can be continuous and RAM area can be used without uneffective area, if graphic area is defined the same number as the actual column number of LCD display. Note that graphic area will be different by character font setting even if horizontal dot number is the same.

4.2.2.3 Mode Set Command

(No data)	1	0	0	0	CG	N2	N1	N0

Mode set command selects character generator (CG ROM Mode/CG RAM Mode), and combination of text/graphic display.

CG	Command
0	CG ROM Mode: built-in 128 character CG ROM (code:00H~ 7FH) and built-in CG RAM (code:80H~FFH) for 128 characters can be used
1	CG RAM Mode: Built-in CG RAM for 256 characters (code : 00H~ FFH) can be used

When CG ROM Mode is selected, character code 00H~ 7FH is selected from built-in CG ROM and 80H~ FFH is automatically selected from CG RAM.

N2	N1	N0	Command
0	0	0	Logically "OR" of Graphic and Text display
0	0	1	Logically "EXOR" of Graphic and Text display
0	1	1	Logically "AND" of Graphic and Text display
1	0	0	Text display only (text can be attributed by the data in graphic area)

Logically "OR", "EXOR" and "AND" of graphic and text display can be displayed by this command. Only text display is attributed because Attribute RAM is located in Graphic RAM area.
(refer 4.5 "Attribute")

4.2.2.4 Display Mode Set Command

(No data)

1	0	0	1	N3	N2	N1	N0

Display mode is selected from combination of following 4 bits by setting "1" at the selected bit.

	Command		
N0	Cursol blink	ON(N0=1)/Cursol blink	OFF(N0=0)
N1	Cursol display	ON(N1=1)/Cursol display	OFF(N1=0)
N2	Text display	ON(N2=1)/Text display	OFF(N2=0)
N3	Graphic display	ON(N3=1)/Graphic display	OFF(N3=0)

After hard reset, all displays are inhibited. (N0=N1=N2=N3=0)

4.2.2.5 Cursor Pattern Select Command

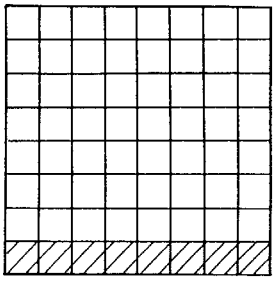
(No data)

1	0	1	0	0	N2	N1	N0

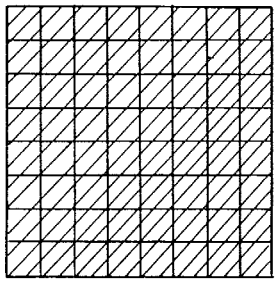
When cursor display is "ON", this command selects the cursor pattern from 1 line width cursor to 8 line width cursor (block).

N2	N1	N0	Cursor pattern
0	0	0	1 line width cursor
0	0	1	2 line width cursor
0	1	0	3 line width cursor
0	1	1	4 line width cursor
1	0	0	5 line width cursor
1	0	1	6 line width cursor
1	1	0	7 line width cursor
1	1	1	8 line width cursor

(1 line width cursor)



(8 line width cursor)



4.2.2.6 Data Auto Write/Data Auto Read

(No data)

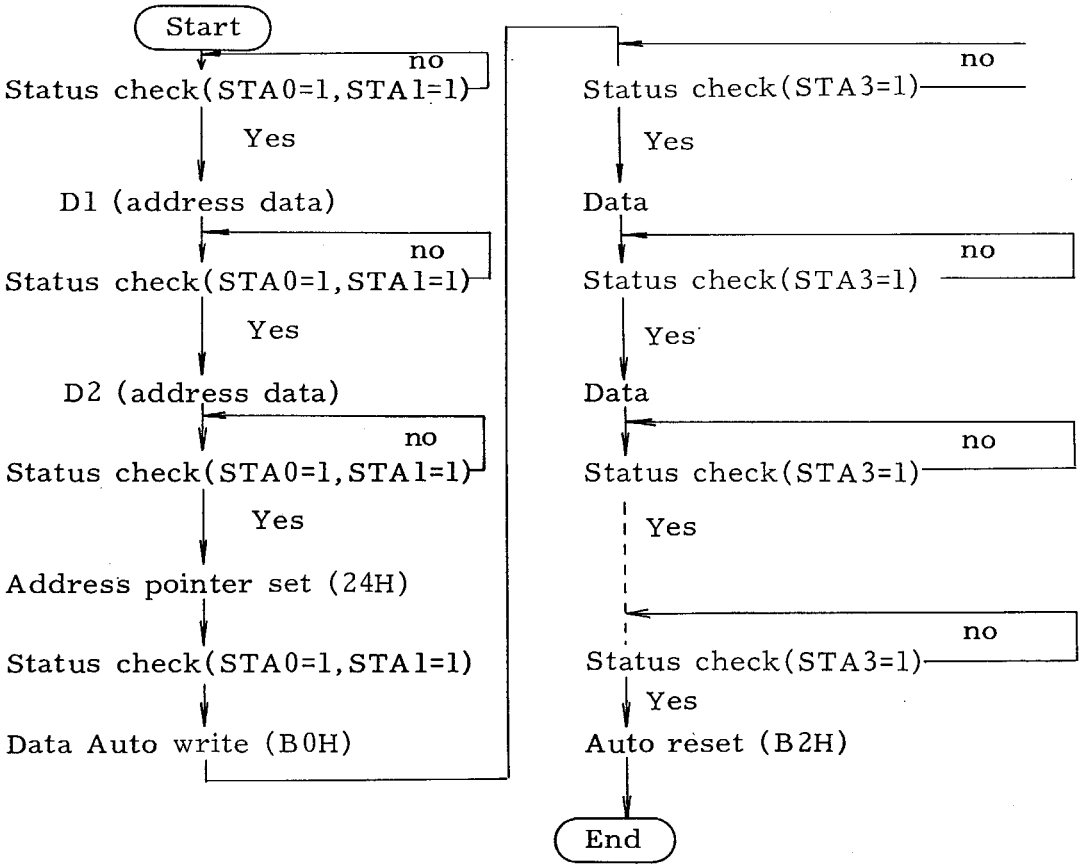
1	0	1	1	0	0	N1	N0

This command is convenient to send full screen data, or recieve full screen data from built-in RAM. After setting auto mode, "data write (or read)" command is not necessary between each data. "Data auto write (or read)" command should follow the "address pointer set" and address pointer is automatically increment by +1 after each data. After sending (or recieving) all data, Auto mode reset is necessary to return normal operation because all data is regarded "display data" and no command can be accepted in the auto mode.

N1	N0	Command
0	0	Data Auto Write set
0	1	Data Auto Read set
1	*	Auto Mode Reset

* : Don't care

Note : Status check for auto mode (STA2, STA3) should be checked between each data. Auto reset should be performed after checking STA3=1 (Data Auto write only). Refer following chart.



4.2.2.7 Data Write/Data Read

D1,

1	1	0	0	0	N2	N1	N0

Note : D1 is necessary only for data write.

This command is used for data write from CPU to built-in RAM, and data read from built-in RAM to CPU. Data write/data read should be executed after setting address by address pointer set command. Address pointer can be automatically increment or decrement by setting this command.

N2	N1	N0	
0	0	0	Data Write (after execution address pointer increment)
0	0	1	Data Read (after execution address pointer increment)
0	1	0	Data Write (after execution address pointer decrement)
0	1	1	Data Read (after execution address pointer decrement)
1	*	0	Data Write (after execution address pointer unchanged)
1	*	1	Data Read (after execution address pointer unchanged)

* : Don't care

This command is necessary for each 1 byte data.

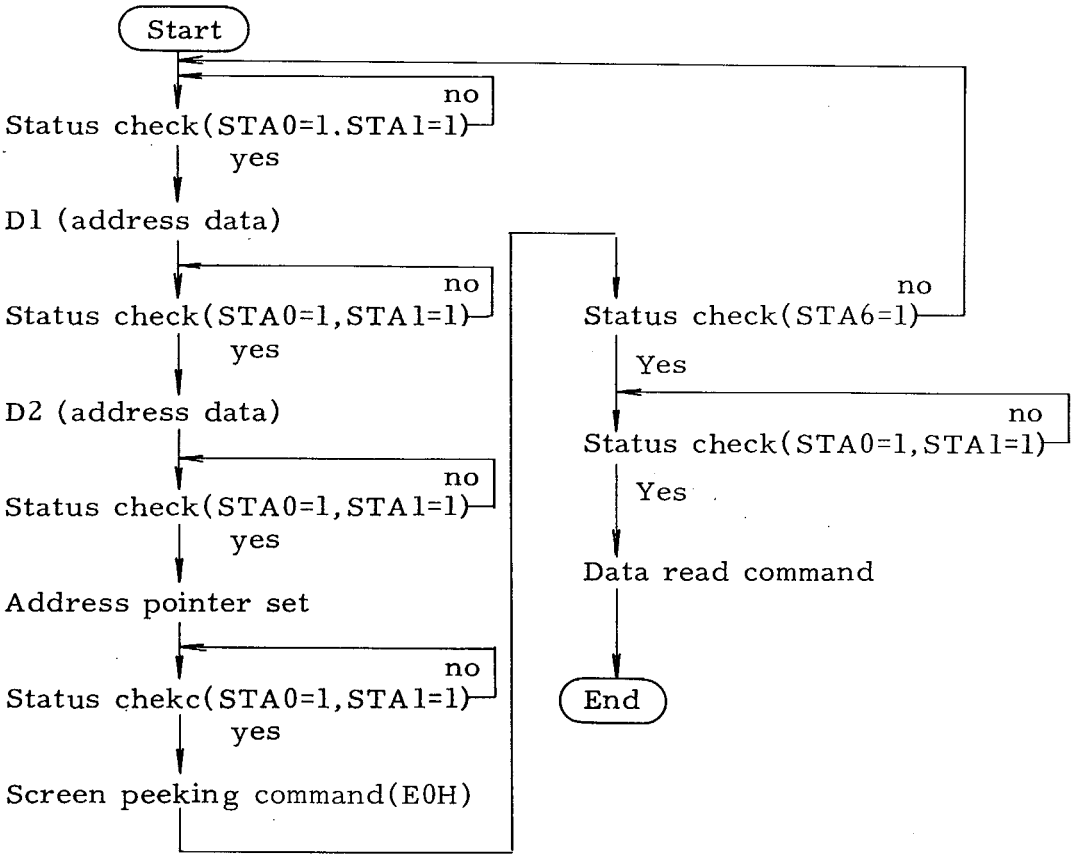
4.2.2.8 Screen Peeking

(No data)

1	1	1	0	0	0	0	0

This command is used to transfer displayed 1 byte data to data stack, and this 1 byte data can be read from CPU by data read command. So, logical combination data of text and graphic display on LCD screen can be read by this command.
Status (STA6) should be checked just after "screen peeking" command. If the address determined by "address pointer set" command is not in graphic RAM area, this command is ignored and status flag (STA6) is set.

The procedure to read displayed data using this command is as follows.



Screen peeking command can be used for getting hardcopy of LCD display. Another application of this command is that modified CG is set in the CG RAM area by reading combination data of text and graphic data and writing to CG RAM area. For example, CG for reverse character is made by this method.

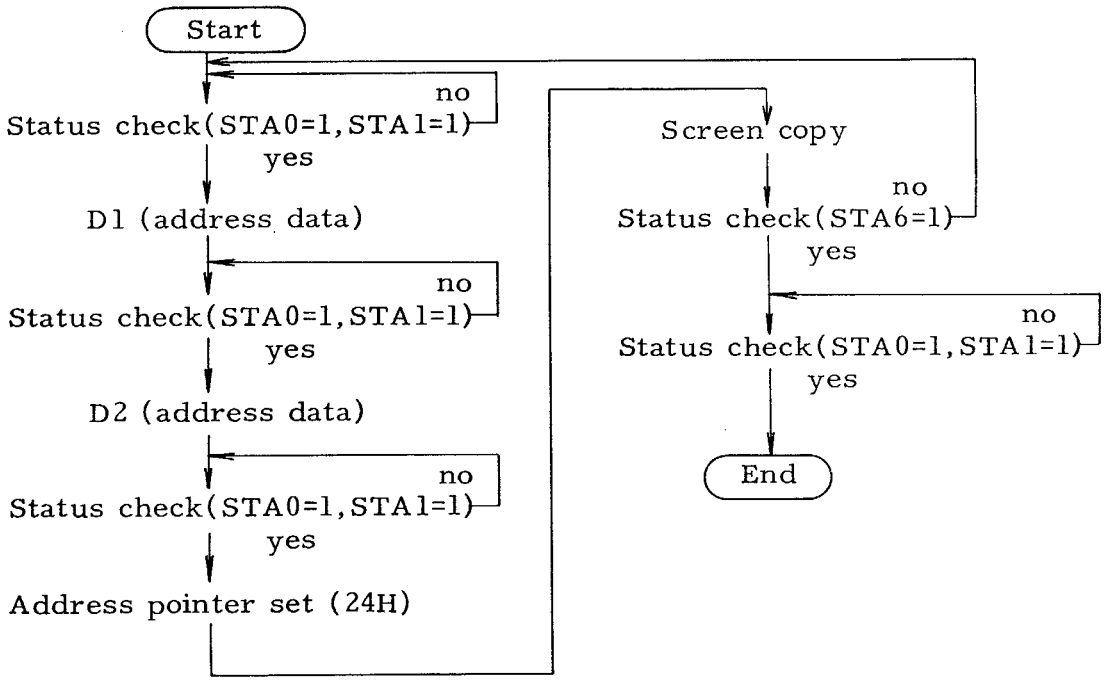
Note: For using this command, Text area set (TA) and Graphic area set (GA) should be defined as same number as "columns of display" in pin setting. (32 columns)

4.2.2.9 Screen Copy

(No data)	1	1	1	0	1	0	0	0

1 low data displayed in LCD screen can be copied to the graphic RAM area specified by "address pointer set" command. Start point of 1 low data in the screen is determined by the "address pointer set" command. If attribute for text display is set by "Mode Set" command, "screen copy" command can not be used.

Status (STA6) should be checked just after this command. If the address determined by "address pointer set" command is not located in graphic RAM area, This command is ignored and status flag (STA6) is set. The procedure to copy the displayed data using this command is as follows.



Note: For using this command, Text area set (TA) and Graphic area set (GA) should be defined as same number as "columns of display" in pin setting. (32 columns)

4.2.2.10 Bit Set, Bit Reset

(No data)	1	1	1	1	N3	N2	N1	N0

One bit in the 1 byte data specified by "address pointer set" command can be set or reset. Plural bits in the 1 byte data cannot be set/reset at a time.

	Discription			
N3	N3=1:bit set, N3=0:bit reset			
N2 N1 N0	N2, N1, N0 specify the bit for set/reset.	N2,N1,N0		
		0	0	0 bit 0 (LSB)
		0	0	1 bit 1
		0	1	0 bit 2
		⋮	⋮	⋮
		1	1	1 bit 7 (MSB)

4.3 Initialization

Initialization by hardware and software is necessary for reset of hardware and to determine home position and number of characters to be displayed. Display data (graphic/text data) should be written to the RAM area defined by initialization ("Text home address set", "Graphic home address set" command etc.).

The address of written data is determined by "Address pointer set" command just before sending display data.

Following is the one of example of initialization and data write procedure for TLX-1391/TLX-1391-E0 (In case of 8 x 8 dots/font).

Command	C/$\overline{D}$	D7	D6	D5	D4	D3	D2	D1	D0	Note
Power on	Power on									
Hard reset (use reset terminal)	RESET="L" (1msec minimum after $V_{DD} \geq 4.75$çV)									
Mode set	1	1	0	0	0	0	0	0	0	"OR" mode
Control word set Graphic home position set (Graphic home position 0000H)	0 0 1	0 0 0	0 0 1	0 0 0	0 0 0	0 0 0	0 0 0	0 0 1	0 0 0	} graphic home address command
Number of graphic area set (Graphic 16x8 dots)	0 0 1	0 0 0	0 0 1	0 0 0	1 0 0	0 0 0	0 0 0	0 0 1	0 0 1	} number of area command
Text home position set (Text home position 1000H)	0 0 1	0 0 0	0 0 1	0 0 0	0 1 0	0 0 0	0 0 0	0 0 0	0 0 0	} text home address command
Number of text area set (Text 16 column)	0 0 1	0 0 0	0 0 1	0 0 0	1 0 0	0 0 0	0 0 0	0 0 0	0 0 1	} number of area command
(Initialize end) (Data Write)										
Address pointer set (address pointer 0000H)	0 0 1	0 0 0	0 0 0	0 0 1	0 0 0	0 0 0	0 0 1	0 0 0	0 0 0	} graphic home address command
Data write (graphic)	0 1	0 1	1 1	0 0	1 0	0 0	1 0	0 0	1 0	Data command
	0 1	1 1	0 1	1 0	0 0	1 0	0 0	1 0	0 0	Data command
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
Address pointer set (address position 1000H)	0 0 1	0 0 0	0 0 0	0 0 1	0 1 0	0 0 0	0 0 1	0 0 0	0 0 0	} Text home address Command
Data write (T) (Text)	0 1	0 1	0 1	1 0	1 0	0 0	1 0	0 0	0 0	Data Command
(O)	0 1	0 1	0 1	1 0	0 0	1 0	1 0	1 0	1 0	Data Command
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
Display Mode Set (text/graphic on)	1	1	0	0	1	1	1	0	0	

Note 1: "Status check" should be inserted between all command and data.

2: Written data is displayed on the LCD just after "Display Mode Set" command (9CH), because display mode set resister is cleared to no display mode by hard reset.

3: Display RAM area is not automatically cleared by initialization, so it is recommended to set "text/graphic on" by "Display Mode Set" command after data of all screen is written to the display RAM.

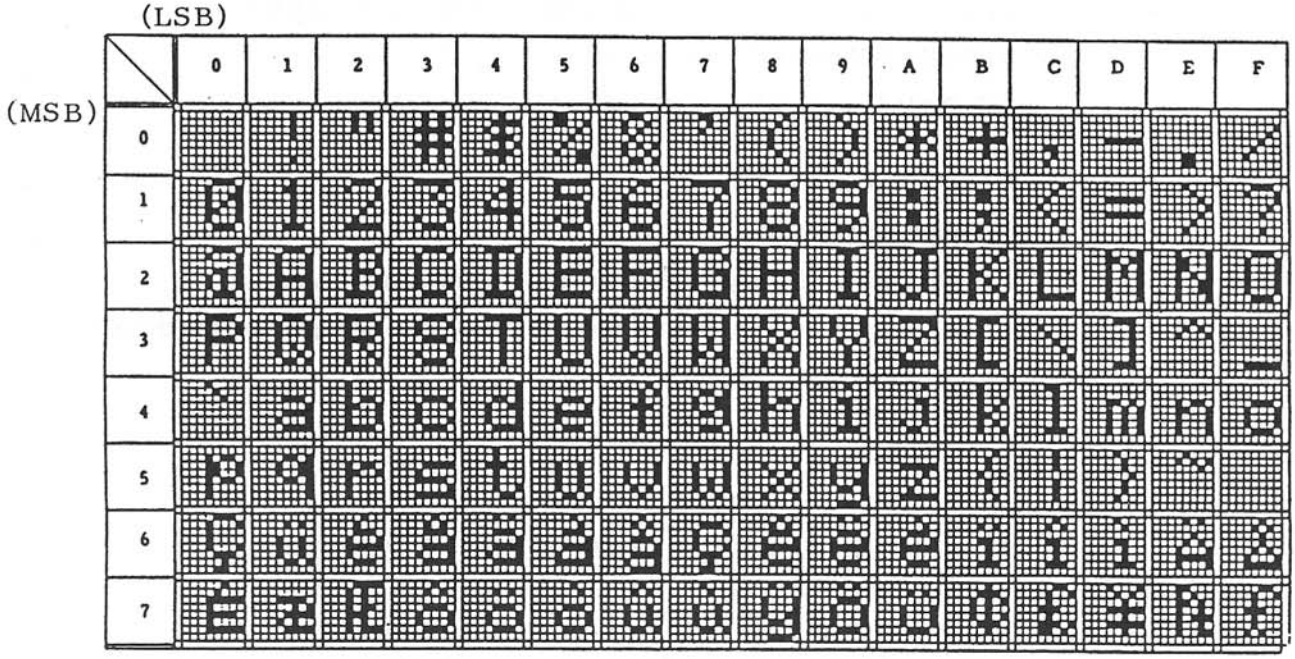
4.4 Character Generator

4.4.1 Character Generator ROM

Character generator ROM for 128 characters is built-in this module. "Mode Set" for "CG ROM Mode" should be selected before using built-in C/G ROM.

Character pattern and character code is shown in following chart.

CG ROM PATTERN



4.4.2 User Character Generator RAM

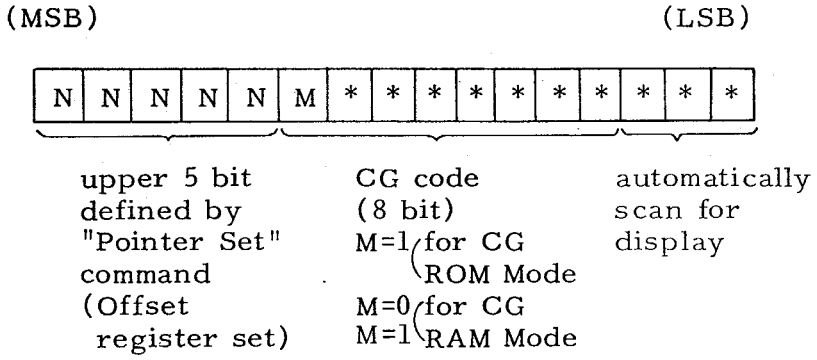
Character generator RAM is the built-in RAM which can be used as character generator after writing character pattern by program. The part of built-in RAM can be used as "User CG RAM" for 256 characters by selecting "CG RAM Mode", or for 128 characters by selecting "CG ROM Mode".

(1) Position of User CG RAM

The upper 5 bits in start address of User CG RAM (NNNNN) is defined by "Pointer Set" command (Offset register set), and following 2048 byte are defined as "User CG RAM" area when CG RAM Mode is selected. 1024 byte (address : NNNNN10000000000∿NNNNN11111111111) is defined as "User CG RAM" area when CG ROM Mode is selected.

(2) Writing to User CG RAM

Character pattern of specified CG code can be written in the pointed address by "Pointer Set" command (Address pointer set). 8 byte data should be sent to following 8 byte address for 1 character.



(3) Display Pattern in User CG RAM

Character pattern can be displayed by sendined CG code with "Data Write" command. But "Display Mode Set" for text display should be selected before using CG.

In case that "CG ROM Mode" is selected, character pattern is selected from built-in CG ROM when MSB=0 (00H-7FH), and from User CG RAM when MSB=1(80H-FFH).

In case that "CG RAM Mode" is selected, all character patterns are selected from User CG RAM (00H-FFH).

(4) Relation between User CG RAM Address and CG code and Character Pattern

When character pattern is written to User CG RAM, relation between CG code and "User CG RAM" address is shown in following chart.

Character Code 7 6 5 4 3 2 1 0	RAM Address for User CG F E D C B A 9 8 7 6 5 4 3 2 1 0	Character Pattern 7 6 5 4 3 2 1 0
M 0 0 0 0 0 0 0	N N N N N M 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	0 0 1	0 0 0 0 1 0 0 0
	0 1 0	0 0 0 0 0 1 0 0
	0 1 1	0 1 1 1 1 1 1 0
	1 0 0	0 0 0 0 0 1 0 0
	1 0 1	0 0 0 0 1 0 0 0
	1 1 0	0 0 0 0 0 0 0 0
	1 1 1	0 0 0 0 0 0 0 0
M 0 0 0 0 0 0 1	N N N N N M 0 0 0 0 0 0 1 0 0 0	0 1 0 0 0 0 1 0
	0 0 1	0 1 1 0 0 1 1 0
	0 1 0	0 1 0 1 1 0 1 0
	0 1 1	0 1 0 1 1 0 1 0
	1 0 0	0 1 0 0 0 0 1 0
	1 0 1	0 1 0 0 0 0 1 0
	1 1 0	0 1 0 0 0 0 1 0
	1 1 1	0 0 0 0 0 0 0 0
M 0 0 0 0 0 1 0	N N N N N M 0 0 0 0 0 1 0 0 0 0	0 1 0 0 0 0 1 0
	0 0 1	0 1 1 0 0 0 1 0
	0 1 0	0 1 0 1 0 0 1 0
≈	≈	≈
	1 1 1	0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1	N N N N N 1 1 1 1 1 1 1 1 0 0 0	0 1 1 1 0 0 0 0
	0 0 1	0 1 0 0 0 0 0 0
	0 1 0	0 1 1 1 1 0 1 0
	0 1 1	0 0 0 1 1 0 1 0
	1 0 0	0 1 1 1 1 0 1 0
	1 0 1	0 0 0 0 1 1 1 0
	1 1 0	0 0 0 0 1 0 1 0
	1 1 1	0 0 0 0 1 0 1 0

Note 1 : Character code in "User CG RAM" is located from 80H to FFH in case of "CG ROM Mode", and from 00H to FFH in case of "CG RAM Mode". So, M in above chart is as follows.

M=1 : "CG ROM Mode"
M=0 : "CG RAM Mode"

2 : "NNNNN" is the upper 5 bits in start address of User CG RAM defined by "Pointer Set" command (Offset Register Set).

3 : It must be careful so that User CG RAM area should not be rewitten by display data etc.

4.5 Attribute

4.5.1 Attribute function

This module has attribute function for "Reverse display", "Blink" in text display mode. Attribute data is written in the "Graphic area" defined by "Control word set" command (Graphic home address set and Graphic area set). So "Text display only" Mode should be selected by "Mode Set" command, and graphic display cannot be displayed.

The attribute data of the 1st character in "Text area" is written at the 1st 1 byte in "graphic area", and attribute data of nth character is written at the nth 1 byte in "Graphic area". Attribute function is defined as follows.

Attribute RAM
1 byte

*	*	*	*	N3	N2	N1	N0

N3	N2	N1	N0	function
0	0	0	0	Normal display
0	1	0	1	Reverse display (Text only)
0	0	1	1	Inhibit display
1	0	0	0	Blink of normal display
1	1	0	1	Blink of reverse display
1	0	1	1	Inhibit display

* : Don't care

4.5.2 Procedure of setting attribute

The example of the setting procedure for attribute is as follows.

Command	C/$\overline{D}$	D7	D6	D5	D4	D3	D2	D1	D0	Note
Graphic display off	1	1	0	0	1	0	*	*	*	
Graphic home address set	0	0	0	0	0	0	0	0	0	} home address
	0	0	0	0	0	1	1	1	0	} 0E00H
	1	0	1	0	0	0	0	1	0	command
Attribute data write	0	0	0	0	0	0	0	0	0	} address
	0	0	0	0	0	1	1	1	0	} 0E00H
	1	0	0	1	0	0	1	0	0	address pointer
	0	0	0	0	0	0	0	0	0	attribute data
	1	1	1	0	0	0	0	0	0	write command
	0	0	0	0	0	1	1	0	0	attribute data
	1	1	1	0	0	0	0	0	0	write command
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
Mode set	1	1	0	0	0	0	1	0	0	
Graphic display on	1	1	0	0	1	1	*	*	*	

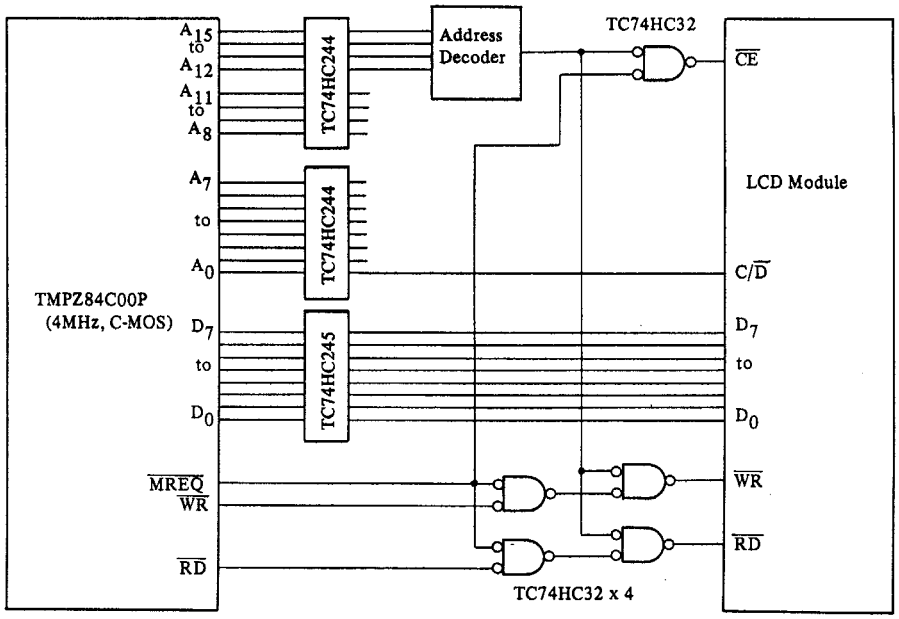
* : Don't care

5. Application Circuit

Following diagrams are the examples of interface circuit with CPU TMPZ84C00P(Z80®, CMOS 4MHz). For the interface to 16 bit CPU, please refer the diagram using PPI LSI (TMP82C55).

5.1 Module Located in the Memory Area of CPU

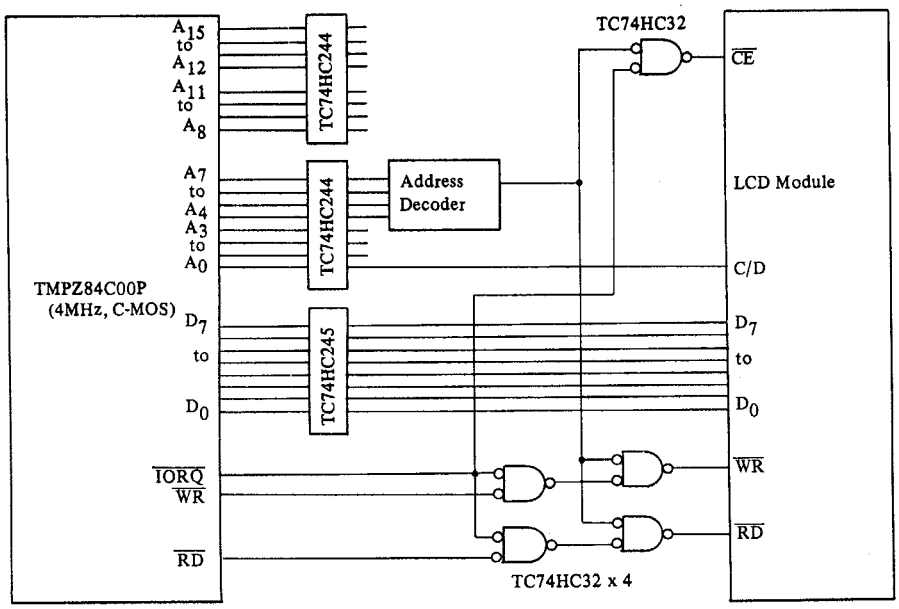
The module can be directly connected to CPU data bus as following diagram. Control signals of the module are made from $\overline{MREQ}$, $\overline{WR}$, $\overline{RD}$ signals of CPU, and chip select signal from address decorder. LSB of address bus (A0) can be used as C/$\overline{D}$ (command/data selection) signal.



5.2 Module located in the I/O Area of CPU

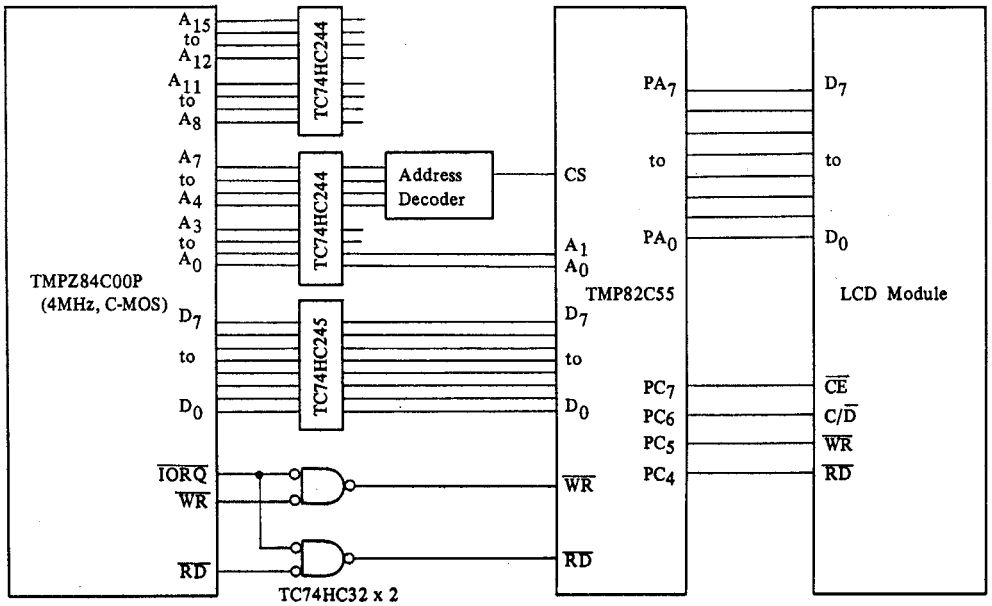
The module can be controlled as the device located in the I/O area. Control signals are made from $\overline{IORQ}$, $\overline{WR}$, $\overline{RD}$ of CPU, and the chip select signal from address decorder. LSB of address bus (A0) can be used as C/$\overline{D}$ (command/data selection) signal.

Note: Z80® is registered trademark of Zilog Inc.



5.3 Interface circuit with PPI LSI (TMP82C55)

The module can be interfaced with PPI LSI as shown in following diagram. 8 bit data bus of the module is connected to A port of PPI, and control signals (C/$\overline{D}$, $\overline{CE}$, $\overline{WR}$, $\overline{RD}$) are sent from upper 4 bit of C port. In following diagram PPI is located in the I/O address area, but interface between CPU and PPI can be left for user's design.



6. Installation

For installation of the module, use four U-shape mounting holes located at the corners of PCB.
The bezel is not intended to be used as a cosmetic purpose. A proper protective cover (Lens) over the LCD surface are recommended to be attached in order to prevent polarizer surface from scratching or staining. The transparent opening dimensions of protective cover is recommended to be smaller than the viewing area specified in Section 2.2 (Page 5).

7. Cautions and Handling Precautions

7.1 Handling

(a) Refrain from strong mechanical shock or applying force to the display plane. It may cause malfunction or damage of LCD.

(b) In the case of leakage of liquid crystal material, avoid ingestion, contact of skin. If liquid crystal material sticks to skin, wash with alcohol and rinse thoroughly with water.

(c) Note that LCD surface (polarizer) is very soft as is easily damaged. Do not press the polarizer surface with hard object.

(d) The polarizer and adhesive used for lamination may be attacked by some organic solvent. When LCD surface becomes dirty wipe softly with absorvent cotton soaked in benzine.

(e) Protect the LCD module from the electro-static discharge. It will damage C-MOS LSI in the module.

7.2 Storage

(a) Do not leave the LCD module in high temperature, especially in high humidity for a long time. It is recommended to store it in the place where the temperature is between 0°C and 35°C, and where the humidity is lower than 70%.

(b) Store the module without exposure to the direct sunlight.

7.3 Operation

(a) Do not connect or remove LCD module to main system with power applied.

(b) Power supplies should always turned on before the independent input signal sources are turned on, and input signals should be turned off before power supplies are turned off.

7.4 Others

(a) Avoid condensation of water, it may cause misoperation or corrosion of electrode.

(b) Ultraviolet ray cut filter is necessary for outdoor operation.

(c) Do not exceed the absolute maximum ratings under the worst probable conditions with respect to supply voltage variation, input voltage variation, environmental temperature etc., otherwise LCD module may be damaged.

(d) The brightness of EL backlighting may be a half of initial value after 2500 hours operating by the typical operating conditions.

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