16-CHANNEL LED DRIVER WITH DOT CORRECTION AND GRAYSCALE PWM CONTROL

FEATURES

- **16 Channels**
- **12-bit (4096 Steps) Grayscale PWM Control**
- **Dot Correction**
  - **6 bit (64 Steps)**
- **Drive Capability (Constant-Current Sink)**
  - **0 mA to 80 mA**
- **LED Power Supply Voltage up to 17 V**
- **V_{CC} = 3.0 V to 5.5 V**
- **Serial Data Interface, SPI Compatible**
- **Controlled In-Rush Current**
- **30-MHz Data Transfer Rate**
- **CMOS Level I/O**
- **Error Information**
  - **LOD: LED Open Detection**
  - **TEF: Thermal Error Flag**

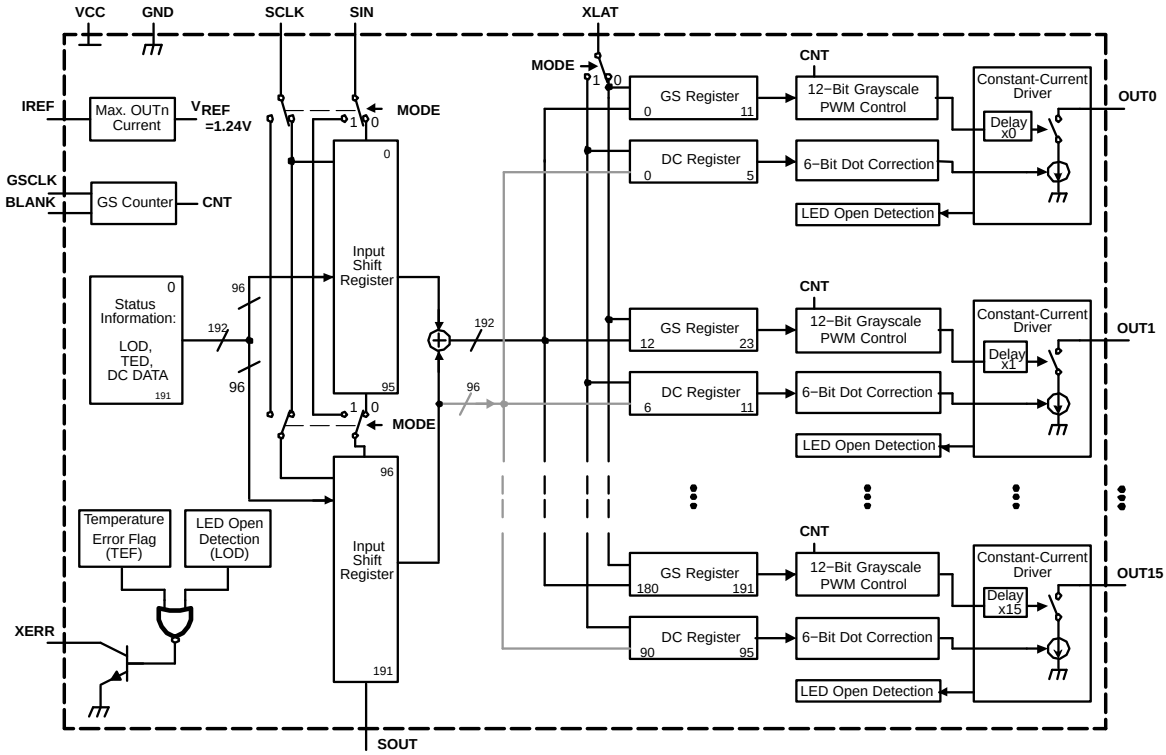
APPLICATIONS

- **Monocolor, Multicolor, Full-Color LED Displays**
- **LED Signboards**
- **Display Back-lighting**

DESCRIPTION

The TLC5941 is a 16-channel, constant-current sink, LED driver. Each channel has an individually adjustable 4096-step grayscale PWM brightness control and a 64-step constant-current sink (dot correction). The dot correction adjusts the brightness variations between LED channels and other LED drivers. Both grayscale control and dot correction are accessible via a serial interface. A single external resistor sets the maximum current value of all 16 channels.

The TLC5941 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an overtemperature condition.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE(1)	PART NUMBER
–40°C to 85°C	28-pin HTSSOP PowerPAD™	TLC5941PWP
–40°C to 85°C	32-pin 5 mm x 5 mm QFN	TLC5941RHB
–40°C to 85°C	28-pin PDIP	TLC5941NT

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS.

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_I	Input voltage range(2)	VCC	–0.3 V to 6 V
I_O	Output current (dc)		90 mA
V_I	Input voltage range	$V_{(BLANK)}$, $V_{(SCLK)}$, $V_{(XLAT)}$, $V_{(MODE)}$	–0.3 V to V_{CC} +0.3 V
V_O	Output voltage range	$V_{(SOUT)}$, $V_{(XERR)}$	–0.3 V to V_{CC} +0.3 V
		$V_{(OUT0)}$ to $V_{(OUT15)}$	–0.3 V to 18 V
	ESD rating	HBM (JEDEC JESD22-A114, Human Body Model)	2 kV
		CDM (JEDEC JESD22-C101, Charged Device Model)	500 V
T_{stg}	Storage temperature range		–55°C to 150°C
T_A	Operating ambient temperature range		–40°C to 85°C
	Package thermal impedance(3)	HTSSOP (PWP)(4)	31.58°C/W
		QFN (RHB)(4)	35.9°C/W
		PDIP (NT)	48°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) With PowerPAD soldered on PCB with 2-oz. trace of copper. See TI application report SLMA002 for further information.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DC Characteristics						
V_{CC}	Supply Voltage		3		5.5	V
V_O	Voltage applied to output (OUT0 - OUT15)				17	V
V_{IH}	High-level input voltage		0.8 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.2 V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 5 V at SOUT			–1	mA
I_{OL}	Low-level output current	V_{CC} = 5 V at SOUT, XERR			1	mA
I_{OLC}	Constant output current	OUT0 to OUT15			80	mA
T_A	Operating free-air temperature range		–40		85	°C
AC Characteristics V_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)						
$f_{(SCLK)}$	Data shift clock frequency	SCLK			30	MHz
$f_{(GSCLK)}$	Grayscale clock frequency	GSCLK			30	MHz
t_{wh0}/t_{wl0}	SCLK pulse duration	SCLK = H/L (1)	16			ns
t_{wh1}/t_{wl1}	GSCLK pulse duration	GSCLK = H/L (2)	16			ns
t_{wh2}	XLAT pulse duration	XLAT = H (3)	20			ns
t_{wh3}	BLANK pulse duration	BLANK = H (2)	20			ns
t_{su0}	Setup time	SIN - SCLK (3)	10			ns
t_{su1}		SCLK - XLAT (3)	10			ns
t_{su2}		MODE - SCLK (4)	10			ns
t_{su3}		MODE - XLAT (4)	10			ns
t_{su4}		BLANK - GSCLK (2)	10			ns
t_{h0}	Hold Time	SCLK - SIN (3)	10			ns
t_{h1}		XLAT - SCLK (3)	10			ns
t_{h2}		SCLK - MODE (4)	10			ns
t_{h3}		XLAT - MODE (4)	10			ns
t_{h4}		BLANK - GSCLK (2)	10			ns

(1) See Figure 8
(2) See Figure 12
(3) See Figure 10
(4) See Figure 6

DISSIPATION RATINGS

PACKAGE	POWER RATING T_A < 25°C	DERATING FACTOR ABOVE T_A = 25°C	POWER RATING T_A = 70°C	POWER RATING T_A = 85°C
28-pin HTSSOP with PowerPAD™ soldered (1)	3958 mW	31.67 mW/°C	2533 mW	2058 mW
28-pin HTSSOP without PowerPAD™ soldered	2026 mW	16.21 mW/°C	1296 mW	1053 mW
32-pin QFN (1)	3482 mW	27.86 mW/°C	2228 mW	1811 mW
28-pin PDIP	2456 mW	19.65 mW/°C	1572 mW	1277 mW

(1) The PowerPAD is soldered to the PCB with a 2-oz. copper trace. See application report SLMA002 for further information.

ELECTRICAL CHARACTERISTICS

V_{CC} = 3 V to 5.5 V, T_A = -40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA, SOUT	V_{CC} –0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, SOUT			0.5	V
I_I	Input current	$V_I = V_{CC}$ or GND; BLANK, TEST, GSCLK, SCLK, SIN, XLAT pin	–1		1	µA
		$V_I = V_{CC}$; MODE pin			50	
		V_I = GND; MODE pin	–1		1	
I_{CC}	Supply current	No data transfer, all output OFF, V_O = 1 V, $R_{(IREF)}$ = 10 kΩ		0.9	6	mA
		No data transfer, all output OFF, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ		5.2	12	
		Data transfer 30 MHz, all output ON, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ		16	25	
		Data transfer 30 MHz, all output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω		30	60	
$I_{O(LC)}$	Constant output current	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω	54	61	69	mA
I_{lkg}	Leakage output current	All output OFF, V_O = 15 V, $R_{(IREF)}$ = 640 Ω , OUT0 to OUT15			0.1	µA
$\Delta I_{O(LC0)}$	Constant current error	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15, –20°C to 85°C		±1	±4	%
		All output ON, V_O = 1 V, $R_{(IREF)}$ = 480 Ω, OUT0 to OUT15, –20°C to 85°C		±1	±6	%
		All output ON, V_O = 1 V, $R_{(IREF)}$ = 480 Ω		±1	±8	%
$\Delta I_{O(LC1)}$		Device to device, averaged current from OUT0 to OUT15,$R_{(IREF)}$ = 1920 Ω (20 mA)		+0.4, -2	±4	%
$\Delta I_{O(LC2)}$		Device to device, averaged current from OUT0 to OUT15,$R_{(IREF)}$ = 480 Ω (80 mA)		+2, -2.7	±4	%
$\Delta I_{O(LC3)}$	Power supply rejection ratio, PSRR	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω OUT0 to OUT15		±1	±4	%/V
		All output ON, V_O = 1 V, $R_{(IREF)}$ = 480 Ω OUT0 to OUT15		±1	±6	
$\Delta I_{O(LC4)}$	Load regulation	All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15		±2	±6	%/V
		All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 480 Ω, OUT0 to OUT15		±2	±8	
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature(1)	150		170	°C
$V_{(LED)}$	LED open detection threshold			0.3	0.4	V
$V_{(IREF)}$	Reference voltage output	$R_{I(REF)}$ = 640 Ω	1.20	1.24	1.28	V

(1) Not tested. Specified by design

SWITCHING CHARACTERISTICS

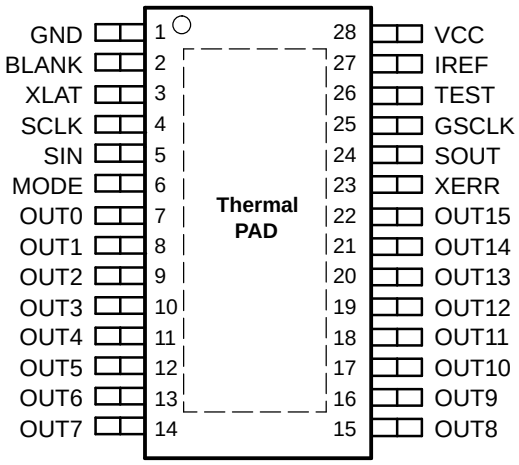
V_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{r0}	Rise time	SOUT			16	ns
t_{r1}		OUTn, V_{CC} = 5 V, T_A = 60°C, DCx = 3F		10	30	
t_{f0}	Fall time	SOUT			16	ns
t_{f1}		OUTn, V_{CC} = 5 V, T_A = 60°C, DCx = 3F		10	30	
t_{pd0}	Propagation delay time	SCLK - SOUT (1)			30	ns
t_{pd1}		BLANK - OUT0 (2)			60	ns
t_{pd2}		OUTn - XERR (2)			1000	ns
t_{pd3}		GSCLK - OUT0 (2)			60	ns
t_{pd4}		XLAT - I_{OUT} (dot correction)			1000	ns
t_d	Output delay time	OUTn - OUT(n+1) (2)		20	30	ns

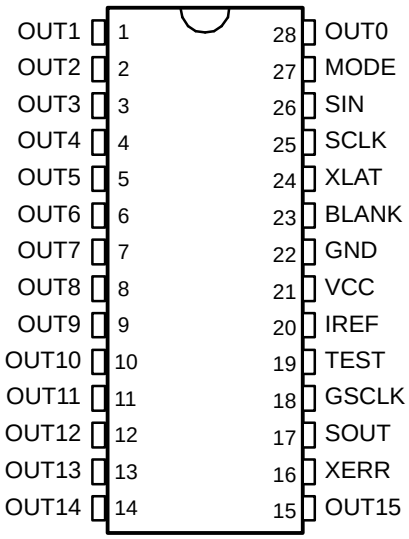
(1) See Figure 10
(2) See Figure 12

DEVICE INFORMATION

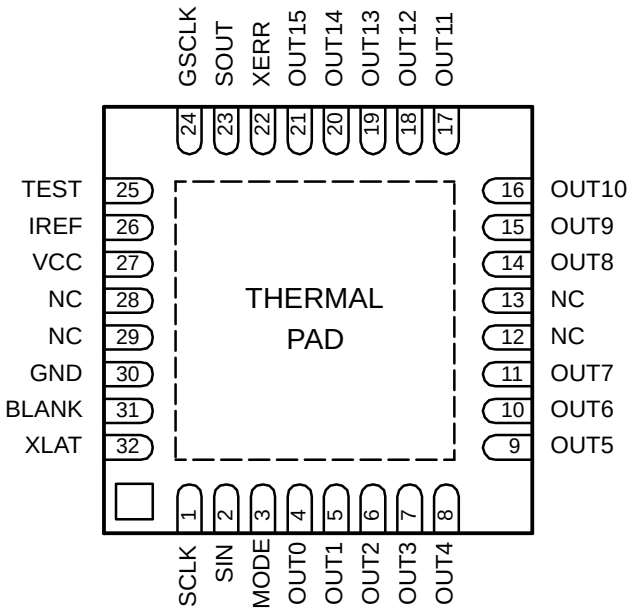
PWP PACKAGE
(TOP VIEW)



NT PACKAGE
(TOP VIEW)



RHB PACKAGE
(TOP VIEW)



NC − No internal connection

DEVICE INFORMATION (continued)

TERMINAL FUNCTION

TERMINAL				I/O	DESCRIPTION
	NT	PWP	RHB		
NAME	NO.	NO.	NO.		
BLANK	23	2	31	I	Blank all outputs. When BLANK = H, all OUTn outputs are forced OFF. GS counter is also reset. When BLANK = L, OUTn are controlled by grayscale PWM control.
GND	22	1	30	G	Ground
GSCLK	18	25	24	I	Reference clock for grayscale PWM control
IREF	20	27	26	I	Reference current terminal
NC	-	-	12, 13, 28, 29		No connection
OUT0	28	7	4	O	Constant-current output
OUT1	1	8	5	O	Constant-current output
OUT2	2	9	6	O	Constant-current output
OUT3	3	10	7	O	Constant-current output
OUT4	4	11	8	O	Constant-current output
OUT5	5	12	9	O	Constant-current output
OUT6	6	13	10	O	Constant-current output
OUT7	7	14	11	O	Constant-current output
OUT8	8	15	14	O	Constant-current output
OUT9	9	16	15	O	Constant-current output
OUT10	10	17	16	O	Constant-current output
OUT11	11	18	17	O	Constant-current output
OUT12	12	19	18	O	Constant-current output
OUT13	13	20	19	O	Constant-current output
OUT14	14	21	20	O	Constant-current output
OUT15	15	22	21	O	Constant-current output
SCLK	25	4	1	I	Serial data shift clock
SIN	26	5	2	I	Serial data input
SOUT	17	24	23	O	Serial data output
TEST	19	26	25	I	Test pin: Connect to VCC
VCC	21	28	27	I	Power supply voltage. It is important to connect both pins to supply voltage to ensure proper operation of the device.
MODE	27	6	3	I	Input mode-change pin. When MODE = GND, the device is in GS mode. When MODE = V_{CC}, the device is in DC mode.
XERR	16	23	22	O	Error output. XERR is an open-drain terminal. XERR goes L when LOD or TEF is detected.
XLAT	24	3	32	I	Data latch. Note that the internal connections are switched by MODE. At XLAT↑ (MODE = GND), GS register gets new data. At XLAT↑ (MODE = V_{CC}), DC register gets new data.

PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

Resistor values are equivalent resistance and not tested.

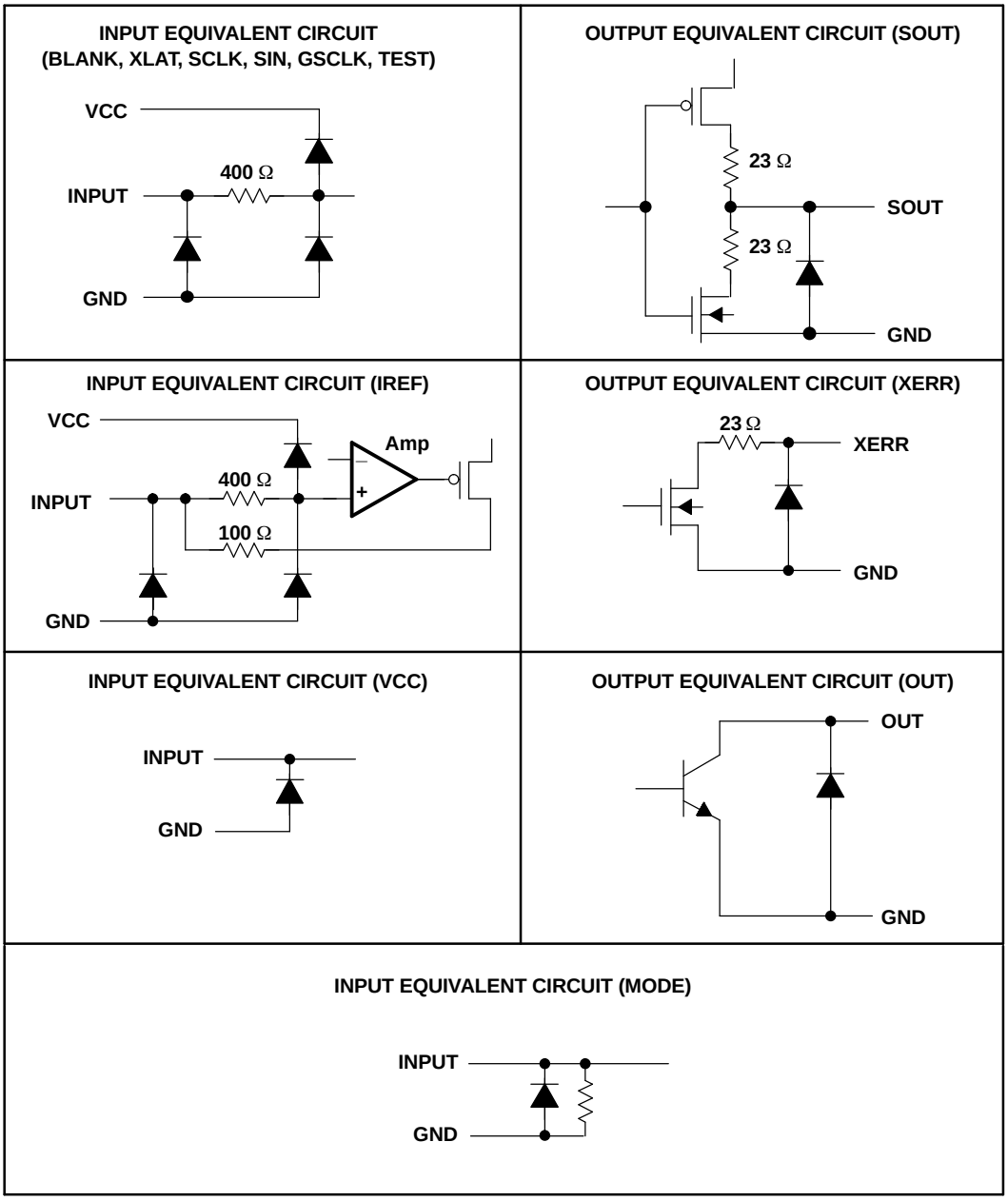


Figure 1. Input and Output Equivalent Circuits

PARAMETER MEASUREMENT INFORMATION (continued)

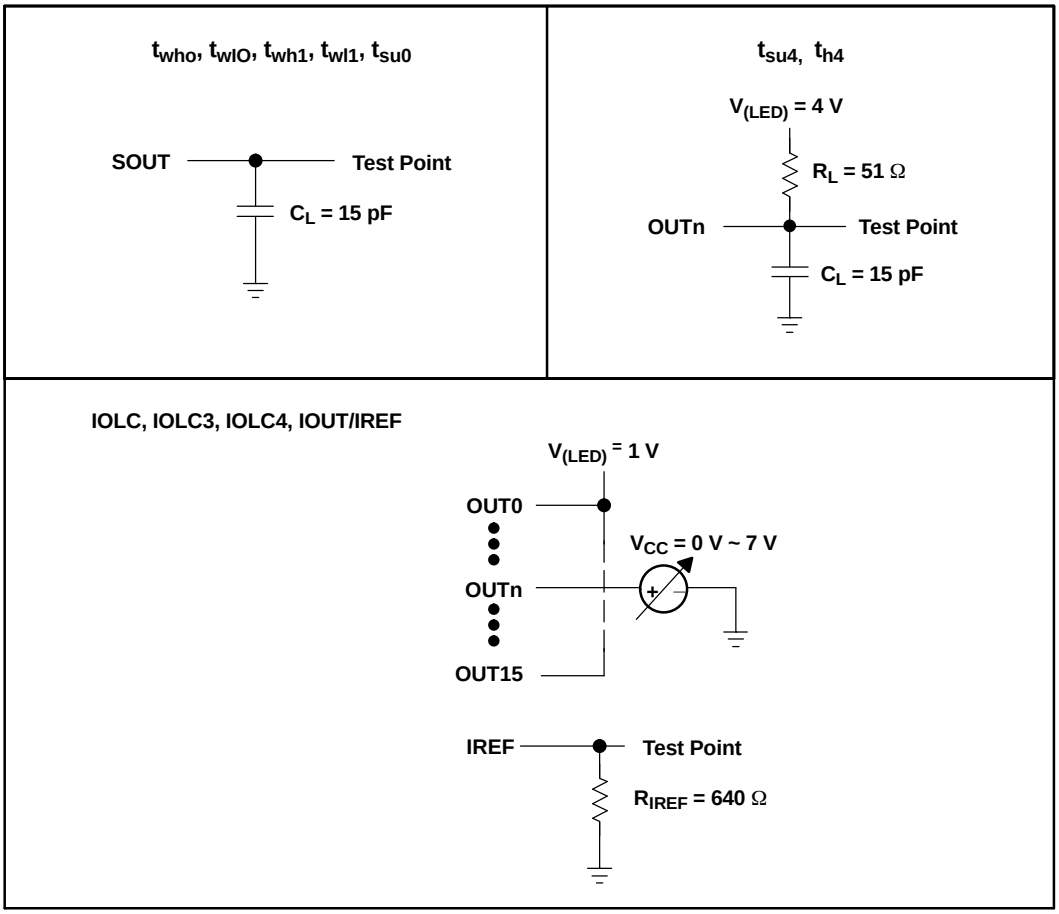


Figure 2. Parameter Measurement Circuits

Typical Characteristics

REFERENCE RESISTOR
vs
OUTPUT CURRENT

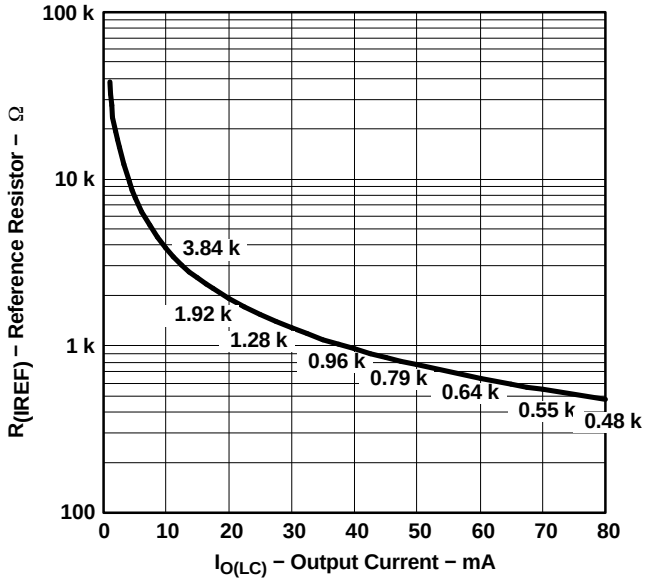


Figure 3.

POWER DISSIPATION RATE
vs
FREE-AIR TEMPERATURE

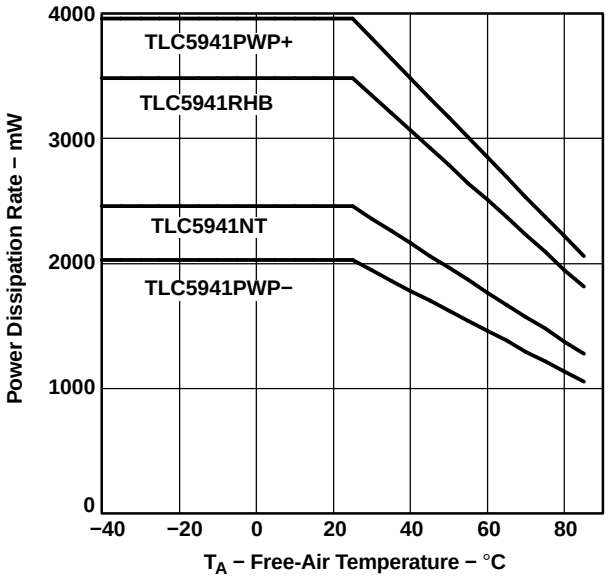


Figure 4.

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

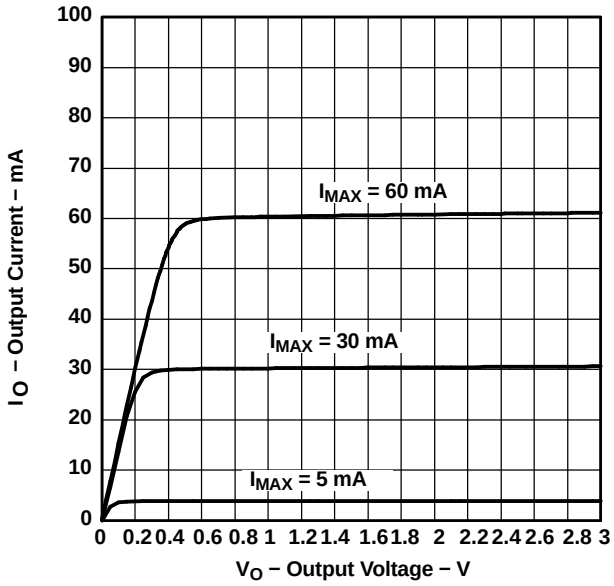


Figure 5.

PRINCIPLES OF OPERATION

SERIAL INTERFACE

The TLC5941 includes a flexible serial interface, which can be connected to microcontrollers or digital signal processors in various ways. Only 3 pins are needed to input data into the device. The rising edge of SCLK signal shifts the data from the SIN pin to the internal register. After all data is clocked in, a rising edge of XLAT latches the serial data to the internal registers. All data are clocked in with the MSB first. Multiple TLC5941 devices can be cascaded by connecting the SOUT pin of one device with the SIN pin of the following device. The SOUT pin can also be connected to the controller to receive status information from the TLC5941. The serial data format is 96-bit or 192-bit wide, depending on programming mode of the device.

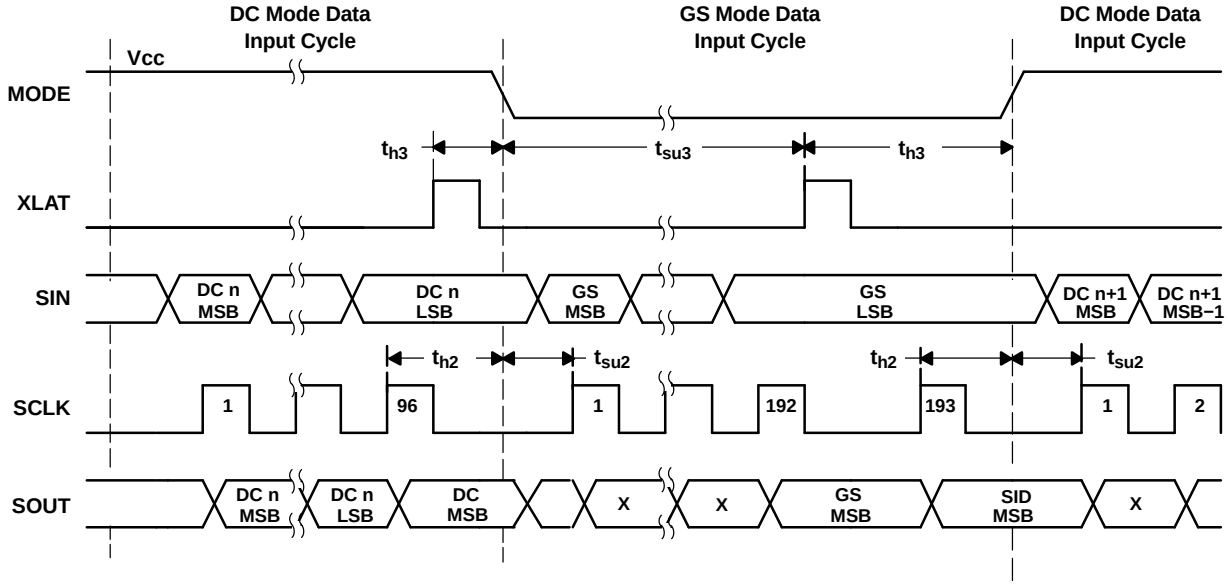


Figure 6. Serial Data Input Timing Chart

ERROR INFORMATION OUTPUT

The open-drain output XERR is used to report both of the TLC5941 error flags, TEF and LOD. During normal operating conditions, the internal transistor connected to the XERR pin is turned off. The voltage on XERR is pulled up to V_{CC} through an external pullup resistor. If TEF or LOD is detected, the internal transistor is turned on, and XERR is pulled to GND. Because XERR is an open-drain output, multiple ICs can be ORed together and pulled up to V_{CC} with a single pullup resistor. This reduces the number of signals needed to report a system error (see Figure 13).

To differentiate LOD and TEF signal from XERR pin, LOD can be masked out with BLANK = HIGH.

Table 1. XERR Truth Table

ERROR CONDITION		ERROR INFORMATION		SIGNALS	
TEMPERATURE	OUTn VOLTAGE	TEF	LOD	BLANK	XERR
$T_J < T_{(TEF)}$	Don't Care	L	X	H	H
$T_J > T_{(TEF)}$	Don't Care	H	X		L
$T_J < T_{(TEF)}$	OUTn > $V_{(LED)}$	L	L	L	H
	OUTn < $V_{(LED)}$	L	H		L
$T_J > T_{(TEF)}$	OUTn > $V_{(LED)}$	H	L		L
	OUTn < $V_{(LED)}$	H	H		L

TEF: THERMAL ERROR FLAG

The TLC5941 provides a temperature error flag (TEF) circuit to indicate an overtemperature condition of the IC. If the junction temperature exceeds the threshold temperature (160°C typical), the TEF circuit trips and pulls XERR to ground. TEF status can also be read out from the TLC5941 status register.

LOD: LED OPEN DETECTION

The TLC5941 provides an LED open-detection circuit (LOD). This circuit reports an error if any one of the 16 LEDs is open or disconnected from the circuit. The LOD circuit trips when the following two conditions are met simultaneously:

1. BLANK is set to LOW
2. When the voltage at OUTn is less than $V_{(LED)}$ of 0.3 V (typical). (Note: the voltage at each OUTn is sampled 1 μs after being turned on.)

The LOD circuit also pulls XERR to GND when tripped. The LOD status of each channel can also be read out from the TLC5941 status information data (SID) in GS data input cycle.

DELAY BETWEEN OUTPUTS

The TLC5941 has graduated delay circuits between outputs. These circuits can be found in the constant-current driver block of the device (see functional block diagram). The fixed-delay time is 20 ns (typical), OUT0 has no delay, OUT1 has 20 ns delay, and OUT2 has 40 ns delay, etc. The maximum delay is 300 ns from OUT0 to OUT15. The delay works by switch on and switch off of each output channel. This means that the on/off time of each channel is the same regardless of delay. These delays prevent large inrush currents and switching noise which reduces the bypass capacitors when the outputs turn on.

OUTPUT ENABLE

All OUTn channels of TLC5941 can be switched off with one signal. When BLANK is set to high, all OUTn channels are disabled, regardless of logic operations of the device. The grayscale counter is also reset. When BLANK is set to low, all OUTn channels work under normal conditions.

Table 2. BLANK Signal Truth Table

BLANK	OUT0 - OUT15
LOW	Normal condition
HIGH	Disabled

SETTING MAXIMUM CHANNEL CURRENT

The maximum output current per channel is programmed by a single resistor, $R_{(IREF)}$, which is placed between IREF pin and GND pin. The voltage on IREF is set by an internal band gap $V_{(IREF)}$ with a typical value of 1.24 V. The maximum channel current is equivalent to the current flowing through $R_{(IREF)}$ multiplied by a factor of 31.5. The maximum output current can be calculated by Equation 1:

$$I_{max} = \frac{V_{(IREF)}}{R_{(IREF)}} \times 31.5 \quad (1)$$

where:

$V_{(IREF)}$ = 1.24 V

$R_{(IREF)}$ = User-selected external resistor.

Figure 3 shows the maximum output current I_O versus $R_{(IREF)}$. $R_{(IREF)}$ is the value of the resistor between IREF terminal to GND, and I_O is the constant output current of OUT0 to OUT15.

POWER DISSIPATION CALCULATION

The device power dissipation needs to be below the power dissipation rate of the device package to ensure correct operation. Equation 2 calculates the power dissipation of device:

$$P_D = \left(V_{CC} \times I_{CC}\right) + \left(V_{OUT} \times I_{MAX} \times N \times \frac{DC_n}{63} \times d_{PWM}\right) \quad (2)$$

where:

V_{CC}: device supply voltage

I_{CC}: device supply current

V_{OUT}: TLC5941 OUTn voltage when driving LED current

I_{MAX}: LED current adjusted by $R_{(IREF)}$ Resistor

DC_n: maximum dot correction value for OUTn

N: number of OUTn driving LED at the same time

d_{PWM}: duty cycle defined by BLANK pin or GS PWM value

OPERATING MODES

Table 3 shows the available operating modes. The TLC5941 GS operating mode (see Figure 10) and shift register values are not defined after power up. One solution to solve this is to set dot correction data after TLC5941 power up and switch back to GS PWM mode. The other solution is to overflow the input shift register with 193 bits of dummy data and latch it while TLC5941 is in GS PWM mode.

Table 3. MODE Signal Truth Table

MODE	INPUT SHIFT REGISTER	OPERATING MODE
LOW	192 bit	Grayscale PWM Mode
HIGH	96 bit	Dot Correction Data Input Mode

SETTING DOT CORRECTION

The TLC5941 has the capability to fine-adjust the output current of each channel (OUT0 to OUT15) independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LEDs connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0% to 100% of the maximum output current I_{max}. Equation 3 determines the output current for each output n:

$$I_{OUTn} = I_{max} \times \frac{DCn}{63} \quad (3)$$

where:

I_{max} = the maximum programmable output current for each output.

DCn = the programmed dot correction value for output n (DCn = 0 to 63).

n = 0 to 15

Dot correction data are entered for all channels at the same time. The complete dot correction data format consists of 16 x 6-bit words, which forms a 96-bit wide serial data packet. The channel data is put one after another. All data is clocked in with MSB first. Figure 7 shows the DC data format.

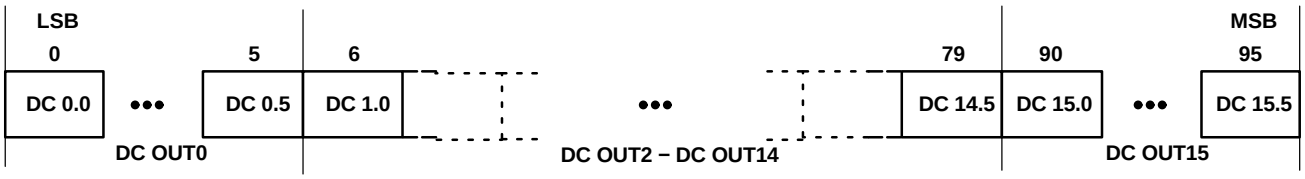


Figure 7. Dot Correction Data Packet Format

To input data into the dot correction register, MODE must be set to V_{CC}. The internal input shift register is then set to 96-bit width. After all serial data are clocked in, a rising edge of XLAT is used to latch the data into the dot correction register. Figure 8 shows the dc data input timing chart.

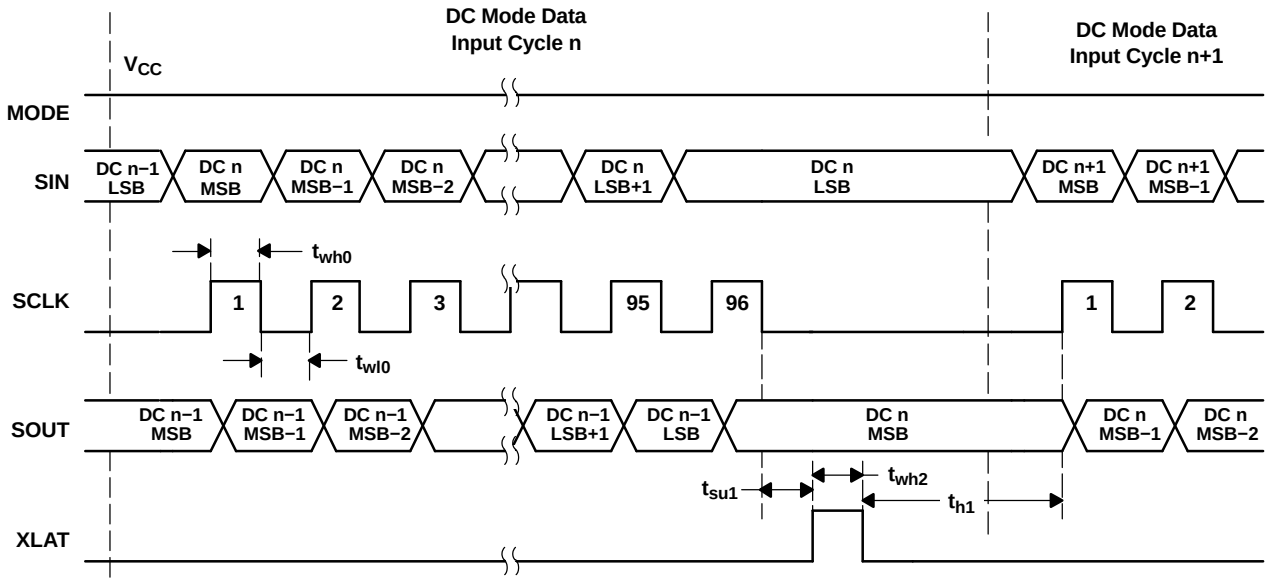


Figure 8. Dot Correction Data Input Timing Chart

SETTING GRAYSCALE

The TLC5941 can adjust the brightness of each channel OUTn using a PWM control scheme. The use of 12 bits per channel results in 4096 different brightness steps, from 0% to 100% brightness. Equation 4 determines the brightness level for each output n:

$$\text{Brightness in \%} = \frac{GSn}{4095} \times 100 \tag{4}$$

where:

GSn = the programmed grayscale value for output n (GSn = 0 to 4095)

n = 0 to 15

Grayscale data for all OUTn

The input shift register enters grayscale data into the grayscale register for all channels simultaneously. The complete grayscale data format consists of 16 x 12 bit words, which forms a 192-bit wide data packet (see Figure 9). The data packet must be clocked in with the MSB first.

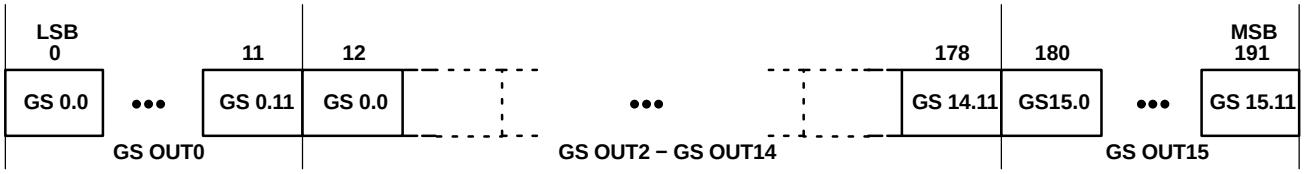


Figure 9. Grayscale Data Packet Format

When MODE is set to GND, the TLC5941 enters the grayscale data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, a rising edge of the XLAT signal latches the data into the grayscale register (see Figure 10). The first GS data input cycle after dot correction requires an additional SCLK pulse after the XLAT signal to complete the grayscale update cycle. All GS data in the input shift register is replaced with status information data (SID) after latching into the grayscale register.

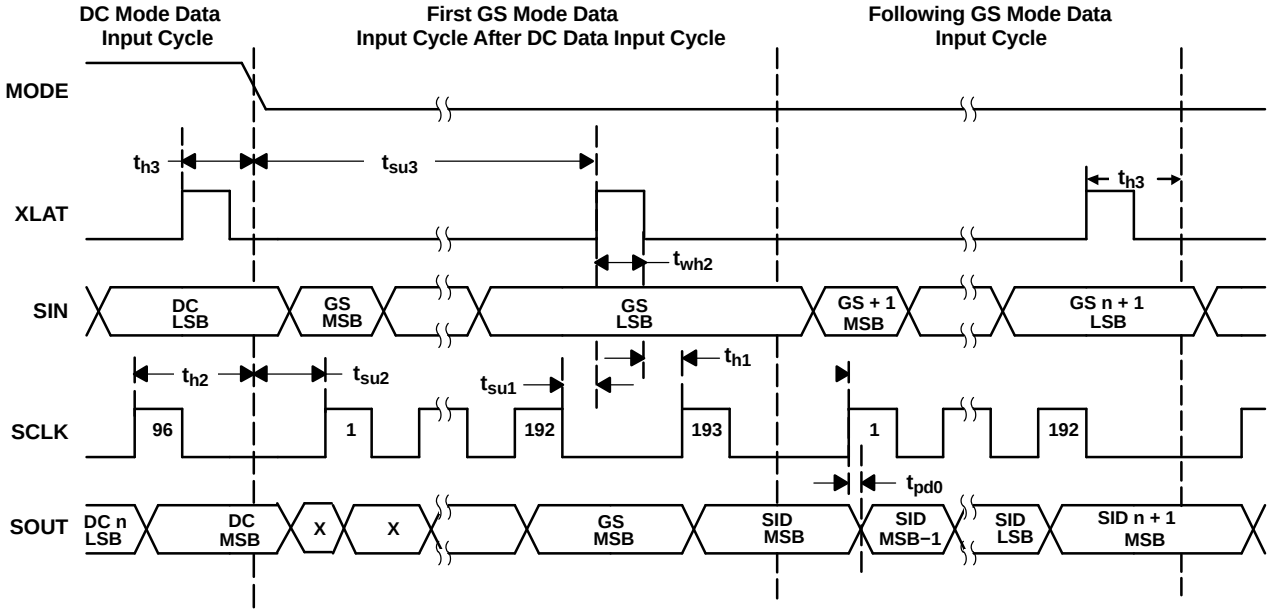


Figure 10. Grayscale Data Input Timing Chart

STATUS INFORMATION OUTPUT

The TLC5941 does have a status information register, which can be accessed in grayscale mode (MODE = GND). After the XLAT signal latches the data into the GS register, the input shift register data is replaced with status information data (SID) of the device (see Figure 10). LOD, TEF, and dot-correction register data can be read out at the SOUT pin. The status information data packet is 192 bits wide. Bits 176 – 191 contain the LOD status of each channel. Bit 175 contains the TEF status. Bits 72 – 167 contain the data of the dot-correction register. The remaining bits are reserved. The complete status information data packet is shown in Figure 11.

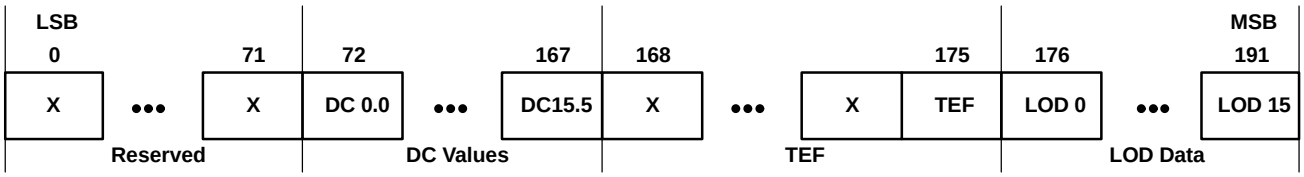


Figure 11. Status Information Data Packet Format

GRAYSCALE PWM OPERATION

The grayscale PWM cycle starts with the falling edge of BLANK. The first GSCLK pulse after BLANK increases the grayscale counter by one and switches on all OUTn with grayscale value not zero. Each following rising edge of GSCLK increases the grayscale counter by one. The TLC5941 compares the grayscale value of each output OUTn with the grayscale counter value. All OUTn with grayscale values equal to counter values are switched off. A BLANK=H signal after 4096 GSCLK pulses resets the grayscale counter to zero and completes the grayscale PWM cycle (see Figure 12).

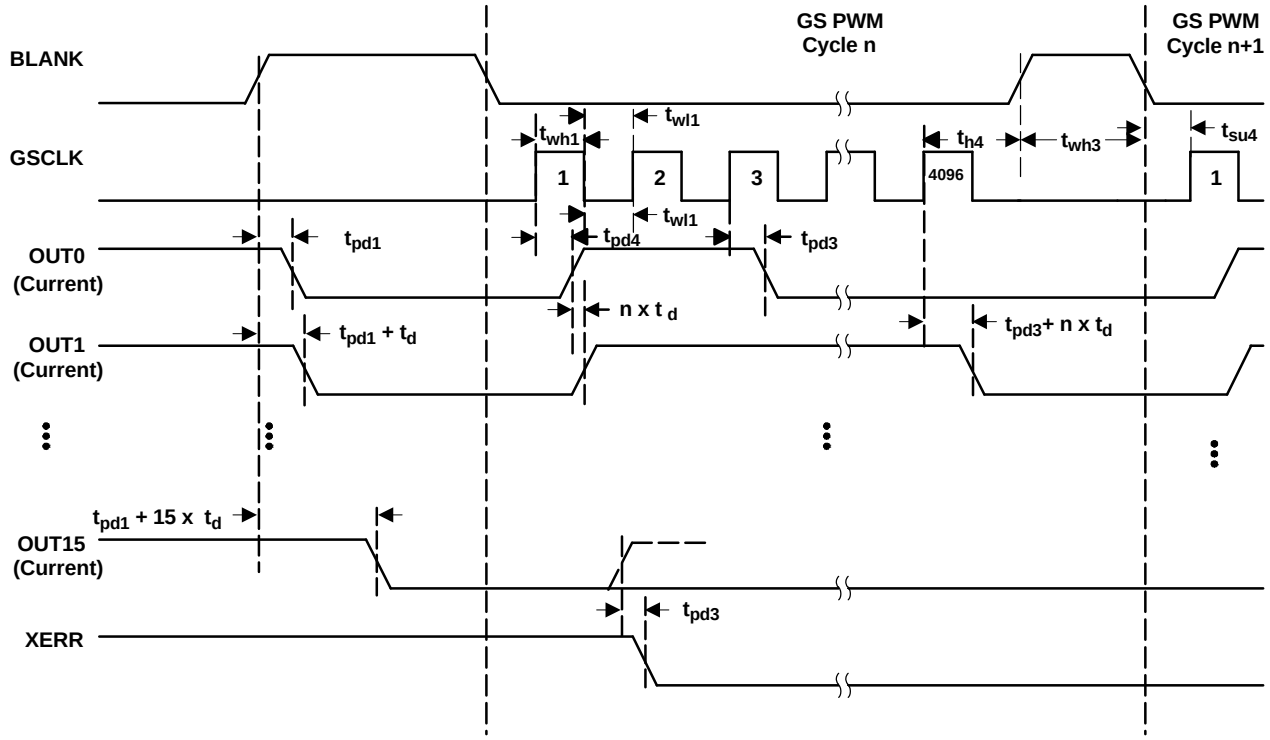


Figure 12. Grayscale PWM Cycle Timing Chart

SERIAL DATA TRANSFER RATE

Figure 13 shows a cascading connection of *n* TLC5941 devices connected to a controller, building a basic module of an LED display system. The maximum number of cascading TLC5941 devices depends on the application system and is in the range of 40 devices. Equation 5 calculates the minimum frequency needed:

$$f_{(GSCLK)} = 4096 \times f_{(update)}$$

$$f_{(SCLK)} = 193 \times f_{(update)} \times n \quad (5)$$

where:

$f_{(GSCLK)}$: minimum frequency needed for GSCLK

$f_{(SCLK)}$: minimum frequency needed for SCLK and SIN

$f_{(update)}$: update rate of whole cascading system

n: number cascaded of TLC5941 device

Application Example

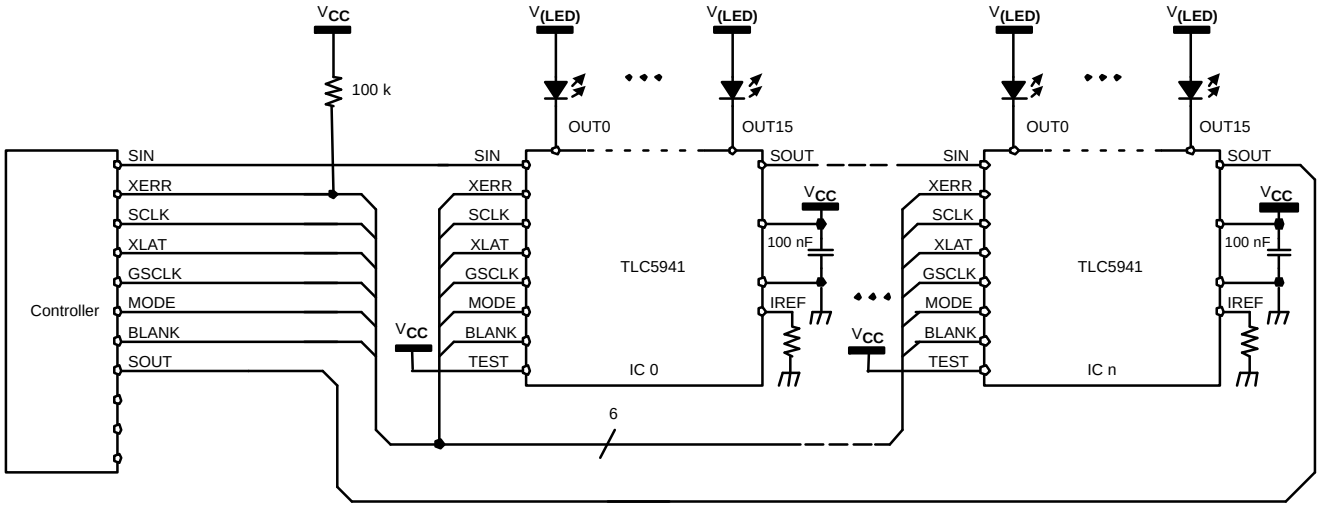


Figure 13. Cascading Devices

THERMAL PAD MECHANICAL DATA

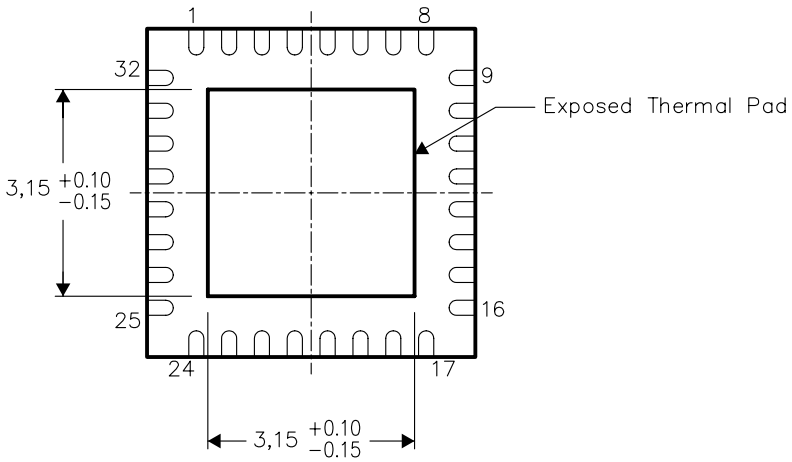
RHB (S–PQFP–N32)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

THERMAL PAD MECHANICAL DATA

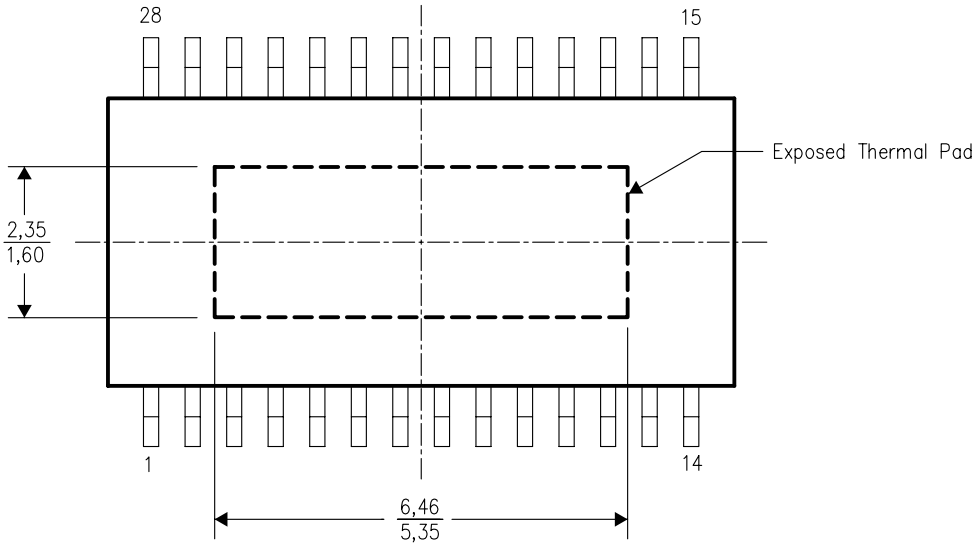
PWP (R–PDSO–G28)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC5941PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5941PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5941PWPRG4	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5941RHB	PREVIEW	QFN	RHB	32		TBD	Call TI	Call TI
TLC5941RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5941RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

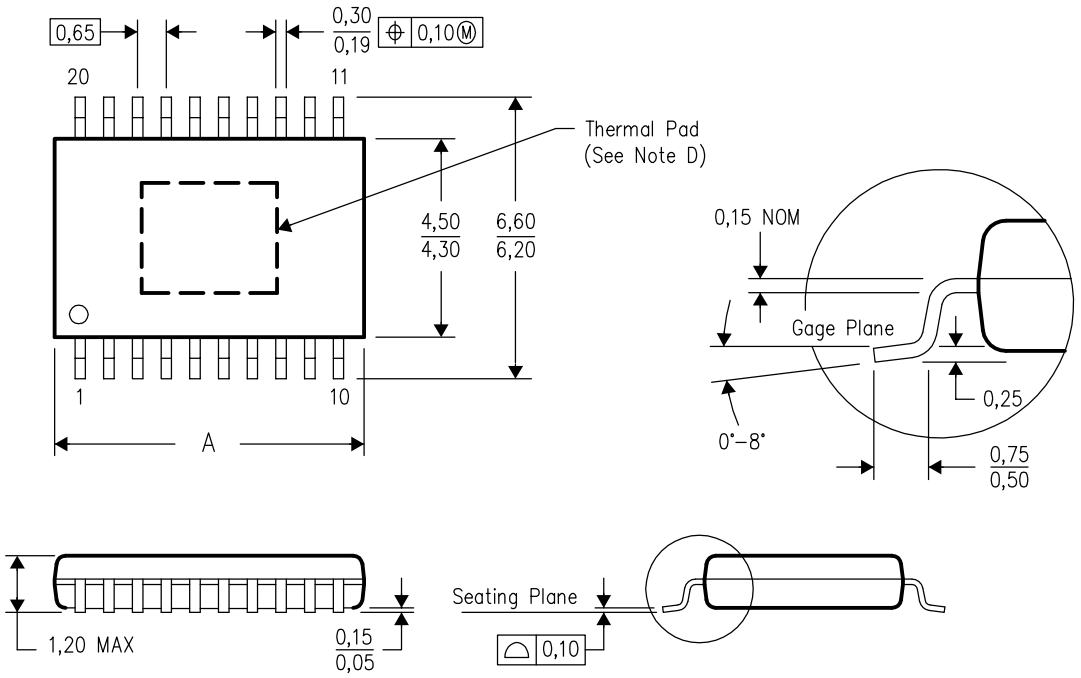
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



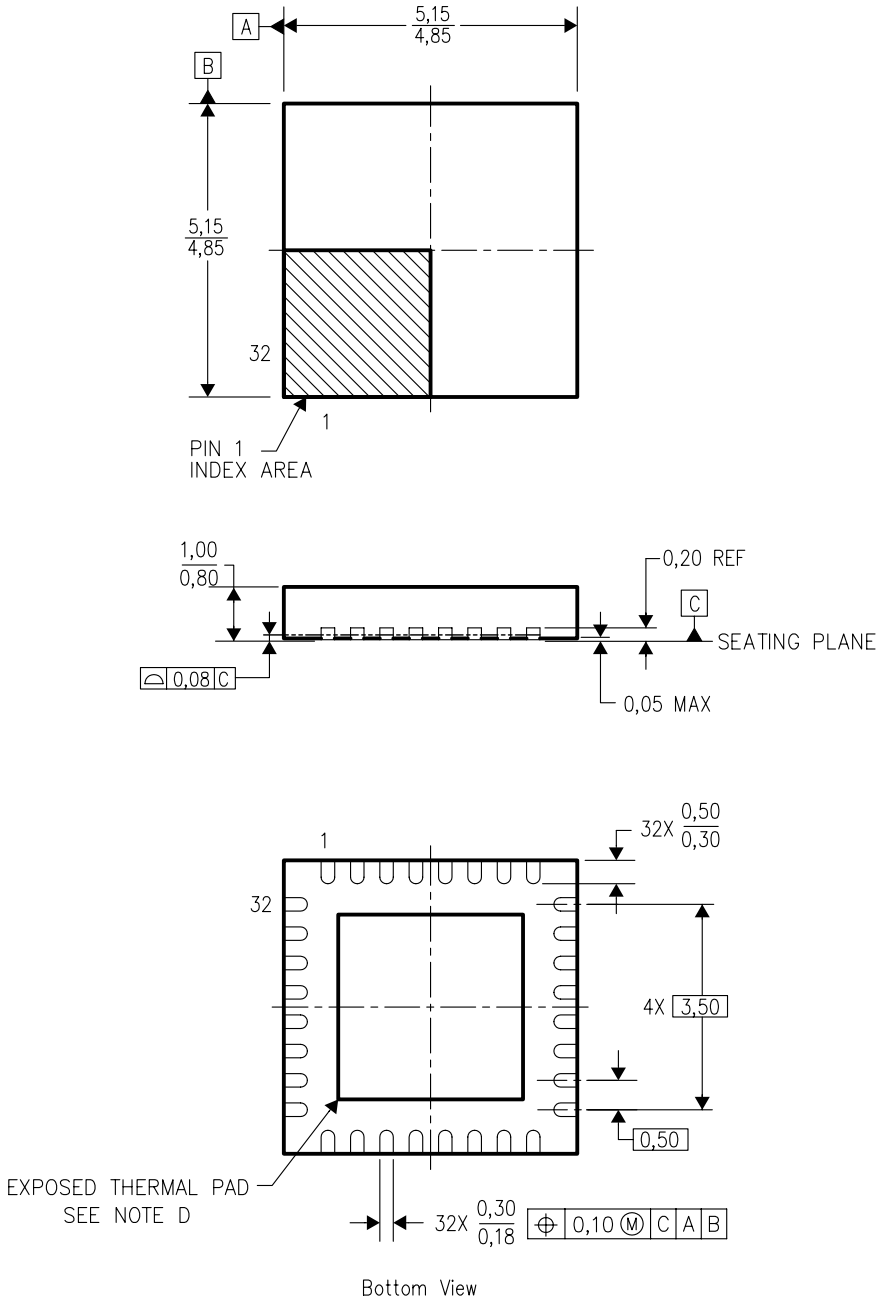
DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



4204326/C xx/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265