MICROCHIP

To: *Valued Distributor Customer*

Subject: ENC28J60 Product Update

Device Information
This letter is to inform you of the latest updates and silicon errata regarding the ENC28J60 Ethernet controller. Revision B1 is currently undergoing engineering evaluation including characterization and qualification testing internal to Microchip. This revision is expected to release to production very soon.

One important point to note is that the original expectation was that an industrial temperature range could be achieved. However, after extensive testing, it became evident that a more conservative temperature rating of 0 to 70C was required to meet the required yield levels. (See Errata item number 3.) All existing orders for industrial temperature devices will automatically be changed to the commercial temperature equivalent.

A list of all other known errata is documented below.

ENC28J60 B1 Errata List

1. **Module: MAC Host Interface**
    Writing/Reading MAC registers may be unreliable when SPI clock is run at frequencies less than 8 MHz.
    Work around
    Run SPI at frequencies ≥ 8 MHz, or use the same clock source for both ENC28J60 and the host controller for synchronization

2. **Module: Reset**
    After sending an SPI reset command, the PHY clock stops but the ESTAT<CLKRDY> bit is not cleared. Therefore polling the CLKRDY bit will not work to detect if the part has come out of reset.
    Work around
    After issuing the reset command, wait at least 1ms in firmware for the part to come out of reset.

3. **Operating Temperature**
    The data sheet specifies that industrial operating temperature range (-40 to +85 °C) is supported, however, B1 and any previous revisions only support commercial temperature range (0 to 70 °C).

4. IEEE 802.3 Conformance Issues

4.1 Differential Output Voltage
The measured peak differential voltage across TD (Transmit Differential) circuit does not fall between specified 2.2 to 2.8V and (-2.2V) to (-2.8V) range. Devices will be tested at a range of 2.0 to 2.9V and (-2.0V) to (-2.9V).
Reference: IEEE 802.3, Clause 14.3.1.2.1

4.2 TP_IDL
The observed TP_IDL pattern transmitted by ENC28J60 was observed to not stay within the standard defined template when using the TPM (Twisted Pair Model) and TP Test Load 2.
Reference: IEEE 802.3, Clause 14.3.1.2.1, Figure 14-10 and 14-11

4.3 Exiting Link Test Fail State
The ENC28J60 was observed to improperly accept a frame with no preceding LTPs (Link Test Pulse). When a device is in the Link Test Fail state, it should exit this state when a valid packet is received, however, the first packet should not be accepted. The second and subsequent packets should be accepted while the device is in the Link Test Pass state.
Reference: IEEE 802.3, Figure 14-6

4.4 Acceptance of Frames with Alignment Errors
The ENC28J60 does not accept a frame with a valid FCS (Frame Check Sequence) and extra bits (alignment errors).
Reference: IEEE 802.3, Clause 4.2.4.2.1

4.5 Collisions
The delay from the collision event to collision enforcement with the jam pattern is approximately 50 BT (bit times), which is greater than the specified limit of 36 BT.
Reference: IEEE 802.3, Annex B, Section B.1.2

If, while transmitting the preamble or SFD, a collision occurs, any remaining preamble and SFD bits should be sent. The ENC28J60, however, does not send out the remaining bits.
Reference: IEEE 802.3, Clause 4.2.5

Data Sheet Clarifications:
1. ENC28J60 supports automatic polarity correction, however, if this feature is used, the device under test will not pass some IEEE 802.3 conformance tests.
2. Currently, the specified wait time after a soft reset is 50us. The new recommended wait time is 1ms for any resets.
3. Typical current consumption is rated at 150mA, with maximum of 250mA.
4. Chip Select must go high between each command.

Microchip Contacts:
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