2N5441-2N5446, T6420 Series

File Number **593**

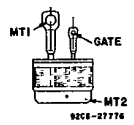
40-A Silicon Triacs

Features:
- *di/dt capability = 100 A/μs*
- *Low switching losses*
- *Low on-state voltage at high current levels*
- *Low thermal resistance*

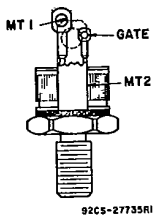
Package \ Voltage	200 V Types	400 V Types	600 V Types
Press-Fit	2N5441	2N5442	2N5443
Stud	2N5444	2N5445	2N5446
Isolated-Stud	T6420B	T6420D	T6420M

RCA triacs are gate-controlled, full-wave silicon ac switches. They are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate-triggering voltages.

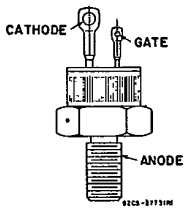
TERMINAL DESIGNATIONS



2N5441-43



T6420 Series



2N5444-46

MAXIMUM RATINGS, *Absolute-Maximum Values:*
For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with resistive or inductive Load

	2N5441 2N5444 T6420B	2N5442 2N5445 T6420D	2N5443 2N5446 T6420M	
* REPETITIVE PEAK OFF-STATE VOLTAGE •, V_{DROM}				
Gate Open, T_J = -65 to 100°C	200	400	600	V
RMS ON-STATE CURRENT (Conduction angle = 360°C), $I_{T(RMS)}$				
Case temperature				
* T_C = 70°C (Press-fit types)		40		A
* T_C = 65°C (Stud types)		40		A
T_C = 60°C (Isolated-stud types)		40		A
For other conditions		See Fig. 3		
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT, I_{TSM}				
For one cycle of applied principal voltage				
* 60 Hz (sinusoidal)		300		A
50 Hz (sinusoidal)		265		A
For more than one cycle of applied principal voltage		See Fig. 4		
RATE OF CHANGE OF ON-STATE CURRENT, dI/dt				
$V_{DM} = V_{DROM}$, I_{GT} = 200 mA, t_r = 0.1 μs (See Fig. 12)		100		A/μs
FUSING CURRENT (for Triac Protection), I^2t				
T_J = -65 to 110°C, t = 1.25 to 10 ms		450		A^2s
* PEAK GATE-TRIGGER CURRENT ■, I_{GTM}				
For 1 μs max.		12		A
* GATE POWER DISSIPATION				
Peak (For 10 μs max., $I_{GTM} \leq 4$ A, P_{GM}		40		W
Average, $P_{G(AV)}$		0.75		W
* TEMPERATURE RANGE Δ				
Storage, T_{stg}		-65 to 150		°C
Operating (Case), T_C		-65 to 110		°C
* TERMINAL TEMPERATURE (During Soldering), T_T				
For 10 s max. (terminals and case)		225		°C
STUD TORQUE, TS				
Recommended		35		in-lb
Maximum (DO NOT EXCEED)		50		in-lb

* In accordance with JEDEC registration data format (JS-14, RDF2) filed for the JEDEC (2N-Series) types.
• For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
■ For either polarity of gate voltage (V_G) with reference to main terminal 1.
Δ For temperature measurement reference point, see Dimensional Outline

2N5441-2N5446, T6420 Series

ELECTRICAL CHARACTERISTICS
At Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature (T_C)

CHARACTERISTIC	SYMBOL	LIMITS FOR ALL TYPES UNLESS OTHERWISE SPECIFIED MIN.	TYP.	MAX.	UNITS
Peak Off-State Current:♦ Gate open, T_J = 110°C, V_{DROM} = Max. rated value	I_{DROM}	–	0.2	4*	mA
Maximum On-State Voltage:♦ For i_T = 100 A (peak), T_C = 25°C	V_{TM}	–	1.7	2	V
For i_T = 56 A (peak), T_C = 25°C		–	1.5	1.85*	
DC Holding Current:♦ Gate open, Initial principal current = 500 mA (dc), v_D = 12V: T_C = 25°C	I_{HO}	–	25	60	mA
T_C = –65°C		–	–	100*	
For other case temperatures		See Fig. 6			
Critical Rate of Rise of Commutation Voltage:♦ For v_D = V_{DROM}, $I_{T(RMS)}$ = 40 A, commutating di/dt = 22 A/ms, gate unenergized, (See Fig. 13): T_C = 70°C (Press-fit types)	dv/dt	5*	30	–	v/μs
= 65°C (Stud types)		5*	30	–	
= 60°C (Isolated-stud types)		5	30	–	
Critical Rate of Rise of Off-State Voltage:♦ For v_D = V_{DROM}, exponential voltage rise, gate open, T_C = 110°C: 2N5441, 2N5444, T6420B	dv/dt	50*	200	–	V/μs
2N5442, 2N5445, T6420D		30*	150	–	
2N5443, 2N5446, T6420M		20*	100	–	
DC Gate-Trigger Current:♦♦ For v_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C — Mode I^+ (V_{MT2} positive, V_G positive)	I_{GT}	–	15	50	mA
Mode III^- (negative, negative)		–	20	50	
Mode I^- (positive, negative)		–	30	80	
Mode III^+ (negative, positive)		–	40	80	
For v_D = 12 V (dc), R_L = 30 Ω, T_C = –65°C — Mode I^+ (positive, positive)		–	–	125*	
Mode III^- (negative, negative)		–	–	125*	
Mode I^- (positive, negative)		–	–	240*	
Mode III^+ (negative, positive)		–	–	240*	
For other case temperatures		See Figs. 7 & 8			
DC Gate-Trigger Voltage:♦♦ For v_D = 12 V (dc), R_L = 30 Ω, T_C = 25°C	V_{GT}	–	1.35	2.5	V
= –65°C		–	1.8	3.4*	
For other case temperatures		See Fig. 9			
For v_D = V_{DROM}, R_L = 125 Ω, T_C = 110°C		0.2	–	–	
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For v_D = V_{DROM}, I_{GT} = 200 mA, t_r = 0.1 μs, i_T = 60 A (peak), T_C = 25°C (See Figs. 10 & 14)	t_{gt}	–	1.7	3	μs
Thermal Resistance, Junction-to-Case: Steady-State Press-fit types	$R_{\theta JC}$	–	–	0.8*	°C/W
Stud types		–	–	0.9*	
Isolated-stud types		–	–	1	
Transient (Press-fit & stud types)		See Fig. 11			

* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N-Series) types.
♦ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
♦ For either polarity of gate voltage (V_G) with reference to main terminal 1.

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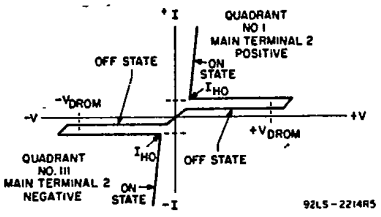

Fig. 1 - Principal voltage-current characteristic.

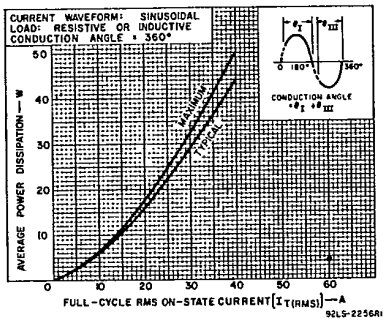

Fig. 2 - Power dissipation vs. on-state current.

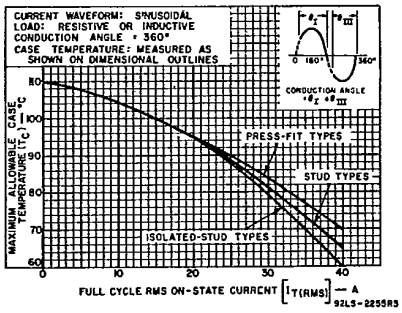

Fig. 3 - Maximum allowable case temperature vs. on-state current.

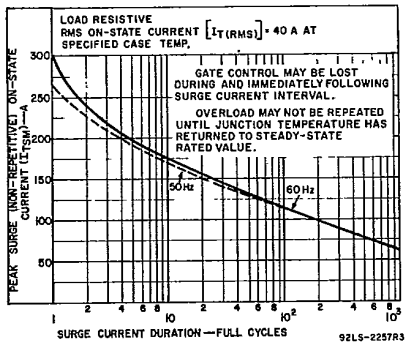

Fig. 4 - Peak surge on-state current vs. surge current duration.

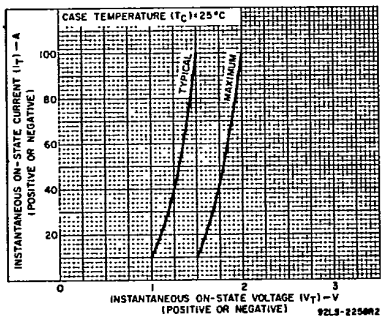

Fig. 5 - On-state current vs. on-stage voltage.

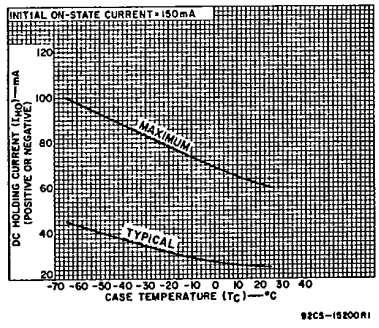

Fig. 6 - DC holding current vs. case temperature.

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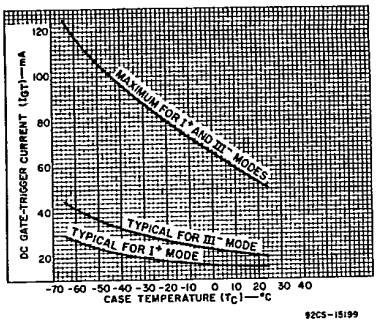

Fig. 7 - DC gate-trigger current vs. case temperature (I^+ & III^- modes).

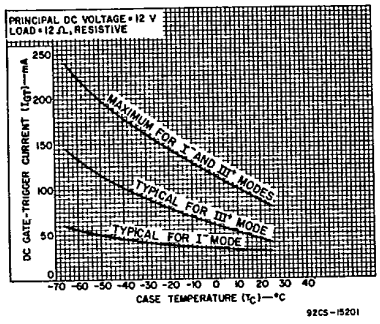

Fig. 8 - DC gate-trigger current vs. case temperature (I^- & III^+ modes).

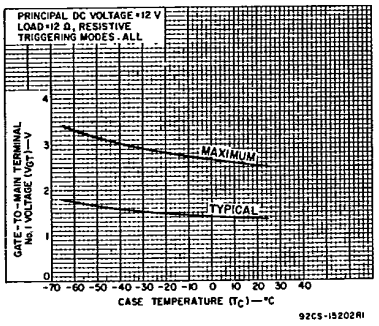

Fig. 9 - DC gate trigger voltage vs. case temperature.

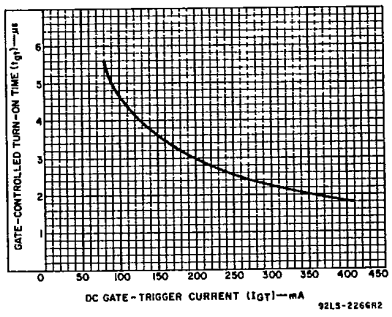

Fig. 10 - Turn-on time vs. gate-trigger current.

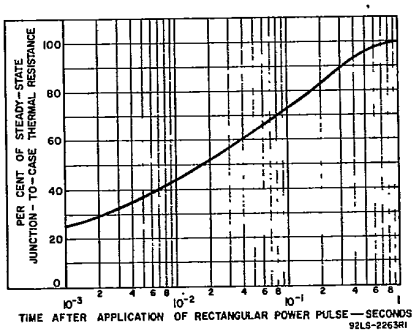

Fig. 11 - Transient junction-to-case thermal reistance vs. time for press-fit and stud types.

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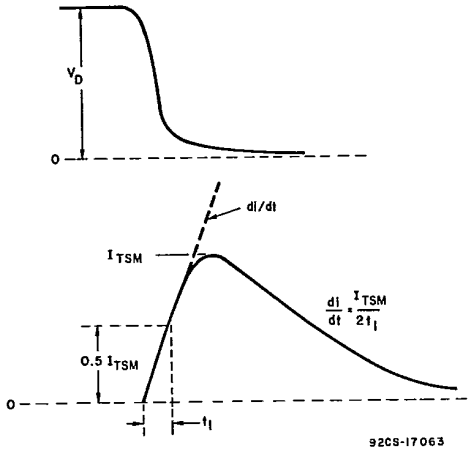

Fig. 12 - Rate of change of on-state current with time (defining di/dt).

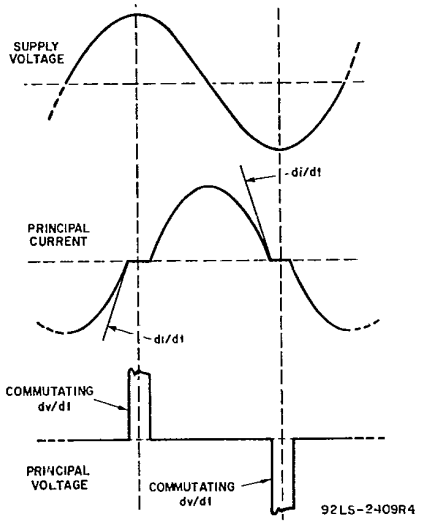

Fig. 13 - Relationship between supply voltage and principal current (Inductive load) showing reference points for definition of commutating voltage (dv/dt).

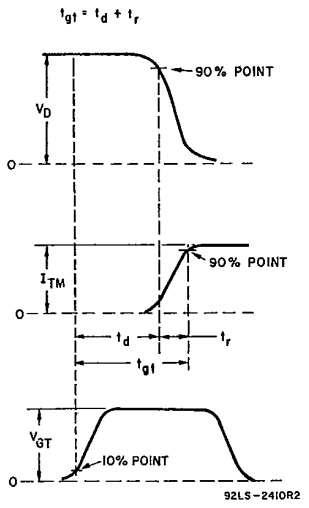

Fig. 14 - Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time (t_{gt}).