NEC Electronics Inc.

APPLICATION NOTE 53
μPD421000/μPD421001/μPD421002
1-MEGABIT DYNAMIC RAMs

T-46-23-03

Description

NEC's μPD421000, μPD421001, and μPD421002 are 1-megabit dynamic RAMs (DRAMs) manufactured with the CMOS 1-μm fine-pattern process and configured as 1,048,576 x 1 bit. As shown in table 1, this family of DRAMs has been developed in a variety of speeds and packages. The package pin layouts appear in figure 1.

Configurations

The μPD421000, μPD421001, and μPD421002 (figures 2, 3, and 4) consist of memory cell arrays, input and output buffers, clock generators, refresh address counters, and row and column decoders.

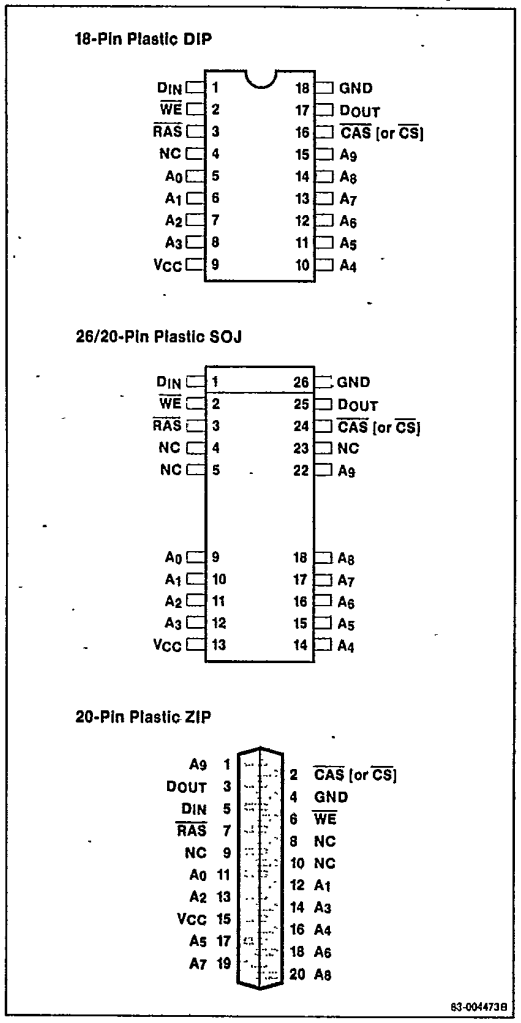
The basic layout of the chips is shown in figure 5. As can be seen from the diagram, the whole memory cell array is divided into 16 smaller 64-kilobit arrays that are accessed separately.

Memory Cell Structure

Dynamic RAMs generally feature one-transistor memory cells, which require only about one-fourth of the area used by four-transistor and six-transistor (flip-flop) memory cells in static RAMs. Although a one-transistor cell provides a big advantage in reducing chip size, data must be rewritten (refreshed) at regular intervals for proper data storage on the memory cell capacitor. A cross-sectional view of the trench-type, one-transistor memory cell used in the μPD421000-series DRAMs is shown in figure 6.

This trench design uses three-dimensional rather than planar capacitors, thereby achieving a larger capacitance in a smaller surface area than in conventional circuits. The capacitance of this type of cell is determined by total trench area, the dielectric constant, and the thickness of the insulating film. To reduce soft errors caused by α-particles, an effective capacitance in excess of 50 femtofarads (fF) is used in the μPD421000, μPD421001, and μPD421002.

Figure 1. Pin Layouts



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μPD421000-SERIES DRAMs

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Table 1. 1,048,576 x 1-Bit DRAM Family

Device	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (min)	Operating Current (max)	Standby Current (max)	High-Speed Mode	Packages
μPD421000-80	80 ns	160 ns	70 mA	1 mA	Fast Page	C = 18-pin plastic DIP V = 20-pin plastic ZIP LA = 26/20-pin plastic SOJ
-10	100 ns	190 ns	60 mA	1 mA		
-12	120 ns	220 ns	50 mA	1 mA		
μPD421001-80	80 ns	160 ns	70 mA	1 mA	Nibble	
-10	100 ns	190 ns	60 mA	1 mA		
-12	120 ns	220 ns	50 mA	1 mA		
μPD421002-80	80 ns	160 ns	70 mA	1 mA	Static Column	
-10	100 ns	190 ns	60 mA	1 mA		
-12	120 ns	220 ns	50 mA	1 mA		

Figure 2. μPD421000 Block Diagram

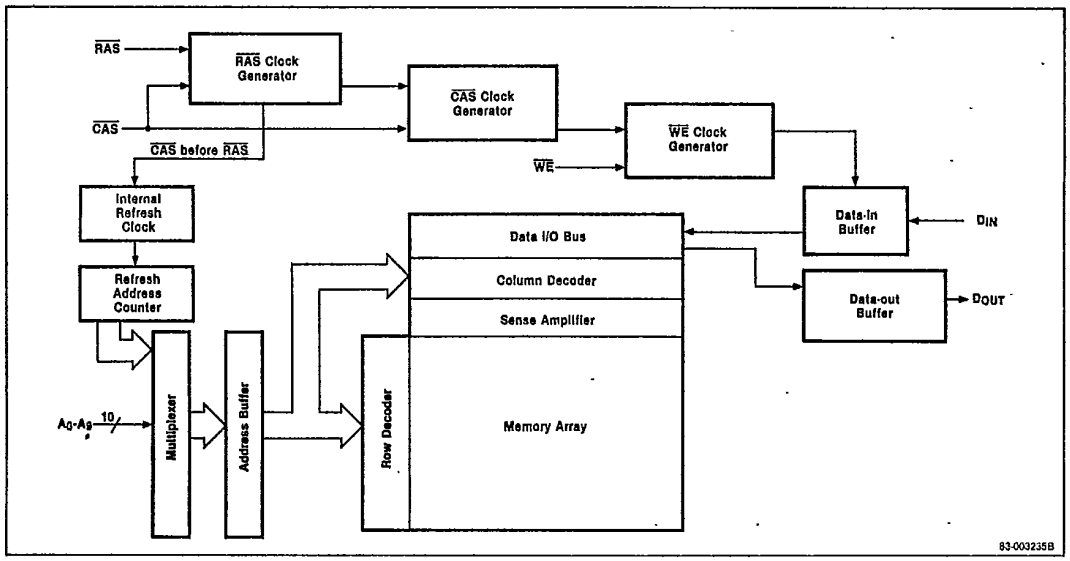

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Figure 3. μPD421001 Block Diagram

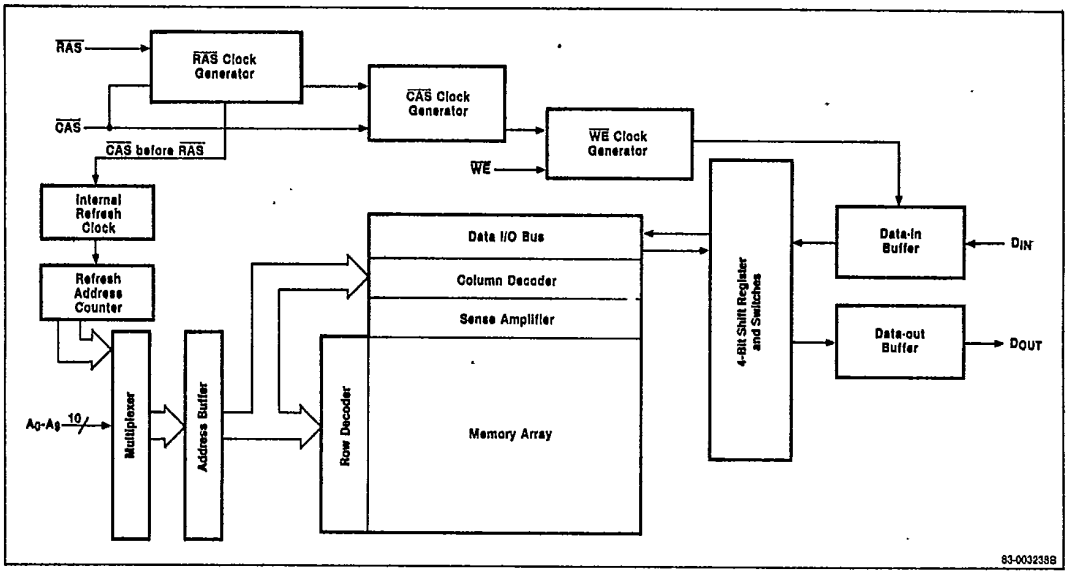

Figure 4. μPD421002 Block Diagram

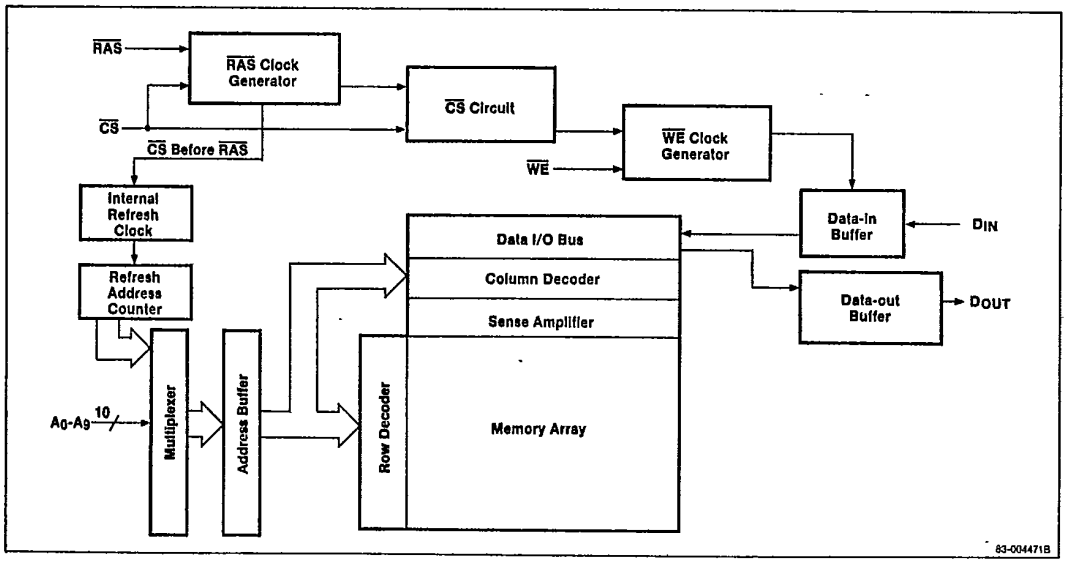

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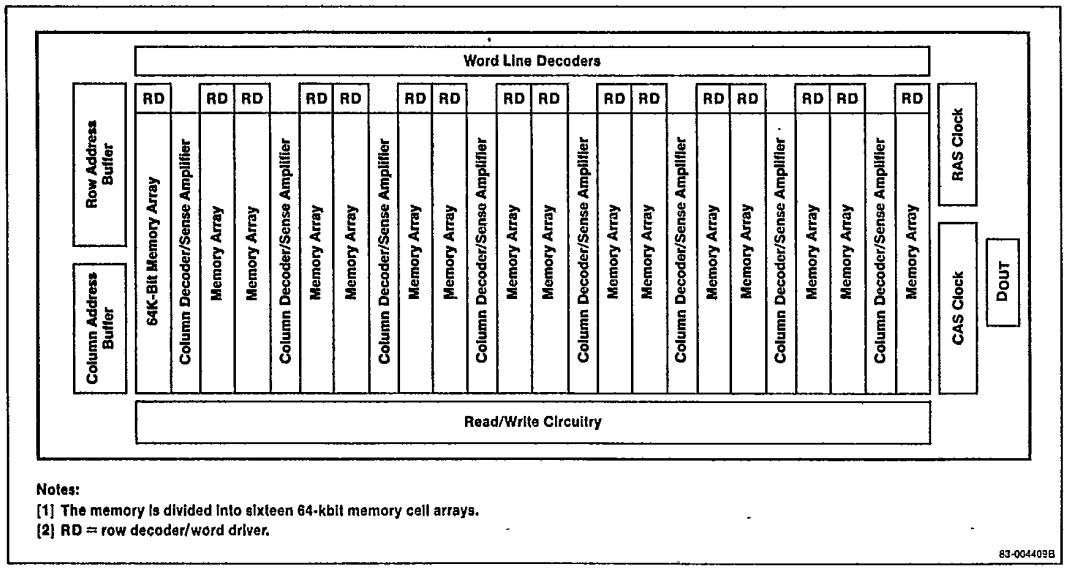
Figure 5. Chip Layout of μPD421000-Series DRAMs



Notes:
[1] The memory is divided into sixteen 64-kbit memory cell arrays.
[2] RD = row decoder/word driver.

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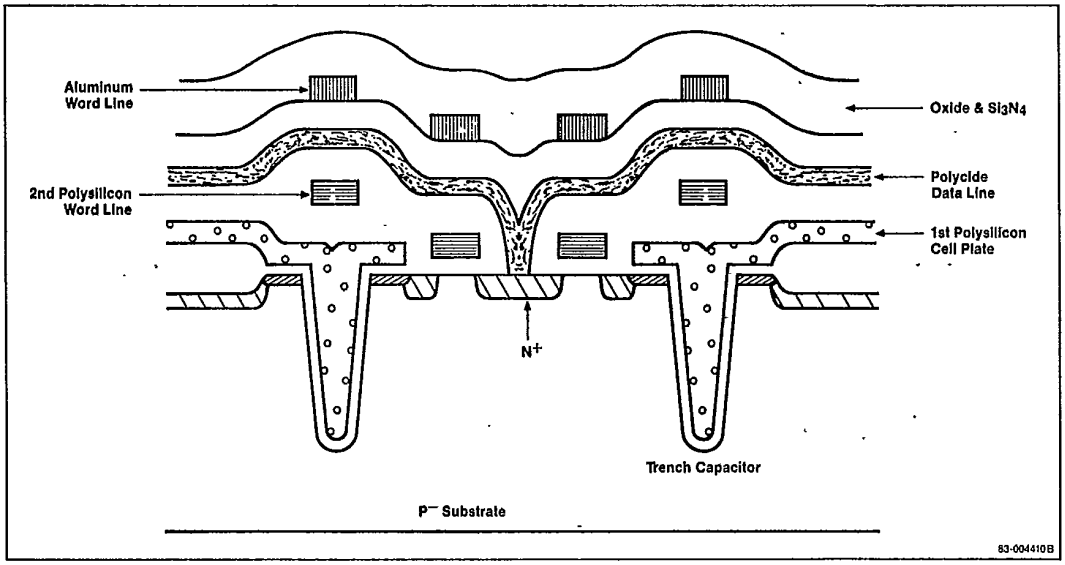
Figure 6. Cross Section of 1-Transistor Memory Cell



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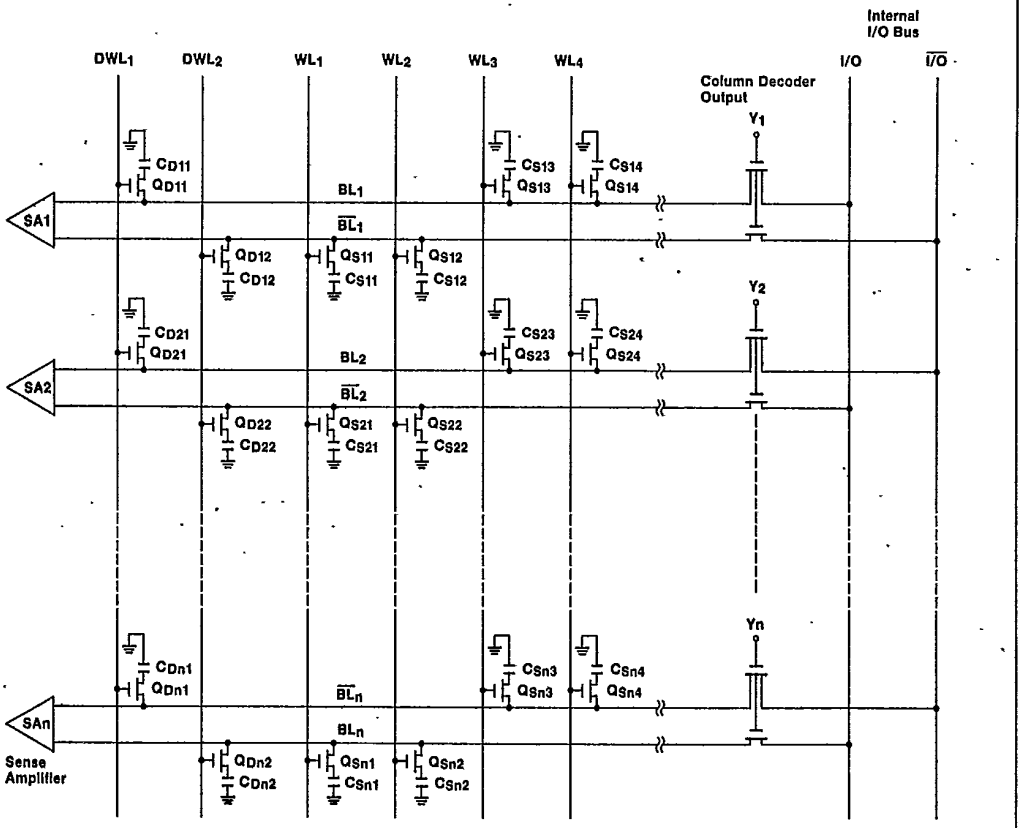
Read/Write Operation

In dynamic RAMs, changes in bit line potential caused by the minute charging and discharging of memory cells are amplified by a sense amplifier to be read as either 1 or 0. Memory cell and sense amplifier equivalent circuits are shown in figure 7.

To read the data from storage cell C_{S11}, the row address selects word line WL_1, and data from memory cells $C_{S11}, C_{S21}, \ldots, C_{Sn1}$ connected to WL_1 is passed to bit lines $BL_1, BL_2, \ldots, BL_n$. These data signals are passed to the sense amplifiers, where they first are compared with data from dummy cells $C_{D11}, C_{D21}, \ldots, C_{Dn1}$, connected simultaneously with the memory cells, and then amplified. At the same time, the original data is rewritten to memory cells $C_{S11}, C_{S21}, \ldots, C_{Sn1}$. Switch Y_1 is then selected by the column address, and the C_{S11} data on the BL_1 line is passed via the I/O bus and a data amplifier to external circuits.

Write and read operations are identical, up to amplification and rewriting of memory cell data selected by a row address. After being passed to the bit line selected by the column address, write data is written into a target memory cell (such as C_{S11}). Since the number of memory cells selected by one row address in the devices is 2048, 2048 memory cells are refreshed simultaneously in each memory or refresh cycle.

Figure 7. Memory Cell and Sense Amplifier Equivalent Circuits



Pin Functions

$\overline{RAS}$ and $\overline{CAS}$ [or $\overline{CS}$]. The μPD421000-series DRAMs include two chip activator inputs: $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$), row address strobe and column address strobe (or chip select). In addition to reading row addresses A_0 through A_9, selecting the relevant word line, and activating the sense amplifiers for read and write operation, the $\overline{RAS}$ input also refreshes the 2048 bits selected by row addresses A_0 through A_8. The $\overline{CAS}$ input latches in column addresses (on the μPD421000 and the μPD421001) and connects the chip's internal I/O bus to the sense amplifiers activated by the $\overline{RAS}$ clock, thereby executing data input or output operations.

A_0 through A_9. Selection of an individual cell from the 1,048,576-word x 1-bit memory cell array requires a 20-bit address input. The three devices all feature an address multiplexing method in which an address is divided into two parts, the lower 10 bits (row address) and the upper 10 bits (column address).

The row address is latched into memory at the falling edge of the $\overline{RAS}$ clock. After an internal timing delay, the column address input circuits become active. Flow-through latches (voltage-level activated, not edge-triggered) for column addresses are enabled on the μPD421000 or μPD421001, and the column addresses immediately begin propagating through the latches to the column decoders. A column address is held in the latches by the falling edge of $\overline{CAS}$. For read cycles on the μPD421002, the column address input circuitry is not controlled by $\overline{CS}$, and column addresses must be held valid until data is read out.

Setup times (t_{ASR} and t_{ASC}) and hold times (t_{RAH} and t_{CAH}) for address inputs are defined in relationship to the falling edges of $\overline{RAS}$ and $\overline{CAS}$ ($\overline{CS}$ or $\overline{WE}$ for write cycles on the μPD421002). In actual operation, a row address is specified before the $\overline{RAS}$ input is activated; once the address bus switches to column addresses, $\overline{CAS}$ (or $\overline{CS}$) is activated.

$\overline{WE}$ [Write Enable]. Read and write cycles are executed by activating the $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) inputs and controlling $\overline{WE}$. An early write cycle is executed if $\overline{WE}$ is activated before the falling edge of $\overline{CAS}$ (or $\overline{CS}$) during a write cycle, and a late write (read-modify-write) cycle is executed if the $\overline{WE}$ input is activated later.

Read and Write Cycles

Read cycles are executed by activating $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) with the $\overline{WE}$ input at a high level (inactive). The $\overline{RAS}$ access time of t_{RAC} is valid if the delay from $\overline{RAS}$ to $\overline{CAS}$ (or $\overline{CS}$) is less than t_{RCD} (max), and the delay from $\overline{RAS}$ to the column address is less than t_{RAD} (max). The $\overline{CAS}$ (or $\overline{CS}$) access time of t_{CAC} is valid if the delay from $\overline{RAS}$ to $\overline{CAS}$ (or $\overline{CS}$) is greater than t_{RCD} (max), and the delay from the column address to $\overline{CAS}$ (or $\overline{CS}$) is greater than t_{ASC} (max). The address access time of t_{AA} is valid if the delay from $\overline{RAS}$ to the column address is greater than t_{RAD} (max), and the delay from the column address to $\overline{CAS}$ (or $\overline{CS}$) is less than t_{ASC} (max). Output data is held valid until $\overline{CAS}$ (or $\overline{CS}$) becomes inactive again (figure 8).

Write cycles are executed by activating the $\overline{RAS}$, $\overline{CAS}$ (or $\overline{CS}$), and $\overline{WE}$ inputs. Write data is latched by the falling edge of $\overline{CAS}$ (or $\overline{CS}$) or $\overline{WE}$, whichever occurs later.

A $\overline{WE}$ input applied before the $\overline{CAS}$ (or $\overline{CS}$) input initiates an early write cycle, whereby write data is latched by the falling edge of $\overline{CAS}$ (or $\overline{CS}$).

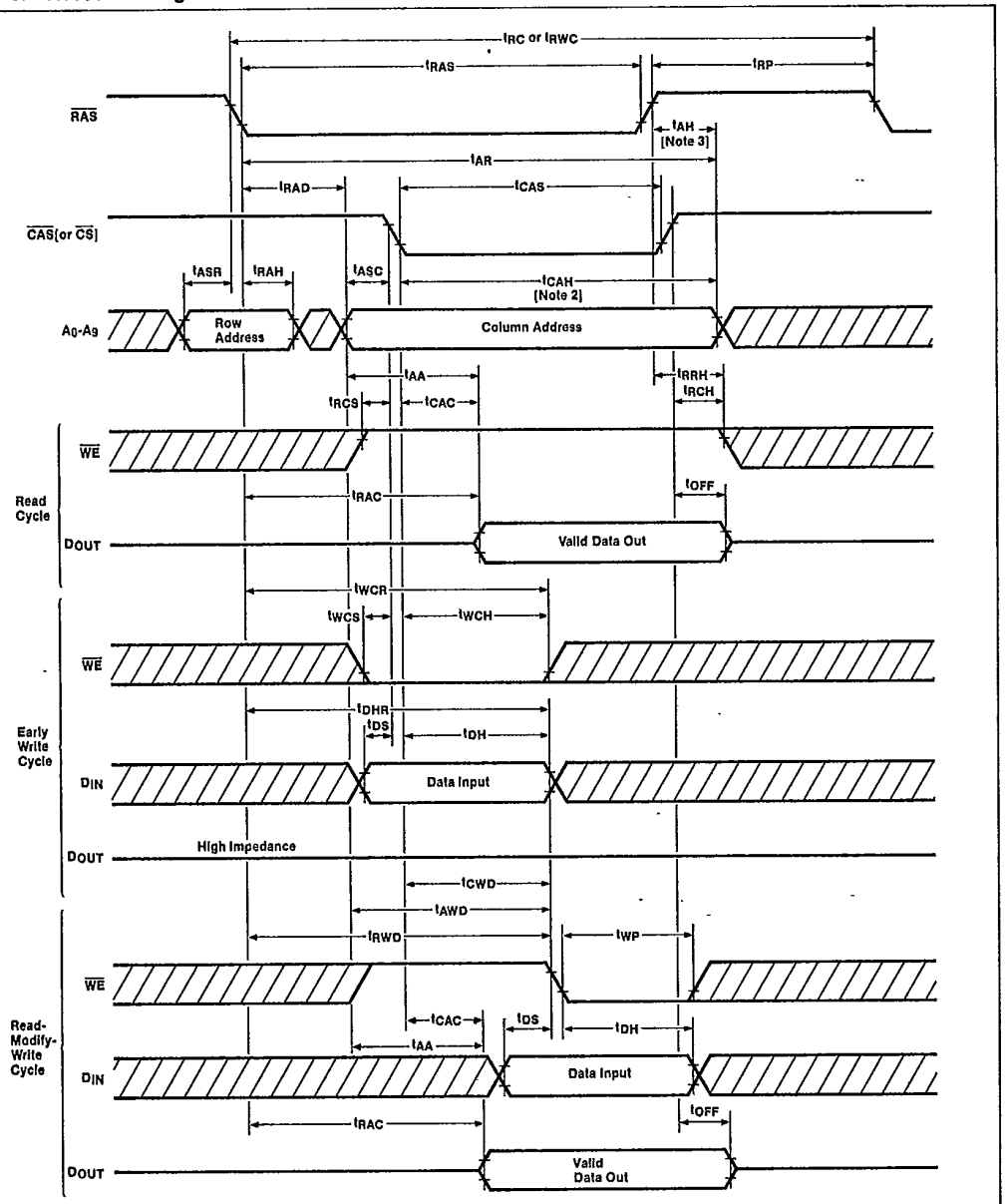
Conversely, a $\overline{WE}$ input applied after the $\overline{CAS}$ (or $\overline{CS}$) input initiates a late write cycle (read-modify-write cycle), whereby write data is latched into the chip by the falling edge of $\overline{WE}$. The status of D_{OUT} is not guaranteed in this case, but depends on the timing of $\overline{WE}$ with respect to $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$). If $\overline{WE}$ is activated at least t_{CWD} after the $\overline{CAS}$ (or $\overline{CS}$) input, and at least t_{RWD} after the $\overline{RAS}$ input, write operation is enabled in the same memory cycle during which the read data is valid.

Refresh Cycles

The process of rewriting data held in a memory cell, refreshing, is performed by a sense amplifier in the μPD421000-series DRAMs. The three devices are capable of executing the same $\overline{RAS}$-only and $\overline{CAS}$ (or $\overline{CS}$)-before-$\overline{RAS}$ refresh cycles as are executed in other conventional, general-purpose DRAMs. All 512 rows of memory cells must be refreshed within any 8-ms period.

Since in image memory applications, row addresses A_0 through A_8 are read or written sequentially within 8 ms, the accessing itself initiates refreshing and no additional refresh cycles are required.

Figure 8. Access Timing



Notes:
[1] In a read-modify-write cycle, cycle time is defined as $t_{RWC} = t_{RWD} + t_{RWL} + 3\,t_T + t_{RP}$.
[2] Timing t_{CAH} applies to the μPD421000 and the μPD421001.
[3] Timing t_{AH} applies to the μPD421002.

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$\overline{RAS}$-Only Refresh Cycle. $\overline{RAS}$-only refreshing is executed simply by leaving the $\overline{CAS}$ (or $\overline{CS}$) input inactive (high level) during a $\overline{RAS}$ clock cycle. This cycle uses the 512 lower addresses specified by row addresses A_0 through A_8 to ensure that all memory cell bits are refreshed. Hence, 2048 bits of memory are refreshed in a single cycle (figure 9).

$\overline{CAS}$ [or $\overline{CS}$]-Before-$\overline{RAS}$ Refresh Cycle. This type of refreshing is executed using the addresses generated by the chip's internal address counter when $\overline{CAS}$ (or $\overline{CS}$) is activated (low level) in advance of the $\overline{RAS}$ input (figure 10).

Even in systems without an address output from the microprocessor, no additional external address counter or refresh address selector is required. $\overline{CAS}$ (or $\overline{CS}$)-before-$\overline{RAS}$ refreshing allows refreshing to be accomplished with a minimum of peripheral circuits (figure 11).

High-Speed Access Cycles

In addition to being capable of standard access, the μPD421000 is equipped with fast-page access, the μPD421001 with nibble access, and the μPD421002 with static-column access (table 2).

Figure 9. $\overline{RAS}$-Only Refresh Cycle

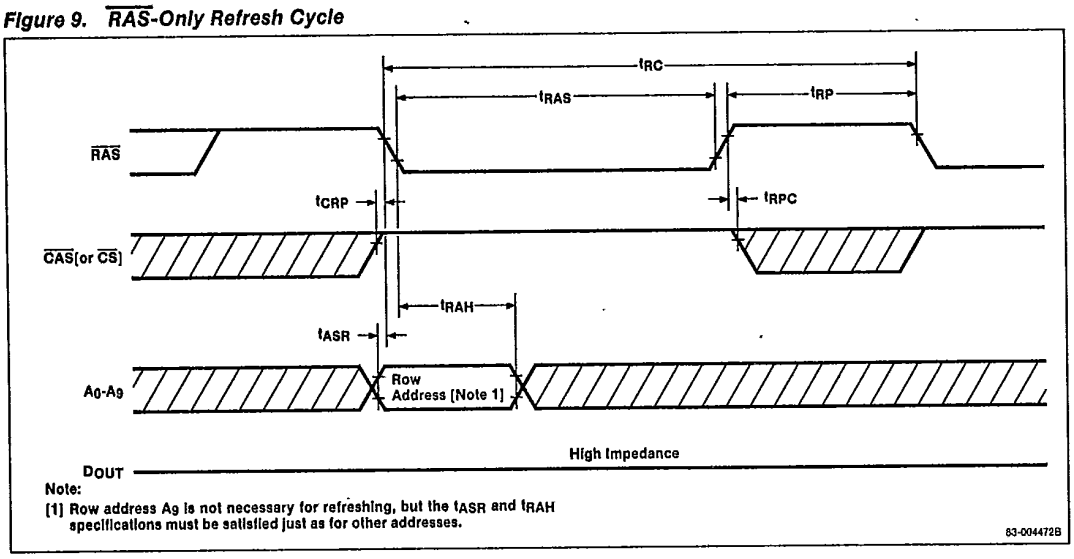

Figure 10. $\overline{CAS}$ (or $\overline{CS}$)-Before-$\overline{RAS}$ Refresh Cycle

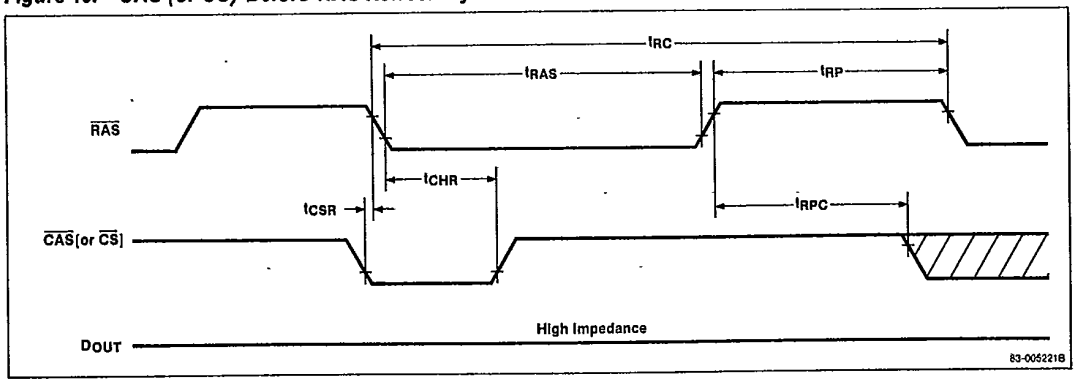

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Figure 11. Address Multiplexing

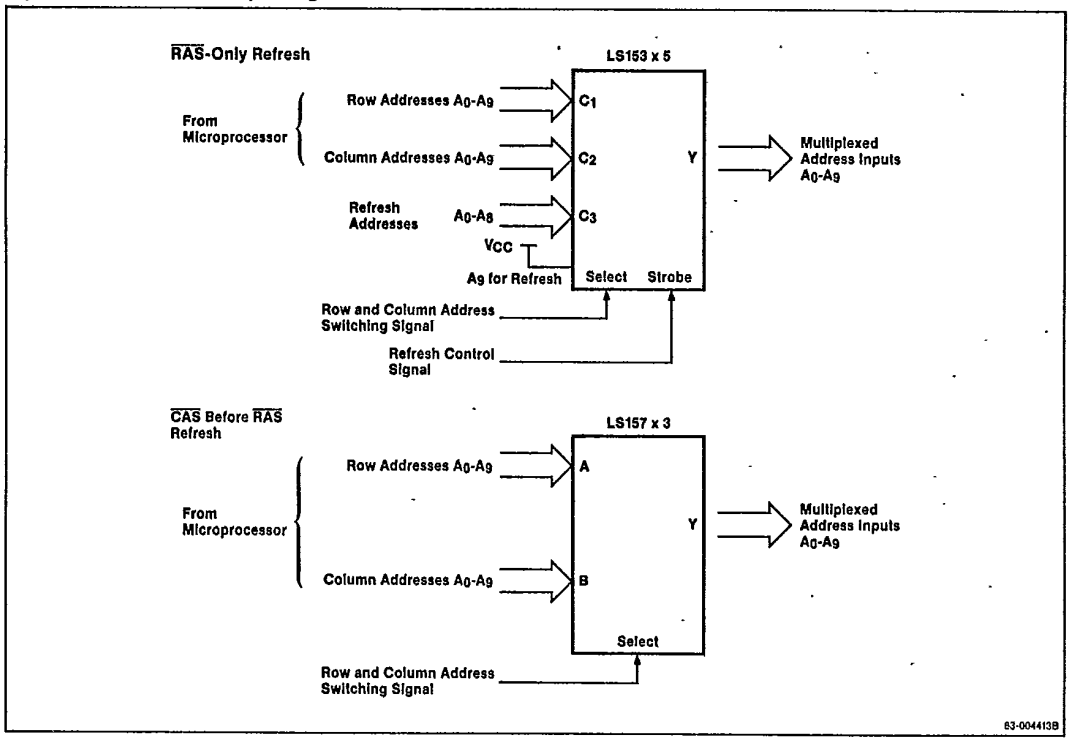

Table 2. Major Characteristics of Fast-Page, Nibble, and Static-Column Modes

Device	Access Time (max)	Cycle Time (min)	Internal Address Usage	High-Speed Access
μPD421000-80	45 ns	50 ns	Row: Page selection Column: Individual cell access on one page	Random access on one page selected by A_0 through A_9
-10	50 ns	60 ns		
-12	60 ns	70 ns		
μPD421001-80	20 ns	40 ns	Row, Column: A_9 inputs set starting location for nibble-mode access	Serial access (4 bits maximum)
-10	25 ns	45 ns		
-12	30 ns	55 ns		
μPD421002-80	45 ns	50 ns	Row: Row selection Column: Individual cell access on one row	Random access on one row selected by A_0 through A_9
-10	50 ns	60 ns		
-12	60 ns	70 ns		

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Fast-Page Mode. Fast-page mode makes it possible to randomly access data in the same row address (figures 12 and 13). The 1024 bits of memory are obtained from the combinations of column address inputs A_0 through A_9 within one row address in the μPD421000. Up to 1998 continuous accesses can be executed on the 80-ns version before the maximum interval for t_{RASP} (100 μs) is reached.

The t_{PC} cycle time for random fast-page read or write cycles is equivalent to $t_{CAS} + t_{CP} + 2t_T$.

Figure 12. Memory Cell/Sense Amplifier Block of the μPD421000

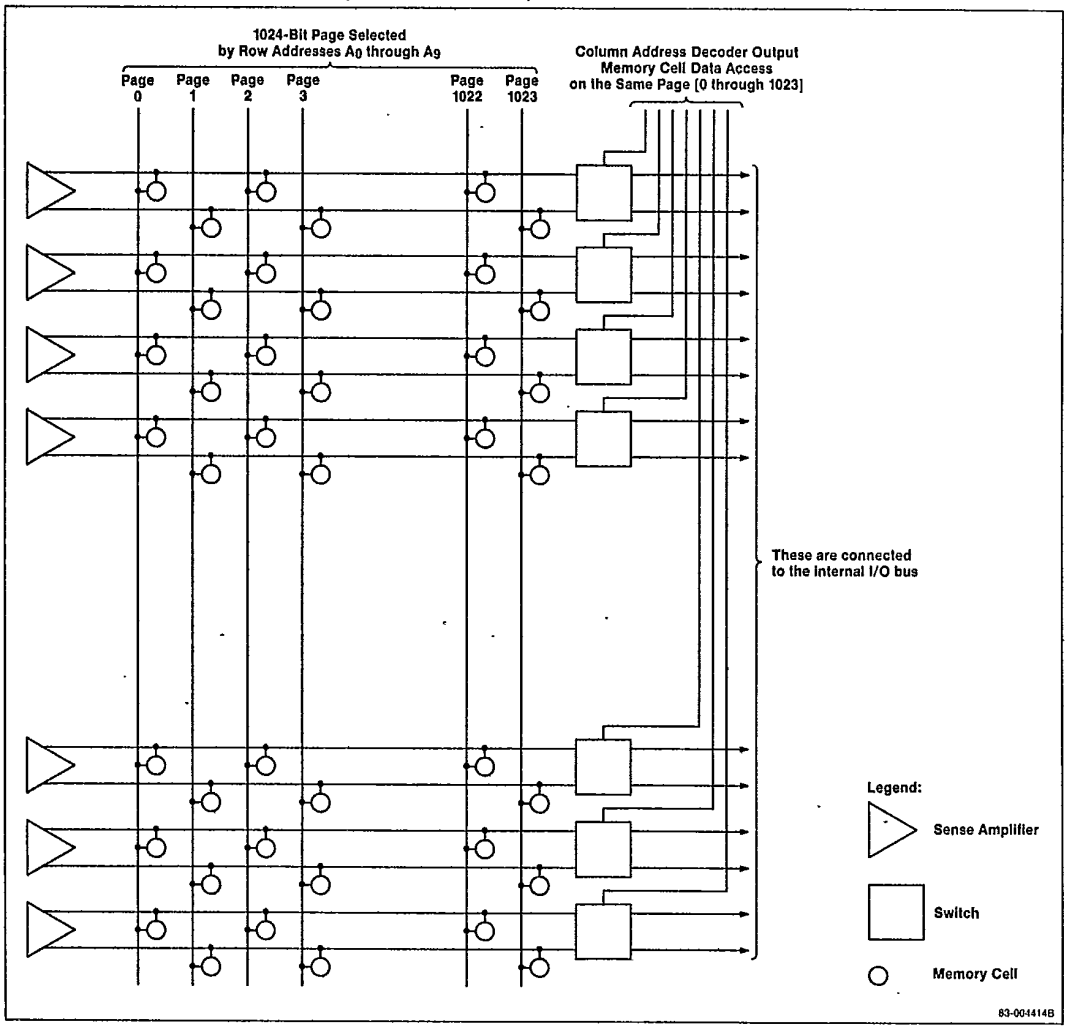
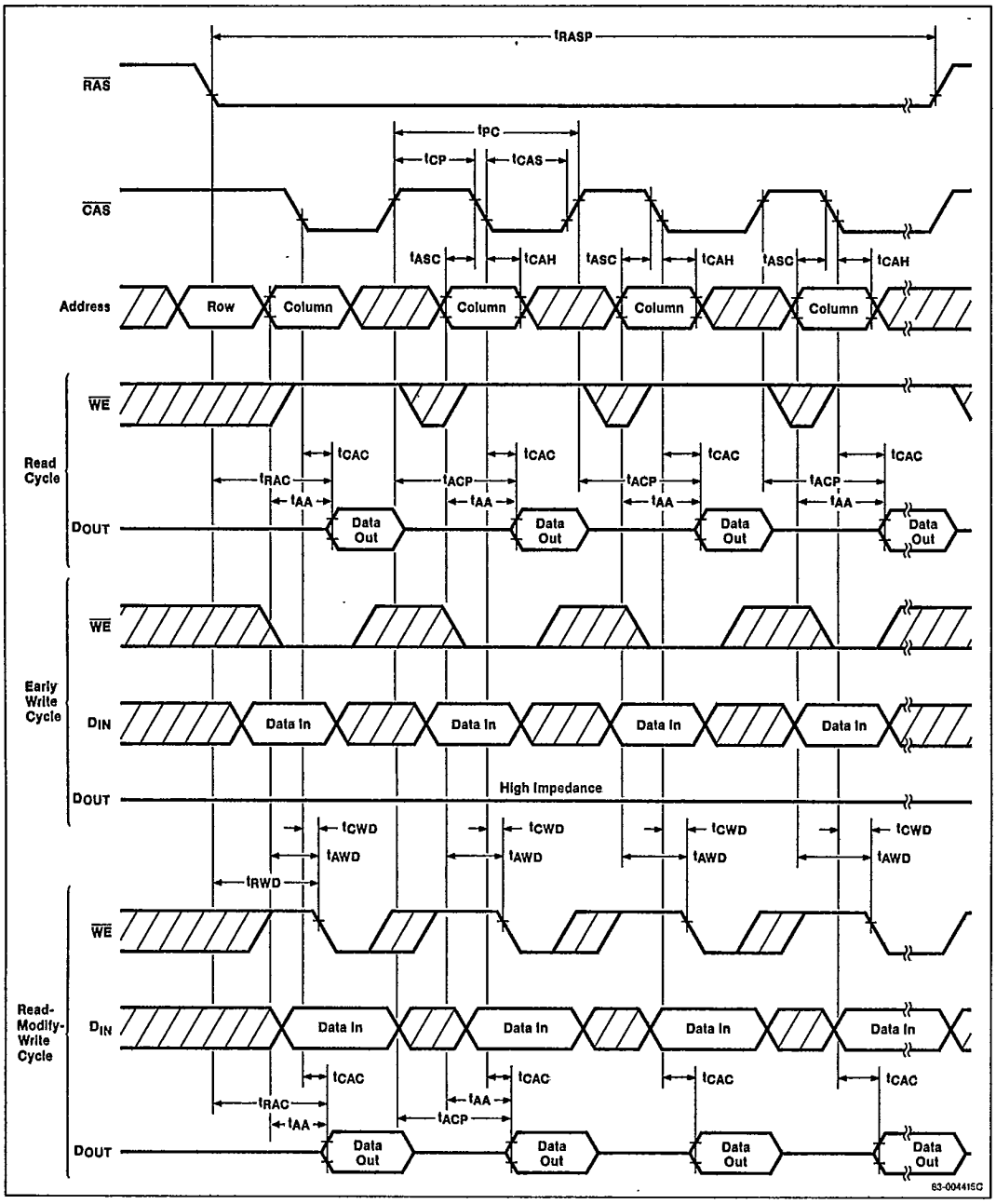
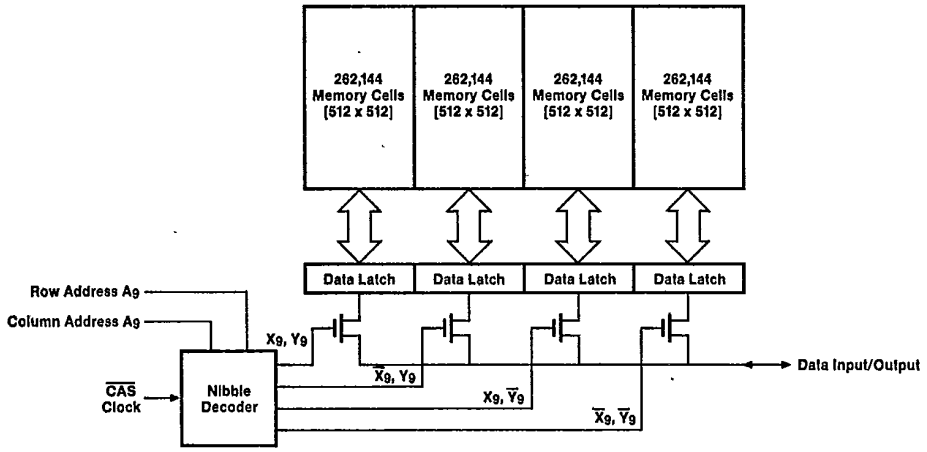


Figure 13. Fast-Page Timing



Nibble Mode. In nibble-mode cycles, the first data location is specified by row and column addresses A_0 through A_9 during a read or write cycle (table 2 and figures 14 and 15). When the μPD421001 internally sequences the two highest-order addresses (A_9) during the next $\overline{CAS}$ clock cycle, read and write cycles can be executed in less time than in fast-page operation.

Figure 14. Nibble-Mode Block Diagram and Example of Access Sequence



Sequence	Nibble Bit	Row Address A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Comment
$\overline{RAS}/\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	External address
$\overline{CAS}$ Cycling	2	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
$\overline{CAS}$ Cycling	3	0	1	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	Internal address
$\overline{CAS}$ Cycling	4	1	1	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	
$\overline{CAS}$ Cycling	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	Repeated sequence

Notes:
[1] X_9 = Row address A_9
[2] Y_9 = Column address A_9

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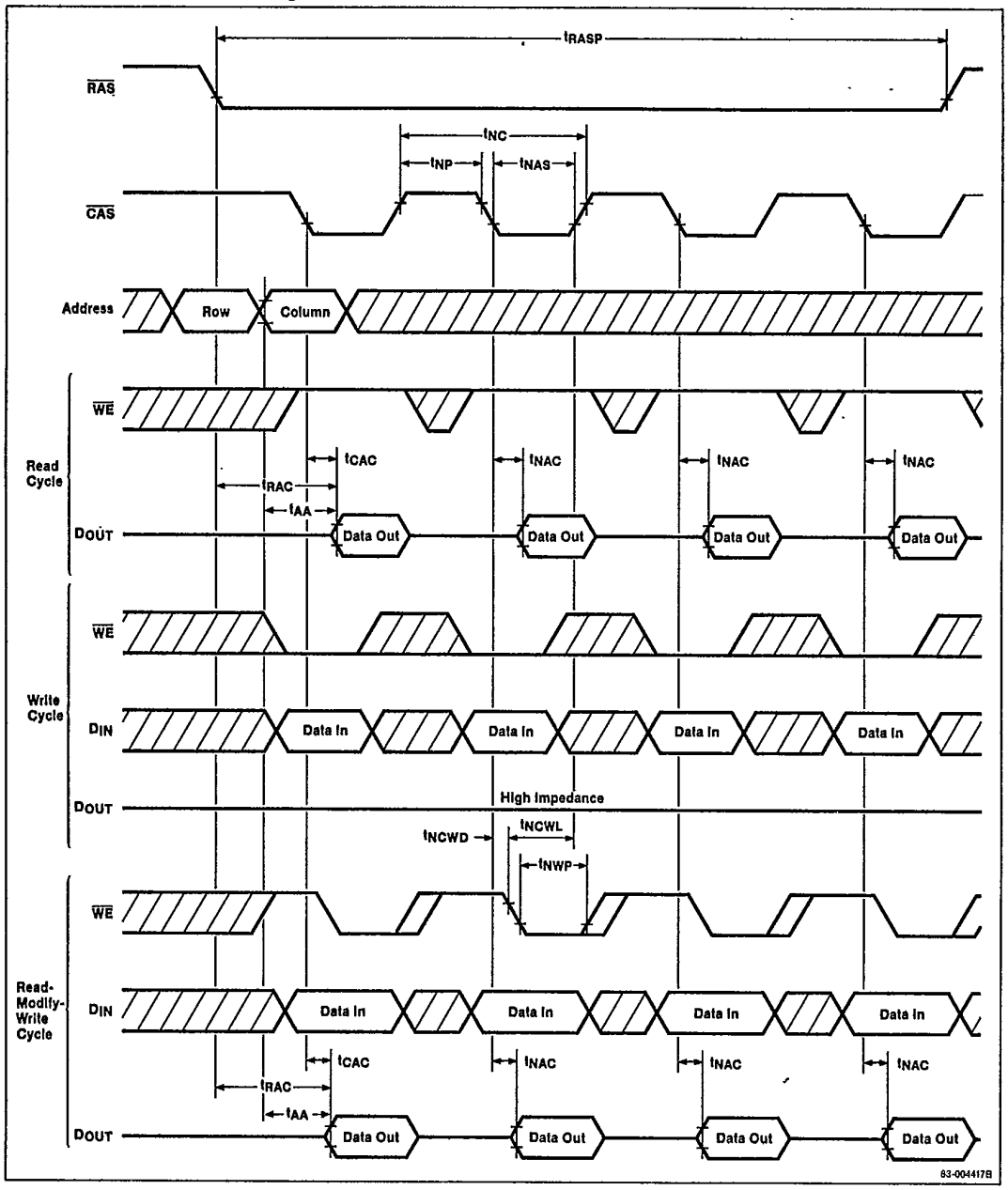
Figure 15. Nibble-Mode Timing



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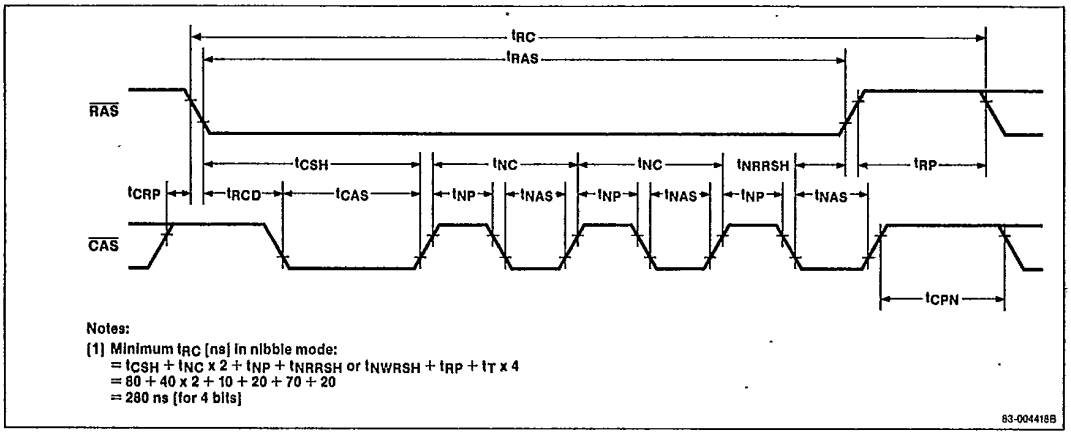
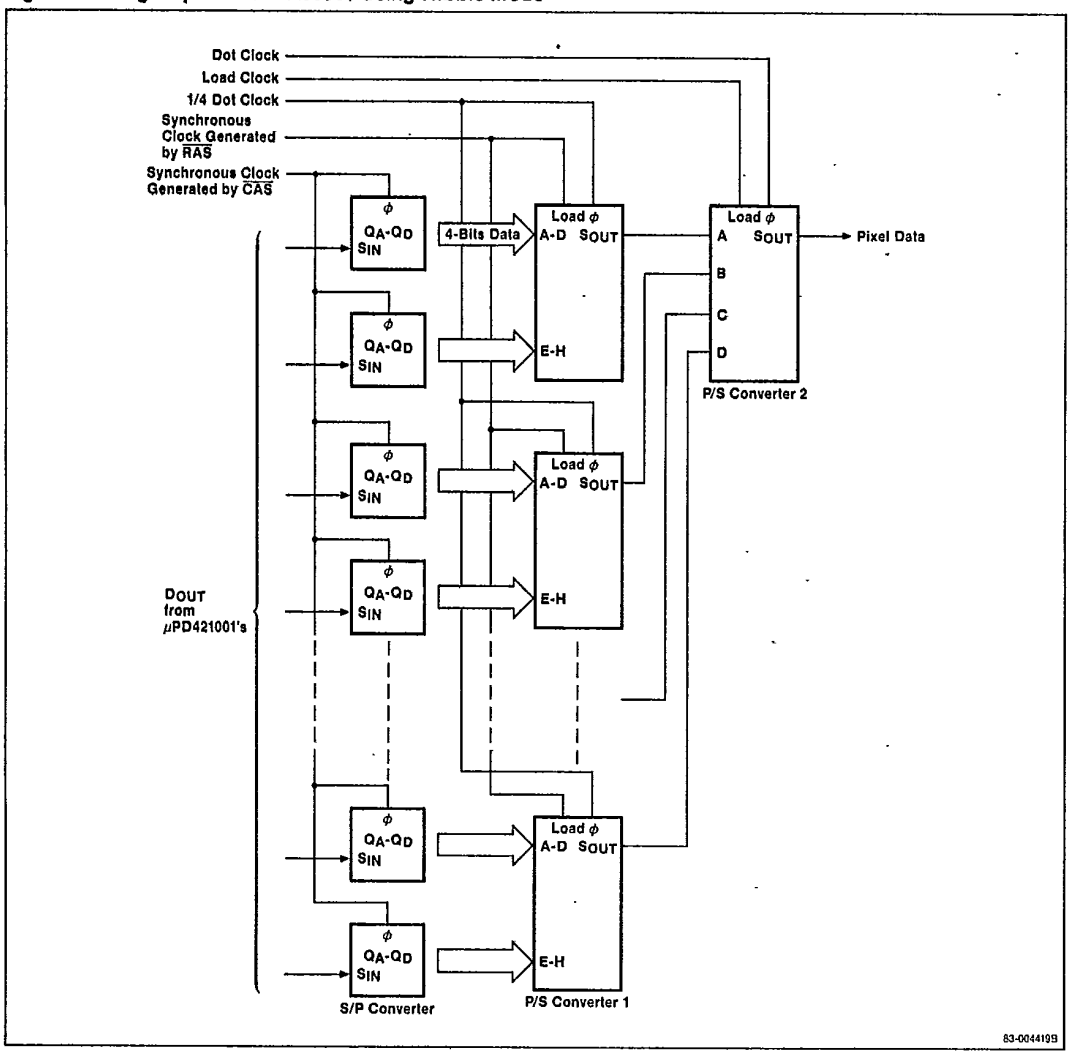
For the 80-ns version, the average cycle time per bit in nibble mode is 70 ns, when 4 bits are accessed during a long t_{RAS} cycle (figure 16). By using multiple μPD421001 devices, high-speed cache and frame buffer applications are possible (figure 17).

Figure 16. Average Data Rate in Nibble Access



Notes:
[1] Minimum t_{RC} [ns] in nibble mode:
$= t_{CSH} + t_{NC} \times 2 + t_{NP} + t_{NRRSH}$ or $t_{NWRSH} + t_{RP} + t_T \times 4$
$= 80 + 40 \times 2 + 10 + 20 + 70 + 20$
$= 280$ ns [for 4 bits]

Figure 17. High-Speed Data Access Using Nibble Mode



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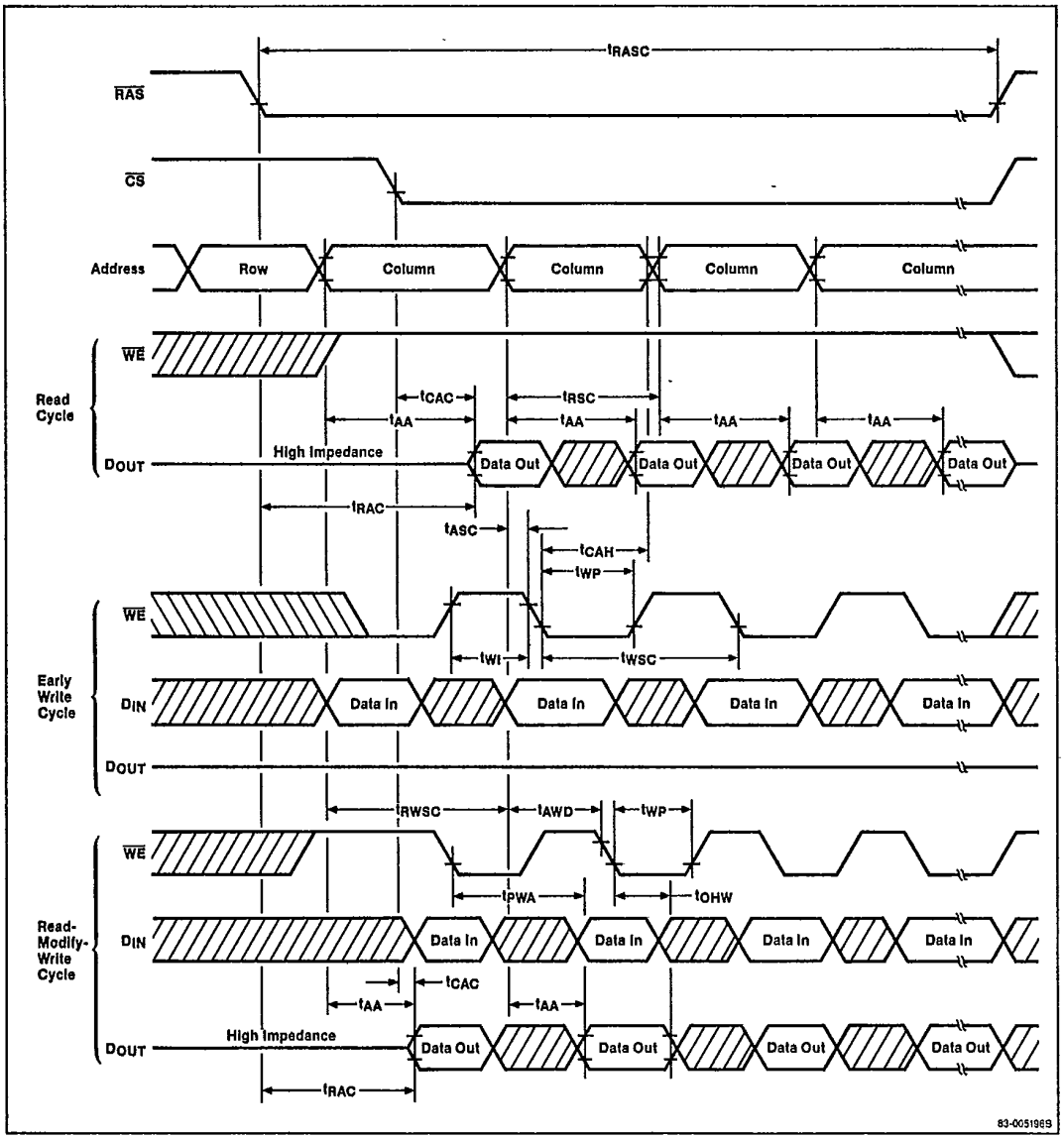
Static-Column Mode. Row and column addresses are functionally equivalent in static-column and fast-page access. The available number of continuous accesses on one row, and the cycle timing, are also similar to fast-page operation.

In a static-column device, there are no setup or hold timing requirements for read addresses; $\overline{CS}$ may be held low continuously in the ON-state. To allow this feature, the column addresses must be maintained as valid inputs for the duration of each cycle. There are few other restrictions on timing (figure 18).

Figure 18. Static-Column Timing



Precautions

Precautions when using the μPD421000, μPD421001, μPD421002, and other DRAMs should be carefully observed in the areas listed below:

- Power-on and initialization
- Supply voltage fluctuations caused by peak currents
- Relationships between address/data inputs and drivers
- $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) generation

Power-On and Initialization. Dynamic RAMs operate by the charging and discharging of gate and internal circuit capacitances. Therefore, dummy $\overline{RAS}$ clock cycles must be executed to charge internal potentials to the prescribed levels when power is applied. Dummy $\overline{RAS}$ cycles are also necessary when there has been no accessing (reading, writing, or refreshing) for periods longer than the refresh interval (figure 19).

To control transistor threshold voltages and decrease internal stray capacitance, DRAMs are usually equipped with a substrate voltage generator circuit to supply the chip's interior with negative voltage. Approximately 100 μs is required to generate an adequate negative voltage level after power is applied and $V_{CC} \geq 4.5$ V.

When the power is switched on, a peak current dependent on the levels of $\overline{RAS}$, $\overline{CAS}$ (or $\overline{CS}$), and $\overline{WE}$ is reached during the rising of V_{CC}. This peak current—maximum when $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) are active and $\overline{WE}$ is inactive—can be minimized by using clock input pullups on $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) so that their rise times correspond to the rise time of the power supply.

Supply Voltage Fluctuations. Since 1 and 0 logic (storage) operations are executed by the charging and discharging of capacitances, including the memory cells, the peak current generated is dependent on charge and discharge timing.

This peak current is concentrated just after $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) transition intervals (figure 20) with a peak value of about 120 mA. Since this current is a source of noise (voltage drop) in the memory system supply voltage, decoupling by multilayer ceramic capacitors with excellent frequency response is necessary. If the average of the 120-mA peak current pulse lasts about 100 ns, the capacitance required to keep the drop in the supply voltage line at about 0.1 V will be calculated as follows:

$$C = \frac{120\ (\text{mA}) \times 100\ (\text{ns})}{0.1\ (\text{V})}$$

$$= 120 \times 10^3\ \text{pF}$$

$$= 0.12\ \mu\text{F}$$

Therefore, when designing the memory board, keep the power and ground leads as short as possible for low inductance. Decoupling capacitors of about 0.2 μF must be inserted between the power supply lines for each memory device. With careful board layout, the use of fewer but larger capacitors is possible. Capacitors used in one of every two memory device locations, with a value of perhaps 0.33 μF, can provide satisfactory decoupling in many cases.

Figure 19. Dummy Cycles after Power Is Applied

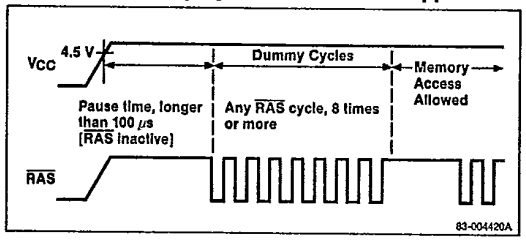
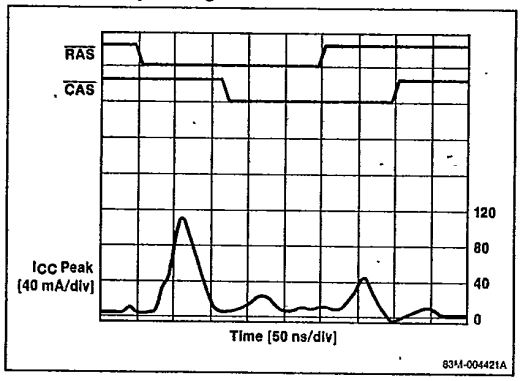


Figure 20. Operating Current Waveform



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Address/Data Inputs and Drivers. Probably the most important consideration in DRAM timing is the relationship between address/data inputs and the external drivers. In address-multiplexed DRAMs such as the μPD421000, μPD421001, and μPD421002 (where row and column addresses are supplied as two sets of inputs), addresses supplied externally have to be switched by a multiplexer.

The sequence of this timing must be designed very carefully. A timing sequence starts with the setting of row addresses. Next, $\overline{RAS}$ falls. After the specified hold time for row addresses is met, the addresses are switched to set up column address input. Once $\overline{CAS}$ (or $\overline{CS}$) falls, the specified hold time for column addresses must be satisfied.

When $\overline{CAS}$ (or $\overline{CS}$) is activated within the time specified for t_{RCD} (max), the setup time for column addresses is more difficult to guarantee than when t_{RCD} is longer than t_{RCD} (max), because one external address driver has to drive more than one address pin in an array of DRAMs. The address multiplexer's delay time is increased by load capacitances larger than the typical value.

For illustration, measurements of output delay times for certain drive load capacitances are shown in figure 21.

In the design of high-density memory boards having a large number of memory devices, partitioning of drivers becomes necessary because of wiring and through-hole capacitances. Special care must be taken to ensure that the setup and hold times for addresses conform with the specifications. Otherwise, invalid or undefined addresses may be latched into the chip, and data may be destroyed even if nothing is written.

$\overline{RAS}$ and $\overline{CAS}$ [or $\overline{CS}$] Generation. In addition to reading the address inputs, $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) also generate the basic timing for all DRAM circuit operations. The internal timing generators are connected in daisy-chain fashion, and are completely controlled by the basic $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) inputs. Because of this control, the memory system design must prevent noise glitches from being generated in the $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) inputs.

$\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) timing is specified in terms of minimum values. High- or low-level pulses that do not satisfy these minimum values can result in incorrect output data (because there is insufficient time for sense amplifier operation), and can also lead to destruction of write data. Therefore, the prevention of noise glitches must be carefully considered in logic and circuit design.

Figure 21. Effect of Load Capacitance on TTL (7404) Output

Delay and Transition Times

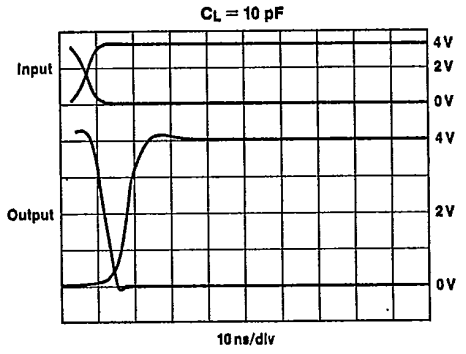
Parameter	Time [ns] C_L = 10 pF	C_L = 110 pF	C_L = 210 pF
t_{PLH}	9	16.5	26
t_{PHL}	5.5	12.5	17
t_R	3.2	7.8	15
t_F	1.5	3.8	5.5

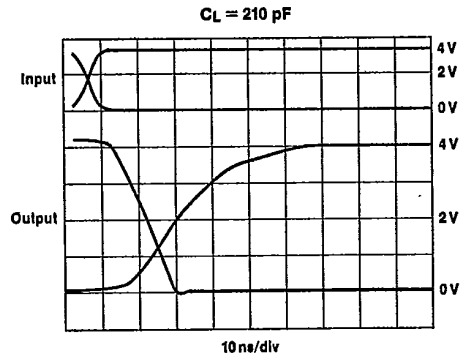
Notes:

[1] t_{PLH}, t_{PHL} are defined as the delay time from V_{IN} = 1.5 V to V_{OUT} = 2.4 V or 0.8 V.

[2] t_R and t_F are defined as the transition time between V_{OH} [min] and V_{OL} [max].

[3] Load capacitance C_L includes the oscilloscope input capacitance.





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V40™ MICROPROCESSOR APPLICATION

Features

The μPD70208 (also known as V40) is a high-performance 8-bit CMOS microprocessor featuring 16-bit architecture in the CPU, and including a number of other peripheral devices within the same chip. The CPU is equipped with a powerful set of instructions that cover bit processing and multiple-length, packed-BCD operations, high-speed multiplications and divisions, and variable-length bit and field manipulations.

This device combines high-speed processing with flexibility in a variety of applications. The on-chip peripherals include a clock generator with a timer/counter and programmable wait control, refresh control, serial control, interrupt control, and DMA control units. In addition to allowing more compact microcomputer systems, the V40 has a simplified system design.

When connected to the μPD421000-series DRAMs, the V40 does not require an external refresh timer or other peripherals, which means a big reduction in the number of external devices required.

Memory Mapping

In the V40, memories of up to 1 megaword can be accessed using address information (A_{19} through A_0) output from the 20-bit address bus (figure 22).

The first 1024 bytes, 0 through 3FFH, are allocated to interrupt vectors (although areas that cannot be used by the system can be used elsewhere). Addresses FFFF0H through FFFFBH are used for starting and resetting purposes; FFFFCH through FFFFFH are reserved for future use and cannot be used here. The remaining address space, 400H through FFFEFH, is not allocated and may be used as desired.

As shown in figure 23, with a data bus width of 8 bits in the V40, CPU connections to the memory require only that the 20-bit address output from the CPU be accepted in the 1-megabyte address space. Byte data is accessed in one bus cycle, and word data is accessed in two bus cycles.

V40 is a trademark of NEC Corporation.

Because of this simple connection requirement, it is only necessary to allocate the system control ROM to addresses of at least FFFF0H and disable the ROM-area RAM (since 1 megabyte is already taken up by eight 1-megabit DRAMs). The method used may involve either deselecting the ROM-area RAM by a decoder, or executing bank switching to use the entire area as RAM area. The example included for this application shows the former method because it is simpler.

Figure 22. V40 Memory Mapping

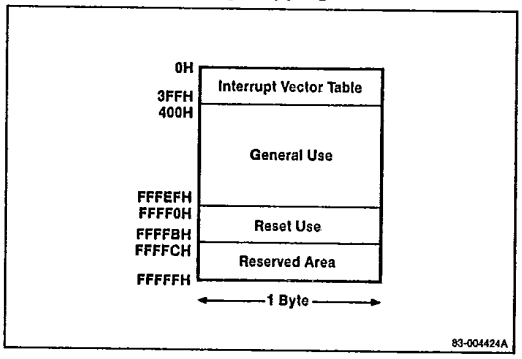
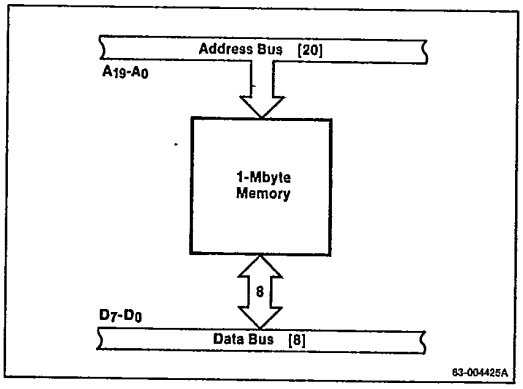


Figure 23. V40 Memory Interface



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Hardware Configuration

Since refresh addresses and the timing control outputs can be supported by programming on-chip circuits, the generation of $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) timing is the only major DRAM support not provided directly by the V40 (figure 24).

Memory Access Timing Generation

Although V40 memory access timing can be generated from either the bus status or MWR/$\overline{MRD}$, the μPD71088 system bus controller is used in this application example to enable connections to slightly slower-speed memories. The $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) signals are thus generated by decoding the bus status.

The $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) generator is shown in figure 25, and the operation timing in figure 26. To generate the control timing with this system controller, bus status signal BS_2 is sampled by the CPU clock output (ϕ_{OUT}) at the rising edge of the T_1 cycle, and $\overline{RAS}$ is generated from FF2 at the falling edge of ϕ_{OUT} at the end of T1. The multiplex control signal (MPX) used in address switching during memory cycles is generated by $\overline{RAS}$. After $\overline{RAS}$ is generated, it is delayed by the rising edge of the external 16-MHz clock to create MPX, which is then passed to the data selector input.

As can be seen from figure 26, memory access time is equal to $2/f(\phi_{OUT}) - (t_{SDK} + \text{TTL delay time})$. Even if an external clock of 16 MHz is used, a -12 device is sufficient ($\overline{RAS}$ access time in the -12 device is 120 ns).

Figure 24. Hardware Configuration for the Use of 1M DRAMs

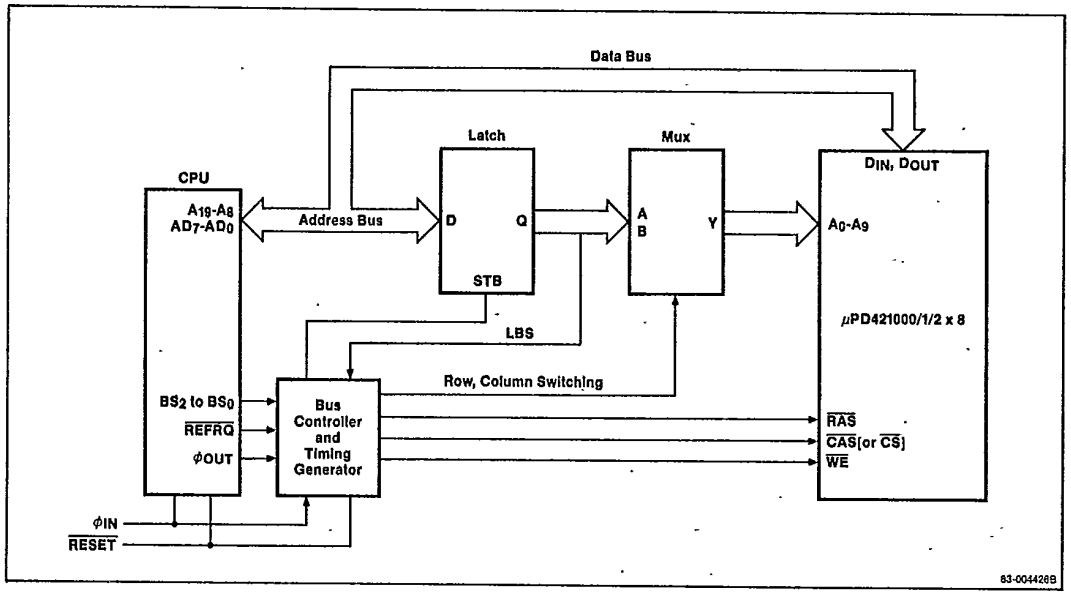

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Figure 25. $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) Timing Generator

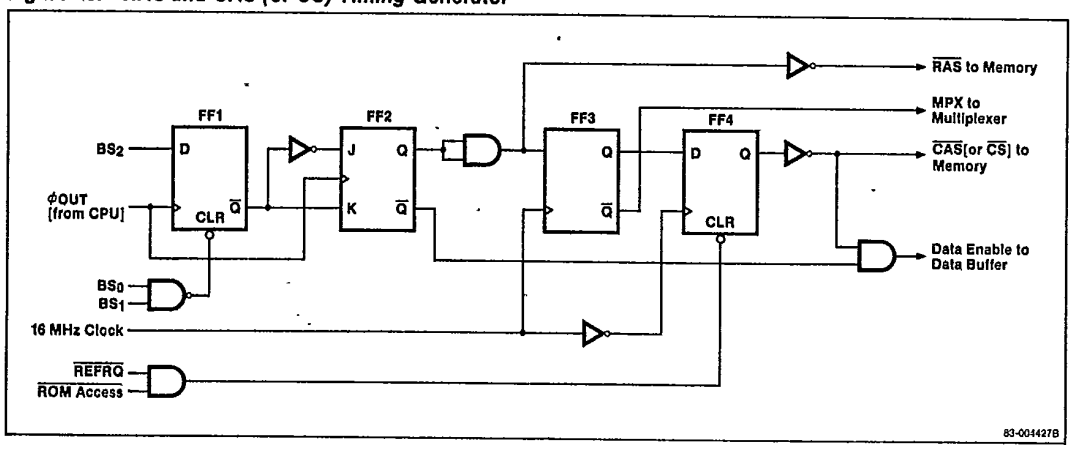

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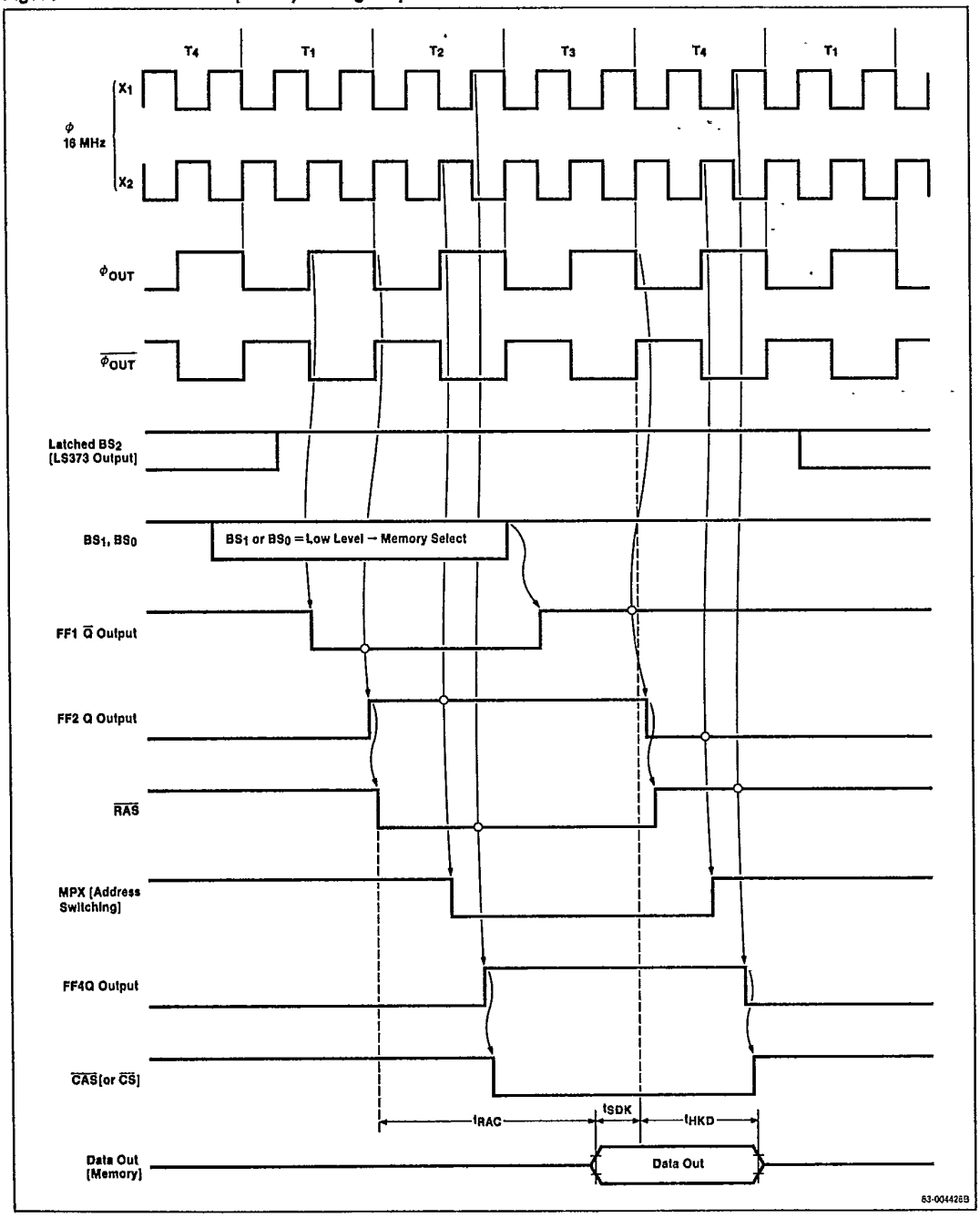
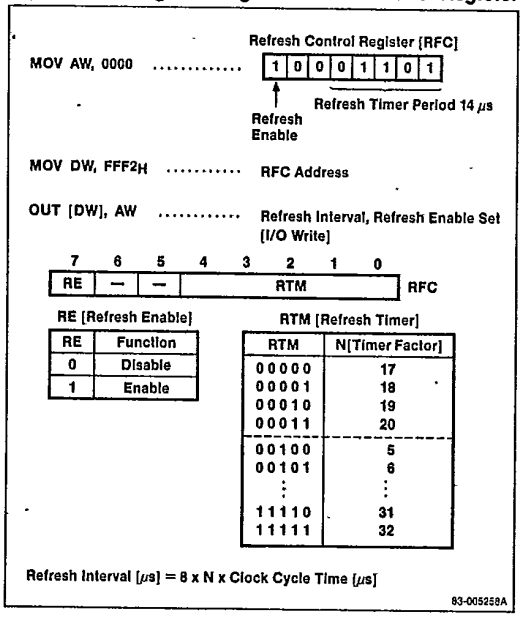
Figure 26. $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) Timing Sequence



Refresh Timing Generation

Refreshing for the μPD421000, μPD421001, and μPD421002 is executed by selecting 512 lines in 8 ms. In the V40, memory refreshing can be handled easily by outputting the $\overline{REFRQ}$ control signal and the A_0 through A_8 refresh addresses. These signals are controlled by programming the refresh control register (RFC), allocated to I/O address FFF2H (figure 27).

Figure 27. Programming of Refresh Control Register



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This function generates the $\overline{\text{REFRQ}}$ control signal in accordance with the programmed interval. In this application example, $\overline{\text{REFRQ}}$ is used to disable generation of the $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) clock during refresh cycles, thereby initiating $\overline{\text{RAS}}$-only refreshing. Figures 28 and 29 show how to generate memory addresses and how to control data input and output by using control signals generated by the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) timing generator. Figure 30 shows the timing for V40-generated refresh addresses.

The programmed values for the control register appear in figure 27 (also refer to the *μPD70208/μPD70216 User's Manual).*

Authorization for the μPD70208/μPD70216 refresh control unit to use the memory bus can be set either to top priority or lowest priority, depending on the hold status of the refresh request. Top priority is set if seven refresh requests are being held, and refreshing is executed consecutively until the number of requests is reduced to three.

Although a wait interval of maximum duration (three clocks) is inserted by the built-in wait control unit, if a reset input is applied after power is applied, no wait interval need be inserted in actual applications. Therefore, the wait control register has to be reset when the V40 is used at 8 MHz.

Wait control registers WCY2 (FFF6H), WCY1 (FFF5H), and WMB (FFF4H) write program data at these I/O addresses using an I/O write instruction (figure 31).

Figure 28. Memory Access Generation

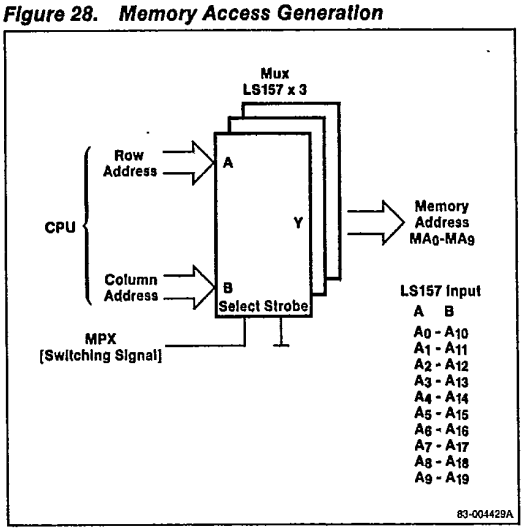


Figure 29. Data Input and Output Control

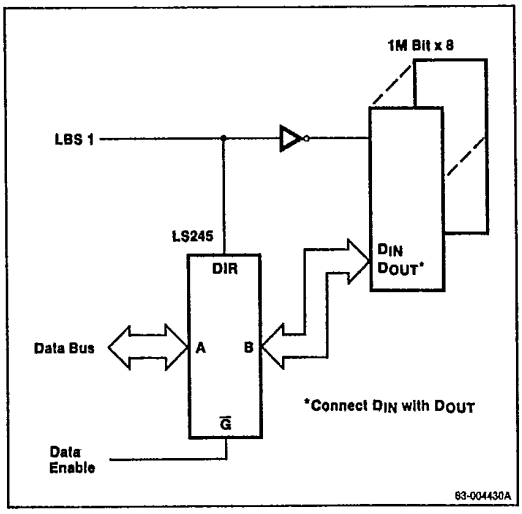
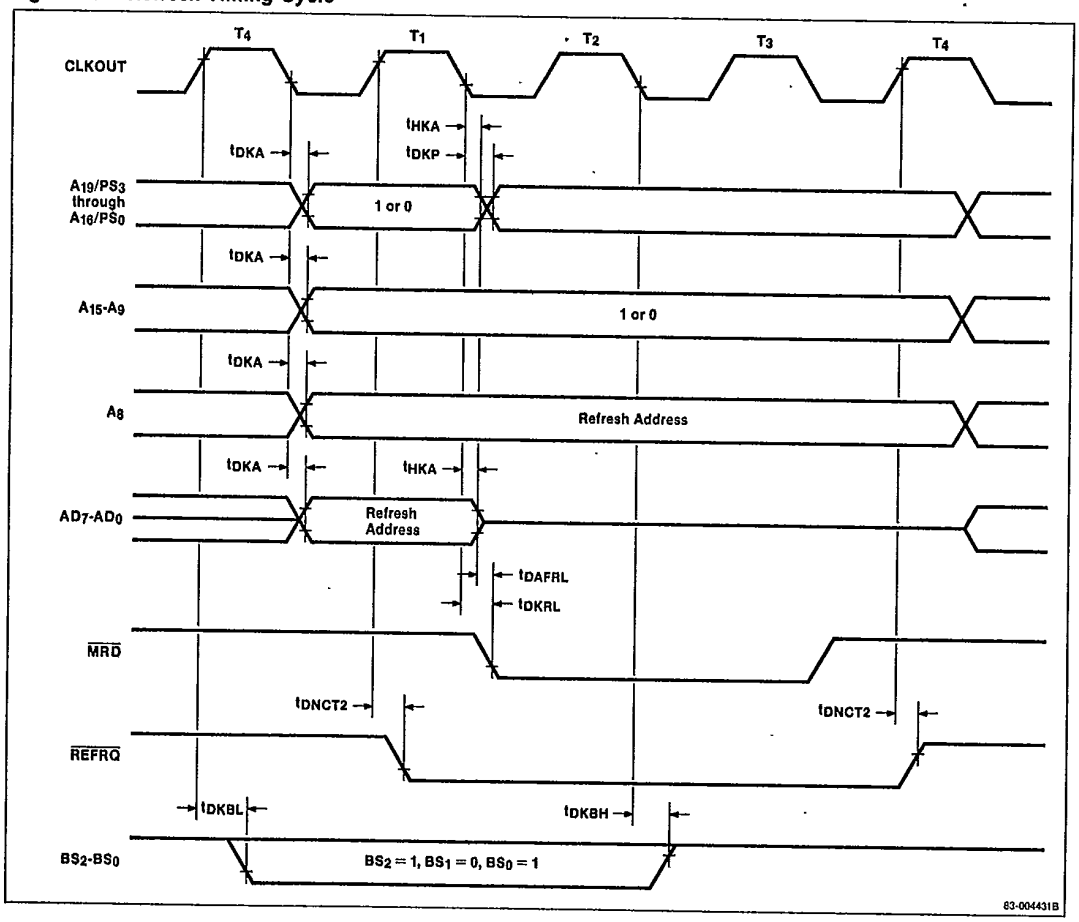


Figure 30. Refresh Timing Cycle



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Dummy Cycles

As explained previously, dummy cycles are required to charge certain internal voltage potentials to proper operating levels in the DRAM's internal circuits after power has been applied.

In the following application example, these dummy cycles are implemented by executing eight write (or read) cycles, from 0000H to 00007H, in the memory.

```
        MOV     AL,0000H
LOOP:   MOV     (BL),0000H
        INC     AL
        CMP     AL,00007H
        JNZ     LOOP
```

Composite Schematic

Figure 32 shows the complete schematic. The V40 and 1M CMOS DRAMs are included, as well as circuits to control timing and refreshing.

Figure 31. Register Programming

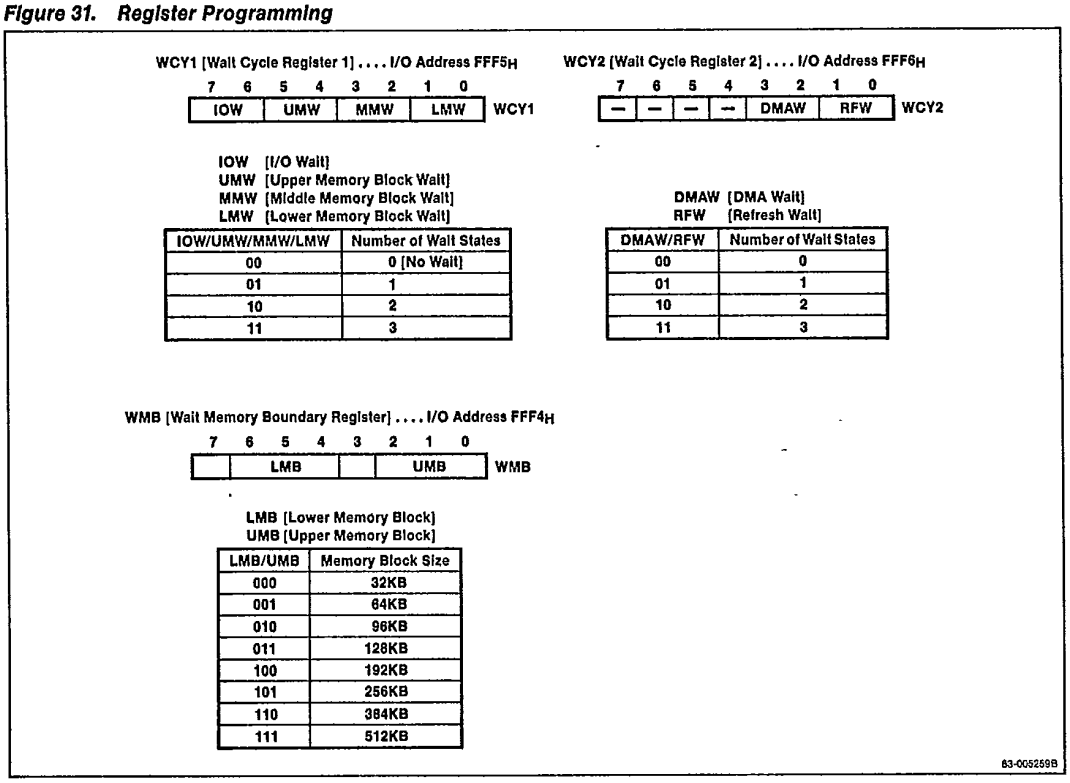
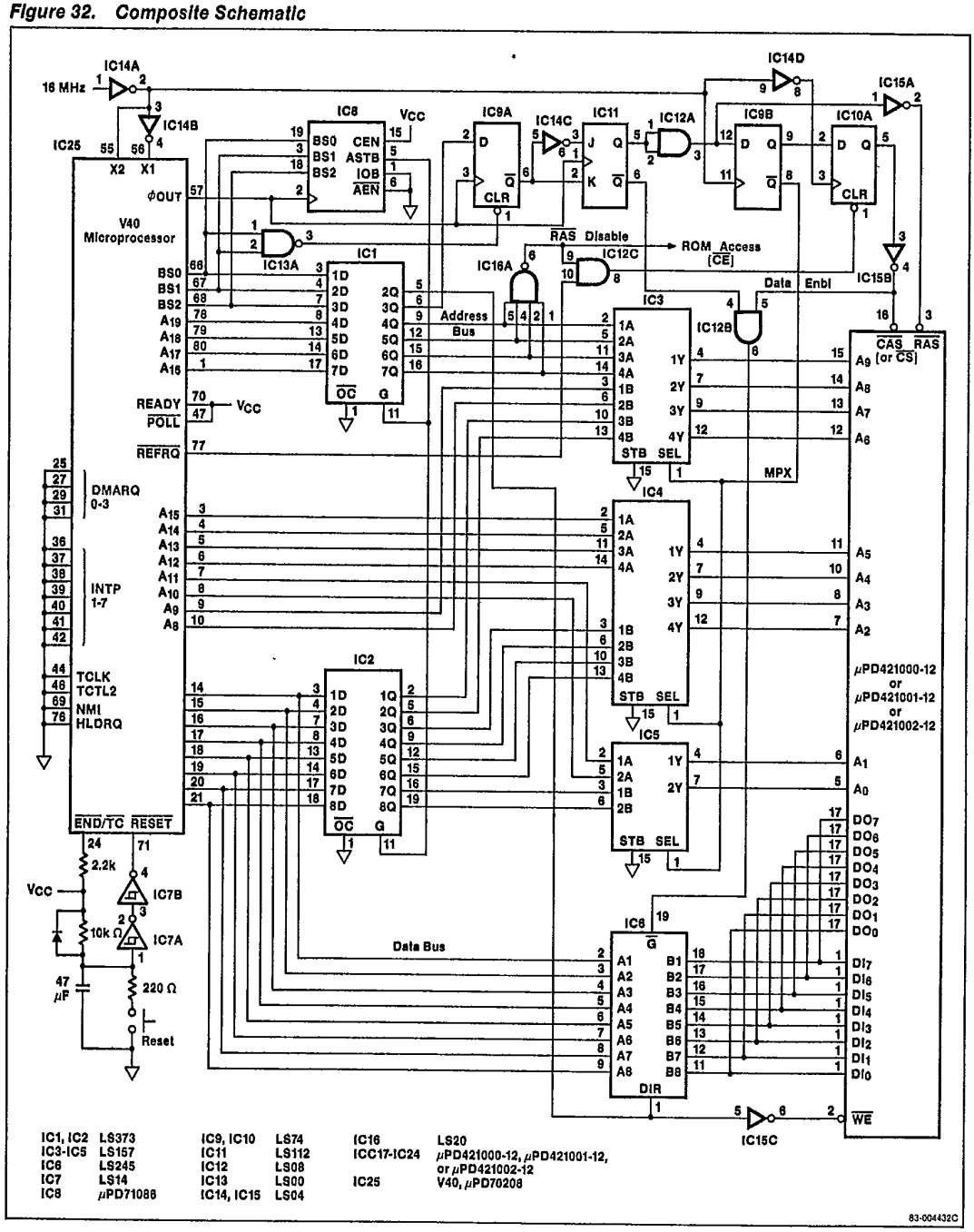


Figure 32. Composite Schematic



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