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FS453/4 and FS455/6
PC to TV Video Scan Converter

FS453/4 and FS455/6
Data Sheet Guides

To make specialized information easier to find, the FS453/4 and FS455/6 Data Sheet is organized into separate reference guides. Each guide addresses a different purpose or user.

☐ The ***FS453/4 and FS455/6 Product Brief*** provides general information for all users.

☐ The ***FS453/4 and FS455/6 Hardware Reference*** is for system designers. It provides information on developing FS453/4 and FS455/6 applications.

☑ **The *FS453/4 and FS455/6 Software/Firmware Reference* is for programmers. It provides information on programming the FS453/4 and FS455/6.**

If you need additional reference guides, contact your Focus Enhancements representative.

Throughout this document "FS453" is used as a general term to reference the FS453, FS454, FS455, and FS456. The FS453 and FS454 are the PQFP versions of the chip, and the FS455 and FS456 are the BGA versions of the chip. The FS454 and FS456 support Macrovision anti-copy protection, while the FS453 and FS455 do not.

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Document Overview

The Software/Firmware Reference provides information necessary for programming the FS453 Video Processor. (For the purpose of this document, the FS453 and the FS454 are identical.) The document has two major parts:

1. **How to Program the FS453** explains two different methods: programming through the Application Programming Interface (API), and programming the device directly using tables. *The programming discussion begins on page 4.*

   Developers who want to write a custom interface to the FS453 can use the API that is provided with the FS453 source code. *Using the Application Programming Interface starts on page 4.*

   Developers who need to program the FS453 in as few steps as possible (BIOS developers for example) can use tables instead. Using tables requires writing register values directly to the FS453 from a table of known values. Developers can simplify the process by using the FS453's built in Quick Program Register to automatically set up the device for a known environment. Then they only need to initialize the Graphics Controller with a complementary set of register values. *Using Tables begins on page 9.*

2. **Control Register Definitions** details all available registers. *This section begins on page 12. The Quick Program Register table is on page 70.*

1. Programming the FS453 Video Processor

1.1 Overview

There are two ways to program the FS453: through the Application Programming Interface (API), and through using tables. Developers who want to write a custom interface to the FS453 can leverage their effort by using the API that comes with the FS453 source code. Developers who need to program the FS453 in as few steps as possible (e.g. BIOS developers), can write register values directly to the device from a table of known values.

1.2 Using the Application Programming Interface

The software support for the FS453 includes source code that organizes device functionality into a set of high-level logical settings and calculates register values necessary for those settings. This manual refers to the source code that maintains state and communicates with the device as the "driver." This selection of source code does not really qualify as a "standalone driver." However, it does include all the functions you will need for your system's video driver. We include a sample test program that incorporates the source code to demonstrate all features of the FS453.

1.2.1 Source File Organization

The FS453 source files are stored in a hierarchical tree. The first level of the tree has a common folder and a folder for each build target. The common folder contains files common to multiple configurations as well as all abstraction-layer files. The build target folders have source files specific to the target as well as necessary project files. For example, the *Windows Prototype Test Application* target includes Microsoft Developer Studio project files and source files to implement a user interface. Multiple projects may be included within a build target folder to support different target hardware platforms.

1.2.2 The FS453 Programming Interface

1.2.2.1 General Design

The programming interface accesses a collection of functions that set various operational parameters of the FS453. All functions that set a parameter have a corresponding “get” function to read back the value set. There are also functions that provide additional information about a particular setting, such as the name of a TV standard in text form, in a format that is suitable for display in a list. These informational functions and “get” functions are not described individually unless they offer some additional functionality.

1.2.2.2 Initialization

Prior to calling any other FS453 functions, the function *FS453_init()* must be called to initialize the driver. If this function returns an error, there is a problem with the FS453 device or the FS453 driver, and programming the FS453 cannot be done.

When a program is finished using the FS453 library, the function *FS453_cleanup()* must be called to disconnect from the FS453 driver.

1.2.2.3 Static Settings

The following settings are static in nature, and generally would only be called while initially configuring the FS453, or when turning TV output on or off.

1.2.2.3.1 TV Standard

The function *FS453_set_tv_standard()* selects the TV standard to use for TV output. Constants are defined for each supported standard and include variants of NTSC and PAL as well as HD modes. The

functions *FS453_get_tv_standard_pixels()* and *FS453_get_tv_standard_lines()* return the active area dimensions for the specified standard.

Since HDTV resolutions are passed through the FS453, the system's GCC needs to be able to support HDTV video before the pass through feature can be used. To provide 1080i, for example, the FS453 must receive the data in that interlaced format. This means that in each 60 Hz field the FS453 needs to receive 540 active lines of 1920 pixels each, as well as appropriate blanking intervals to match the HD HTOTAL of 2200 and the VTOTAL of 1125. In other words, the HACTIVE must be 1920 and the VACTIVE should be 1080. By "interlaced" it means that it takes two fields to deliver all 1125 lines with the dot clock running at 74.25 MHz.

1.2.2.3.2 VGA mode

The function *FS453_set_vga_mode()* selects the VGA mode that the FS453 will assume for VGA input. Constants are defined for each supported VGA mode, including special modes that correspond to HDTV dimensions. The function *FS453_set_yprpb()* selects an input mode where VGA data driven to the part is in the YPrPb color space, rather than RGB. The function *FS453_set_vga_totals()* allows a caller to override the HTOTAL and VTOTAL values calculated by the driver and force external values. Note that overriding VTOTAL sets the vertical scaling ratio, and prevents adjustable scaling using *FS43_set_vga_position().* The function *FS453_get_vga_totals_actual()* returns the actual values of HTOTAL and VTOTAL used in the driver, whether calculated or specified by *FS453_set_vga_totals().*

1.2.2.3.3 Video output mode and DAC control

The function *FS453_set_video_mode()* selects the type of video connection to use, such as Composite, S-video, SCART, or HD YPrPb. The video connection assigned must be compatible with the TV standard selected. The function *FS453_set_dac_signal()* routes a particular video signal to the specified pin. Use this function to accommodate special designs with specific routing requirements, or to drive out multiple copies of Composite or S-video signals.

1.2.2.3.4 TV On and Off

The function *FS453_set_tv_on()* enables or disables TV output. Program the settings for TV standard and VGA screen size before enabling TV output. Disabling TV output powers down most of the device, but does not clear any state information.

1.2.2.4 Dynamic Settings

The following settings are dynamic in nature, and might be exposed through an interface control to allow a user to adjust the setting to suit individual preference.

1.2.2.4.1 Position of VGA video

The function *FS453_set_vga_position()* sets the coordinates within the TV active area that will display the VGA image. Note that horizontal scaling resolution is somewhat coarse; not all coordinates are available. The VGA image will be placed at the closest possible location. The function *FS453_get_vga_position()* will return the same coordinates set. The function *FS453_get_vga_position_actual()* will return the actual settings made, which may differ due to clipping or granularity error.

1.2.2.4.2 Filtering

The functions *FS453_set_flicker_filter()* and *FS453_set_sharpness()* configure the flicker filter settings for the VGA-to-TV conversion. Flicker filtering requires a tradeoff between vertical resolution and visible flicker. A high sharpness setting, for example, will appear to have slightly more flicker than a low one, but fine detail, such as lettering, will be cleaner.

Valid flicker filter settings range from 0 (no filtering, maximum visible flicker) to 16 (maximum filtering, minimum visible flicker). Valid sharpness settings range from 0 (no sharpness enhancement) to 20

(maximum sharpness enhancement). The sharpness adjustment modifies the effect of the flicker filter for short horizontal lines, like those found in text. Sharpness has little effect when the flicker filter setting is low, and maximum effect when the setting is high.

The function *FS453_set_ring_filter()* configures the horizontal luma bandwidth filter. This filter limits or enhances the edge rate on the luma signal, which softens or sharpens vertical lines on the TV. Valid values range from –128 to +127, where negative values enhance edges, and positive values soften edges. In a system without user-adjustable horizontal filtering, a slightly negative value can be used to tune the part for precise frequency response.

The function *FS453_set_yc_filter()* enables or disables luma and chroma filtering for composite video signals (SDTV) in the encoder. Generally, these filters should be off for maximum image quality, but they can improve the displayed image on some televisions without internal filters.

1.2.2.4.3 Encoder Adjustments

The functions *FS453_set_brightness()*, *FS453_set_contrast()*, and *FS453_set_color()* configure brightness, contrast, and saturation values in the output encoder.

1.2.2.4.4 Closed-captioning

The function *FS453_set_cc_enable()* enables or disables closed-captioning. When closed-captioning is enabled, the FS453 drives out the closed-captioning waveform on the proper line, based on the TV standard. The function *FS453_cc_send()* configures the FS453 to place a close-captioning character pair waveform in one field. Parameters to the function control whether the characters are placed in the first field or second field, and whether the function should wait for the next field if this field's data has not yet been sent. To send a sequence of characters, a caller can just loop through the sequence, sending the character pairs with the wait flag set. A better solution is to set the characters for a field in a VGA vertical interrupt handler, without setting the wait flag, to avoid the overhead of polling the FS453.

1.2.2.4.5 Wide-screen Signaling

The function *FS453_set_wss()* selects a wide-screen signaling mode or disables wide-screen signaling. Three modes are supported, 4:3, 4:3 letterbox, and 16:9.

1.2.3 FS453 Driver Design and Implementation

The FS453 driver source code is organized in layers. Higher-level layers implement the basic functionality needed to program the FS453 for any operating system and hardware platform combination. There are sets of interchangeable low-level layers specific to an operating system or hardware platform. One member from each of these sets can be selected to build a driver for a particular target system.

1.2.3.1 Interface Layer

The interface layer is the topmost layer, implemented in *iface.c*. It implements the public functions defined in *FS453.h*. It handles device initialization and maintains the device state.

1.2.3.2 Configuration Layer

The configuration layer, implemented in *config.c*, provides functions that calculate register values for selected device settings. It programs registers through the access layer and fills VGA timing values in a structure maintained by the interface layer.

1.2.3.3 Access Layer

The access layer is split into two levels. The source file *access.c* implements access functions to allow access to device registers. It calls functions in a separate Serial I/O implementation layer in *I2C_Focus.c* to read and write values on the Serial I/O bus. This, in turn, uses the lower level abstraction layer described below to actually set Serial I/O line states. When creating a target design, it's possible to

implement a replacement for the low-level layer or to implement a replacement for the entire Serial I/O block, if Serial I/O transfers are to be handled in a different manner.

1.2.3.4 Low-level Abstraction Layers

The low-level abstraction layers in the FS453 driver allow a code structure that supports reuse of most of the code used in drivers for different platforms and operating systems. There are four low-level abstraction layers. These are the Operating System Abstraction Layer, the Direct Memory Abstraction Layer, the Platform Abstraction Layer, and the Low-level Serial I/O Abstraction Layer.

Functions that must be implemented by a low-level abstraction layer are prototyped in header files named with the abstraction layer abbreviation. Source files that implement an abstraction layer are named with the abstraction layer abbreviation connected by an underscore to a description of the specific target. For example, the Operating System Abstraction Layer header file is *OS.h*, and the Windows user-mode implementation of that layer is *OS_Windows_User.c*.

1.2.3.4.1 Operating System Abstraction Layer

The most basic abstraction layer is the Operating System Abstraction Layer, abbreviated as “OS”. This layer abstracts various OS-specific functions, like memory allocation and delays.

1.2.3.4.2 Direct Memory Abstraction Layer

The Direct Memory Layer, abbreviated as “DM”, abstracts access to physical memory addresses and ports. Specific implementations of this layer generally correspond to operating systems.

1.2.3.4.3 Platform Abstraction Layer

The Platform Abstraction Layer, abbreviated as “PL”, abstracts functionality that is specific to a particular target platform. Normally, this abstraction is made for a specific chipset, or even a specific motherboard. This layer is used only in the FS453 driver. The functions it provides include programming the graphics controller and hardware platform-specific settings for the FS453.

1.2.3.4.4 Low-level Serial I/O Abstraction Layer

The Low-level Serial I/O Abstraction Layer, abbreviated as “LLSIO”, provides functions to set the line state for the clock and data lines as well as to get the line state of the data line. The Serial I/O implementation uses these functions to perform transfers on the Serial I/O bus. This layer is separate from the Platform Abstraction Layer because different implementations of the same platform might connect the Serial I/O lines to different GPIOs, or to an entirely different piece of hardware.

1.2.4 Component Diagram

The following diagram (Figure 1) shows the general hierarchical design of the components of the FS453 user-mode library and kernel-mode driver. Components generally correspond to source files.

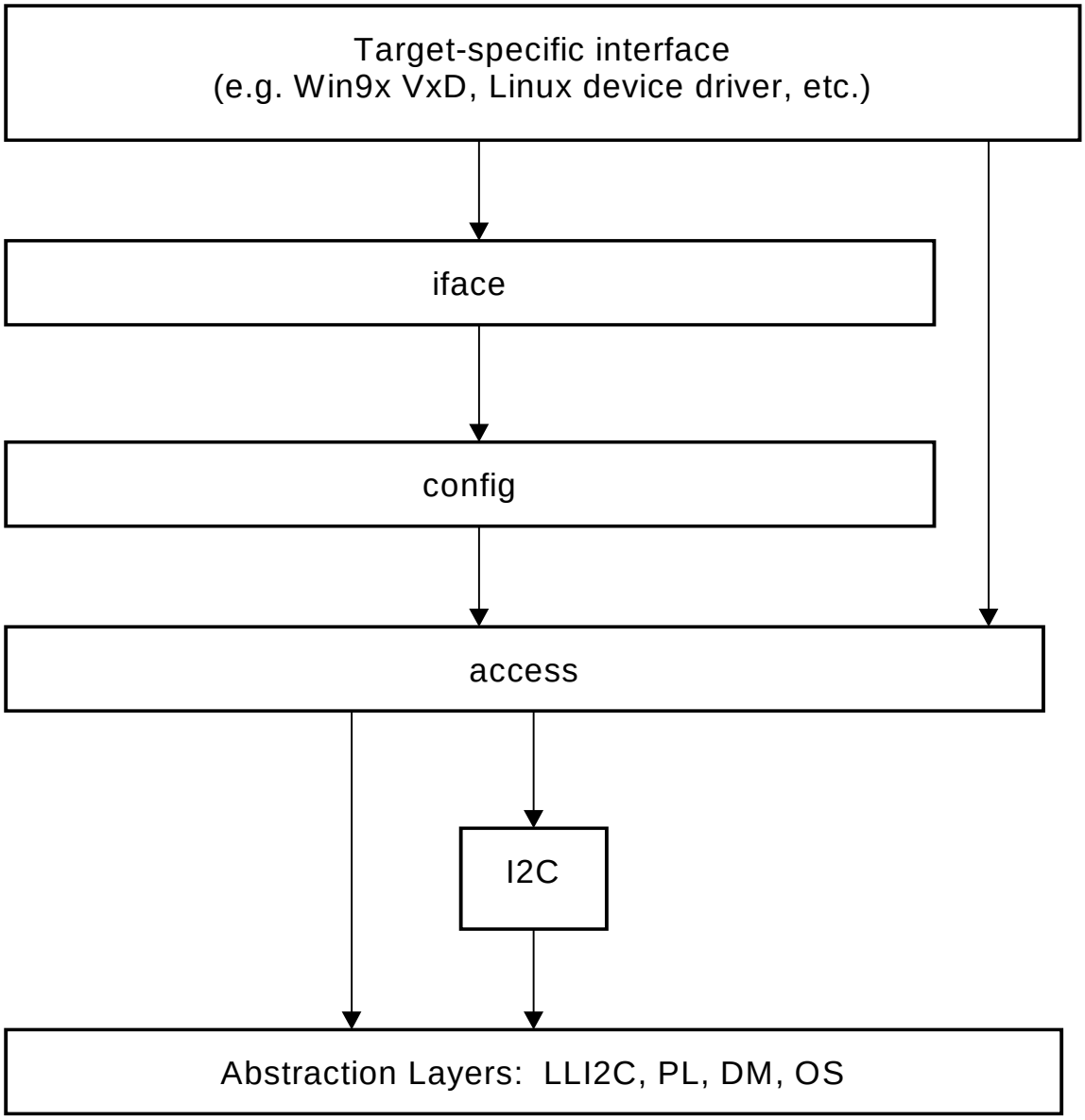

Figure 1: General design of the FS453 driver

1.3 Using Tables

Some applications favor reduced volumes of code to initialize the FS453. Examples include BIOS code, Boot Loaders, and simple test programs that are a small part of a larger test suite. For these applications, the flexibility afforded by a complete driver (written with the FS453 API) can be sacrificed for efficient code. Under such circumstances, it is desirable to program the FS453's registers directly from a static table of default values. There are two ways to approach this tabular code format for the FS453. The first method is to generate a complementary table of FS453 and Graphic Controller registers, and then write a program to initialize the ASICs with those values. The second (and often simpler) method is to use the FS453's built in Quick Program Register to automatically setup the FS453 for a known environment. The programmer then only has to initialize the Graphics Controller with a complementary set of register values.

1.3.1 Creating a Table of FS453 Registers

Descriptions of FS453 registers and their default values are found on page 12.

1.3.2 Using the Quick Program Register (QPR)

The Quick-Program Register (QPR) sets nearly all the registers in the part to known values based on a selected configuration. This greatly simplifies the process of initializing the FS453. The QPR is designed for use in a system where code space or time to program the device is limited. One example would be enabling the TV out during system boot (i.e. BIOS). Another example would be a hardware system that uses a microcontroller to program the FS453.

1.3.2.1 General Design

Using the QPR simultaneously sets multiple registers in the FS453 to a selected predefined mode. Writing to the QPR causes a set of register values to be taken from an on-chip ROM and written into most of the device registers, just as if the values had been programmed normally over the SIO bus. The part is issued a soft-reset, the bridge is resynchronized, and the device is operating in a normal state as soon as the register write to the QPR completes.

The QPR is a 16-bit register. The upper 4-bits are reserved and must be set to the binary value 1001. The lower 12-bits of the register are used to configure the FS453 settings. The Quick Program Register table on page 70 gives a complete description of the bits.

In any given QPR mode, the registers in the graphics controller must be programmed to work with the selected QPR values.

A successful write to the QPR register can be followed immediately by additional serial I/O writes. This allows the programmer to modify registers that are affected by the QPR logic, without worrying about timing constraints. For example, a certain design might require different DAC signal routing, or provide different input sync polarity than expected.

1.3.2.2 Graphics Modes for SDTV

The QPR allows selection from four different VGA modes, two SDTV standards, and overscan or underscan. The 16 combinations of these selections result in different CRTC ("Cathode Ray Tube Controller") settings that must be programmed in the GCC. These settings are controlled by bits 3-0 in the QPR REGISTER on page 70. Table 1 on page 10 lists the required CRTC values for each of the 16 modes.

The QK_PN bits determine whether a PAL or an NTSC video standard is selected.

The QK_GMODE bits determine which VGA mode will be expected. Possible choices are 640 x 480, 720 x 480 (or 720 x 576), 800 x 600, and 1024 x 768. (Which 720 x NNN mode is available depends on the

TV standard selected. NTSC uses a 720 x 480 mode; PAL uses a 720 x 576 mode.) Note that DOS character mode, used on many systems during boot, is usually a 720 pixel mode.

The QK_UO bits select the Scan mode. Underscan reduces the video image in size to fit within the television viewable area. Overscan completely fills the television "active" area. The Underscan mode area is approximately ten to fifteen percent smaller than the corresponding Overscan mode area.

Mode QPR[3-0]	HTOTAL	HACTIVE	HSYNC_Start/ Width	VTOTAL	VACTIVE	VSYNC_Start/ Width
0000	936	640	819/64	525	480	501/2
0001	864	640	783/64	525	480	501/2
0010	936	720	859/64	525	480	501/2
0011	864	720	823/64	625	576	599/2
0100	1008	800	935/64	650	600	624/2
0101	1008	800	935/64	650	600	624/2
0110	1248	1024	1167/64	825	768	795/2
0111	1284	1024	1185/64	825	768	795/2
1000	936	640	819/64	625	480	551/2
1001	864	640	783/64	625	480	551/2
1010	936	720	859/64	625	480	551/2
1011	864	720	823/64	750	576	662/2
1100	1008	800	935/64	775	600	686/2
1101	1008	800	935/64	775	600	686/2
1110	1248	1024	1167/64	1000	768	883/2
1111	1284	1024	1185/64	1000	768	883/2

Table 1: CRTC values for SDTV modes

1.3.2.3 Graphic Modes for HDTV

In addition to its SDTV settings, the QPR allows selection from three different HDTV standards. The QK_OS bits select between SDTV, 480p, 720p, and 1080i modes. When any HDTV standard is selected, the SDTV settings (QK_PN, QK_GMODE, QK_UO, and QK_FF) are ignored or are irrelevant. The HDTV standards have specific requirements for CRTC timing (See Table 2 below).

Bit Register	480p	720p	1080i
HTOTAL	858	1650	2200
VTOTAL	525	750	1125
HACTIVE	720	1280	1920
VACTIVE	480	720	1080
HSYNC_START	738/64	1350/80	1965/88
VSYNC_START	487/7	723/5	1080/10

Table 2: CRTC values for HDTV modes

1.3.2.4 Output Mode

The QPR allows selection from four different output modes. (Not all output modes are valid with all output standards.) The QK_OM bits select from four output modes: S-video with CVBS; Component YPrPb; Component SCART with CVBS; and VGA pass-through. S-video with CVBS is valid with any SDTV mode, and makes both S-video and composite video versions of the output signal available. Component YPrPb is valid for both SDTV and HDTV modes. In SDTV modes, composite video is also available. Component SCART is valid with any SDTV mode, but is most commonly used with PAL. VGA pass-through is not strictly speaking a TV mode. It configures the device to pass the digital input data straight to the DAC, in order to drive a VGA monitor (See Section 1.4 on page 11.)

1.3.2.5 Flicker Filter

The QPR allows selection of two different flicker-filtering modes. The QK_FF bit selects whether flicker filtering is completely disabled, or is set to a relatively high setting useful for text. The “on” setting in the QPR does not set flicker filtering to the maximum possible value.

1.3.2.6 Input Mode

The QPR allows the selection of three different input modes as well as RGB and YCrCb. The three supported input modes are controlled by the QK_IM bits, and pick from NVIDIA, Intel, and National modes. This selection sets the appropriate UIM mode. The QK_YCRCB bit controls whether input data is provided to the device in the YCrCb color space, or the RGB color space.

1.4 VGA Pass-Through

The FS453 supports a DAC-only mode referred to as VGA pass-through. This mode routes the incoming digital RGB video data directly to the DAC, so that the device can be used to directly drive the RGB signals to a monitor. The HSync and VSync signals driven to the monitor must come directly from the graphics controller.

The VGA pass-through mode can be set by writing 9030h to the QPR register.

2. Control Register Definitions

This section organizes and defines the registers for the FS453. Note that the function groups given in Table 3 below are general guidelines.

2.1 Register Reference Table

The General Function labels of the FS453 registers are intended to help design engineers determine which registers will affect specific functions of the FS453.

SDTV Input: Affect settings to the FS453 inputs in SDTV applications.
SDTV Output: Affect FS453 SDTV output settings.
HDTV Output: Affect FS453 HDTV output settings.
Control: Affect FS453 control parameters.
Clock: Affect FS453 clock settings.
Color Matrix: Affect the FS453's input color conversion matrices.
QPR: Are the Quick Program Registers (For rapid programming of the entire FS453).

General Function	Name	Offset	Default Value	Page Number
SDTV Input	IHO	00h	0000h	15
SDTV Input	IVO	02h	0000h	15
SDTV Input	IHW	04h	02D0h	16
SDTV Input	VSC	06h	0000h	16
SDTV Input	HSC	08h	0000h	16
Control	BYPASS	0Ah	0000h	17
Control	CR	0Ch	0003h	18
Control	MISC	0Eh	8000h	20
Clock	NCON	10h	00020000h	25
Clock	NCOD	14h	00020000h	25
Clock	PLL M AND PUMP CONTROL	18h	0409h	26
Clock	PLL N	1Ah	00AEh	27
Clock	PLL POST-DIVIDER	1Ch	0505h	28
SDTV Input	SHP	24h	0000h	32
SDTV Input	FLK	26h	0000h	32
Control	GPIO	28h	0000h	33
Control	ID	32h	FE05h	34
Control	STATUS PORT	34h	0008h	34
Control	FIFO_SP	36h	0000h	35
SDTV Input	FIFO_LAT	38h	0512h	35
SDTV Output	CHR_FREQ	40h	1F7CF021h	36
SDTV Output	CHR_PHASE	44h	00h	36
SDTV Output	MISC_45	45h	00h	37

General Function	Name	Offset	Default Value	Page Number
SDTV Output	MISC_46	46h	09h	37
SDTV Output	MISC_47	47h	00h	38
SDTV Output	HSYNC_WID	48h	7Eh	38
SDTV Output	BURST_WID	49h	44h	39
SDTV Output	BPORCH	4Ah	76h	39
SDTV Output	CB_BURST	4Bh	3Bh	39
SDTV Output	CR_BURST	4Ch	00h	40
SDTV Output	MISC_4D	4Dh	00h	40
SDTV Output	BLACK_LVL	4Eh	0246h	40
SDTV Output	BLANK_LVL	50h	003Ch	41
SDTV Output	NUM_LINES	57h	0183h	41
SDTV Output	WHITE_LVL	5Eh	00C8h	42
SDTV Output	CB_GAIN	60h	89h	42
SDTV Output	CR_GAIN	62h	89h	42
SDTV Output	TINT	65h	00h	43
SDTV Output	BR_WAY	69h	16h	43
SDTV Output	FR_PORCH	6Ch	20h	43
SDTV Output	NUM_PIXELS	71h	00B4h	44
SDTV Output	1ST_LINE	73h	15h	44
SDTV Output	MISC_74	74h	02h	45
SDTV Output	SYNC_LVL	75h	48h	46
SDTV Output	VBI_BL_LVL	7Ch	004Ah	46
SDTV Output	SOFT_RST	7Eh	00h	46
SDTV Output	ENC_VER	7Fh	20h	47
SDTV Output	WSS_CONFIG	80h	07h	47
SDTV Output	WSS_CLK	81h	0072h	48
SDTV Output	WSS_DATAF1	83h	000000h	48
SDTV Output	WSS_DATAF0	86h	000000h	49
SDTV Output	WSS_LNF1	89h	00h	49
SDTV Output	WSS_LNF0	8Ah	00h	50
SDTV Output	WSS_LVL	8Bh	03FFh	50
SDTV Output	MISC_8D	8Dh	00h	51
Control	VID_CNTL0	92h	0000h	53
HDTV Output	HD_FP_SYNC	94h	0000h	55
HDTV Output	HD_YOFF_BP	96h	0000h	55
HDTV Output	SYNC_DL	98h	0000h	56
Control	LD_DET	9Ch	0000h	57

General Function	Name	Offset	Default Value	Page Number
Control	DAC_CNTL	9Eh	0000h	59
Control	PWR_MGNT	A0h	000Fh	60
Color Matrix	RED_MTX	A2h	0000h	61
Color Matrix	GRN_MTX	A4h	0000h	61
Color Matrix	BLU_MTX	A6h	0000h	61
Color Matrix	RED_SCL	A8h	0000h	62
Color Matrix	GRN_SCL	AAh	0000h	62
Color Matrix	BLU_SCL	ACh	0000h	62
SDTV Output	CLOSED CAPTION FIELD 1	AEh	0000h	63
SDTV Output	CLOSED CAPTION FIELD 2	B0h	0000h	64
SDTV Output	CLOSED CAPTION CONTROL	B2h	0000h	64
SDTV Output	CLOSED CAPTION BLANKING VALUE	B4h	0000h	65
SDTV Output	CLOSED CAPTION BLANKING SAMPLE	B6h	0000h	65
HDTV Output	HACT_ST	B8h	0000h	66
HDTV Output	HACT_WD	BAh	0000h	66
HDTV Output	VACT_ST	BCh	0000h	67
HDTV Output	VACT_HT	BEh	0000h	67
SDTV Output	PR AND PB RELATIVE SCALING	C0h	0000h	68
SDTV Output	LUMA BANDWIDTH	C2h	0000h	69
QPR	QUICK PROGRAM REGISTER	C4h	8000h	70

Table 3: Register Reference Table

2.2 Register Definitions

All FS453/4 and FS455/6 registers are addressed as SIO registers. In the following register definitions, range is defined as: {[min value] : [max value]}. Registers are listed in the order of their addresses. The Attribute field in the register description can be R for Read-only registers or R/W for Read/Write registers.

2.2.1.1 IHO - Input Horizontal Offset

Address Offset 00h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					IHO										

Bits	Name	Description
15-11	Reserved	
10-0	IHO	**Input horizontal offset.** Horizontal displacement of the graphics converter image in pixels from the leading edge of horizontal sync. IHO is an unsigned number.

Range: {0d : [Total Pixels/Line]-1d}

2.2.1.2 IVO - Input Vertical Offset

Address Offset 02h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					IVO										

Bits	Name	Description
15-11	Reserved	
10-0	IVO	**Input vertical offset.** Vertical displacement of the graphics converter image in lines from the leading edge of vertical sync minus a one line bias. IVO is an unsigned number.

Range: {0d : [Total Lines/Frame]-1d}

2.2.1.3 IHW - Input Horizontal Width

Address Offset 04h
Default Value 02D0h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						IHW									

Bits	Name	Description
15-10	Reserved	
9-0	IHW	**Input horizontal width.** Total number of active VGA pixels per line. IHW is an unsigned number. IHW must be even.

Range: {0d : 970d}

2.2.1.4 VSC – Vertical Scaling Coefficient

Address Offset 06h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSC															

Bits	Name	Description
15-0	VSC	**Vertical scaling coefficient.** Vertical up and down scaling factor = (1 + VSC/65,536). VSC is a two's complement number. If VSC = 0, then the image is not scaled vertically.

Range: { [-32,768d] : 32,767d}

2.2.1.5 HSC – Horizontal Down/Up Scaling Coefficients

Address Offset 08h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HUSC								HDSC							

Bits	Name	Description
15-8	HUSC	**Horizontal up scaling coefficient.** Horizontal up scaling factor = (1 + HUSC/128). HUSC is a two's complement number. If HUSC = 0, then the image is not affected.
7-0	HDSC	**Horizontal down scaling coefficient.** Horizontal down scaling factor = (1 + HDSC/128). HDSC is a two's complement number. If HDSC = 0, then the image is not affected.

HDSC Range: { [-63d] : 0d }

HUSC Range: { 0d : 127d }

2.2.1.6 BYPASS

Address Offset 0Ah
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											B_BYPASS	CAC_BYPASS	Reserved	HDS_BYPASS	Reserved

Bits	Name	Description
15-5	Reserved	**Reserved**: Set to 0.
4	B_BYPASS	**Bridge Bypass.** Set to 1 for HD modes.
3	CAC_BYPASS	**CAC Bypass.** Set to 1 when not using horizontal down scaler.
2	Reserved	**Reserved**: Set to 0.
1	HDS_BYPASS	**HDS Bypass.** Set to 1 when not using horizontal down scaler.
0	Reserved	**Reserved**: Set to 0.

2.2.1.7 CR - Command Register

Address Offset 0Ch
Default Value 0003h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	GCC_CK_LVL	P656_LVL	Reserved	P656_OUT	CBAR_480P	PAL_NTSCIN	SYNC_MS	FIFO_CLR	CACQ_CLR	CDEC_BP	Reserved		NCO_EN	SRESET

Bits	Name	Description
15	Reserved	
15	Reserved	**Reserved.** Must be set to 0.
13	GCC_CK_LVL	**Graphics Controller Clock Switching Level.** If = 1, the GCC clock output switching level is Low Voltage (1.5V to 3.3V) signaling determined by pin 57. If = 0, it is open-drain GTL signaling.
12	P656_LVL	**Pixel Port ITU-R BT.656 Output Switching Level.** If = 1, the ITU-R BT.656 port output switching level is LVTTL (3.3V). If = 0, it is open-drain GTL signaling.
11	P656_IN	**Pixel Port ITU-R BT.656 In.** Enables an auxiliary ITU-R 656 input port when = 1. See note below for restrictions on this bit.
10	P656_OUT	**Pixel Port ITU-R BT.656 Out.** Enables an auxiliary ITU-R 656 port when = 1. See note below for restrictions on this bit.
9	CBAR_480P	**480P Color Bars.** When = 1, it enables the high definition 480P color bar test pattern generator.
8	PAL_NTSCIN	**ITU-R BT.656 PAL or NTSC Input.** Sets the number of lines written through the FIFO. When = 1, there are 576 lines for PAL. When =0, there are 487 lines for NTSC.
7	SYNC_MS	**Sync Master or Slave.** When = 1, FS453 outputs HSync and VSync to the GCC. When = 0, syncs are accepted from the GCC.
6	FIFO_CLR	**FIFO Clear.** Setting this bit to 1 clears the FIFO depth registers and the FIFO State register. The bit must remain set to 1 for at least one field to ensure state is cleared.
5	CACQ_CLR	**CACQ Clear.** Setting this bit to 1 clears the CACQ status flag in register 34h (STATUS PORT).
4	CDEC_BP	**Chroma Decimator Bypass.** Set to 0.
2-3	Reserved	
1	NCO_EN	**Enable NCO Latch.** When this bit is set, it transfers the NCO and PLL words from the Serial I/O registers into the NCO and PLL. This ensures all parameters take effect simultaneously. (The PLL Post-divider register is not latched by this bit; post-divider values take effect immediately.) See note.
0	SRESET	**Soft Reset.** Resets the FS453. Register settings are preserved and all state machines are reset. While SRESET is high (= 1), DAC outputs are blanked.

Note:

NCO_EN: The NCO_EN bit has no effect if internal device clocks are disabled for power-down mode. In the PWR_MGNT register (A0h) bit 11 (CLKOFF) must be set to 0 for the NCO_EN bit to latch the PLL and NCO settings.

Video port guidelines:

The FS453's video port is only available when the Graphics input mode does not use the upper 12 bits of the pixel port (P_{12}-P_{23}). Port connections are shown in Table 4 below. P656_IN and P656_OUT cannot both be set to 1.

P Port	Signal	FBGA Pin Number	PQFP Pin Number	I/O	Signal Description	
					Input (P656_IN=1)	Output (P656_OUT=1)
P23	V601_F	M9	34	X/O	No Connect	CCIR 656 FREF (field reference)
P22	V601_V	N8	33	O	CCIR 656 VREF (vertical reference)	
P21	V601_H	M8	32	O	CCIR 656 HREF (horizontal reference)	
P20	X	N6	29	O/X	Pixel Qualifier *	No Connect
P19	V656_7	M6	28	I/O	Bit 7 of the video port	
P18	V656_6	N5	27	I/O	Bit 6 of the video port	
P17	V656_5	M5	26	I/O	Bit 5 of the video port	
P16	V656_4	N4	25	I/O	Bit 4 of the video port	
P15	V656_3	M4	24	I/O	Bit 3 of the video port	
P14	V656_2	N3	23	I/O	Bit 2 of the video port	
P13	V656_1	L1	18	I/O	Bit 1 of the video port	
P12	V656_0	K2	17	I/O	Bit 0 of the video port	
XTAL_IN	CLK	B10	63	O**	27 MHz reference clock	

* The Pixel Qualifier selects between video and graphics data

Table 4: Pixel Port (P Port) ITU-R BT.656 Connections

Video port guidelines:
P19 through P12 are inputs and P23 is disabled when P656_IN is set to 1.
P19 through P12 are outputs and P20 is disabled when P656_OUT is set to 1.

ITU-R BT.656 data streams require a 27 MHz clock. In FS453 designs that utilize the optional ITU-R BT.656 video port, the video port's 27 MHz clock must be derived from the FS453's 27 MHz reference clock. It is never a good idea to share a single, un-buffered, clock signal with multiple devices. **Designs that rely on the FS453's video port should use a clock source that provides multiple buffered copies of a 27 MHz reference clock signal.

The first output from the clock buffer must be connected to the FS453's pin 63 (XTAL_IN). A second output from the clock buffer must to be connected to the ITU-R BT.656 companion chip in the design. When the FS453's video port is configured as an input, the second reference clock must drive the ITU-R BT.656 video source (in effect slaving it to the FS453). When the FS453's video port is configured as an output, the second reference source must be routed with the ITU-R BT.656 output data to the target device.

Note that the 27 MHz clock does not follow the same electrical path as the ITU-R BT.656 data. The 27 MHz clock connects directly between the clock buffer and the ITU-R BT.656 companion chip, while the ITU-R BT.656 data is processed by a video ASIC; the ITU-R BT.656 video source when the port is an input and the FS453 when the port is an output. This means that there will be an unknown phase delay between the 27 MHz clock and the ITU-R BT.656 data. The total delay between the 27 MHz clock and the ITU-R BT.656 data is not critical, but the relative phase delay between the two is critical. One must ensure that the setup and hold time requirements of the FS453's Digital Pixel Input Port are met if the video port is configured as an input. If the video port is configured as an output, the setup and hold time requirements of the target ITU-R BT.656 device must be met. If the setup and hold time requirements are not met, the length of the ITU-R BT.656 27 MHz clock trace (the second output from the clock buffer) should be changed.

2.2.1.8 MISC - Miscellaneous Bits Register

Address Offset 0Eh
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				P_ORDER	BRDG_RST	UIM_E	UV_SWAP	UIM_DEC	Reserved	UIM_CCLK	UIM_DCLK	UIM_MOD			

Bits	Name	Description
12-15	Reserved	
11	P_ORDER	**Pixel Order 48 bit mode.** Setting this bit to 1 swaps the input pixel order in 48 bit modes (UIM modes 11 and 12).
10	BRDG_RST	**Bridge Pointer Reset.** Setting this bit to 1 enables a pointer reset of the input VGA clock bridge FIFO for seven VSyncs. A low to high transition on this bit immediately resets the pointers.
9	UIM_E	**UIM Control/Data Eye.** In multiplexed modes, set this bit to 1 if the control lines change state in the middle of a pixel (between the first and second data words.) Set this bit to 0 if the control lines change state at the edge of a pixel. In non-multiplexed modes, set this bit to 0.
8	UV_SWAP	**Chroma U and V Swap.** When set to 1, swaps the Cr (V) and Cb (U) internal input signals. Normally set to 0.
7	UIM_DEC	**Universal Input Mux Decimator.** Setting this bit to 1 turns on the horizontal prescaler divide by 2 to support high resolution VGA mode.
6	Reserved	**Note:** Must be set to 0.
5	UIM_CCLK	**Universal Input Mux Control Clock Mode.** Setting this bit to 1 inverts the edge on which input control is latched. See Table 5 on page 21 for mapping information.
4	UIM_DCLK	**Universal Input Mux Data Clock Mode.** Setting this bit to 1 inverts the edge on which input data is latched. See Table 5 on page 21 for mapping information.
0-3	UIM_MOD	**Universal Input Mode Select.** Selects the VGA interface mode (see Table 5 through Table 8 on the following pages).

2.2.1.9 Miscellaneous Bits Register Tables

The following tables supply information for setting the Miscellaneous Bits Register.

UIM_MOD Mapping: The UIM_MOD (Universal Input Mux, UIM) bits select the mode for P0-P23. The intention is to support as many different 3D and GCC graphic controllers, CPU support chips, and integrated CPUs as possible (collectively referred to in this data sheet as "GCC"). Table 5 shows the mapping in each mode for the digital RGB from the GCC to the appropriate port or extended port pin:

UIM_MOD	0		1		1		2		3	3	3
P Port	M888D		M888I		M565I		M555		N888	N666	N565
	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH			
P23	X	X	X	X	X	X	X	X	R7	R5	R4
P22	X	X	X	X	X	X	X	X	R6	R4	R3
P21	X	X	X	X	X	X	X	X	R5	R3	R2
P20	X	X	X	X	X	X	X	X	R4	R2	R1
P19	X	X	X	X	X	X	X	X	R3	R1	R0
P18	X	X	X	X	X	X	X	X	R2	R0	0
P17	X	X	X	X	X	X	X	X	R1	0	0
P16	X	X	X	X	X	X	X	X	R0	0	0
P15	X	X	X	X	X	X	X	X	G7	G5	G5
P14	X	X	X	X	X	X	X	X	G6	G4	G4
P13	X	X	X	X	X	X	X	X	G5	G3	G3
P12	X	X	X	X	X	X	X	X	G4	G2	G2
P11	G3	R7	G4	R7	G2	R4	G2	X	G3	G1	G1
P10	G2	R6	G3	R6	G1	R3	G1	R4	G2	G0	G0
P9	G1	R5	G2	R5	G0	R2	G0	R3	G1	0	0
P8	G0	R4	B7	R4	B4	R1	B4	R2	G0	0	0
P7	B7	R3	B6	R3	B3	R0	B3	R1	B7	B5	B4
P6	B6	R2	B5	G7	B2	G5	B2	R0	B6	B4	B3
P5	B5	R1	B4	G6	B1	G4	B1	G4	B5	B3	B2
P4	B4	R0	B3	G5	B0	G3	B0	G3	B4	B2	B1
P3	B3	G7	G0	R2	0	0	X	X	B3	B1	B0
P2	B2	G6	B2	R1	0	0	X	X	B2	B0	0
P1	B1	G5	B1	R0	0	0	X	X	B1	0	0
P0	B0	G4	B0	G1	0	0	X	X	B0	0	0

Table 5: GCC RGB Port Mapping Modes

Notes:

1) Shaded modes require padding with zeroes at input port.
2) All input bits are MSB justified.
3) See Table 8: Input Port Clocking, on page 24, for a definition of LOW and HIGH words.

Table 6 provides YCrCb Port Mapping Modes for the system's graphic controller chip (GCC).

UIM_MOD	4		5		6		7		8	9	10
P Port	M444C		M444T1		M565T2		M422		N656	N601	N444
	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH			
P23	X	X	X	X	X	X	X	X	X	X	Cb7
P22	X	X	X	X	X	X	X	X	X	X	Cb6
P21	X	X	X	X	X	X	X	X	X	X	Cb5
P20	X	X	X	X	X	X	X	X	X	X	Cb4
P19	X	X	X	X	X	X	X	X	X	X	Cb3
P18	X	X	X	X	X	X	X	X	X	X	Cb2
P17	X	X	X	X	X	X	X	X	X	X	Cb1
P16	X	X	X	X	X	X	X	X	X	X	Cb0
P15	X	X	X	X	X	X	X	X	X	C7	Cr7
P14	X	X	X	X	X	X	X	X	X	C6	Cr6
P13	X	X	X	X	X	X	X	X	X	C5	Cr5
P12	X	X	X	X	X	X	X	X	X	C4	Cr4
P11	Cr7	Y7	Y3	Cr7	Y4	Cr7	C7	Y7	YC7	C3	Cr3
P10	Cr6	Y6	Y2	Cr6	Y3	Cr6	C6	Y6	YC6	C2	Cr2
P9	Cr5	Y5	Y1	Cr5	Y2	Cr5	C5	Y5	YC5	C1	Cr1
P8	Cr4	Y4	Y0	Cr4	Cb7	Cr4	C4	Y4	YC4	C0	Cr0
P7	Cr3	Y3	Cb7	Cr3	Cb6	Cr3	C3	Y3	YC3	Y7	Y7
P6	Cr2	Y2	Cb6	Cr2	Cb5	Y7	C2	Y2	YC2	Y6	Y6
P5	Cr1	Y1	Cb5	Cr1	Cb4	Y6	C1	Y1	YC1	Y5	Y5
P4	Cr0	Y0	Cb4	Cr0	Cb3	Y5	C0	Y0	YC0	Y4	Y4
P3	Cb7	Cb3	Cb3	Y7	Y0	Cr2	X	X	X	Y3	Y3
P2	Cb6	Cb2	Cb2	Y6	Cb2	Cr1	X	X	X	Y2	Y2
P1	Cb5	Cb1	Cb1	Y5	Cb1	Cr0	X	X	X	Y1	Y1
P0	Cb4	Cb0	Cb0	Y4	Cb0	Y1	X	X	X	Y0	Y0

Table 6: GCC YCrCb Port Mapping Modes

Notes:

1) All input bits are MSB justified.
2) For GCC to P/E Mapping, see Table 5 on page 21.
3) See Table 8: Input Port Clocking, on page 24, for a definition of LOW and HIGH words.

Table 7 provides 48 Bit Port Mapping Modes for the system's graphic controller chip (GCC).

UIM_MOD	11		12	
P Port	Multiplexed High/Low		Multiplexed Even/Odd	
	LOW	HIGH	LOW	HIGH
P23	G3(even)	G3(odd)	G3(even)	R7(even)
P22	G2(even)	G2(odd)	G2(even)	R6(even)
P21	G1(even)	G1(odd)	G1(even)	R5(even)
P20	G0(even)	G0(odd)	G0(even)	R4(even)
P19	B7(even)	B7(odd)	B7(even)	R3(even)
P18	B6(even)	B6(odd)	B6(even)	R2(even)
P17	B5(even)	B5(odd)	B5(even)	R1(even)
P16	B4(even)	B4(odd)	B4(even)	R0(even)
P15	B3(even)	B3(odd)	B3(even)	G7(even)
P14	B2(even)	B2(odd)	B2(even)	G6(even)
P13	B1(even)	B1(odd)	B1(even)	G5(even)
P12	B0(even)	B0(odd)	B0(even)	G4(even)
P11	R7(even)	R7(odd)	G3(odd)	R7(odd)
P10	R6(even)	R6(odd)	G2(odd)	R6(odd)
P9	R5(even)	R5(odd)	G1(odd)	R5(odd)
P8	R4(even)	R4(odd)	G0(odd)	R4(odd)
P7	R3(even)	R3(odd)	B7(odd)	R3(odd)
P6	R2(even)	R2(odd)	B6(odd)	R2(odd)
P5	R1(even)	R1(odd)	B5(odd)	R1(odd)
P4	R0(even)	R0(odd)	B4(odd)	R0(odd)
P3	G7(even)	G7(odd)	B3(odd)	G7(odd)
P2	G6(even)	G6(odd)	B2(odd)	G6(odd)
P1	G5(even)	G5(odd)	B1(odd)	G5(odd)
P0	G4(even)	G4(odd)	B0(odd)	G4(odd)

Table 7: GCC 48 Bit Port Mapping Modes

Notes:

1) All input bits are MSB justified.
2) For GCC to P/E Mapping, see Table 5 on page 21.
3) See Table 8: Input Port Clocking, on page 24, for a definition of LOW and HIGH words.
4) See Table 9: UIM_MOD values for Typical Graphic Controller Chips, on page 24.

If the mode and clock bits are set to the specified values, then the input clocks will be sampled as follows.

Mode	UIM_CCLK	UIM_DCLK	Control	LOW	HIGH
Non-Mux	High	High	↓ CLKIN_P	↑ CLKIN_P	↑ CLKIN_P
Non-Mux	Low	High	↑ CLKIN_P	↑ CLKIN_P	↑ CLKIN_P
Non-Mux	High	Low	↑ CLKIN_P	↓ CLKIN_P	↓ CLKIN_P
Non-Mux	Low	Low	↓ CLKIN_P	↓ CLKIN_P	↓ CLKIN_P
Mux	High	High	↓ CLKIN_P	↑ CLKIN_P	↓ CLKIN_P
Mux	Low	High	↑ CLKIN_P	↑ CLKIN_P	↓ CLKIN_P
Mux	High	Low	↑ CLKIN_P	↓ CLKIN_P	↑ CLKIN_P
Mux	Low	Low	↓ CLKIN_P	↓ CLKIN_P	↑ CLKIN_P

Table 8: Input Port Clocking

Note:

↓ CLKIN_P means that the item is sampled on the falling edge of CLKIN_P. ↑ CLKIN_P means that the item is sampled on the rising edge of CLKIN_P.

Typical GCCs	UIM_MOD
Intel	0
NVIDIA	1
National	3

Table 9: UIM_MOD values for Typical Graphic Controller Chips

Note:

For Intel designs, use the following guideline for setting UIM_DCLK and UIM_CCLK:

If RGBA_CLKOUT0 is connected to CLKIN_P and RGBA_CLKOUT1 is connected to CLKIN_N, then UIM_DCLK=0 and UIM_CCLK=1.

If RGBA_CLKOUT1 is connected to CLKIN_P and RGBA_CLKOUT0 is connected to CLKIN_N, then UIM_DCLK=1 and UIM_CCLK=0.

2.2.1.10 NCON - Numerator of NCO Word

Address Offset 10h
Default Value 00020000h
Attribute R/W
Size 32 Bits

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							NCON																								

Bits	Name	Description
31-25	Reserved	
24-0	NCON	**Numerator of NCO Word.** Numerator of clock synthesizer used to generate the pixel input clock to the graphics converter. NCON is a 24 bit unsigned number.

Range: {0d : NCOD/2}

Note:
For a complete description on how to configure the NCON, NCOD, PLL M, PLL N, PLL_EP and PLL_IP registers, please see the note that follows 1Ch, the PLL Post-Divider register description on page 29.

2.2.1.11 NCOD - Denominator of NCO Word

Address Offset 14h
Default Value 00020000h
Attribute R/W
Size 32 Bits

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							NCOD																								

Bits	Name	Description
31-25	Reserved	
24-0	NCOD	**Denominator of NCO Word**. Denominator of clock synthesizer used to generate the pixel input clock to the graphics converter. NCOD is a 24 bit unsigned number.

Range: {NCON*2d : (2^{24}-1)d}

Note:
For a complete description on how to configure the NCON, NCOD, PLL M, PLL N, PLL_EP and PLL_IP registers, please see the note that follows 1Ch, the PLL Post-Divider register description on page 29.

2.2.1.12 PLL M and Pump Control

Address Offset 18h
Default Value 0409h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	PLLG			PLLM											

Bits	Name	Description
15	Reserved	
14-12	PLLG	**PLL Charge Pump Gain.** The PLL Charge Pump gain is changed depending on input reference and output PLL frequency. See Table 10 below.
11-0	PLLM	**PLL M Divider.** The PLL M divider multiplies the incoming reference frequency by M. PLLM is programmed as (M-17). M has a range of 250 to 3000.

Note:
For a complete description on how to configure the NCON, NCOD, PLL M, PLL N, PLL_EP and PLL_IP registers, please see the note that follows 1Ch, the PLL Post-Divider register description on page 29.

PLL Output Frequency	PLL Input Reference Frequency			
	100 kHz	300 kHz	500 kHz	1 MHz
100 MHz	1	2	X	X
150 MHz	2	3	2	X
200 MHz	3	4	3	X
250 MHz	4	5	4	3
300 MHz	5	6	5	4

Table 10: Suggested PLLG Settings

2.2.1.13 PLL N

Address Offset 1Ah
Default Value 00AEh
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							PLLN								

Bits	Name	Description
15-9	Reserved	
8-0	PLLN	**PLL N Divider.** The PLL N divider divides the incoming reference (or NCO output if NCO is used) by N. PLLN is programmed as (N-1).

Note:
For a complete description on how to configure the NCON, NCOD, PLL M, PLL N, PLL_EP and PLL_IP registers, please see the note that follows 1Ch, the PLL Post-Divider register description on page 29.

2.2.1.14 PLL Post-Divider

Address Offset 1Ch
Default Value 0505h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	PLL_EP							Reserved	PLL_IP						

Bits	Name	Description
15	Reserved	
14-8	PLL_EP	**PLL External Post-Divider.** The PLL External Divider divides the PLL Output Clock by EP before it is output at the GCC Clock pin. PLL_EP is programmed as (EP-1). EP is from 1 to 128. Even divisors produce a 50% duty cycle and odd divisors produce a duty cycle that is approximately 50% (within one PLL VCO clock cycle).
7	Reserved	
6-0	PLL_IP	**PLL Internal Post-Divider.** The PLL Internal Divider divides the PLL Output Clock by IP. IP is from 1 to 128. PLL_IP is programmed as (IP-1).

Notes:
Normally the internal and external Post-Dividers are equal, but can be offset for use in systems where the GCC clock is manipulated in frequency before it is returned to the FS453.

For a complete description on how to configure the NCON, NCOD, PLL M, PLL N, PLL_EP and PLL_IP registers, please see the extended note on page 29.

2.2.1.15 Notes for NCON, NCOD, PLL M, PLL N, PLL_EP and PLL_IP Registers:

The FS453 synthesizes a 0.78125-150 MHz clock from the 27 MHz XTAL_IN and supplies this clock (CLKOUT) to the GCC. The clock is buffered and returned to the FS453 (CLKIN_P) synchronous to the pixel data and sync information. This clock has a 1.5 Hz resolution and can be adjusted so that the VGA scaled input data rate exactly matches the ITU-R BT.656 output data rate.

The FS453 clock generation circuit operates in one of two modes, NCO mode or PLL mode. In NCO mode, the numerically controlled oscillator is used to achieve the finest clock resolution, using a dithered clock. In PLL mode, the NCO is bypassed and the clock is not dithered.

The NCON, NCOD, PLL M, PLL N registers are latched when the NCO_GN bit in Register CR (0Ch) on page 18 is set =1.

Output clock frequency calculation and limits, in the order handled by the clock generation circuit:

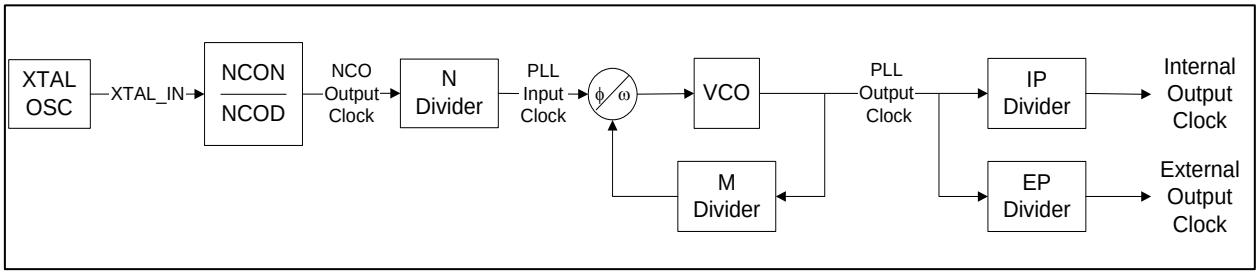

Figure 2: Clock Generation Circuit

The **reference clock (XTAL_IN)** is always 27 MHz.

The NCO multiplies the **reference clock** by the NCO fraction, which is NCON/NCOD to generate the **NCO output clock**. The NCO fraction must be greater than 0 and less than 1/2. The NCO can alternately be bypassed by programming NCON and NCOD to equal values. Therefore, when the NCO is bypassed, the NCO output clock is 27 MHz. When the NCO is enabled, the NCO output is 0 to 13.5 MHz.

The N divider divides the **NCO output clock** by N to create the **PLL input clock**. The **PLL input clock** must be between 100 kHz and 1000 kHz. For example, when the NCO is bypassed, this limits N to a number from 27 to 270. When the NCO is used, N can be smaller, as long as the PLL input frequency limits are met. The minimum value for N, in any case, is 2.

The M divider multiplies the **PLL input clock** by M to create the **PLL output clock**. The **PLL output clock** must be between 100 MHz and 300 MHz. In addition, M is limited to a number from 250 to 3000.

The P divider divides the **PLL output clock** by EP and IP to create the **output clocks.** The IP value creates a version of the **output clock** used internally by the FS453. This clock must be set to the actual pixel clock rate desired for the FS453. The EP value creates a version of the **output clock** that is externally routed to the FS453 CLKOUT pin. In normal use, the **external output clock** matches the **internal output clock**. If necessary, the **external output clock** can be a fraction or multiple of the pixel clock, which will be multiplied up or divided down by the graphics controller, to match the pixel clock prior to returning the clock to the FS453 at CLKIN_P. Both **output clocks** must be less than 150 MHz.

Formula defining the relationship between VGA timing and TV timing:

VGA frequency / 656 frequency = (VGA-HTotal x VGA-VTotal) / (TV-HTotal x TV-VTotal)

VGA frequency / 656 frequency = (NCON / NCOD) x M / (N x P)

NTSC: TV_HTotal = 858	This is the total number of pixels in NTSC 656 line (active and blank)
NTSC: TV_VTotal = 525	This is the total number of lines in NTSC 656 field
PAL: TV_HTotal = 864	This is the total number of pixels in PAL 656 line (active and blank)
PAL: TV_VTotal = 625	This is the total number of lines in PAL 656 field

Example, using NCO:

Consider an SVGA mode where VGA active is 800 by 600 and VGA total is 1001 by 625.

Set M=512, N=32, and P=4, so that the PLL provides a net multiplication of x4.

Set NCON = 1001 x 625 = 625,625.

For NTSC, set NCOD = 858 x 525 x 4 = 1,801,800.

For PAL, set NCOD = 864 x 625 x 4 = 2,160,000.

Registers for NTSC:
10h (NCON) = 00098BD9h
14h (NCOD) = 001B7E48h
18h (PLL_M) = 21EFh
1Ah (PLL_N) = 001Fh
1Ch (PLL_P) = 0303h

Registers for PAL:
10h (NCON) = 00098BD9h
14h (NCOD) = 0020F580h
18h (PLL_M) = 21EFh
1Ah (PLL_N) = 001Fh
1Ch (PLL_P) = 0303h

Method for calculating PLL numbers in non-NCO mode, for adjustable scaling:

Set M equal to VGA-VTotal. This constrains the VGA-VTotal to 250 through 3000, which should not pose a problem.

Set N x P equal to TV-HTotal x TV-VTotal / VGA-HTotal. Select VGA-HTotal to contain factors of (TV-HTotal x TV-VTotal). For NTSC, the product factors to (2 x 3 x 3 x 5 x 5 x 7 x 11 x 13). For PAL, the product factors to (2 x 2 x 2 x 2 x 2 x 3 x 3 x 3 x 5 x 5 x 5 x 5). Be careful to leave factors that can be used as P.

The following requirements must also be met: N must be a number within 27 to 270. The minimum pixel clock multiplied by P must be at least 100 MHz. The maximum pixel clock multiplied by P must be at most 300 MHz.

To adjust vertical scaling, VGA-VTotal must be changed. The M value must be changed to match VGA-VTotal. The N and P values will be constant.

Example, not using NCO:

Consider an SVGA mode where VGA active is 800 by 600.

Let M equal the VGA-VTotal, which can be adjusted for scaling. The value of VGA-VTotal and M for overscan would be around 650.

For NTSC, N x P must equal 858 x 525 / VGA-HTotal. Select VGA-HTotal as 975. N x P must equal 462. A value of 3 for P will allow a pixel clock frequency range of 33 to 100 MHz, which is sufficient for this VGA mode. This means N is 154.

For PAL, N x P must equal 864 x 625 / VGA-HTotal. Select VGA-HTotal as 1000. N x P must equal 540. A value of 3 for P will allow a pixel clock frequency range of 33 to 100 MHz, which is sufficient for this VGA mode. This means N is 180.

Set NCON and NCOD to 0.

Registers for NTSC:
10h (NCON) = 00000000h
14h (NCOD) = 00000000h
18h (PLL_M) = 2279h
1Ah (PLL_N) = 0099h
1Ch (PLL_P) = 0202h

Registers for PAL:
10h (NCON) = 00000000h
14h (NCOD) = 00000000h
18h (PLL_M) = 2279h
1Ah (PLL_N) = 00B3h
1Ch (PLL_P) = 0202h

How to program the clock control values in registers:

NCON is programmed in register 10h. It is limited to a 24-bit number.

NCOD is programmed in register 14h. It is limited to a 24-bit number.

M is programmed in register 18h. Program the PLLM bits equal to (M – 17).

N is programmed in register 1Ah. Program the PLLN bits equal to (N – 1).

P is programmed in register 1Ch. Program the PLL_IP and PLL_EP bits equal to (P – 1). PLL_IP and PLL_EP represent the internal and external post-dividers, respectively.

2.2.1.16 SHP - Sharpness Filter

Address Offset 24h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											SHP				

Bits	Name	Description
15-5	Reserved	
4-0	SHP	**Flicker Filter Sharpness.** SHP accentuates sharpness of a flicker-filtered image. By activating the SHP register, the flicker filter adapts to different input source material. SHP is an unsigned number.

Range: {0d : 31d} Provides 0 to 31/16 (6 dB) joint high horizontal and vertical frequency boost.

2.2.1.17 FLK - Flicker Filter Coefficient

Address Offset 26h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											FLK				

Bits	Name	Description
15-5	Reserved	
4-0	FLK	**Flicker Filter Coefficient.** Provides weighting factors for the three line average function of the graphics converter's flicker filter. FLK is an unsigned number.

Range: {0d : 23d}

Note:
The FS453 Flicker Filter is more complex than a three-line average (TLA) flicker filter. The flicker filter incorporates both a vertical averaging function (FLK) and an adaptive horizontal function (SHP). Adjusting the FLK coefficient modifies the vertical filter from no filtering (FLK=0) to a three line average (FLK=16), giving the user the best choice of filtering options. The SHP coefficient controls a two dimensional peaking function that accentuates the joint high vertical - high horizontal spatial frequencies (an "edge enhancer"). The flicker coefficients have usable ranges of 0 to 16/16 for FLK, and 0 to 31/16 for SHP.

2.2.1.18 GPIO – General Purpose I/O and General Purpose Output Enable

Address Offset 28h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								$GPOE_{3-0}$				$GPIO_{3-0}$			

Bits	Name	Description
15-8	Reserved	
7-4	$GPOE_{3-0}$	**General Purpose Output Enable.** Enables the GPIO pin outputs to match the internal register contents. If 1, enables the corresponding GPIO pin as an output. If 0, the corresponding pin is not driven. For GPIO pin mapping, see Table 11 below.
3-0	$GPIO_{3-0}$	**General Purpose I/O.** When this register is written, it contains values to be driven out the GPIO pins for all pins enabled using GPOE. When this register is read, it contains the current state of the GPIO pins. GPIO reads will copy the external pin values as given in Table 11 below.

GPIO	Pin
0	50
1	52
2	3
3	2

Table 11: GPIO Bit to Pin Map

2.2.1.19 ID – Part Identification Number

Address Offset 32h
Default Value FE05h
Attribute R
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID															

Bits	Name	Description
15-0	ID	**Part Number.** The part identification number for software ID purposes. This register should always return FE05h. (If it does not, the device was never issued a hard reset.)

2.2.1.20 Status Port

Address Offset 34h
Default Value 0008h
Attribute R
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								REV						FIFO_ST	CACQ_ST

Bits	Name	Description
15-8	Reserved	
2-7	REV	**Revision Level.** Indicates part design revision level.
1	FIFO_ST	**FIFO Status.** Output FIFO status (=1 if over/under flowed). To clear the FIFO_ST register, set bit 6 in register CR (0CH) to 1. See CR - Command Register on page 18.
0	CACQ_ST	**Counter Acq Status.** Status of TV Counter Acquisition (=1 if re-acquired). To clear the CACQ_ST register, set bit 5 in register CR (0CH) to 1. See CR - Command Register on page 18.

Notes:

FIFO Status: The FS453 does not have a frame memory. In the FS453, the scaled input data frame rate and the SDTV output data field rate are the same. The FIFO takes up the slack during the asynchronous horizontal blanking interval of the input and output. If a data overrun occurs, the FIFO data overrun flag is set.

Counter Acq Status: At any time, if the input and output data frame/field timing are offset, then the TV counter will re-acquire, removing that effect. The event will set the Counter Acq Status Flag.

2.2.1.21 FIFO_SP – FIFO Status Port Fill/Underrun

Address Offset 36h
Default Value 0000h
Attribute R
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFOF								FIFOU							

Bits	Name	Description
15-8	FIFOF	**FIFO Status Port Fill.** Maximum number of FIFO memory locations used during a VGA frame (multiply by 8 to get number of pixels filled). Unsigned number. To reset FIFOF, set bit 6 in register CR (0CH) on page 18 to 1.
7-0	FIFOU	**FIFO Status Port Underrun.** Maximum number of FIFO memory locations underrun during the VGA image (multiply by 8 to get number of pixels corrupted). Unsigned number. To reset FIFOU, set bit 6 in register CR (0CH) on page 18 to 1.

Range: {0d : 255d}

2.2.1.22 FIFO_LAT - FIFO Latency

Address Offset 38h
Default Value 00C8h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								FIFO_LAT							

Bits	Name	Description
15-8	Reserved	
7-0	FIFO_LAT	**FIFO Latency.** Time between the initiation of VGA writes to the FIFO memory and the TV reads from it. Multiply by 4 to get the number of 27 MHz clock delays. When the vertical scaler is programmed for down scaling, set to 164d. Otherwise, set to 130d.

Range: {1d : 255d}

2.2.1.23 CHR_FREQ - Chroma Subcarrier Frequency

Address Offset 40h
Default Value 1F7CF021h
Attribute R/W
Size 32 Bits

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHR_FREQ_{7-0}								CHR_FREQ_{15-8}								CHR_FREQ_{23-16}								CHR_FREQ_{31-24}							

Bits	Name	Description
31-0	CHR_FREQ	**Chroma Subcarrier Frequency.** Sets the subcarrier frequency. Subcarrier = 27 MHz x CHR_FREQ / 2^{32}

Note:

For NTSC	CHR_FREQ	=	21F07C1Fh	Program as:	1F7CF021h
For PAL	CHR_FREQ	=	2A098ACBh	Program as:	CB8A092Ah
For PAL-M	CHR_FREQ	=	21E6EFE3h	Program as:	E3EFE621h

2.2.1.24 CHR_PHASE – Chroma Phase

Address Offset 44h
Default Value 00h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
CHR_PHASE							

Bits	Name	Description
7-0	CHR_PHASE	**Pre-set Subcarrier Phase.** This register adjusts the SC-H phase. The angle is CHR_PHASE / 256 x 360 degrees. Normally set this register to zero.

2.2.1.25 MISC_45 – Miscellaneous Bits Register 45

Address Offset 45h
Default Value 00h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
Reserved						CLRBAR	BYPYCLP

Bits	Name	Description
7-2	Reserved	
1	CLRBAR	**Color Bar Mode.** When set =1, causes the YC inputs in the SDTV encoder to be ignored and forces a color bar pattern on to the encoder input. The color bar pattern is a repeating sequence of 8 colors at 75/100 and 100/100 (amplitude / saturation).
0	BYPYCLP	**Bypass Y Clamp.** Allows for non-standard range of Luma on Y inputs. 0 = Luma expected in range [16:235], and clamped to this range. 1 = Luma expected in range [0:255] and with no clamping.

2.2.1.26 MISC_46 - Miscellaneous Bits Register 46

Address Offset 46h
Default Value 09h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
RGB_SETUP	RGB_SYNC			YC_DELAY			CVBS_EN

Bits	Name	Description
7	RGB_SETUP	**RGB Setup.** If set to 1, blank level is provided as setup for RGB output. If set to 0, black level is provided instead.
6-4	RGB_SYNC	**RGB Sync.** Provide sync to RGB components: [bit6] = 1 sync on red, [bit5] = 1 sync on green, [bit 4] = 1 sync on blue.
3-1	YC_DELAY	**YC Delay.** Relative pipeline delay between luma and chroma outputs.
0	CVBS_EN	**CVBS Enable.** Enables composite and luma/chroma outputs from the encoder. Set to 1.

2.2.1.27 MISC_47 - Miscellaneous Bits Register 47

Address Offset 47h
Default Value 00h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
Reserved				CHR_BW_1	COMP_YUV	COMP_GAIN	

Bits	Name	Description
7-4	Reserved	
3	CHR_BW_1	**Chroma Filter Bandwidth Control.** See Table 12 below: 00=narrow, 01=wide, 10=extra wide, 11=ultra wide. (See MISCELLANEOUS BIT REGISTER 74 for bit 0).
2	COMP_YUV	**Component YUV.** If set to 1, encoder outputs YUV. If set to 0, encoder outputs RGB.
1-0	COMP_GAIN	**Composite Chroma Gain.** Percentage of chroma used in composite output: 00=100%, 01=25%, 10=50%, 11=75%.

CHR_BW Setting	Cutoff Frequency
00	0.6 MHz
01	1.4 MHz
10	1.8 MHz
11	2.5 MHz

Table 12: Chroma Filter Bandwidth Map

2.2.1.28 HSYNC_WID - HSync Width

Address Offset 48h
Default Value 7Eh
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
HSYNC_WID							

Bits	Name	Description
7-0	HSYNC_WID	**HSync Width.** Width of SDTV HSync in 27 MHz clock cycles (LSB is tied to zero).

2.2.1.29 BURST_WID - Burst Width

Address Offset 49h
Default Value 44h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
Reserved	BURST_WID						

Bits	Name	Description
7	Reserved	
6-0	BURST_WID	**Burst Width.** Width of the SDTV color burst in 27 MHz clock cycles.

2.2.1.30 BPORCH - Back Porch Width

Address Offset 4Ah
Default Value 76h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
BPORCH							

Bits	Name	Description
7-0	BPORCH	**Back Porch Width.** Width of the SDTV back porch in 27 MHz clock cycles (LSB is tied to zero).

2.2.1.31 CB_BURST - Cb Burst Amplitude

Address Offset 4Bh
Default Value 3Bh
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
CB_BURST							

Bits	Name	Description
7-0	CB_BURST	**Cb Burst Amplitude Setting.** This is the amplitude of the Cb component of the burst. It is a 2's complement number where positive values are normal.

2.2.1.32 CR_BURST - Cr Burst Amplitude

Address Offset 4Ch
Default Value 00h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
CR_BURST							

Bits	Name	Description
7-0	CR_BURST	**Cr Burst Amplitude Setting.** This is the amplitude of the Cr component of the burst. It is a 2's complement number where positive values are normal.

2.2.1.33 MISC_4D - Miscellaneous Bits Register 4D

Address Offset 4Dh
Default Value 00h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
Reserved						ENC_MODE	

Bits	Name	Description
7-2	Reserved	
1-0	ENC_MODE	**Encoder Input Timing Mode.** Set to 01b.

2.2.1.34 BLACK_LVL - Black Level

Address Offset 4Eh
Default Value 0246h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						$BLACK\_LVL_{1-0}$		$BLACK\_LVL_{9-2}$							

Bits	Name	Description
15-10	Reserved	
9-6	$BLACK\_LVL_{1-0}$	**Black Level.** This is the SDTV setup amplitude value.
7-0	$BLACK\_LVL_{9-2}$	

2.2.1.35 BLANK_LVL - Blank Level

Address Offset 50h
Default Value 003Ch
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						$BLANK\_LVL_{1-0}$		$BLANK\_LVL_{9-2}$							

Bits	Name	Description
15-10	Reserved	
9-8	$BLANK\_LVL_{1-0}$	**Blanking Level.** This is the SDTV blank level amplitude value.
7-0	$BLANK\_LVL_{9-2}$	

Note:
See also register 7Ch, VBI BLANK LEVEL, on page 46.

2.2.1.36 NUM_LINES - Number of Lines

Address Offset 57h
Default Value 0183h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						NUM_LINES_{1-0}		NUM_LINES_{9-2}							

Bits	Name	Description
15-10	Reserved	
9-8	NUM_LINES_{1-0}	**Number of Lines.** Number of total lines in a frame. Because register 4Dh bit 0 on page 40 is set, this register is filled automatically and should not be programmed.
7-0	NUM_LINES_{9-2}	

2.2.1.37 WHITE_LVL - White Level

Address Offset 5Eh
Default Value 00C8h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						$WHITE\_LVL_{1-0}$		$WHITE\_LVL_{9-2}$							

Bits	Name	Description
15-10	Reserved	
9-8	$WHITE\_LVL_{1-0}$	**White level.** This is the SDTV white level amplitude value.
7-0	$WHITE\_LVL_{9-2}$	

2.2.1.38 CB_GAIN - Cb Color Saturation

Address Offset 60h
Default Value 89h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
CB_GAIN							

Bits	Name	Description
7-0	CB_GAIN	**Cb Color Saturation Control.** This is the U saturation adjustment value. The nominal value is 128.

2.2.1.39 CR_GAIN - Cr Color Saturation

Address Offset 62h
Default Value 89h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
CR_GAIN							

Bits	Name	Description
7-0	CR_GAIN	**Cr Color Saturation Control.** This is the V saturation adjustment value. The nominal value is 128.

2.2.1.40 TINT - Tint

Address Offset 65h
Default Value 00h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
TINT							

Bits	Name	Description
7-0	TINT	**Tint Adjustment on Chroma.** This is the chroma tint (or hue) adjustment value. The nominal value is 0. This is a 2's complement number. Does not affect HDTV output modes.

2.2.1.41 BR_WAY - Width of Breezeway

Address Offset 69h
Default Value 16h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
Reserved			BR_WAY				

Bits	Name	Description
7-5	Reserved	
4-0	BR_WAY	**Width of Breezeway.** Width of the SDTV breezeway in 27MHz clocks (LSB bit 0 tied to zero).

Note:
"Breezeway," "Front Porch" and other common video terms refer to specific sections of the composite video waveform:

2.2.1.42 FR_PORCH - Front Porch

Address Offset 6Ch
Default Value 20h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
Reserved		FR_PORCH					

Bits	Name	Description
7-6	Reserved	
5-0	FR_PORCH	**Front Porch.** Width of the SDTV front porch in 27MHz clocks (LSB bit 0 tied to zero).

2.2.1.43 NUM_PIXELS – Total Number of luma/chroma Pixels

Address Offset 71h
Default Value 00B4h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					NUM_PIXELS_{2-0}			NUM_PIXELS_{10-3}							

Bits	Name	Description
15-11	Reserved	
10-8	NUM_PIXELS_{2-0}	**Total Number of luma/chroma Pixels.** Number of 27MHz clocks in active video line (1440 is normal, 720 luma pixels and 720 chroma (Cb and Cr) pixels; the 2 LSB bits [1:0] are tied to zero). Because register 4D bit 0 on page 40 is set, this register is filled automatically and should not be programmed.
7-0	NUM_PIXELS_{10-3}	

2.2.1.44 1ST_LINE - First Video Line

Address Offset 73h
Default Value 15h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
1ST_LINE							

Bits	Name	Description
7-0	1ST_LINE	**First Line of Video.** Line number for the first line of SDTV active video in a field. It is programmed as N-1, where N = the line number desired.

2.2.1.45 MISC_74 - Miscellaneous Bits Register 74

Address Offset 74h
Default Value 02h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
UV_ORDER	PAL_MODE	CHR_BW_0	INVERT_TOP	SYS625_50	CH_PH_R		VSYNC5

Bits	Name	Description
7	UV_ORDER	**UV order.** Switches the ordering of U and V inputs. Set to 0.
6	PAL_MODE	**PAL or NTSC Mode.** 0 = NTSC encoding. 1 = PAL encoding.
5	CHR_BW_0	**Chroma filter bandwidth control.** 00 = narrow, 01 = wide, 10 = extra wide, 11 = ultra wide (see Miscellaneous Bit Register 87 for bit 1). See MISC 47h on page 38 for CHR_BW_1.
4	INVERT_TOP	**Invert field ID polarity.** This bit sets which field contains the first line of active video. The normal value is 1 for PAL or 0 for NTSC.
3	SYS625_50	**System field format.** 0 = 525 lines and 59.94 fields/sec system. 1 = 625 lines and 50 fields/sec system.
2-1	CH_PH_R	**Chroma Phase Reset Interval.** 0 = every 8 fields, 1 = every 4 fields, 2 = every other line, 3 = once. Normal value is 0.
0	VSYNC5	**VSync equalization pulses.** 0 = 6 and 1 = 5 VSync equalization and broad pulses.

2.2.1.46 SYNC_LVL - Sync Level

Address Offset 75h
Default Value 48h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
SYNC_LVL							

Bits	Name	Description
7-0	SYNC_LVL	**Sync Level.** SDTV sync level during non-VBI lines.

2.2.1.47 VBI_BL_LVL - VBI Blank Level

Address Offset 7Ch
Default Value 004Ah
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						$VBIBL\_LVL_{1-0}$		$VBIBL\_LVL_{9-2}$							

Bits	Name	Description
15-10	Reserved	
9-8	$VBIBL\_LVL_{1-0}$	**VBI Blanking Level.** This is the SDTV blank level amplitude value for VBI lines
7-0	$VBIBL\_LVL_{9-2}$	

Note:
Refer to Register 50h, Blank Level, on page 41.

2.2.1.48 SOFT_RST - Encoder Soft Reset

Address Offset 7Eh
Default Value 00h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
Reserved							SOFT_RST

Bits	Name	Description
7-1	Reserved	
0	SOFT_RST	**Encoder Soft Reset.** If set to 1, there is no signal from the video encoder and all counters are reset.

2.2.1.49 ENC_VER - Encoder Version

Address Offset 7Fh
Default Value 20h
Attribute R
Size 8 Bits

7	6	5	4	3	2	1	0
ENC_VER							

Bits	Name	Description
7-0	ENC_VER	**Encoder Version Number.** Contains the version of the encoder. This is a read-only register.

2.2.1.50 WSS_CONFIG – WSS Configuration Register

Address Offset 80h
Default Value 07h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
Reserved	WSSF1_EN	WSSF0_EN	WSS_TYPE	WSS_CLKBY	WSS_EDGE		Reserved

Bits	Name	Description
7	Reserved	
6	WSSF1_EN	**WSS Field 1 Enable.** Enables WSS signal in Field 1.
5	WSSF0_EN	**WSS Field 0 Enable.** Enables WSS signal in Field 0.
4	WSS_TYPE	**WSS Type.** 1=PAL, ITU-R BT.1119-2, 0=NTSC, EIAJ CPR-1204
3	WSS_CLKBY	**WSS Clock Bypass.** Typically this is set =0. WSS_CLKBY =1 Causes the chroma clock to be used as the WSS clock, WSS_CLKBY =0 forces the local 12-bit WSS clock to be used.
2-1	WSS_EDGE	**WSS Edge Rate Control.** Edge rates are proportional to the frequency of the WSS clock, but can also be scaled by the WSS_EDGE parameter. Higher numbers indicate faster rise and fall times on the WSS pulses.
0	Reserved	

2.2.1.51 WSS_CLK – WSS Clock

Address Offset 81h
Default Value 0072Fh
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				WSS_CLK_{3-0}				WSS_CLK_{11-4}							

Bits	Name	Description
15-12	Reserved	
11-8	WSS_CLK_{3-0}	**WSS Clock Frequency.**
7-0	WSS_CLK_{11-4}	

Note:
WSS Clock Frequency = (WSS_CLK / 2^{12}) x (27 MHz)

2.2.1.52 WSS_DATAF1 – WSS Data Field 1

Address Offset 83h
Default Value 000000h
Attribute R/W
Size 24 Bits

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				WSS_DATAF1_{3-0}				WSS_DATAF1_{11-4}								WSS_DATAF1_{19-12}							

Bits	Name	Description
23-20	Reserved	
19-16	WSS_DATAF1_{3-0}	**WSS Data for Field 1.** Consult the WSS standard for data definitions: ITU-R BT.1119-2 for PAL and EIAJ CPR-1204 for NTSC.
15-8	WSS_DATAF1_{11-4}	
7-0	WSS_DATAF1_{19-12}	

2.2.1.53 WSS_DATAF0- WSS Data Field 0

Address Offset 86h
Default Value 000000h
Attribute R/W
Size 24 Bits

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				WSS_DATAF0_{3-0}				WSS_DATAF0_{11-4}								WSS_DATAF0_{19-12}							

Bits	Name	Description
23-20	Reserved	
19-16	WSS_DATAF0_{3-0}	**WSS Data for Field 0.** Consult the WSS standard for data definitions.
15-8	WSS_DATAF0_{11-4}	
7-0	WSS_DATAF0_{19-12}	

2.2.1.54 WSS_LNF1 - WSS Line Number Field 1

Address Offset 89h
Default Value 00h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
WSS_LNF1							

Bits	Name	Description
7-0	WSS_LNF1	**Field 1 WSS Line.** Line number (relative to the previous VSync) at which the WSS data will appear in Field 1.

2.2.1.55 WSS_LNF0 - WSS Line Number Field 0

Address Offset 8Ah
Default Value 00h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
WSS_LNF0							

Bits	Name	Description
7-0	WSS_LNF0_{7-0}	**Field 0 WSS Line.** Line number (relative to the previous VSync) at which the WSS data will appear in Field 0.

2.2.1.56 WSS_LVL - WSS Level

Address Offset 8Bh
Default Value 03FFh
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						WSS_LVL_{1-0}		WSS_LVL_{9-2}							

Bits	Name	Description
15-10	Reserved	
9-8	WSS_LVL_{1-0}	**WSS High Level.** WSS waveform will rise from VBIBL_LVL to WSS_LVL in a 0 to 1 transition.
7-0	WSS_LVL_{9-2}	

2.2.1.57 MISC_8D – Miscellaneous Bits Register 8D

Address Offset 8Dh
Default Value 00h
Attribute R/W
Size 8 Bits

7	6	5	4	3	2	1	0
Reserved			NOTCH_EN	NOTCH_WD	NOTCH_FREQ		

Bits	Name	Description
4	NOTCH_EN	**Y Notch Filter Enable.** 1=On, 0=Off.
3	NOTCH_WD	**Y Notch Filter Wide Bandwidth.** 1=wide, 0=narrow.
2-0	NOTCH_FRQ	**Y Notch Frequency.** Set to 2 for NTSC. Set to 5 for PAL.

2.2.1.58 Composite Video Waveform and Terminology

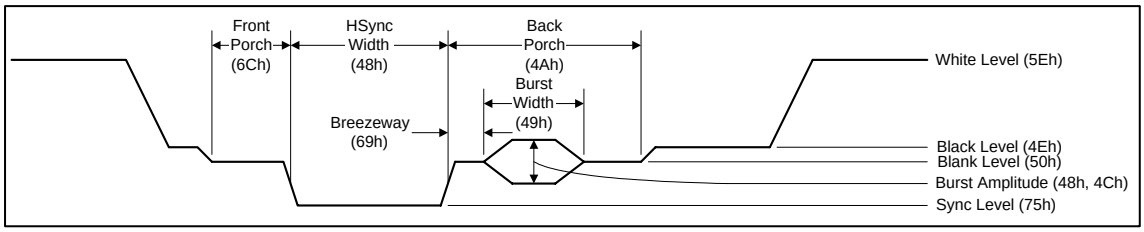

Figure 3: Composite Video Waveform Showing Terminology and Register Locations

2.2.1.59 Examples of SDTV Register Values

Hex Index	Register	NTSC	PAL	PAL-M	PAL-N	Combination PAL-N
40h	CHR_FREQ	0x1F7CF021h	0xCB8A092Ah	0xE3EFE621h	0xCB8A092Ah	0x4694F612h
44h	CHR_PHASE	00h	00h	00h	00h	00h
48h	HSYNC_WID	7Eh	7Eh	7Eh	7Eh	7Eh
49h	BURST_WID	44h	40h	44h	40h	44h
4Ah	BPORCH	76h	8Ah	76h	8Ah	8Ah
4Bh	CB_BURST	3Bh	2Ch	29h	29h	2Ch
4Ch	CR_BURST	00h	1Fh	1Dh	1Dh	1Fh
4Eh	BLACK_LVL	011Ah	00FBh	011Ah	011Ah	00FBh
50h	BLANK_LVL	00F0h	00FBh	00F0h	00F0h	00FBh
5Eh	WHITE_LVL	0320h	0320h	0320h	0320h	0320h
60h	CR_GAIN	89h	91h	89h	89h	91h
62h	CB_GAIN	89h	91h	89h	89h	91h
69h	BR_WAY	16h	1Ah	12h	1Ah	1Ah
6Ch	FRNT_PORCH	20h	18h	20h	18h	18h
$74h_0$	$Misc\_74_0$ VSYNC5	0b	1b	0b	0b	1b
$74h_{1-2}$	$MISC\_74_{1-2}$ CH_PH_R	10b	00b	00b	00b	00b
$74h_3$	$Misc\_74_3$ SYS625_50	0b	1b	0b	1b	1b
$74h_4$	$Misc\_74_4$ INVERT_TOP	0b	1b	1b	1b	1b
$74h_6$	$Misc\_74_6$ PAL_MODE	0b	1b	1b	1b	1b
75h	SYNC_LVL	10h	10h	10h	10h	10h
7Ch	WSS_LVL	00F0h	00FBh	00F0h	00F0h	00FBh

Table 13: Typical Encoder Register Values for SDTV Standards

Note:
The Quick Program Register automatically programs the correct register settings for NTSC and PAL.

2.2.1.60 VID_CNTL0 – Video Control 0

Address Offset 92h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOP_FIELD	OBIN_USIG	PRPB_SYNC	VSYNC5_6	BLANK_INV	FIELD_INV	VSYNC_INV	HSYNC_INV	INT_PROG	FIELD_MS	SYNC_LVL	SYNC_BI_TRI	SYNC_ADD	MATRIX_BYP	VID_MODE	

Bits	Name	Description
15	TOP_FIELD	**Top Field.** Selects the Interlaced HDTV Top Field. If set =1, the first active line is in Field 2, otherwise the first active line is in Field 1.
14	OBIN_USIG	**Offset Binary or Unsigned.** If set =1, RED_SCL, GRN_SCL, and BLU_SCL process input data in the YCrCb offset binary format. If clear, input data is scaled in the RGB unsigned format. See Table 15: Matrix Configurations on page 63.
13	PRPB_SYNC	**Sync on Pr and Pb.** When set =1, inserts syncs on Y, Pr, and Pb components. When clear, inserts sync on Y component only.
12	VSYNC5_6	**Vertical Sync Width.** Selects HDTV composite vertical sync width parameter. When set =1, VSync is 5 half lines, otherwise it is 6 half lines long.
11	BLANK_INV	**Blank Invert.** Inverts the input BLANK signal. If set to 0, BLANK (pin 38) low indicates active pixels, and high indicates pixels that are in the blanking area. If set to 1, BLANK high indicates active pixels, and low indicates pixels that are in the blanking area. Note that a BLANK signal is not required. At a minimum the pin must be tied high or low, with this bit set appropriately, in order to see a picture.
10	FIELD_INV	**Field Invert.** Inverts the sensed field state for an interlaced input. This bit is only used if the FIELD_MS bit is set to 0 and the input mode is interlaced. (For normal use, this is only HDTV 1080i mode.) If set to 0, HSync low at the falling edge of VSync indicates that the current field state is high. If set to 1, HSync low at the falling edge of VSYNC indicates that the current field state is low. (In HDTV 1080i mode, the field state is low during the first field.) Note that HSync and VSync for purposes of this logic are inverted with respect to the actual input signals if the HSYNC_INV or VSYNC_INV bits are set, respectively.
9	VSYNC_INV	**Vertical Sync Invert.** Inverts the input VSync signal. If set to 0, vertical timing is measured with respect the rising edge of VSync (active high). If set to 1, vertical timing is measured with respect to the falling edge of VSync (active low).
8	HSYNC_INV	**Horizontal Sync Invert.** Inverts the input HSync signal. If set to 0, horizontal timing is measured with respect the rising edge of HSync (active high). If set to 1, horizontal timing is measured with respect to the falling edge of HSync (active low).

7	INT_PROG	**Interlaced/Progressive.** When set =1, input image is interlaced.
6	FIELD_MS	**Field Master or Slave.** This bit selects the source for the field signal used to determine the current output field for interlaced output modes. Normally set to 0 for HDTV modes or 1 for SDTV modes. (See Note below.)
5	SYNC_LVL	**Sync Level.** When set =1, HDTV sync amplitude is 300 mV, otherwise amplitude is 286 mV.
4	SYNC_BI_TRI	**Sync Bi-level or Tri-level.** When set =1, inserts Bi-level HDTV syncs, otherwise inserts Tri-level syncs.
3	SYNC_ADD	**Sync Add.** When set =1, inserts HDTV syncs.
2	MATRIX_BYP	**Matrix Bypass.** When set =1, bypasses RGB to YUV matrix. See Table 15: Matrix Configurations on page 63.
1,0	VID_MODE	**Video Output Mode.** See Table 14: Video Output Modes below.

Note:
Field Master or Slave: When this bit is set to 1, or if the input image is progressive, the field is arbitrarily generated internal to the FS453. That is, the FS453 is the field master. When set to 0 and the input image is interlaced, the field is generated by decoding the incoming HSync and VSync signals. That is, the FS453 is the field slave, and the current field state is provided to the FS453 by the graphics controller. If this bit is set to 0 and the input image is progressive, the FS453 will still arbitrarily generate an internal field state for an interlaced output, but the state will not appear on pin 37, which will always be low. (Note that SDTV modes normally use a progressive input mode.)

2.2.1.61 FS453 Video Output Modes

VIDEO OUTPUT MODE	VID_MODE	Encoder Mode	Matrix Bypass	Signal 0	Signal 1	Signal 2	Signal 3
Composite & S-Video	0	Normal	--	Y	C	Ground	CVBS
SDTV YPrPb	1	YUV	--	Y	Pr	Pb	CVBS
SCART	1	Normal	--	GRN	RED	BLU	CVBS
HDTV YPrPb	2	--	0	Y	Pr	Pb	Ground
VGA RGB	2	--	1	GRN	RED	BLU	Ground

Table 14: Video Output Modes

2.2.1.62 HD_FP_SYNC – Horizontal Front Porch and HSync Width

Address Offset 94h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FP_WID								HSYNC_WID							

Bits	Name	Description
15-8	FP_WID	**Horizontal Front Porch / Serration Width.** HDTV horizontal Front Porch and Serration High width.
7-0	HSYNC_WID	**HSync Width.** HDTV sync width.

2.2.1.63 HD_YOFF_BP – HDTV Luminance Offset and Back Porch

Address Offset 96h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y_OFF								HBP_WID							

Bits	Name	Description
15-8	Y_OFF	**Luminance Offset.** 2's complement value that offsets the HDTV Luma signal, either plus or minus, to adjust brightness. Refer to Registers B8-BE on pages 66 to 67 to program the offset active region.
7-0	HBP_WID	**Horizontal Back Porch / Broad Pulse Width.** HDTV horizontal Back Porch and Broad Pulse High width.

2.2.1.64 SYNC_DL – Sync Delay Value

Address Offset 98h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC_DL															

Bits	Name	Description
15-8	SYNC_DL	**Sync Delay Value.** Delays the insertion of the HDTV sync, in the output, by this number of HDTV pixels.

2.2.1.65 LD_DET – DAC Load Detect

Address Offset 9Ch
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	DET_RDY	LD_MSK				LD_VAL									

Bits	Name	Description
15	Reserved	
14	DET_RDY	**DAC Load Detection Ready.** Returns a 1 when the DAC load detection cycle has been completed. Bit is set =0 when the DAC Load Mask is written.
13-10	LD_MSK	**DAC Load Mask.** When written, a 1 selects the DAC() to be tested. When read, a 1 indicates that a load was present on the tested DAC(s). Each DAC is assigned to a LD_MSK bit in order, starting with DAC A at LD_MSK_0 (Bit 10).
9-0	LD_VAL	**DAC Load Value.** Selects value output to DAC during a Load Test. The nominal value 314 detects whether or not a load is present in a doubly-terminated (normal) system.

2.2.1.66 Load Detection Guidelines

The FS453's DACs are capable of detecting when they are connected to a load (like a TV). Focus has load-detection software that can read the state of the DACs and automatically program the FS453 to output the correct video signals for the type of cables that are connected to the system. The load-detection software will only work on systems that use Focus' standard FS453 DAC routing:

DAC	Signals
DAC A	Y, Green
DAC B	C, Red, Pr
DAC C	Blue, Pb
DAC D	CVBS

The load-detection software can tell the difference between when a system is connected to a YPrPb TV and when it is connected to an S-Video TV (CVBS is always enabled). The load-detection software cannot tell the difference between interlaced and progressive TVs, and YPrPb and SCART TVs.

When a DAC performs load-detection, it does not output a video signal. As a result, load detection must be performed while the system is booting, and when it changes video modes. Systems that rely on load-detection should include the load-detection software in both the BIOS and the driver.

In order for a system to work with load-detection, the video cables must be connected to the device and the TV before the device is powered on. If the cabling is changed while the system is running, then the user will have to manually tell the system to reconfigure its DAC assignments. Likewise, the user will have to manually tell the system to switch between interlaced and progressive outputs. When progressive outputs are enabled, S-Video and CVBS will be disabled.

To disable load detection and return to normal use, write the value 8000h to LD_DET.

The LD_DET register has no effect if the device clocks are disabled for power-down mode. In the PWR_MGNT register (A0h), bit 11 (CLKOFF) must be set to 0 for the load detection circuit to function.

2.2.1.67 DAC_CNTL – DAC Control

Address Offset 9Eh
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DAC_DMUX		DAC_CMUX		DAC_BMUX		DAC_AMUX	

Bits	Name	Description
15-8	Reserved	
7-6	DAC_DMUX	**DAC D Output Mux.** 0: Signal 0 to DAC D 1: Signal 1 to DAC D 2: Signal 2 to DAC D 3: Signal 3 to DAC D
5-4	DAC_CMUX	**DAC C Output Mux.** 0: Signal 0 to DAC C 1: Signal 1 to DAC C 2: Signal 2 to DAC C 3: Signal 3 to DAC C
3-2	DAC_BMUX	**DAC B Output Mux.** 0: Signal 0 to DAC B 1: Signal 1 to DAC B 2: Signal 2 to DAC B 3: Signal 3 to DAC B
1-0	DAC_AMUX	**DAC A Output Mux.** 0: Signal 0 to DAC A 1: Signal 1 to DAC A 2: Signal 2 to DAC A 3: Signal 3 to DAC A

Note:
See Table 14: Video Output Modes on page 54 for definitions of signals based on video output modes.

2.2.1.68 PWR_MGNT – Power Management

Address Offset A0h
Default Value 000Fh
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		GTLIO_PD	PLL_PD	CLKOFF	CLK_SOFF		DAC_D_LP	DAC_C_LP	DAC_B_LP	DAC_A_LP	BGAP_OFF	DAC_D_OFF	DAC_C_OFF	DAC_B_OFF	DAC_A_OFF

Bits	Name	Description
15-14	Reserved	
13	GTLIO_PD	**GTL I/O Power Down.** If set =1, puts all the GTL pins into power down mode. If set =0, normal mode.
12	PLL_PD	**PLL Power Down.** If set =1, turns off the GCC PLL. If set =0, normal mode.
11	CLKOFF	**Clock Off.** If set =1, turns off FS453 clocks to minimize power. The serial interface logic always remains active. If set =0, normal mode. After changing this bit to 0 to re-enable the device, a soft reset must be issued. See bit 0 of the CR register (0Ch).
10-9	CLK_SOFF	**Clock Select Off.** Selectively disables clocks in the FS453. Setting SOFF =01b will turn off the HDTV clock. Setting SOFF =10b will turn off the SDTV clock. The serial interface logic always remains active. These bits also select between SD and HD routing to the DAC MUXs. In normal mode, exactly one of these bits must be set.
8	DAC_D_LP	**DAC D Output Low Power.** If set =1, puts DAC D in low power state. If set =0, DAC D runs in normal mode.
7	DAC_C_LP	**DAC C Output Low Power.** If set =1, puts DAC C in low power state. If set =0, DAC C runs in normal mode.
6	DAC_B_LP	**DAC B Output Low Power.** If set =1, puts DAC B in low power state. If set =0, DAC B runs in normal mode.
5	DAC_A_LP	**DAC A Output Low Power.** If set =1, puts DAC A in low power state. If set =0, DAC A runs in normal mode.
4	BGAP_OFF	**DAC Bandgap Reference OFF.** If set =1, turns off the DAC's reference.
3	DAC_D_OFF	**DAC D Output OFF.** If set =1, turns off DAC D. If set =0, turns DAC D on.
2	DAC_C_OFF	**DAC C Output OFF.** If set =1, turns off DAC C. If set =0, turns DAC C on.
1	DAC_B_OFF	**DAC B Output OFF.** If set =1, turns off DAC B. If set =0, turns DAC B on.
0	DAC_A_OFF	**DAC A Output OFF.** If set =1, turns off DAC A. If set =0, turns DAC A on.

Note: DAC should be in normal power mode for HDTV output modes 720p and 1080i.

2.2.1.69 RED_MTX – RGB to YCrCb Matrix Red Coefficient

Address Offset A2h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RED_MTX							

Bits	Name	Description
15-8	Reserved	
7-0	RED_MTX	**RED_MTX. RGB to YCrCb Matrix Red Coefficient.** See Table 15 on page 63. Refer to Input Color Space Conversion.

2.2.1.70 GRN_MTX – RGB to YCrCb Matrix Green Coefficient

Address Offset A4h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								GRN_MTX							

Bits	Name	Description
15-8	Reserved	
7-0	GRN_MTX	**GRN_MTX. RGB to YCrCb Matrix Green Coefficient.** See Table 15 on page 63. Refer to Input Color Space Conversion.

2.2.1.71 BLU_MTX – RGB to YCrCb Matrix Blue Coefficient

Address Offset A6h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								BLU_MTX							

Bits	Name	Description
15-8	Reserved	
7-0	BLU_MTX	**BLU_MTX. RGB to YCrCb Matrix Blue Coefficient.** See Table 15 on page 63. Refer to Input Color Space Conversion.

2.2.1.72 RED_SCL – RGB to YCrCb Scaling Red Coefficient

Address Offset A8h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							RED_SCL								

Bits	Name	Description
15-9	Reserved	
8-0	RED_SCL	**RED_SCL. RGB to YCrCb Scaling Red Coefficient.** See Table 15 on page 63. Refer to Input Color Space Conversion.

2.2.1.73 GRN_SCL – RGB to YCrCb Scaling Green Coefficient

Address Offset AAh
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							GRN_SCL								

Bits	Name	Description
15-9	Reserved	
8-0	GRN_SCL	**GRN_SCL. RGB to YCrCb Scaling Green Coefficient.** See Table 15 on page 63. Refer to Input Color Space Conversion.

2.2.1.74 BLU_SCL – RGB to YCrCb Scaling Blue Coefficient

Address Offset ACh
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							BLU_SCL								

Bits	Name	Description
15-9	Reserved	
8-0	BLU_SCL	**BLU_SCL. RGB to YCrCb Scaling Blue Coefficient.** See Table 15 below. Refer to Input Color Space Conversion.

2.2.1.75 Typical Matrix Configurations

VIDEO OUTPUT & FORMAT	VIDEO INPUT	Matrix Bypass	Offset Binary	RED_MTX	GRN_MTX	BLU_MTX	RED_SCL	GRN_SCL	BLU_SCL
NTSC (ALL)	RGB	0	--	77	150	29	160	219	126
NTSC (ALL)	YCrCb	1	1	--	--	--	256	256	256
PAL (ALL)	RGB	0	--	77	150	29	160	219	126
PAL (ALL)	YCrCb	1	1	--	--	--	256	256	256
480p (YPrPb)	RGB	0	--	77	150	29	88	138	74
480p (YPrPb)	YCrCb	1	1	--	--	--	146	160	146
720p (YPrPb)	RGB	0	--	54	183	19	88	138	74
720p (YPrPb)	YCrCb	1	1	--	--	--	146	160	146
1080i (YPrPb)	RGB	0	--	54	183	19	88	138	74
1080i (YPrPb)	YCrCb	1	1	--	--	--	146	160	146
VGA (RGB)	RGB	1	0	--	--	--	138	138	138

Table 15: Matrix Configurations

2.2.1.76 CC_F1 - Closed Caption Field 1 Data

Address Offset AEh
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC_F1															

Bits	Name	Description
15-0	CC_F1	**Closed Captioning Field 1.** Contains the 16-bit value to write in the next NTSC Field 1 (odd field) Closed Caption line. Returns 0 when value has been written. Note that the Closed Caption specification dictates what value should appear in which field. In PAL, values written to this register appear in PAL Field 2 (odd field).

2.2.1.77 CC_F2 - Closed Caption Field 2 Data

Address Offset B0h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC_F2															

Bits	Name	Description
15-0	CC_F2	**Closed Captioning Field 2.** Contains the 16-bit value to write in the next NTSC Field 2 (even field) Closed Caption line. Returns 0 when value has been written. Note that in PAL, values written to this register appear in PAL Field 1 (even field).

2.2.1.78 Closed Caption Control

Address Offset B2h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	CC_EN_F2	CC_EN_F1	EPARITY	F2_LOS						F1_LOS					

Bits	Name	Description
15	Reserved	
14	CC_EN_F2	**CC Enable Field 2.** If set =1, enables the Closed Caption for NTSC Field 2. If set =0, disables.
13	CC_EN_F1	**CC Enable Field 1.** If set =1, enables the Closed Caption for NTSC Field 1. If set =0, disables.
12	EPARITY	**Even Parity.** If set =1, parity of the CC data sent will be even; if set clear (=0), parity will be odd. Parity of input CC data is ignored. The CC specification requires odd parity.
11-6	F2_LOS	**F2 CC Line Offset.** Selects the NTSC Field 2 Closed Caption line number.
5-0	F1_LOS	**F1 CC Line Offset.** Selects the NTSC Field 1 Closed Caption line number. In NTSC the line number is 21. In PAL, the line number is 23.

2.2.1.79 Closed Caption Blanking Value

Address Offset B4h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RGB_BLNK								YC_BLNK							

Bits	Name	Description
15-8	RGB_BLNK	**RGB CC Blanking Value.** Eight bit Closed Caption RGB Blanking Value. Set to zero for automatic operation.
7-0	YC_BLNK	**YC CC Blanking Value.** Eight bit Closed Caption Luma Blanking Value. Set to zero for automatic operation.

2.2.1.80 CC_BKS - Closed Caption Blanking Sample

Address Offset B6h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CC_BKS									

Bits	Name	Description
15-10	Reserved	
9-0	CC_BKS	**CC Blanking Sample Value.** Sets the horizontal position of the start of the closed-caption signal. Set to 0 for automatic operation, which starts the signal immediately after the rising edge of the TV HSync.

2.2.1.81 HACT_ST - HDTV Horizontal Active Start

Address Offset B8h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HACT_ST											

Bits	Name	Description
15-12	Reserved	
11-0	HACT_ST	**Horizontal Active Area Start**. The distance from the rising edge of the incoming HSync to the start of the HDTV active area is HACT_ST plus the value in register 98h, SYNC_DL, on page 55. The active area brightness is adjusted by HDTV luma offset as programmed in register 94h, HD_YOFF_BP, on page 55.

2.2.1.82 HACT_WD - HDTV Horizontal Active Width

Address Offset BAh
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				HACT_WD											

Bits	Name	Description
15-12	Reserved	
11-0	HACT_WD	**Horizontal Active Width**. Defined as the horizontal width of the active area for HDTV luma offset as programmed in register 94h, HD_YOFF_BP on page 55.

2.2.1.83 VACT_ST - HDTV Vertical Active Start

Address Offset BCh
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				VACT_ST											

Bits	Name	Description
15-12	Reserved	
11-0	VACT_ST	**Vertical Active Start**. The distance in lines from the rising edge of the incoming VSync to the top of the HDTV active area. The active area brightness is adjusted by HDTV luma offset as programmed in register 94h, HD_YOFF_BP, on page 55.

2.2.1.84 VACT_HT - HDTV Vertical Active Height

Address Offset BEh
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				VACT_HT											

Bits	Name	Description
15-12	Reserved	
11-0	VACT_HT	**Vertical Active Height**. Defined as the vertical height of the active area for HDTV luma offset as programmed in register 94h, HD_YOFF_BP, on page 55.

2.2.1.85 Pr and Pb Relative Scaling

Address Offset C0h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PB_SC								PR_SC							

Bits	Name	Description
15-8	PB_SC	**Pb Scaling.** Scales the Standard Definition Pb channel amplitude relative to the Composite video output. Unity is 128.
7-0	PR_SC	**Pr Scaling.** Scales the Standard Definition Pr channel amplitude relative to the Composite video output. Unity is 128.

2.2.1.86 Y_BW – SDTV Luma Bandwidth

Address Offset C2h
Default Value 0000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								Y_BW							

Bits	Name	Description
15-8	Reserved	
7-0	Y_BW	**SDTV Luma Bandwidth.** 2's complement value attenuates or amplifies the high frequency response. Y_BW = 0 for flat response, Y_BW = 127 for 10 dB of cut, and Y_BW = -128 for 5dB of boost. See Figure 4: Luminance Frequency Response below.

2.2.1.87 Luminance Frequency Response

This graph illustrates the expected frequency response of the FS453 video output at the limits of the Luminance Bandwidth settings.

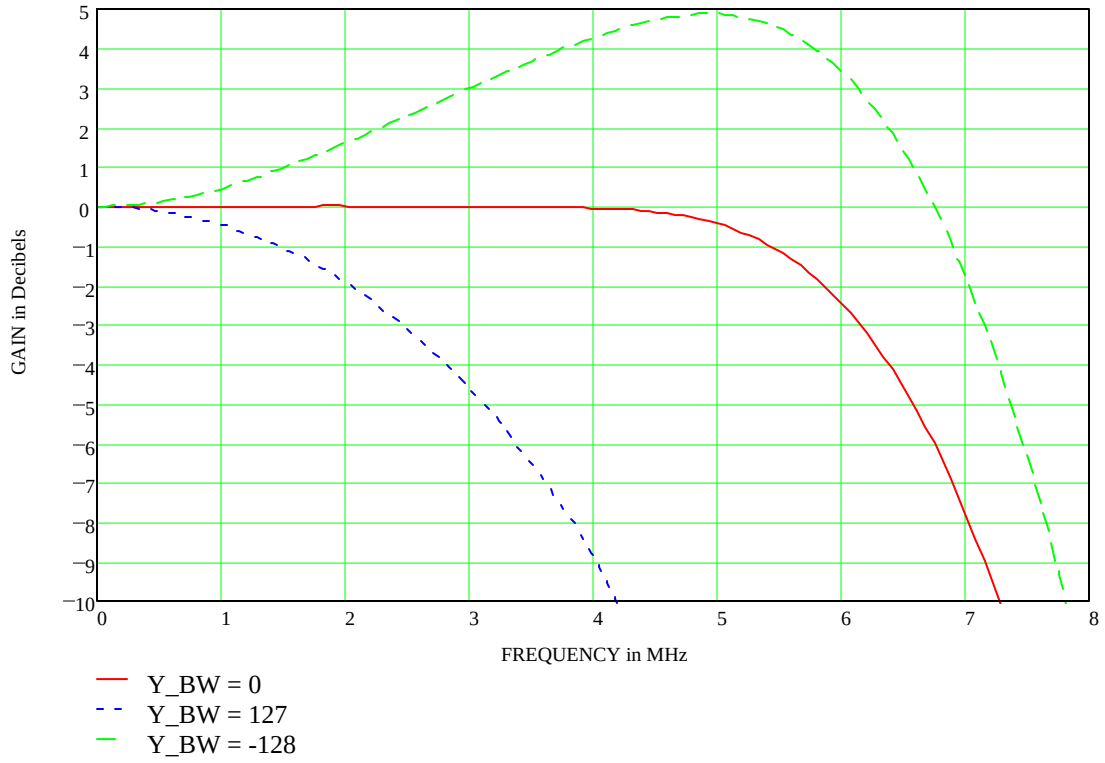

Figure 4: Luminance Frequency Response

2.2.1.88 Quick Program Register

Address Offset C4h
Default Value 8000h
Attribute R/W
Size 16 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	QK_UIM		QK_OS		QK_YC_IN	QK_FF	QK_OM		QK_UO	QK_ GMODE		QK_PN

Bits	Name	Description
15-12		**Required**. Must be 1001 to initiate a program.
11-10	QK_UIM	**Quick Universal Input Mode.** Select the input clocking and muxing mode. 0 : Reserved : 00b 1: NVIDIA : 01b 2: Intel : 10b 3: National : 11b
9-8	QK_OS	**Quick Output Standard.** Configures for the following output standards: 0 : SDTV (NTSC or PAL) : 00b 1: 480p : 01b 2: 720p : 10b 3: 1080i : 11b
7	QK_YC_IN	**Quick YCrCb Input.** If set =1, input is YCrCb. If set =0, input is RGB.
6	QK_FF	**Quick Flicker Filter.** If set =1, programs flicker filter on. If set =0, flicker filter is disabled.
5-4	QK_OM	**Quick Output Mode.** Configures for the following output modes: 0 : S-Video and Composite : 00b 1: Component YPrPb : 01b 2: Component SCART : 10b 3: VGA Pass-through : 11b
3	QK_UO	**Quick Underscan/ Overscan.** If set =1, scaler will underscan the television image.
2-1	QK_GMODE	**Quick Graphics Mode.** Configures for the following VGA modes: 0 : 640x480 : 00b 1: 720x480 or 720x576 : 01b 2: 800x600 : 10b 3: 1024x768 : 11b
0	QK_PN	**Quick PAL/NTSC.** If set =1, programs system for PAL. If set =0, system is NTSC.

Note:
When using this register, you must also program the CRTC registers in the GCC. See Table 1: CRTC values for SDTV modes, on page 10 and Table 2: CRTC values for HDTV modes on page 10 for more information.

3. Revision History

August 20, 2002: Release, V1.0. Data Sheet reorganized into separate reference guides. The new Data Sheet package consists of a Product Brief, Hardware Reference, Software/Firmware Reference, and a Physical (Layout) Reference. Software/Firmware Reference revised.

December 13, 2002: Release, V2.0. New tables and figures added. Notes revised. Register names clarified.

July 1, 2004: Release V3.0 Added FS455/6 packaging information. Incorporated video port and DAC application notes. Miscellaneous minor edits.

January 24, 2005: Release V3.1 Updated Lead-Free ordering information. Minor modifications to *PLL M and Pump Control* and *TINT* register information.

4. Order Information

Order Number	Temperature Range	Screening	Package	Product
444-2133	0°C to 70°C	Commercial	80 Lead PQFP	FS453, Tape & Reel
444-2134	0°C to 70°C	Commercial	80 Lead PQFP	FS454, Tape & Reel
444-2137	0°C to 70°C	Commercial	88 Lead FBGA	FS455, Tape & Reel
444-2138	0°C to 70°C	Commercial	88 Lead FBGA	FS456, Tape & Reel

Package Markings:

FOCUS
Enhancements
<FS45x><LF><solder>
<YYWWR>
<fab lot id>

where x = 3, 4, 5 or 6; LF = lead free; YY = year; WW = work week; R = die revision

solder = lead-free solder type (only present on devices with lead-free solder)
See HTTP://WWW.JEDEC.ORG/DOWNLOAD/SEARCH/JESD97.PDF

Note:
Any of the above SKUs can be ordered with lead-free solder. To place an order for a part with lead-free solder, append "LF" to the end of the SKU. For example 444-2137LF would be an FS455 with lead-free solder. All of these devices utilize the same die. They function identically except for Macrovision features (enabled in FS454 :& FS456), package type, and solder type.

Please forward suggestions and corrections as soon as possible to the email address below. The information herein is accurate to the best of FOCUS' knowledge, but not all specifications have been characterized or tested at the time of the release of this document. Parameters will be updated as soon as possible and updates made available.

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FOCUS Enhancements, Inc.

1370 Dell Avenue
Campbell, CA 95008
WWW.FOCUSINFO.COM

Phone: (408) 866-8300
Fax: (408) 866-4859
Email: INFO@FOCUSINFO.COM

