MAX2769 Universal GPS Tuner Application Note
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This note describes the MAX2769, a low cost, single conversion, low IF frequency GPS receiver chip that offers more flexibility and performance than its predecessors for a wide range of GPS applications such as mobile handsets, PDA's and embedded PC, and automotive applications. It represents the most flexible, high performance, low power receiver on the market.

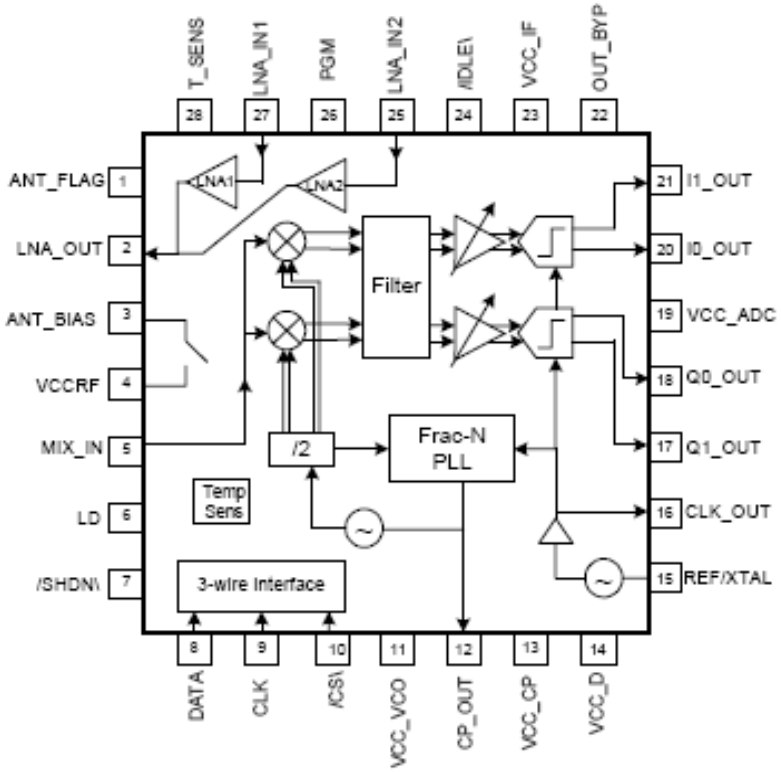

Figure 1. MAX2769 Block Diagram and pinout

Functional Overview
The MAX2769 offers a choice of two LNA's: LNA1 has a higher gain and a lower noise figure for use with a passive antenna, while LNA2 offers a higher IP3 and lower power consumption at the expense of a slightly lower gain and higher noise figure, for use with active external antennas. The pin-out is provided for an external GPS-band filter between the LNA output and the down-converter mixer input. There is a wide selection of available reference and IF frequencies. The I and Q channel select filters also have a wide variety of bandwidth selection and can be selected as either 3rd or 5th order. In this way, the baseband processor can adjust (or fix) the desired channel bandwidth for best sensitivity. The MAX2769 provides 115 dB cascaded gain and a 1.5 dB cascaded NF in LNA1 mode.

An on-chip fractional-N synthesizer tuned with the help of an external loop filter provide high IF selectivity with low phase noise. The IF output is adjustable in 63 steps between 0 and 12.5 MHz, with a default setting of 4.092 MHz. The A to D converters can be set to 1, 2, or 3-bit resolution.

Detailed Description of Key MAX2769 features

Very Low DC power consumption.
In standard mode, power required is typically 18-21mA @ 3V. There are also several reduced-power modes that require as little as 13 mA typical current consumption. The device can be placed in idle mode through SPI control. In this mode, only the clock buffer and temperature sensor are active and the current consumption drops to 0.5mA.

Very Low associated BOM cost and size.
This is a direct down-conversion design with internal filtering which eliminates the need for external channel filtering components. The excellent noise figure of 1.5 dB for the cascaded chain (with a 0.8 dB typical first stage noise figure) means this device can be used with a passive antennas - no external LNA is required. The removal of intermediate frequency filtering and pre-amplification means less board space is required to implement a receiver.

Flexibility for applications involving active antennas.
If a user desires to use this device with an active antenna, as in an automotive application, a second internal path can be selected leading to a different LNA (LNA2) with lower gain (12 vs. 18 dB) and a slightly higher noise figure (1.5 vs. 0.8 dB), resulting in a power savings to the user (16-19 vs. 18-21 mA @3V in default mode). A voltage is provided at pin 3 specifically to bias the active device. While it can be turned off by SPI control for passive antenna applications, if it is enabled, LNA selection can be done automatically depending on whether there is an active antenna present.

In the LNA-gated mode, the receiver is configured to automatically switch between the two LNA's depending on whether a load current in excess of 1.5mA is detected at the antenna bias pin. A user would then not need separate designs for applications using active and passive antennas. The chip would automatically select the appropriate LNA for any application. If not desired, the automatic LNA selection could be disabled through Config1 <14:13>.

The default LNA (LNA1) could also be used with an active antenna in ultra-low power mode, yielding a still respectable 2.7-3 dB cascaded NF, 14 dB nominal first stage gain, and a considerable power savings (13 to 15 mA @3V). However in this mode, the IP3 is reduced about 15dB, compromising immunity to nearby transmissions, so this mode should only be used in specialized applications requiring the very lowest power consumption.

Internal capacitive load trimming for crystal references.
When using this device with a crystal reference, no tuning of external load capacitors is required to match devices – a bank of internal crystal load capacitors can be programmed thorough SPI commands to trim the load to yield the correct reference frequency. The internal bank can be programmed over a range of about 11 to 17 pF. A single series capacitor is placed between the crystal and the crystal/reference input. If the desired load value is between 11 and 17 pF, the value of this coupling capacitor can be made large, say 10 nF, so as not to affect the programmed value. For crystals with load capacitances below 11 pF, the coupling capacitor can be made small to add in series with the internal bank, reducing the load seen at the device. Either way, the final frequency trimming can be done internally through SPI control.

Reference and IF Frequency Flexibility.
The design accommodates a wide range of reference frequencies between 8 and 44 MHz with a default setting of 16.328 MHz, and the IF frequency is adjustable in 63 steps between 0 and 12.5 MHz, with a default setting of 4.092 MHz. (It is however recommended that the IF frequency be kept at or below 4.092 MHz as additional steps may need to be taken to assure stability at higher frequencies). Because of a fractional-N synthesizer that permits small step size while maintaining excellent phase noise, this flexibility does not compromise performance. No other product on the market has this degree of flexibility.

IF Filter Flexibility.
Filtering at IF is important as it limits the noise bandwidth and improves sensitivity while eliminating interference. The MAX2769 IF filtering is highly flexible. There is a choice of either a 3^{rd} or 5^{th} order complex poly-phase Butterworth bandpass or lowpass designs, with programmable center frequencies corresponding to the IF frequency selected. The 3dB bandwidths can be selected as 2.6, 4.6, 8.6 or 24 MHz. Users can select a design that optimizes performance for their application.

An improvement over the previous generation tuner (MAX2741), is that a 4.8 MHz fixed low-pass filter is no longer the only option for selecting the 4.092 MHz IF. In the MAX2769, a 2.6 MHz bandpass design can also be employed, reducing the noise bandwidth by nearly 3 dB and enhancing system sensitivity. For IF frequencies below 1.6 MHz, the 2.6 MHz low-pass option might be more appropriate. Filters are designed to have no more than 1dB droop at $f_c \pm 1.023$ MHz.

High system gain with a wide range of level control.
To use the device without an active antenna in a low signal strength environment, it is imperative that the receiver have sufficient gain. The MAX2769 has typically up to 115 dB available gain (in default mode) with 60-65 dB of gain adjustment.

Access to the amplified RF signal for Coexistence Filtering.
While no external filtering is required for stand-alone applications, coexistence with cellular or WiFi transmissions in close proximity may require additional filtering to

prevent overdriving the GPS receiver front end. On the MAX2769, the RF signal has been made accessible between the first LNA stage output and mixer input (pins 2 and 5 respectively). If filtering is not desired these ports can be connected through a coupling capacitor. However, filtering introduced at this point will have minimal effect on the excellent sensitivity of the receiver. (For instance, for typical device parameters, a SAW filter with 1 dB insertion loss would degrade cascaded NF (and thus GPS sensitivity) by only about 0.15 dB.

It was demonstrated on the MAX2741 GPS receiver IC that a simple/ inexpensive LC filter preceding the LNA, followed by a SAW filter placed after the first stage LNA will provide immunity to 2.45GHz WiFi transmissions of up to +8 dBm (received at the GPS antenna), while causing only a fraction of a dB reduction in sensitivity. Using the same approach, the MAX2769 GPS receiver can be placed in small enclosures such as PDA's and cell phones and coexist with their transmissions.

Flexibility of Output modes.
Most GPS receivers provide only a single output mode. The MAX2769 output can be programmed to be analog, CMOS, or limited differential logic, in unsigned or complimentary binary format, with one to three bits output from the ADC.

Temperature sensor and status monitoring.
A temperature sensor is included which can be calibrated externally if desired. While lock detect status can be obtained at the LD pin, the part can be programmed to instead provide the output signal, the reference clock, results from a sigma-delta test, or fuse burn status at this port. It can also be programmed to provide a short to the active antenna, or to be an independent test point for voltage.

The part is programmed through ten registers across a 3-wire SPI interface. Registers are described in Table 1.

REGISTER	ADDRESS	FUNCTION	DEFAULT
CONF1<31:0>	0000	Configures RX and IF sections, Sets Antenna Bias and Auto LNA select	A2519A3
CONF2<31:0>	0001	Configures AGC and Output Format	02A821C
CONF3<31:0>	0010	Configures PGA, and details of AGC, Filtering, and Data Streaming	B4FB15C
PLLCONFIG <31:0>	0011	Sets PLL, VCO, and CLK Settings	9EC000E
DIV<31:0>	0100	Sets PLL Main and Reference Division Ratios	0C00080
FDIV<31:0>	0101	Sets PLL Fractional Div. Ratios	8000070
STRM<31:0>	0110	Configures DSP Interface frame streaming	8000000
CLK<31:0>	0111	Sets Fractional Clock Div. values	10061B2
TEST1<31:0>	1000	Sets up Test Mode	1E2D400
TEST2<31:0>	1001	Sets up Test Mode	2220000

Table 1: Description of SPI Configuration Registers

The details of these registers are given in the MAX2769 data sheet.

Appendix A
Suggested Test Procedure for Initial Device Characterization:

Refer to the Table 1 below which summarizes the parameters to be tested.

U8 should be installed - make sure only U8 or Y2 is installed. The software assumes a reference frequency of 16.368 MHz. If another frequency is used, change PLLCONFIG<22:21>. On the EV Kits, remove U28, R61, R62, R63, R64, R65, C68, and C69. C26 should be installed, but U11 should not be installed on the board. For cascade measurements, connect J8 to J12 using an RF cable. If you want to evaluate the SAW (U11) in cascade measurements, the trace from LNA OUT to the connector J8 and from the connector J12 to the MIX_IN should be cut by removing the capacitors at the break points in both traces.

For analog measurements (which cover steps 1-16 below), insert R47, R48, R52, and R54. This connects the output path through the differential-to-single-ended line receivers (MAX4444's) to ports J3 (I out) and J2 (Q out), where measurements can be made. A 50 ohm load (such as a cable to a spectrum analyzer) should be placed on the ports for correct loading. (Note that baluns T2 and T3 are not required and should not be loaded).

Jumpers should be set as follows:

Connect W1 –W9

Connect top two pins of W16, W17 (connecting signal paths), and W23 (shorting signal to ground)

Do not connect W13-W15, W18, and W28

For initial characterization in a MAX2769 EV Kit, the parameters listed in Table 2 can be measured. A suggested procedure for measuring these follows. The EV Kit data sheet should be consulted for more details. Some settings differ from default values to facilitate testing; users are free to select different settings.

A photograph of the MAX2769 EV Kit is shown in figure 2.

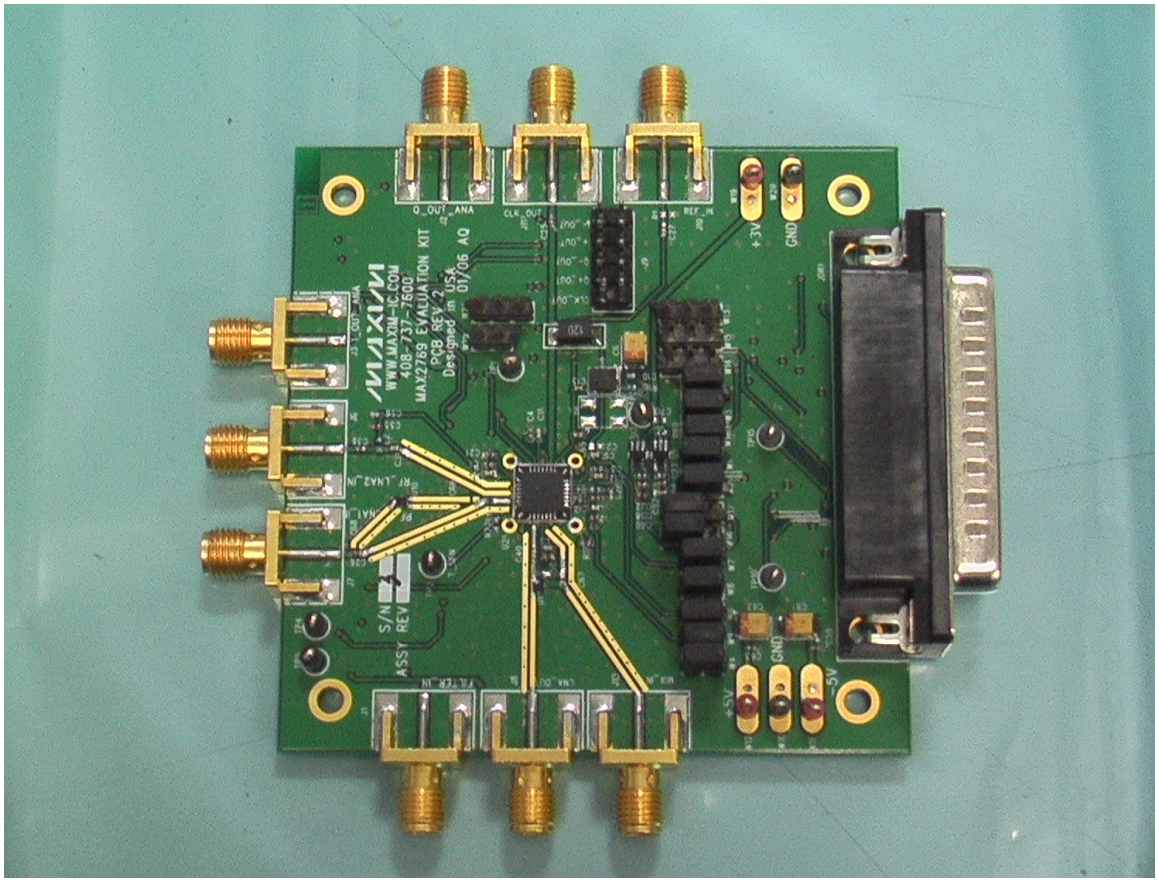

Figure 2. MAX2769 EV Kit

Parameter	Where measured (pins) on device	Where measured (connectors) on EV Kit	Target value
LNA1 gain	27-2	J7-J8	18 dB
LNA2 gain	25-2	J6-J8	12 dB
System IP3 w/LNA1	27-18	J7-J2	-25 dBm
System IP3 w/LNA2	25-18	J6-J2	-23 dBm
LNA1 NF (default mode)	27-2	J7-J8	0.8 dB
LNA2 NF	25-2	J6-J8	1.5 dB
Cascaded system NF, LNA1	27-18	J7-J2	1.5 dB
Cascaded system NF, LNA2	25-18	J6-J2	3.5 dB
Current consumption (default mode, LNA1)	11,13,14,19,23	W19, W20, W11, W12	21 mA (36 mA @3V, 140mA @±5V, EV Kit)
IF Out Gain range (4.092 MHz IF)	27-18	J6 or J7-J2	55-115dB
3 dB IF filter passband	27-18	J7-J2	2.6 MHz (default)
4 MHz offset filter rejection	18	J7-J2	29dB (3rd order BPF) 48dB (5th order BPF)
Digital output	25, 27 – 17, 18, 20, 21	J12-J9	CMOS square wave with 50% duty cycle
AGC Function	25, 27 – 17, 18, 20, 21	J12-J9	Flat, -105 to -65 dBm in

Table 2: Parameters to be tested in suggested procedure

LNA1 tests (default current mode):

1) Apply 3V, ±5V, GND, at W19, W20, W11, and W12.

2) Run software to set up new default register configurations as shown in the appendix. (Note these are not necessarily default values). Make sure SHDN and IDLE are set to 1, the disabled state for both.

3) Measure current consumption at W19, W20, W11, and W12, at +3, +5, and -5V.

4) To establish PLL lock, look at mixer-in port (J12) for the presence of the LO at 1571.328 MHz. This will be a weak signal around -70 MHz. You may also look for the VCO signature at 3142.656 MHz. This will be around -55 to -60 dBm.

5) Input a -60 dBm 1575.42 MHz CW signal at J7. Measure and record LNA1 gain between J7 and J8 (this assumes that the path to J8 is connected and U11 is not loaded). Raise level until you get 1 dB compression to get P1dB. Be sure to correct for line losses, roughly 1 dB.

6) Inject a -80 dBm signal at J12. Measure gain with default settings by monitoring the 4.092 MHz output at J2. Gain should be around 68 dB, resulting in a -12dBm output. (Split the signal using a BNC tee at J2 output with one end going into the spectrum analyzer and the other to an oscilloscope. Monitor the signal on the scope - you should see a sine wave output. Use the 1M input on the scope so there is no loss at the spectrum analyzer input. DC-couple signal and monitor DC offset. It should be no more than 50-60 mV.)

7) Raise the input level, monitoring the output at J2. Raise level until you get 1 dB gain compression. This will be at around Pout = 10 dBm.

8) Raise gain by setting <3:27-22> to 63 (Config 3: FEFE15C). Reduce input to around -115 dBm or lower so as not to compress the output (note value of P1dB from previous step). Record maximum cascaded gain. This should be 115 dB. Total gain is this result plus the LNA gain from step 5. Record this. Measure minimum gain as well by setting <3:27-22> =0 (Congig.3: 02F15C).

9) With default gain setting (<3:27-22> = 58), measure IP3 using LNA1. Combine two sources at -60 dBm input at F1=1587.42 MHz and F2=1599.42 MHz (where 2*F1-F2 falls in-band at 1575.42 MHz) and inject into J7. Measure strength of 4.092 MHz product at J2 (Q out). Note: analog mode must be selected. Drop both inputs 1 dB and note that product drops by 3 dB. (If not, you are compressing and need to use a lower input level.) A typical signal level for a -60 dBm input would be -45 dBm. G=86 dB for nominal settings (68 dB from mixer-in onward +18 dB LNA1). For this example, IP3 in = (3*Pout – product)/2 – Gain = (3*(-60+86)-(-45))/2-86 = 61.5-86 = -24.5dBm.

10) Measure LNA1 noise figure if NF meter available. Otherwise, measure NF of the cascaded chain can be determined by setting gain to max. (see step 8), reducing spectrum analyzer resolution bandwidth and measuring output S/N ratio. For example, using a 300 Hz RBW, the input noise would be -174dBm/Hz * 27dB Hz = -147 dBm. For example, with an input of -110 dBm and with 112 dB gain for the system, the receiver will not be in compression. The input S/N would therefore be -110 – (-147) = 37 dB. We might measure an output signal at J2 of 2 dBm and a background noise level of -32 dBm, yielding a SNR around 34 dB. The noise figure of the system would then be the degradation in the S/N ratio, or 3 dB. The result is approximate as measurement precision is poor. Record this value.

    Alternatively, if a noise source is available, a more accurate y-factor method could be used for the cascaded noise figure. Be certain to de-embed the input

losses on the board of roughly 0.5 dB from the measured result.

11) Set up nominal gain and use an input level at J12 at least 10dB below value that leads to 1dB compression, typically -80 dB. Sweep input frequency from 1572.9 to 1577.9 MHz to yield pass band of IF BPF filter (2.6MHz). Set the filter BW to 4.6 MHz <1:4-3> = 01 (Config. 1: A2519BB). Sweep input frequency from 1571.9 to 1578.9 MHz. This measurement can be made by using the max. hold option on the spectrum analyzer and ideally you can capture the screen view which shows a plot of the spectrum and include this in the IPS. Otherwise, indicate the flatness across the frequency spectrum in a table or EXCEL plot.

12) Raise input frequency to 1579.42 MHz and record attenuation at 4 MHz offset (8.092 MHz) relative to gain at center band. Select 3rd order IF filter (CONF1<2> = 1) and repeat measurement. Reset to default 5th order filter (CONF1<2> = 0).

13) Set up the AGC in the autonomous mode (CONF2<12:11> = 00), and analog output mode, feed into the LNA1 input a signal at -105dBm and select LNA1. Note the tone power at the output while raising the input level to -65dBm. It should remain approximately the same.

LNA2 Tests

14) Switch to LNA2 (CONF1<14:13> = 01). Input a -60 dBm 1575.42 MHz CW signal at J6. Measure LNA2 gain at J8 and record. Raise level until you get 1 dB compression to get P1dB. Total gain is the linear gain measured here plus the gain from the mixer-in port to J2 from step 8. Record this value.

15) If NF meter available, measure LNA2 noise figure between J6 and J8. Otherwise, measure NF following procedure of step 10 above.

16) With default gain setting (<3:27-22> = 58), measure IP3 using LNA2. Combine two sources at -60 dBm input at F1=1587.42 MHz and F2=1599.42 MHz (where 2*F1-F2 falls in-band at 1575.42 MHz) and inject into J6. Measure strength of 4.092 MHz product at J2 (Q out). Note: analog mode must be selected. Drop both inputs 1 dB and note that product drops by 3 dB. (If not, you are compressing and need to use a lower input level.) A typical signal level for a -60 dBm input would be -45 dBm. G=86 dB for nominal settings (68 dB from mixer-in onward +18 dB LNA1). For this example, IP3 in = (3*Pout – product)/2 – Gain = (3*(-60+86)-(-45))/2-86 = 61.5-86 = -24.5dBm.

Digital Tests

For digital measurements, R47, R48, R52, and R54 should be removed, isolating the signals from the MAX4444's. (Once again baluns T2 and T3 are not required and should not be loaded). Measurements can be made at J9 A, B, C, and D. Signals are also sent to a 74LV07 driver chip for buffering and passed back to the computer on connector JDR1. If customers want to process these output signals, for instance in a soft GPS application, they can access them at either J9 or JDR1.

17) Change to a digital output (CONFIG<2:10-9>=01), and monitor the signal at the scope. You should have a square wave CMOS output (2.8V amplitude) at J9.

18) Feed a -60 dBm 1570 MHz input into the Mixer-in port (J12). The IF baseband signal should appear at 1.328 MHz. Check the duty cycle of the 0.75 us output signals at J9: Q_OUT+ output should exhibit a near-50% duty cycle square wave. Q_OUT- output should display a more complicated waveform with the correct density.

Appendix: Suggested Register Settings for Initial Test

Config1: Test: A2951A7
This register:

enables the chip (default)
disables the idle (default)
sets default current programming
sets non-default LO current programming
sets default mixer current programming
selects 13 MHz passive filter pole at mixer output (default)
selects LNA1 output (default is gated mode)
enables mixer (default)
turns off bias to external active antenna (default is bias on)
selects Fc=4.092 MHz
selects 2.6 MHz polyphase IF BP filter
selects 26 dB IF filter gain (default is 17 dB)

Config2: Test: 0A0328C
This register:

selects I channel only (default)
sets AGC gain to 320 (default is 170)
sets bit counter length to 1024 bits (default is 256)
selects sign/magnitude output format (default)

selects 2-bit AGC (default is 1-bit)
selects a CMOS output driver (default is limited differential logic)
disables LO buffer (default)
enables temperature sensor (default)

Config3: Test: EAFE15C
This register:

sets the PGA gain for level/LSB at 58 (default is 45)
chooses the nominal ADC input scale (default)
selects the nominal loading for the output driver (default)
enables the ADC (default)
enables the output driver (default)
enables the filter DC offset cancellation circuitry (default)
enables the IF filter (default)
enables AGC for both channels (default is I enabled only)
enables high pass coupling between the filter and AGC (default)
sets a 50KHz high pass pole corner frequency (default is 20 KHz)
selects no DSP interface for data streaming (default)
sets the default data counter length
selects 2-bit streaming (default)
enables sync pulse outputs (default)
enables frame sync pulse outputs (default)
disables data sync pulse outputs (default)
disables DSP interface reset (default)

PLL Config: Test: 9EC0008
This register:

enables the VCO in normal current mode (default)
disables external VCO bias compensation (default)
sets clock output driver to CMOS mode (default)
sets clock frequency to XTAL frequency
selects buffer nominal current of 130 mA for crystal (default, range is 130 to 700 mA)
sets capacitive load programming to 3.6 pF (default, nominal for C_L>12 pF)
selects PLL lock detect as output at LD pin (default)
selects nominal change pump operation with 0.5 mA current (default)
selects 2ns. charge pump on-time selection (default)
selects integer-N PLL (default is non-integer-N)
disables power save (default is power save enable)
selects low current mode for prescalar E2C's (default is high current mode)

PLL Division: Test: 0C00080
This register:

sets N=1536 for low side injection (default, LO = 1536 x 1.023 MHz = 1571.328 MHz)
sets R=16 (default, step size = 16.368 MHz / 16 = 1.023 MHz)

PLL Fractional Divide: Test: 8000070
This register:

sets fractional division ratio = 80000 (default)
selects nominal current and filter trim values

STRM: Test: 8000000
This register:

sets nominal stream interface control to start at a frame given by FRAME_COUNT

CLK: Test: 10061B2
This register:

sets the L counter to 256
sets the M counter to 1563
selects a fractional clock input to the fractional clock divider to come after the reference divider
selects the serializer clock to come from the reference divider
TEST1: Test: 1E3C400
This register:

Sets nominal gain hysteresis (default)
Sets high side DC offset hysteresis setting at 3, (default is 2)
Sets low side DC offset hysteresis setting at 12, (default is 13)
disables filter trim control by SPI (default)
disables ADC and PGA testing at PGMCNTL and ANT_FLAG pins (default)
disables DSP interface test (default)

TEST2: Test: 1440000
This register:

sets filter op-amp input stage current programming to 50uA for 1st and 100uA for subsequent op amps (default is 100uA for 1st and 50 uA for subsequent op amps)
sets filter op-amp output stage current programming to 10uA for 1st and 40uA for subsequent op amps (default)

disables filter testing and temperature sensor calibration through SPI lines (default)
selects nominal temperature sensor calibration with word set to 32 (default)

The screen format for setting configurations is shown in figure 3.

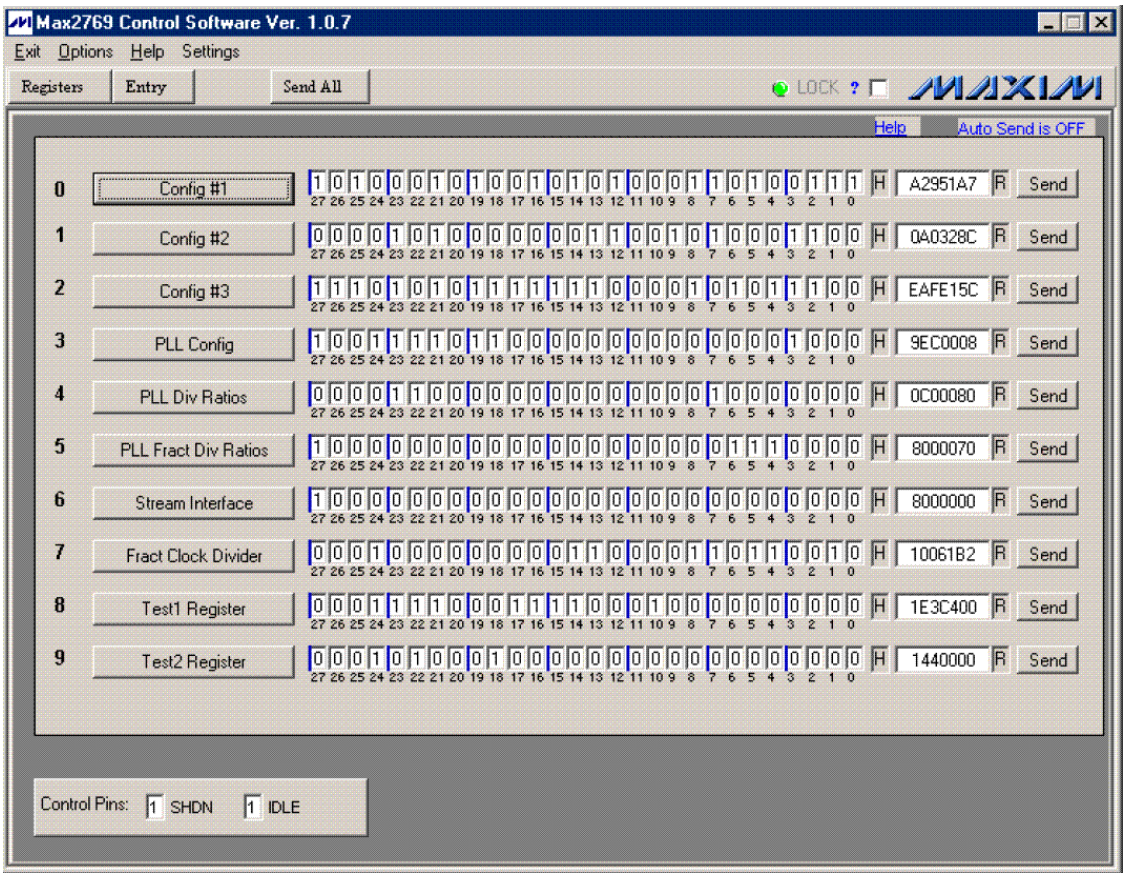

Figure 3 : EV Kit Test Software screen format showing suggested settings