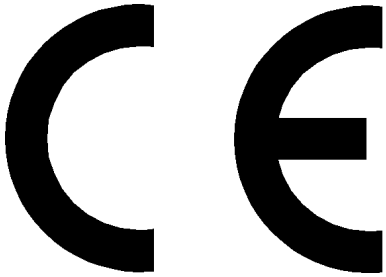
NEC

User's Manual

K_Line – Play it!

Demonstration Kit for the K_Line Family

Document No. K_LINEPLAYITV100
Date Published December 2002



K_Line - Play it! complies with the EMC protection requirements

CAUTION

This equipment should be handled like a CMOS semiconductor device. The user must take all precautions to avoid build-up of static electricity while working with this equipment. All test and measurement tool including the workbench must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare hands.

EEDT-ST-004-10

Revision History

Date	Revision	Chapter	Description
06-12-2002	V1.0	---	First release

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1. Introduction

K_Line – Play it! is a battery powered demonstration kit for the NEC's microcontroller family. It supports download and real time execution of small application programs up to 1 KBytes of program code for the 78K CPU module and up to 4 KBytes of program code for the V850 CPU module. The board is prepared to be connected to user hardware parts such as digital I/O or analogue signals.

1.1 Main features of *K_Line – Play it!*

- Easy to use device demonstration capabilities
  K_Line - Play it! contains elements to easily demonstrate simple I/O-functions, i.e. push buttons, LED output, AD reference voltage, I/O lines, RS232 serial interface.

- Battery powered
  K_Line - Play it! is battery powered for portability reasons.

- Serial communication interface program
  A Windows based download GUI allows to select and download application programs to *K_Line - Play it!* for evaluation purposes.

- Analogue to digital signal conversion is supported

- Various input / output signals available, such as

  - All I/O ports prepared to be connected to user hardware
  - Timer input / output signals
  - Two or three wire serial I/O
  - RS232 signals including RTS / CTS
  - 5 analogue input lines
  - 9 I/O ports connected to LED
  - 2 push buttons prepared for external interrupt generation

- Embedded Workbench for 78K0/K0S and 78K0 System Simulator / Debugger are included. These packages are restricted in such that maximum program code size is limited to 4 KB of program code.

- Embedded Workbench for V850 and C-Spy Simulator / Debugger are included. These packages are restricted in such that maximum program code size is limited to 4 KB of program code.

- Full documentation is included for the NEC 78K0/KF1, NEC V850ES/KF1, IAR Systems Embedded Workbenches, IAR Systems C-Spy and NEC 78K0 System Simulator.

***K_Line - Play it!* is not intended for code development. NEC does not allow and does not support in any way any attempt to use *K_Line - Play it!* in a commercial or technical product.**

1.2 System requirements

HOST PC

A PC supporting Windows 95, Windows 98, Windows NT, Windows 2000 or Windows XP is required for the IAR Systems Workbench- and NEC Simulator-demo-version.
Pentium 166 MHz (at least), 64 MB of RAM, 256-color display (1024 * 768), mouse, CD-ROM drive and 40 Mbytes of free hard disk space are required to install the tool packages.

Above listed requirements are valid if the IAR Systems Embedded Workbench or the NEC System Simulator shall be installed. The communication interface program does not need to be installed to the local hard disk. It can be started from the CDROM.

Host interface

Serial (RS232C) interface capable to handle communication at 9600 baud.

1.3 Package contents

Please verify that you have received all parts listed in the package contents list attached to the *K_Line - Play it!* package. If any part is missing or seems to be damaged, please contact the dealer from whom you received your *K_Line - Play it!*.

Note: Updates to this User Manual, additional documentation and/or utilities for *K_Line - Play it!*, if available, may be downloaded from the NEC WEB page(s) at **http://www.ee.nec.de/updates**.

2. *K_Line - Play it!* system configuration

The *K_Line - Play it!* system configuration is given in the diagram below:

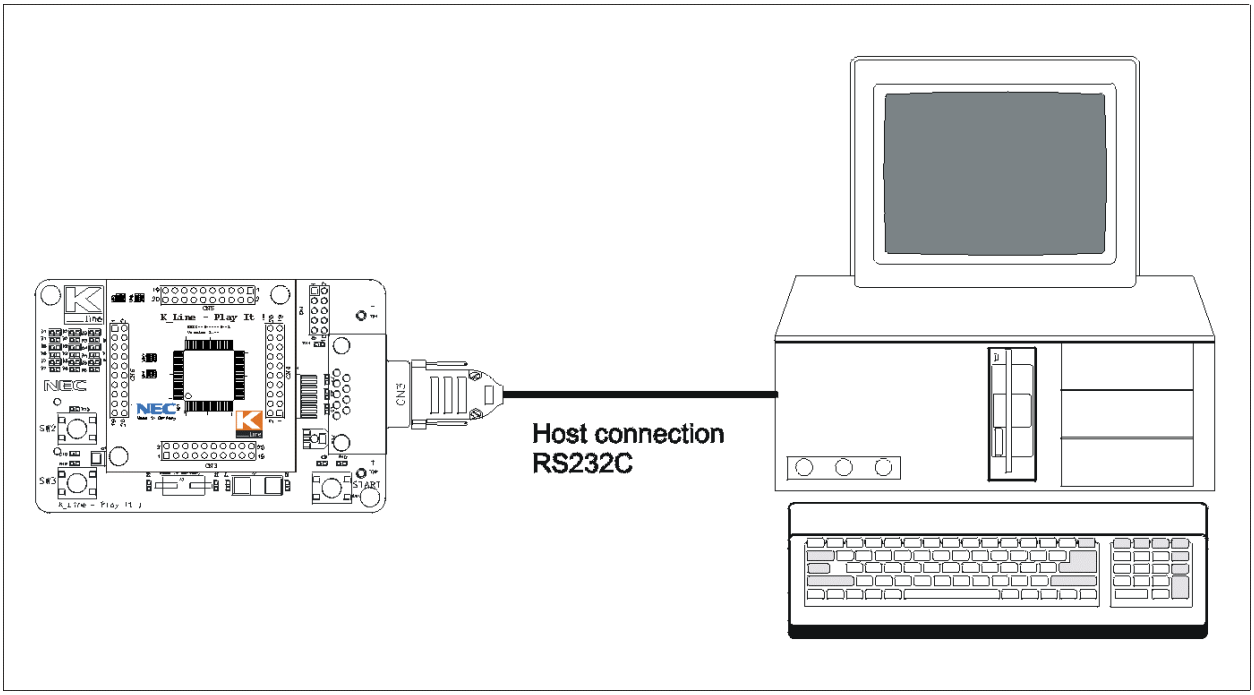


Figure 1: *K_Line - Play it!* system configuration

2.1 *K_Line - Play it!*

K_Line - Play it! is a demonstration kit for the NEC K_Line family devices. Two CPU modules are included each using a KF1 device as a typical device from K_Line with 78K0 and V850ES core.
It is equipped with a serial interface and a small monitor program to accept download program files for program execution.
The *K_Line - Play it!* board is connected to the host system via RS232C serial interface cable. The host system may be used to download and start application programs on *K_Line - Play it!* platform.
K_Line - Play it! runs both CPU modules at 8.0000 MHz operating speed. Sub-clock is provided with 32.768 kHz.

2.2 Host computer

The RS232 host interface enables communication to the *K_Line - Play it!*. RS232 data transfer speed must be set to 9600 bps.

For a detailed specification of the host interface please refer to the chapter “Connectors and Cables” of this document.

2.3 Battery power supply

The *K_Line - Play it!* is equipped with three batteries of AA type.

Before using *K_Line - Play it!* please remove the isolation strip inserted between the battery and the battery holder.

Please note that a battery voltage below 3V may cause malfunction of the serial interface driver.

Note: The built-in monitor program switches *K_Line - Play it!* to a power saving STOP mode in case serial communication is not established within ten minutes after power on. Press the START button to switch *K_Line - Play it!* back to operation mode.

3. *K_Line - Play it!* Baseboard components

The *K_Line - Play it!* baseboard is equipped with push buttons, LEDs and with several connectors in order to be connected to host computers an Flash-programmer.

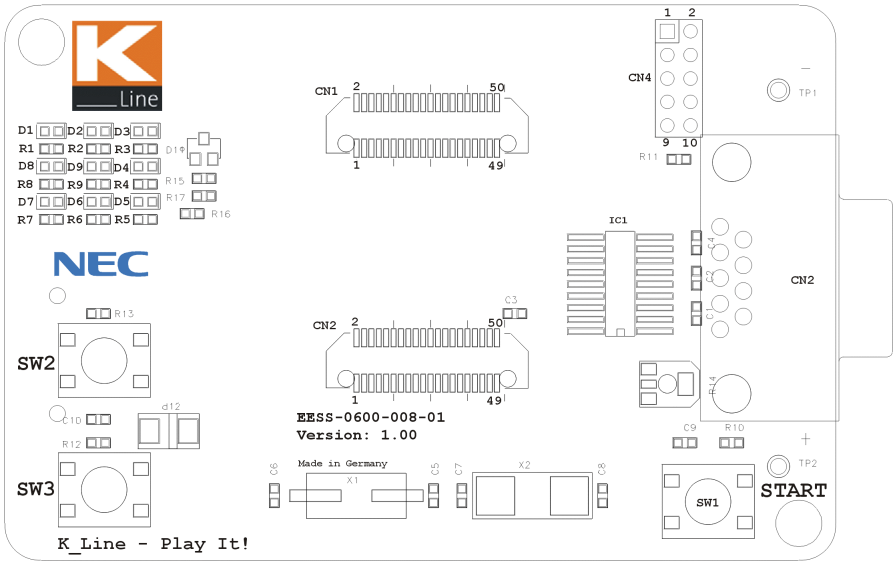


Figure 2: *K_Line - Play it!* baseboard connectors, switches and LEDs

Some of the *K_Line - Play it!* components are free for user application hardware and software. Please read the user's manual of the 78K0/KF1- and the V850ES/KF1-device carefully to get information about the electrical specification of the available I/O ports before you connect any external signal to the *K_Line - Play it!* board!

3.1 Start button SW1

SW1 is a reset button. It activates the power on reset. It is connected to the reset input of CPU module.

3.2 User button SW2

SW2 is a push button connecting V_{CC} to external interrupt input INTP2 of the CPU module. This is port P31 of the 78K0 CPU module and port P05 of the V850ES CPU module. The port may be programmed to generate interrupt INTP2. The necessary initialisation for this purpose is described in the user's manual of the 78K0/KF1- and the V850ES/KF1-device. The port is connected to a 1.2K pull down resistor.

3.3 User button SW3

SW3 is a push button connecting V_{CC} to external interrupt input INTP3 of the CPU module. This is port P32 of the 78K0 CPU module and port P06 of the V850ES CPU module. The port may be programmed to generate interrupt INTP2. The necessary initialisation for this purpose is described in the user's manual of of the 78K0/KF1- and the V850ES/KF1-device. The port is connected to a 1.2K pull down resistor.

3.4 RS232 serial interface connector CN3

RS232 interface lines are connected to UART6 of the 78K0/KF1- and UART0 of the V850ES/KF1-device via a 9pin female Sub-D connector CN3.The control lines RTS and CTS are connected as well.

CN3	Port 78K0/KF1	Port V850ES/KF1	RS232
1	--	--	NC
2	RXD6	RXD0	RxD
3	TXD6	TXD0	TxD
4	--	--	NC
5	--	--	Ground
6	--	--	NC
7	P17	P33	CTS
8	P16	P32	RTS
9	--	--	NC

Table 1: CN3 connection to RS232 and 78K0/KF1 or V850ES/KF1 respectively

For program download serial communication speed is fixed to 9600 baud. Data format is 8 data bits, 1 stop bit, no parity.
If the serial interface is used from a downloaded application program, any other communication speed or data format may be used according to the 78K0/KF1- and the V850ES/KF1- capabilities. Please refer to the user's manuals for details.

Note: P141 at 78K0/KF1 or P35 at V850ES/KF1 respectively output signal may be used to shut down the MAX3222 serial line driver. It is recommended to shut down the MAX3222 driver if the serial interface is not used. This will extend the battery life time.
A low signal output at P141 or P35 respectively will shut down the MAX3222. A high signal will wake up MAX3222.
P140 at 78K0/KF1 or P34 at V850ES/KF1 respectively output signal must be set to low signal to enable MAX3222.

3.5 Connector CN1 and CN2

CN1 and CN2 are connectors for the CPU module.

3.6 Connector CN4

CN4 connector allows connecting the PG-FP4 flash programmer to K_Line - playing *it!* in order to program application programs into the CPU internal flash memory of the connected CPU module. PG-FP4 is a separate product from NEC and it is not included in this package.

3.7 External Potentiometer R1

A 10K potentiometer R1 is connected between P46 of 78K0/KF1 or PCT6 of V850ES/KF1 respectively and ground. The potentiometer arm is connected to ANI2 analogue input.

3.8 AD converter reference voltage input

A 1.235V reference voltage is connected to ANI0 input. The reference voltage must be enabled by port P44 of 78K0/KF1 or PCT4 of V850ES/KF1 respectively.

3.9 Supply voltage monitor

For reference purposes V_{CC} / 2 is connected to ANI3 input. The supply voltage monitor must be enabled by port P41 of 78K0/KF1 or PCT1 of V850ES/KF1 respectively.

3.10 External LED1 – LED9

LED9 to LED1 are LED connected to P7 of the 78K0/KF1. LED9 is an LED connected to P50 of the 78K0/KF1. For V850ES/KF1 port PDL15 to PDL8 are connected to LED8 to LED1. LED9 is an LED connected to PDL0 of V850ES/KF1.

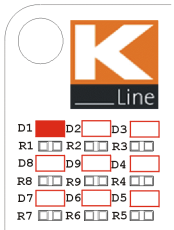
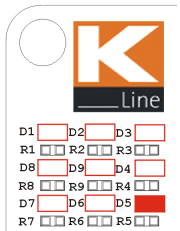
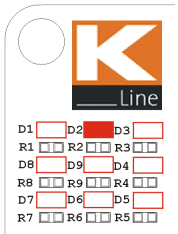
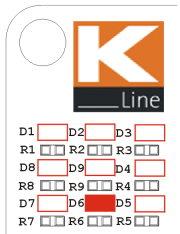
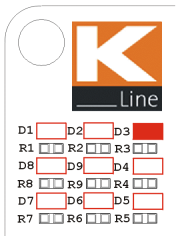
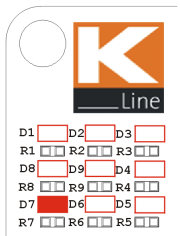
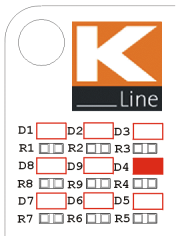
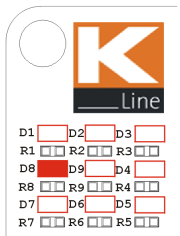
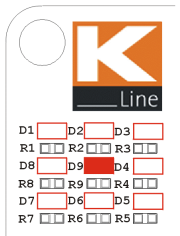
Port	Segment	Display	Port	Segment	Display
P77 78K0/KF1 PDL15 V850ES/KF1	LED1		P73 78K0/KF1 PDL11 V850ES/KF1	LED5	
P76 78K0/KF1 PDL14 V850ES/KF1	LED2		P72 78K0/KF1 PDL10 V850ES/KF1	LED6	
P75 78K0/KF1 PDL13 V850ES/KF1	LED3		P71 78K0/KF1 PDL09 V850ES/KF1	LED7	
P74 78K0/KF1 PDL12 V850ES/KF1	LED4		P70 78K0/KF1 PDL08 V850ES/KF1	LED8	
			P50 78K0/KF1 PDL00 V850ES/KF1	LED9	

Table 2: LED1 – LED9 connection

A low signal output at each port switches the corresponding LED on.

4. *K_Line - Play It! CPU module* components

Both K_Line - Play It! CPU modules are equipped with 4 connectors in order to be connected to user defined hardware. One module is the 78K0/KF1 CPU and the other for the V850ES/KF1 CPU

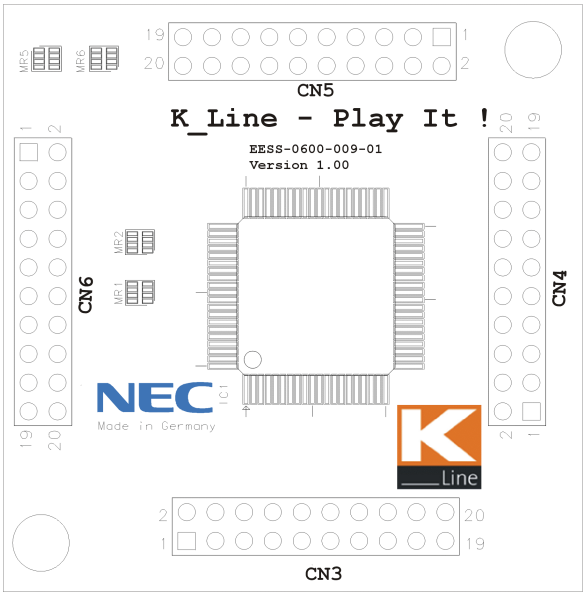


Figure 3: *K_Line - Play It!* CPU module components

4.1 External connector CN3,CN4, CN5, and CN6

CN3, CN4, CN5, and CN6 are connectors for external user hardware. The pinning is different for each CPU module.

CN3	Port 78K0/KF1
1	AV_{REF}
2	AV_{SS}
3	P120, INTP0
4	P33,TI51,TO51,INTP4
5	P32, INTP3
6	P31, INTP2
7	P30, INTP0
8	IC, V_{PP}
9	V_{DD}
10	REGC
11	V_{SS}
12	X1
13	X2
14	RESET
15	XT1
16	XT2
17	P130
18	P10, SCK10, TxD0
19	P11, SI10, RxD0
20	P12, SO10

CN4	Port 78K0/KF1
1	P13, TxD6
2	P14, RxD6
3	P15, TOH0
4	P16, TOH1, INTP5
5	P17, TI50, TO50
6	P140, PCL, INTP6
7	P141, BUZ, BUSY0, INTP7
8	P63
9	P62
10	EV_{SS}
11	EV_{DD}
12	P61
13	P60
14	P142, SCKA0
15	P143, SIA0
16	P144, SOA0
17	P145, STB
18	P06, TI011,TO01
19	P05, SSI11, TI001
20	P04, SCK11

CN5	Port 78K0/KF1
1	P03, SI11
2	P02, SO11
3	P01, TI010, TO00
4	P00, TI000
5	P67, ASTB
6	P66, WAIT
7	P65, WR
8	P64, WD
9	P57, A15
10	P56, A14
11	P55, A13
12	P54, A12
13	P53, A11
14	P52, A10
15	P51, A9
16	P50, A8
17	P47, AD7
18	P46, AD6
19	P45, AD5
20	P44, AD4

CN6	Port 78K0/KF1
1	P43, AD3
2	P42, AD2
3	P41, AD1
4	P40, AD0
5	P77, KR7
6	P76, KR6
7	P75, KR5
8	P74, KR4
9	P73, KR3
10	P72, KR2
11	P71, KR1
12	P70, KR0
13	P27, ANI7
14	P26, ANI6
15	P25, ANI5
16	P24, ANI4
17	P23, ANI3
18	P22, ANI2
19	P21, ANI1
20	P22, ANI0

Table 3: CN3, CN4, CN5, and CN6 connection to 78K0/KF1

CN3	Port V850/KF1
1	AV_{REF}
2	AV_{SS}
3	P00, TOH0
4	P01, TOH1
5	P02, NMI
6	P03, INTP0
7	P04, INTP1
8	IC, V_{PP}
9	V_{DD}
10	REGC
11	V_{SS}
12	X1
13	X2
14	RESET
15	XT1
16	XT2
17	P05, INTP2
18	P06, INTP3
19	P40, SI00
20	P41, SO00

CN4	Port V850/KF1
1	P42, SCK00
2	P30, TxD0
3	P31, RxD0
4	P32, ASCK0
5	P33, TI000,TO00
6	P34, TI001
7	P35, TI010, TO01
8	P38
9	P39
10	EV_{SS}
11	EV_{DD}
12	P50, TI011, RTP00, KR0
13	P51, TI50, RTP01, KR1
14	P52, TO50, RTP02, KR2
15	P53, SIA0, RTP03, KR3
16	P54, SOA0, RTP04, KR4
17	P55, SCKA0, RTP05, KR5
18	P90, TxD1, KR6
19	P91, RxD1, KR7
20	P96, TI51, TO51

CN5	Port V850/KF1
1	P97, SI01
2	P98, SO01
3	P99, SCK01
4	P913, INTP4
5	P914, INTP5
6	P915, INTP6
7	PCS0, CS0
8	PCS1, CS1
9	PCM0, WAIT
10	PCM1, CLKOUT
11	PCM2, HLDAK
12	PCM3, HLDRQ
13	PCT0, WR0
14	PCT1, WR1
15	PCT4, RD
16	PCT6, ASTB
17	PDL0, AD0
18	PDL1, AD1
19	PDL2, AD2
20	PDL3, AD3

CN6	Port V850/KF1
1	PDL4, AD4
2	PDL5, AD5
3	PDL6, AD6
4	PDL7, AD7
5	PDL8, AD8
6	PDL9, AD9
7	PDL10, AD10
8	PDL11, AD11
9	PDL12, AD12
10	PDL13, AD13
11	PDL14, AD14
12	PDL15, AD15
13	P77, ANI7
14	P76, ANI6
15	P75, ANI5
16	P74, ANI4
17	P73, ANI3
18	P72, ANI2
19	P71, ANI1
20	P70, ANI0

Table 4: CN3, CN4, CN5, and CN6 connection to V850ES/KF1

4.2 78K0/KF1 memory map

The 78K0/KF1 memory layout is shown in the table below.

Address area	0Xffff 0xFF00	SFR Area	Free for application software
	0xFEDF 0xFB00	Internal high speed RAM	
	0xFAFF 0xF800	Reserved	
	0xF7FF 0xF400	Internal expansion RAM	Used by application software
	0xF3FF 0xF000	External memory	
	0xEFFF 0x0000	Flash memory	Used by download monitor

Table 5: 78K0/KF1 memory map

4.3 V850ES/KF1 memory map

The V850ES/KF1 memory layout is shown in the table below.

Address area	0x3FFFFFF 0x3FFF000	SFR Area	Free for user application software
	0x3FFEFFF 0x3FFE800	Internal high speed RAM	
	0x3FFE7FF 0x3FFD800	Internal high speed RAM	Used by application software (*)
	0x3FFD7FF 0x1000000	Reserved	
	0x0FFFFFF 0x0100000	External memory	
	0x00FFFFF 0x0000000	Flash memory	Used by download monitor

Table 6: V850ES/KF1 memory map

(1): If the application code doesn't use the complete RAM area, this area can also be used as application RAM.

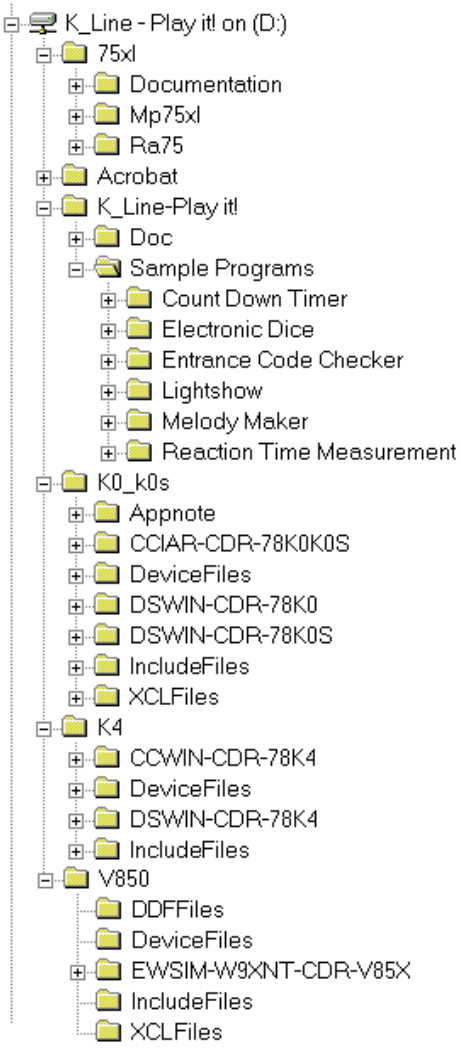
5. *K_Line - Play it!* installation and operation

5.1 Getting started

K_Line - Play it! is equipped with a simple download monitor that allows communication with a PC host system via RS232 serial interface line. Before you can run and download a program, hardware and software must be installed properly.

5.1.1 CD-ROM contents

The CD-ROM shows following directory structure:



CD-ROM ROOT
Demo for uPD75XL device family
- Documentation
- System Simulator 75XL
- Reloc. Assembler for 75XL
Acrobat Reader for 32Bit Windows OS
K_Line - Play it!
- Documentation
- Sample programs for …
… count down timer
… electronic dice
… entrance code checker
… lightshow
… melody maker
… reaction time measurement
78K0/K0S demo tools
- Application note 780034
- Embedded Workbench 78K0/K0S
- 78K0/K0S device files
- System Simulator 78K0
- System Simulator 78K0S
- 78K0/K0S include files
-78K0/K0S XLINK command file templates
78K4 demo tools
- Embedded Workbench 78K4
- 78K4 device files
- System Simulator 78K4
- 78K4 include files
V850 demo tools
- V850 DDF files
- V850 device files
- Embedded Workbench V850 (incl. C-Spy)
- V850 include files
- V850 XLINK command file templates

Table 7: K_Line - Play it! CD-ROM directory structure

5.1.2 Hardware installation

After unpacking *K_Line - Play it!* please remove the battery isolation strip inserted between the battery and the power connection on the back side of *K_Line - Play it!.*
After pressing the START button LED1 to LED8 will flash one after the other. If you press one of the buttons SW2 or SW3 the flashing speed will increase.
LED flashing indicates that *K_Line - Play it!* is ready to be connected to a host computer.

Connect *K_Line - Play it!* to your host computer using the provided serial interface cable. The communication speed is fixed to 9600 bps.

5.1.3 Software installation

The *K_Line - Play it!* package comes with the several software demo packages:

- IAR Systems Embedded Workbench for 78K0/K0S, including C compiler, assembler, linker and librarian
- NEC 78K0 System Simulator for 78K0
- IAR Systems Embedded Workbench for V850, including C compiler, assembler, linker and librarian
- IAR Systems Simulator C-Spy
- Communication interface for program download
- Sample programs

The IAR Systems Embedded Workbench and the NEC System Simulator must be installed on your PC. For detailed installation hints, refer to the documentation of the corresponding products.

The communication interface can be started from the CDROM without installation. Also sample programs can be downloaded end executed directly form the CDROM. Only if you intend to modify some of the sample programs it is necessary to copy them to your local hard disk.

5.1.3.1 IAR Systems Embedded Workbench for 78K0/K0S installation

To install the IAR Systems Embedded Workbench for 78K0/K0S, select the `SETUP` program in the directory `\k0_k0s\CCIAR-CDR-78K0K0S\CCIAR-CDR-78K0K0S\` of the CDROM.
The setup dialogues will guide you through the installation process.

5.1.3.2 NEC System Simulator 78K0 installation

To install the NEC System Simulator for 78K0, select the `SETUP` program in the directory `\k0_k0s\DSWIN-CDR-78K0\DSWIN-CDR-78K0` of the CDROM.
The setup dialogues will guide you through the installation process.

5.1.3.3 Device File installation

The System Simulator requires device files to be installed before it can be activated. The device file installer DFINST is part of the system simulator package and will be installed with the system simulator.
To install device files, activate DFINST from the installation directory of the system simulator:

Figure 4: DFINST device file installer

At startup, DFINST will show empty list boxes if no device files are installed on your PC:

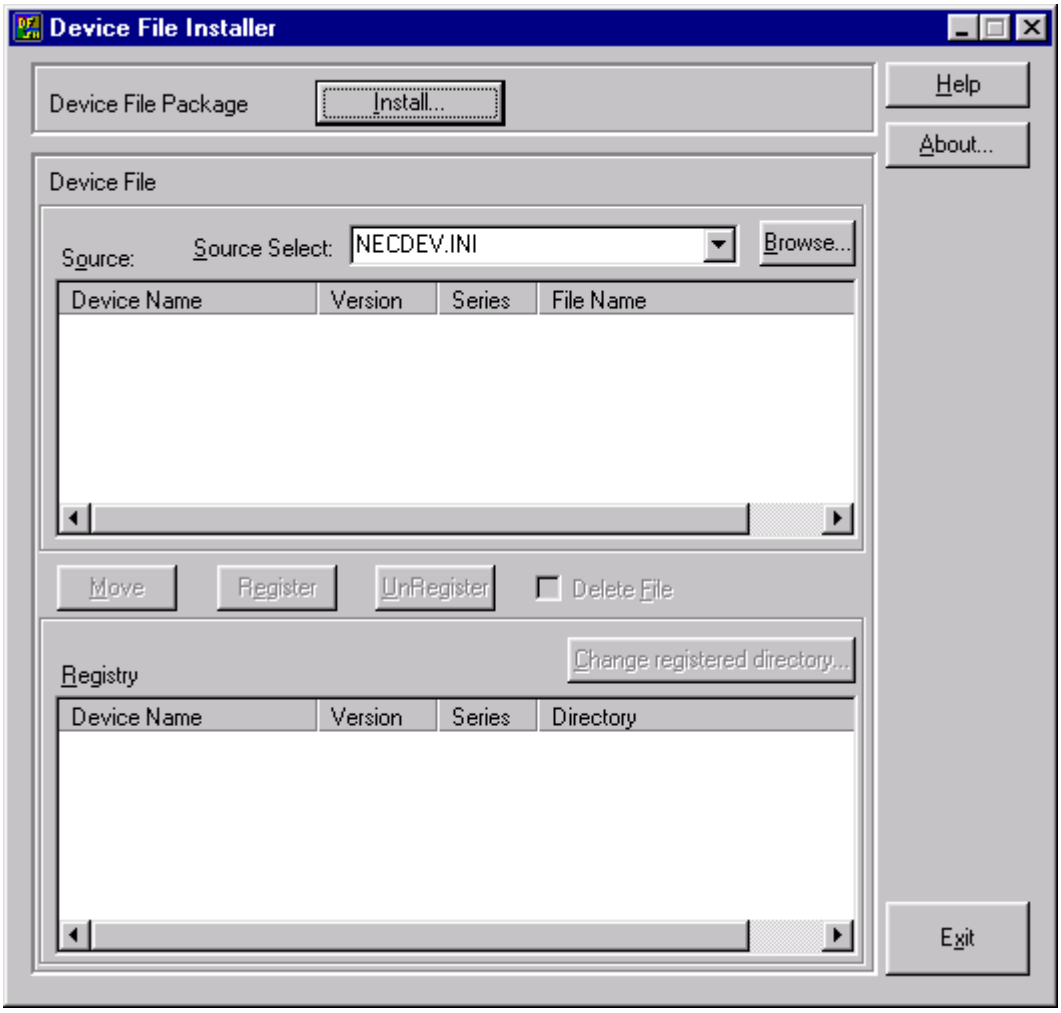


Figure 5: DFINST entry screen

Activate the **Browse** button and select the directory from the CDROM where device files are located. It is the `\78K0_K0S\devicefiles` directory:

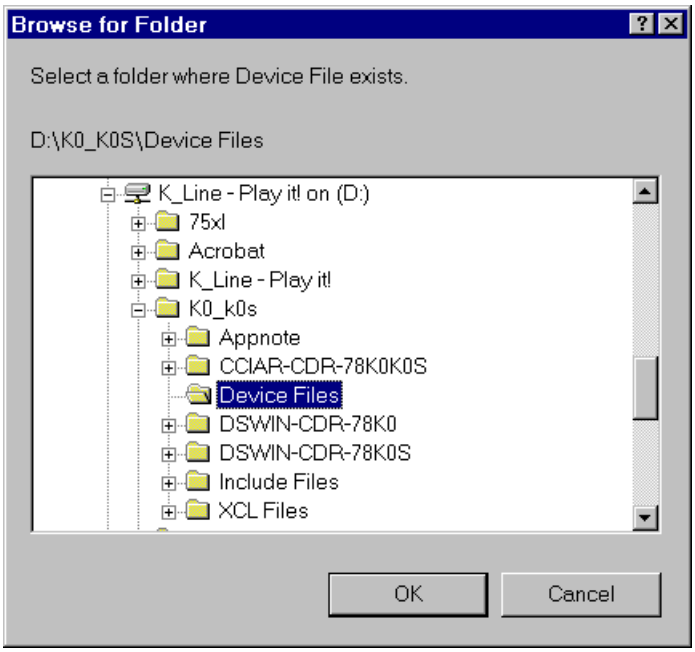


Figure 6: CDROM device files directory

After a few seconds, DFINST will list all device files in the upper list box:

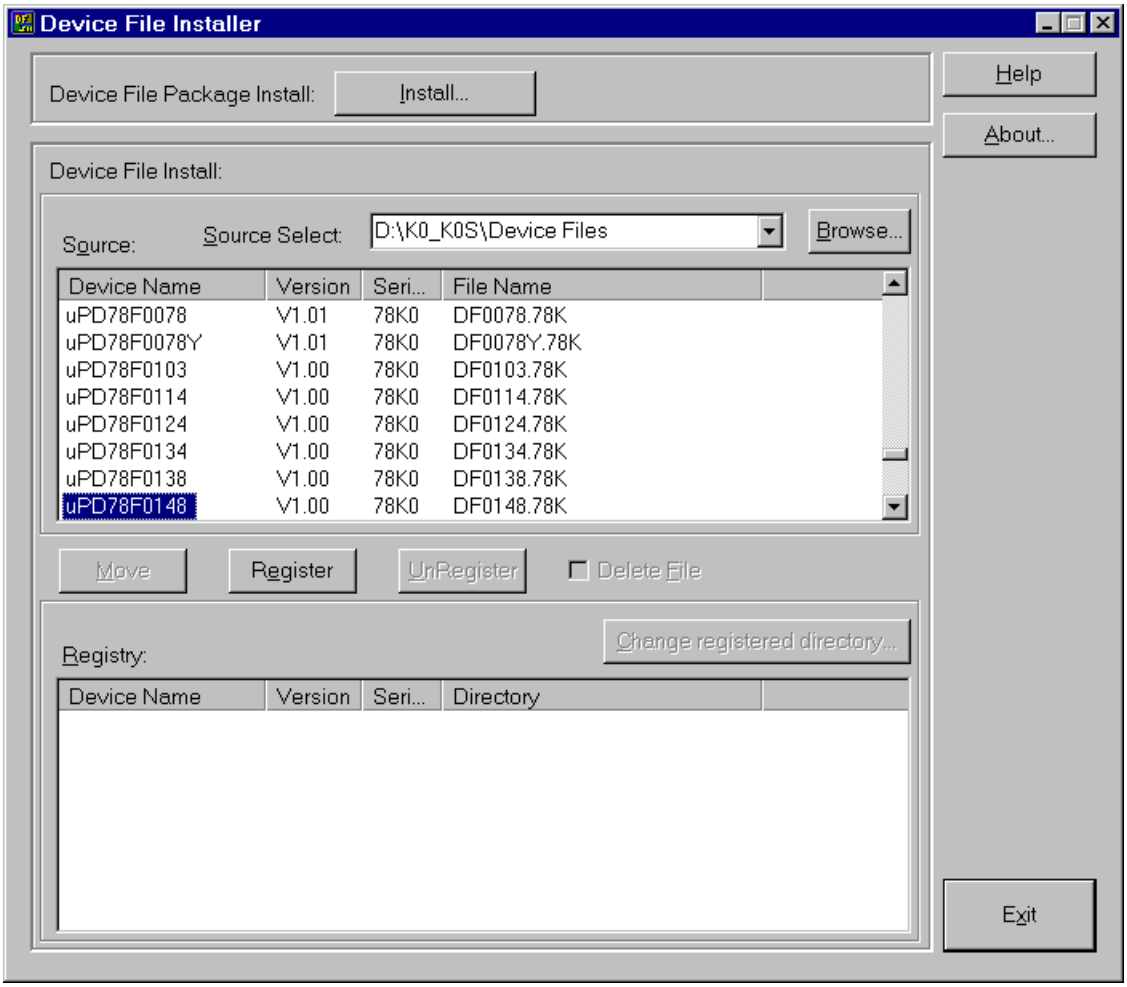


Figure 7: DFINST device file selection

Select the uPD78F0148 or even more device file(s) and press the **Register** button. DFINST will copy the selected device files to your PC and it will register the devices file so that the system simulator has access to them. Confirm your selection in next upcoming dialogue boxes.

After successful registration, DFINST will list the registered device files in the lower list box:

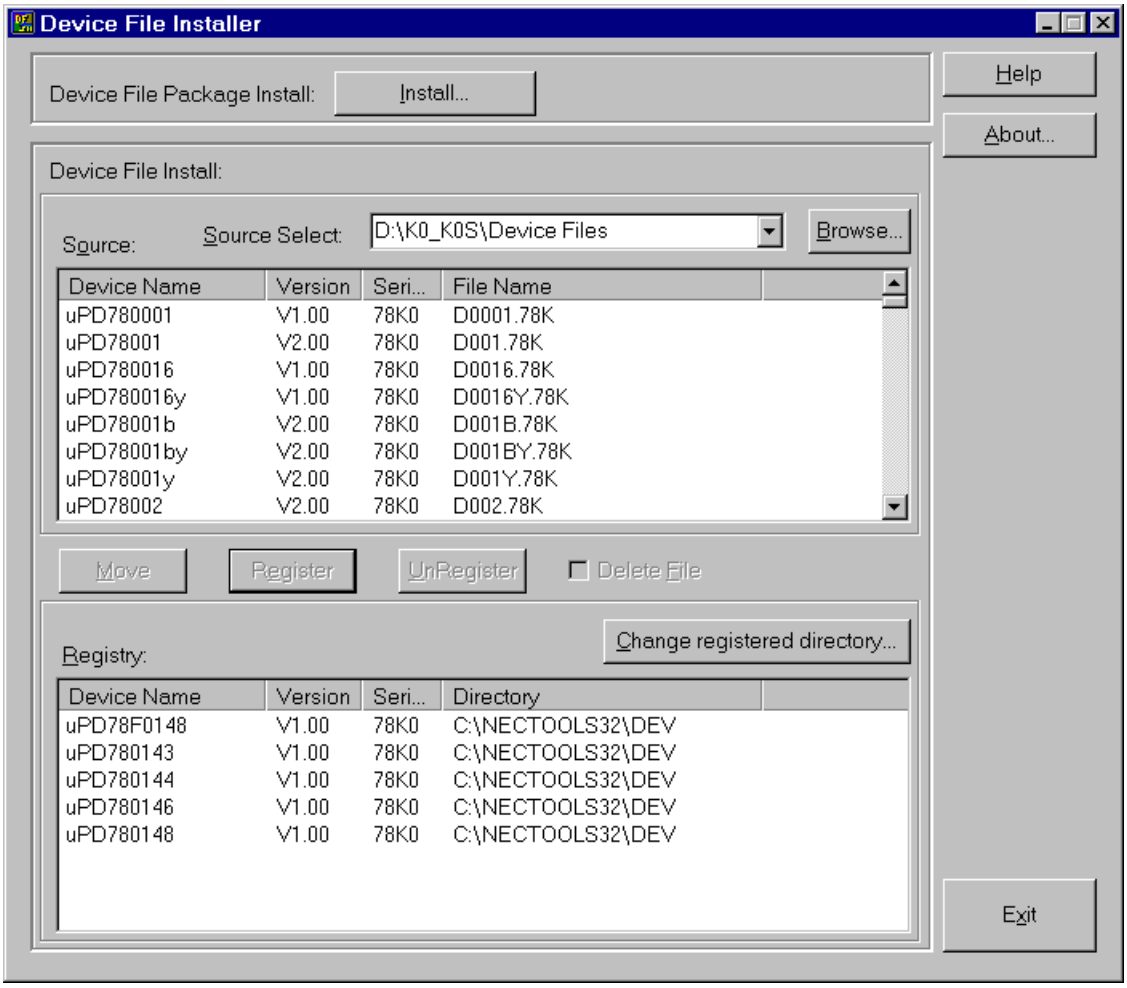


Figure 8: List of registered device files

You may repeat these steps if you would like to install other device files. After completion, press **Exit**. Device file installation is complete now.

5.1.3.4 IAR Systems Embedded Workbench for V850 installation

To install the IAR Systems Embedded Workbench for 78K0/K0S, select the `SETUP` program in the directory `\v850\EWSIM-W9XNT-CDR-V85X\EWSIM-W9XNT-CDR-V85X\` of the CDROM.
The setup-dialogues will guide you through the installation process.

5.1.3.5 Communication interface installation

The communication interface program is available in the `\K_Line-Playit!\` directory of the CDROM. It does not require any installation. It can be started directly from the CDROM or it can be copied into any directory of your local hard disk.

5.1.3.6 Sample program installation

The sample programs do not require any installation for download.
If the sample programs shall be modified it is required to copy them into any directory of your local hard disk. A file copy using the Windows explorer is the recommended procedure.

5.2 Download monitor resources

The ROM monitor program is contained in the internal flash area of the micro controller of the *K_Line - Play it!*. It uses some resources for its own purposes.
As soon as an application program starts execution, resources are returned to the system and all of them are available for user application programs.
Despite of that, some features of the 78K0/KF1 micro controller or V850ES/KF1 micro controller respectively are not available to the user.

Resources not available to the user:

- CALLT functions and CALLF functions cannot be used because the internal flash memory of the 78K0/KF1 micro controller cannot be modified during download or execution of a user application program.
- The user application program cannot use the RESET vector.
- The internal expansion RAM cannot be used for data storage because the user application program will be downloaded into this memory area.

The user application program can use all interrupt functions (except RESET). The download monitor will redirect any interrupt to a shadow interrupt vector table. Depending on the used CPU module this shadow interrupt vector is starting according to the following table. The user must make sure that the interrupt vector table has been located from that address onwards for *K_Line - Play it!*. For detailed explanation, please refer to the sample program descriptions.

CPU module	Start address
V850ES/KF1	0x3FFD800
78K0/KF1	0x000F400

Table 8: Shadow interrupt vector table

6. *K_Line - Play it!* communication interface

`Playit_GUI.exe` is the communication interface for program download. It downloads user application programs to *K_Line - Play it!* and start them automatically.
`Playit_GUI.exe` can be executed in Windows 9x, Windows NT, Windows 2000,Windows ME, and Windows Xp environment.

When `Playit_GUI` starts, following screen will appear:

Figure 9: Playit_GUI startup screen

Several actions may be initiated by menu selections from this communication interface.

6.1 Settings menu

The Settings menu allows selecting the communication port and establishing communication to the K_Line - playing *it!* hardware.

Figure 10: Settings menu

6.1.1 Ports

When activating the Ports menu, a communication setting dialogue opens.

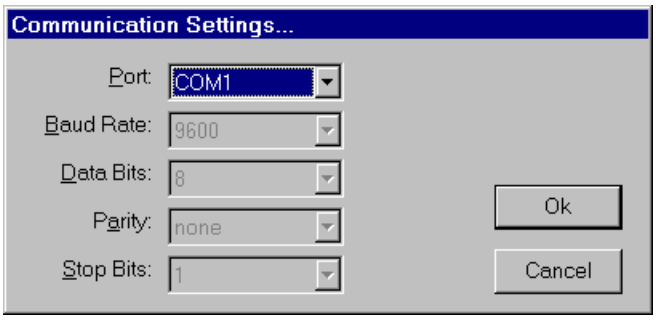


Figure 11: Communication Settings dialogue

In this dialogue, only the communication port can be selected. Other parameters are fixed.

6.1.2 Connect

When the Connect menu item is activated, communication to the *K_Line - Play it!* will be established. Make sure that the *K_Line - Play it!* is connected to the correct port of your PC before you activate this menu. On successful communication link, the main window will display a message depending on the used CPU module in its headline:

Figure 12: Well-established communication message for 78K0/KF1 CPU module

Figure 13: Well-established communication message for V850ES/KF1 CPU module

On the *K_Line - Play it!* the LED2, LED4, LED6 and LED8 will be switched on to indicate the connection status. In case an error occurs, an error message will be displayed. For details about the error messages please have a look at chapter 6.4.

6.2 File menu

The File menu allows selecting program files for download.

Figure 14: File menu

6.2.1 Download

When the Download menu is activated, a file open dialogue allows to select a HEX file for downloading to the *K_Line - Play it!*

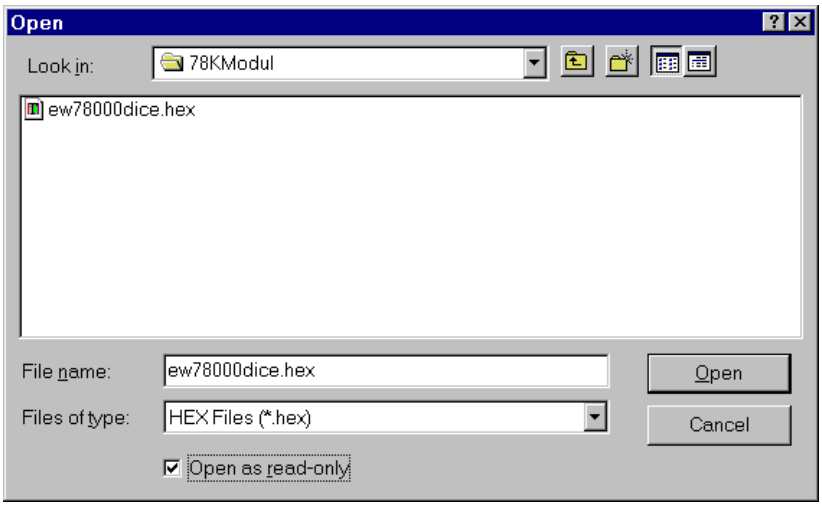


Figure 15: Select download file dialogue

Select the download file and activate OK. The selected file will be downloaded to *K_Line - Play it!* . The *K_Line - Play it!* will indicate the download activity by some flashing LED.
When the download is completed, a message box will indicate that the application program will start automatically. Please note that after program download the *K_Line - Play it!* is disconnected automatically. Since the downloaded application program may use UART and other resources, communication interface program cannot communicate to *K_Line - Play it!* any more. Therefore you have to d re-connect before downloading a new application. On the *K_Line - Play it!* you have to press the reset-button SW1 to leave the application before re-connecting.

6.2.2 Exit

The Exit menu will leave the communication interface program.

6.3 Help menu

The Help menu allows selecting an About box. On-line help is not yet provided with this communication interface program.

Figure 16: Help menu

6.3.1 About menu

The About box shows the version number of the `Playit_GUI.exe` communication interface program.

Figure 17: About box

6.4 Questions and Messages

During operation the following message boxes may occur informing the user or forcing a confirmation.

6.4.1 Questions to confirm a selected action

The user must confirm the following actions:

Selected action	Question	Possibilies
Exit while connected	Do you really want to disconnect and exit K_Line - Play it?	Yes / No
Exit while disconnected	Do you really want to exit K_Line - Play it?	Yes / No

Table 9: User confirmation messages

6.4.2 Informational Messages

The following messages inform the user about the current action or a currently restriction of the selected action:

Messages
Program downloading and executing...
Parameters cannot be changed while being connected to K_Line - Play it!!
K_Line - Play it! has been disconnected. Press RESET button before re-connecting!

Table 10: User confirmation messages

6.4.3 Fatal Error Messages

If one of the following fatal errors occur, an error message is displayed and after the confirmation the program aborts:

Number	Message	Reason
E100	Error while loading neccom.dll. Application will be closed!	Playit_GUI could not find or load NECCOM.DLL.
E101	No RS232 communication interface detected. Application will be closed!	No valid RS232 communication port found on current PC.

Table 11: Fatal error messages

6.4.4 RS232 Connection Error Messages

Number	Message	Reason
E200	K_Line - Play it! does not answer!	There is no response coming from K_Line - Play it! when sending a ***Connect*** command. Reasons could be • no board connected • board switched off • board in run or connection mode • wrong COM connection
E201	K_Line - Play it! returned unknown or incomplete Board ID!	The information received on a ***Connect*** command cannot be evaluated. The data does not identify one of the allowed monitors. Please check board type, RS232 line and connection parameters.

Table 12: RS232 connection error messages

6.4.5 Download and File Handling Error Messages

In case of a download- or file handling error, the download aborts, but the *K_Line - Play it!* stays in valid connection status. It is possible to select another download file.

Number	Message	Reason
E300	Cannot open download file.	The selected download file cannot be opened for reading. Error comes from OS.
E301	Error reading download file.	The download file cannot be read. Either EOF has been reached or file access problems have occurred. Error comes from OS.
E302	Mixed extended format (S).	The program download file in intel extended hex format contains a mixture of segmented and linear file format and is invalid.
E303	Mixed extended format (L).	The program download file in intel extended hex format contains a mixture of segmented and linear file format and is invalid.
E304	Invalid record in download file.	The program download file contains an invalid record identifier and is invalid.
E305	Incomplete line in download file.	The program download file contains less data than specified in the record header and is invalid.
E306	Address out of range.	The program download file contains address information exceeding the available ROM space in the target device.
E307	Invalid File Format	The program download file is not of intel hex file format.

Table 13: Download an file handling error messages

6.4.6 NECCOM.DLL Error Messages

A problem with the NEC communication DLL is shown by the following messages. No workaround is available.

Number	Message	Reason
E400	Connection failed!	Opening the communication channel failed.
E401	Disconnection failed!	Closing the communication channel failed.
E402	Illegal parameter selection!	Illegal communication parameters selected.

Table 14: NECCOM.DLL error messages

7. Sample programs

7.1 General Introduction

Each of the sample programs is located in a single directory, which will be called main-directory of the sample. This main directory of each sample contains the complete project inclusive all output files of the development tools. All sample programs use the same directory structure:

78KModul		File Folder	output files for 78K0/KF1 CPU module
c-spy		File Folder	output files for C-Spy simulator (only V850/KF1)
ddf		File Folder	device specific C-Spy simulator files (only V850ES/KF1)
inc		File Folder	C header files
settings		File Folder	configuration files Embedded Workbench V850
sm78k		File Folder	output files for System Simulator (only 78K0/KF1)
source		File Folder	C source files
V850Modul		File Folder	output files for V850/KF1 CPU module
xcl		File Folder	xcl files
description.txt	1KB	Text Document	example description
ew78000timer.dtp	1KB	DTP File	project configuration Embedded Workbench 78K0/K0S
ew78000timer.prj	6KB	IAR EW Project	project file Embedded Workbench 78K0/K0S V2.31e
ewV850.pew	7KB	IAR IDE Project	project file Embedded Workbench V850 V2.20a
StartSimulator	1KB	Shortcut	Shortcut to start the System Simulator

Table 15: Example directory structure

The main directory contains only the project files for the IAR Systems Embedded Workbench 78K0K0S and V850, a short description file and a shortcut to start the NEC 78K0 System Simulator. Please check the shortcut properties and correct the path to your installation path of the NEC simulator before using this shortcut.
All source files are located in the directory **`source`** and the **`inc`** directory contains the header files. Each sample project uses two targets for each micro controller. One target is the simulator (NEC System Simulator or IAR Systems C-Spy) and the other is the demonstration kit hardware (with 78K0/KF1 CPU module or V850ES/KF1 CPU module). All targets use the same source files, but they differ in the memory mapping. The different memory mapping is defined in the linker control files (*.xcl) which are located in the directory **`xcl`**. The linker control files `Df0148_sm78k0.XCL` and `v850eskx1_96k_ROM_6k_RAM.xcl` define the ROM segments in the address area of the FLASH memory of the real device. This mapping must be used for the simulator. To download the sample program to the demonstration kit all ROM segments are defined in the address area of the internal RAM of the real device. This mapping is defined in the linker control files `78KModul.xcl` for the 78K0/KF1 CPU module and `V850Modul.xcl` for the V850/KF1 CPU module. According to the connected CPU module one of these must be used to generate a downloadable file for the demonstration kit.

All output files of the development tools for each target are generated in the directories **`sm78k`** and **`78KModule`** for the 78K0/KF1 CPU module and in the directories **`c-spy`** and **`V850Module`**. Additional the directory **`sm78k`** contains the project file for the NEC 78K0 System Simulator.

Note: Although the project files for the IAR Systems Embedded Workbench and the NEC 78K0 System Simulator have the same extension, they have a different file format and contain different information.

To open the IAR Systems Embedded Workbench for a sample program please double-click on the corresponding project file in the main directory of the sample program. Due to a change in the project file format only an Embedded Workbench 78K0/K0S version v2.31 or later can open the project files for 78K0/KF1. For the V850ES/KF1 an Embedded Workbench V850 version v3.3 or later is required
If you use an older version, a warning message appears. If you want to use a former Embedded Workbench version you have to create a new project file on your own, using the above description of the files and their location. Figures 20 and 21 on the next page show screenshots the IAR Systems Embedded Workbench.

For details of using Embedded Workbench, C-Spy Simulator and 78K0 System Simulator please refer to the manuals.

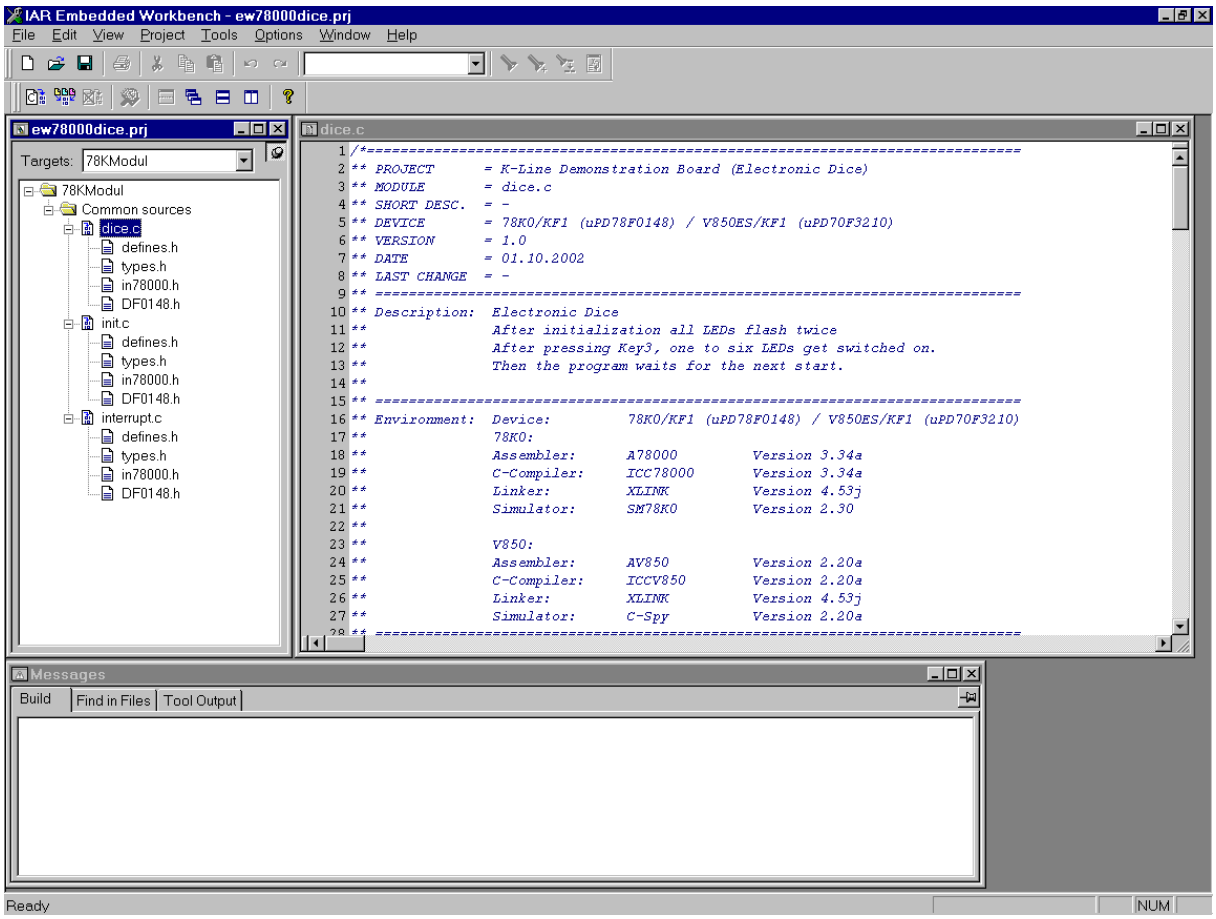


Figure 18: IAR Systems Embedded Workbench 78K0/K0S

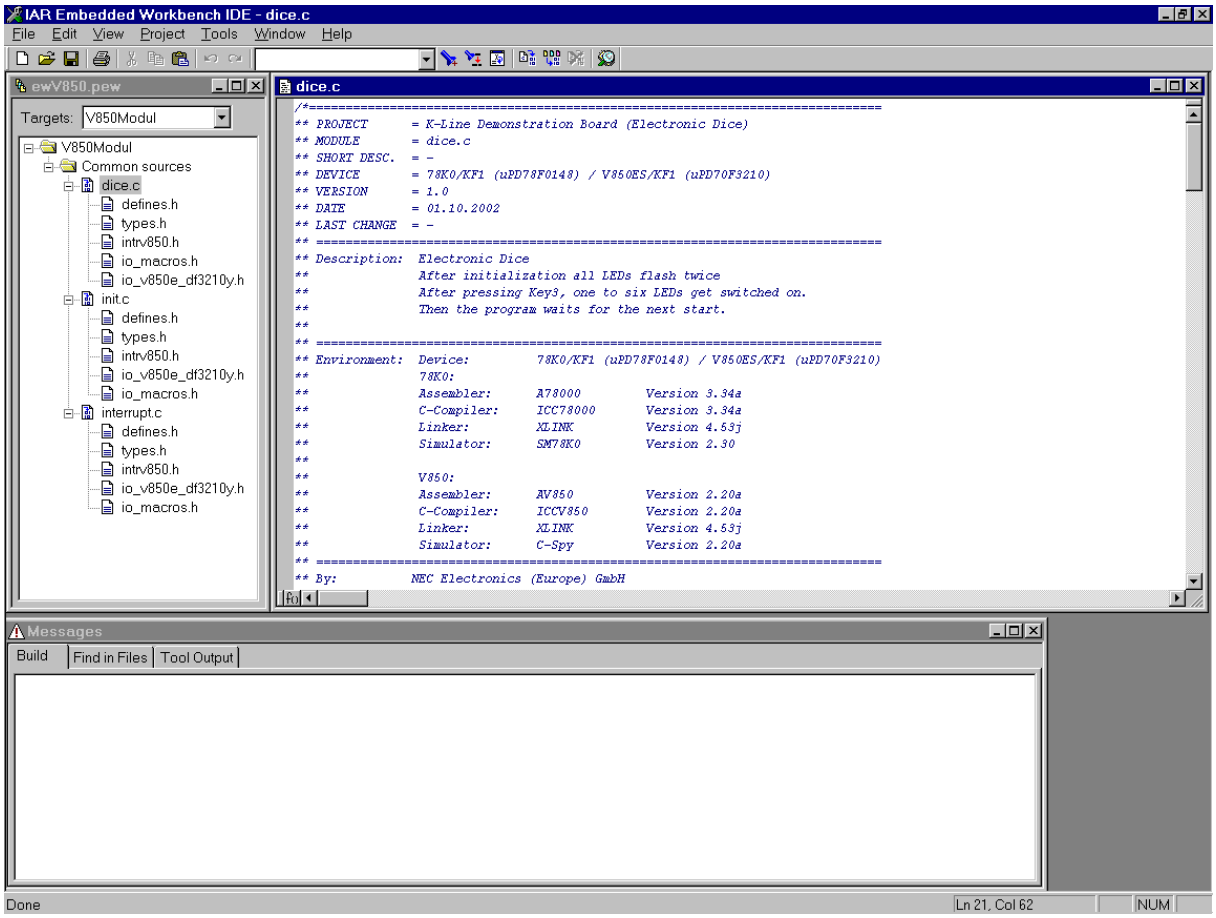


Figure 19: IAR Systems Embedded Workbench V850

To start the 78K0 simulator you can use the shortcut after you adjusted the path information to your installation path of the 78K0 simulator. Alternative you can start the simulator, select the 78F0148-device-file and open the corresponding simulator project file (*.prj) in the directory **`sm78k`** manually.
The simulator project files requires 78K0 simulator version 2.30 or later. It can't be used with earlier versions.

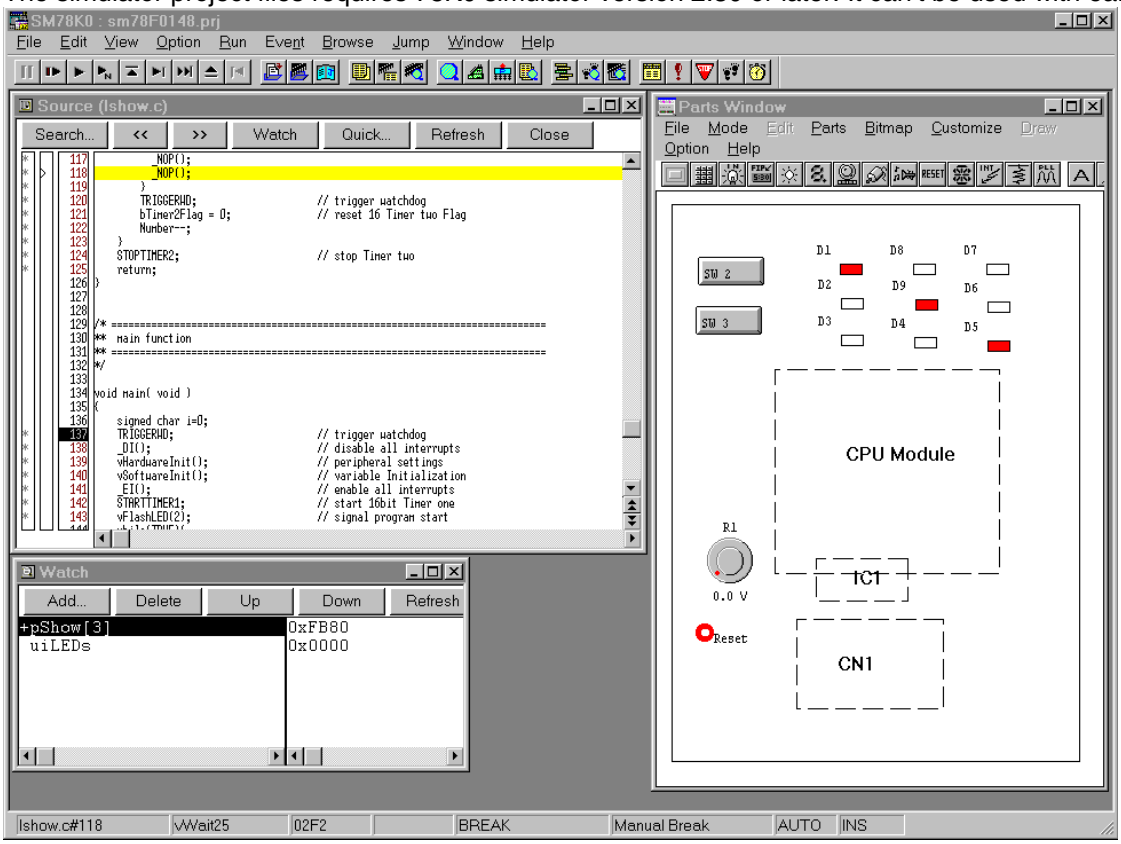


Figure 20: NEC 78K0 System Simulator

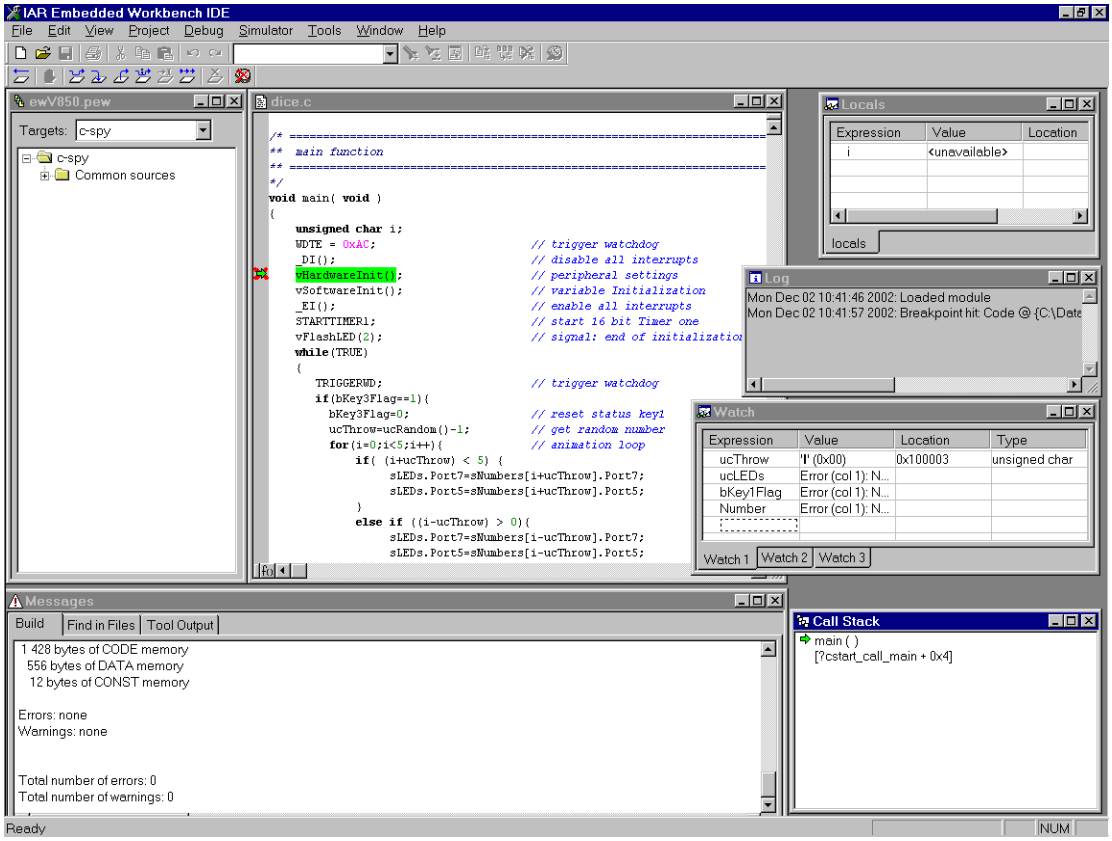


Figure 21: IAR System V850 C-Spy Simulator

7.2 Common description of all sample programs

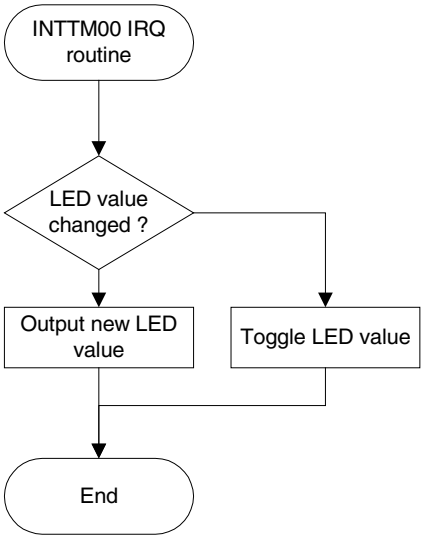
As the demonstration kit hardware is powered by a battery some power saving features are implemented in all sample programs:

- Usage of a pulsed signal (100Hz) to control the LEDs instead of a static signal. The pulsed LED control is implemented as an interrupt function of Timer00.

- All hardware components (RSR232 driver, reference voltage, potentiometer, etc) are disabled if they aren't used in an application.
  Therefore, if you write your own application be aware that the hardware you want to use is enabled.

To signal the program start after the download, all LEDs flash two times in a one-second interval.

Flowchart of the Timer00 interrupt function to generate the pulsed LED control:



7.3 Electronic dice

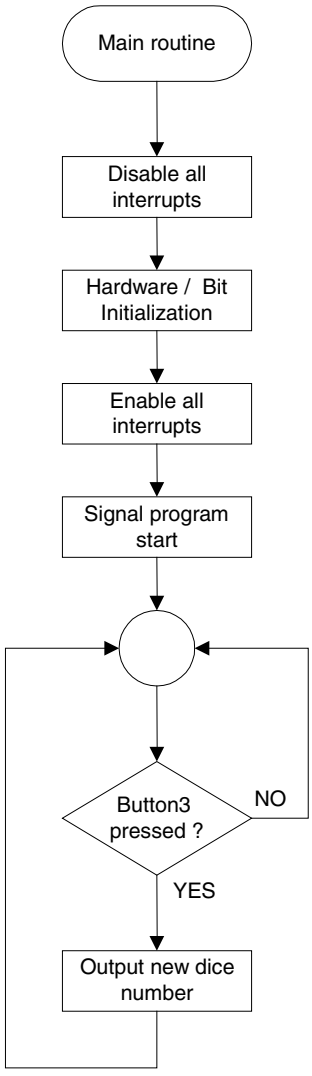
This sample program simulates a dice. After the program-start-signal, the program waits for a press of button 3. After an animation of a rolling dice a random number between one and six is generated and shown at the LEDs.

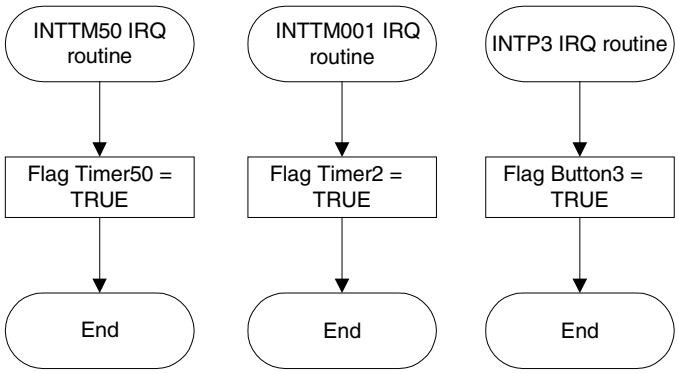
The ‘random’ number is generated by a transformation of the timer value of Timer50 to number between one and six. Timer50 is working at 2MHz using a compare value of 64 in the modus ‘clear and start on match between TM50 and CR50’. The result is an interrupt repetition time of 31,25 KHz. Timer01 is working in the same modus to generate a 25ms timebase.

Used Internal Peripherals	Used External Parts	Source Modules	
Timer00	LEDs	dice.c	main function
Timer01	Button3	init.c	Hardware and Bit initialization
Timer50		interrupt.c	interrupt functions

To end the program and return to the download program again please press the START button.

Flowcharts of the main routine and the interrupt functions:





7.4 Lightshow

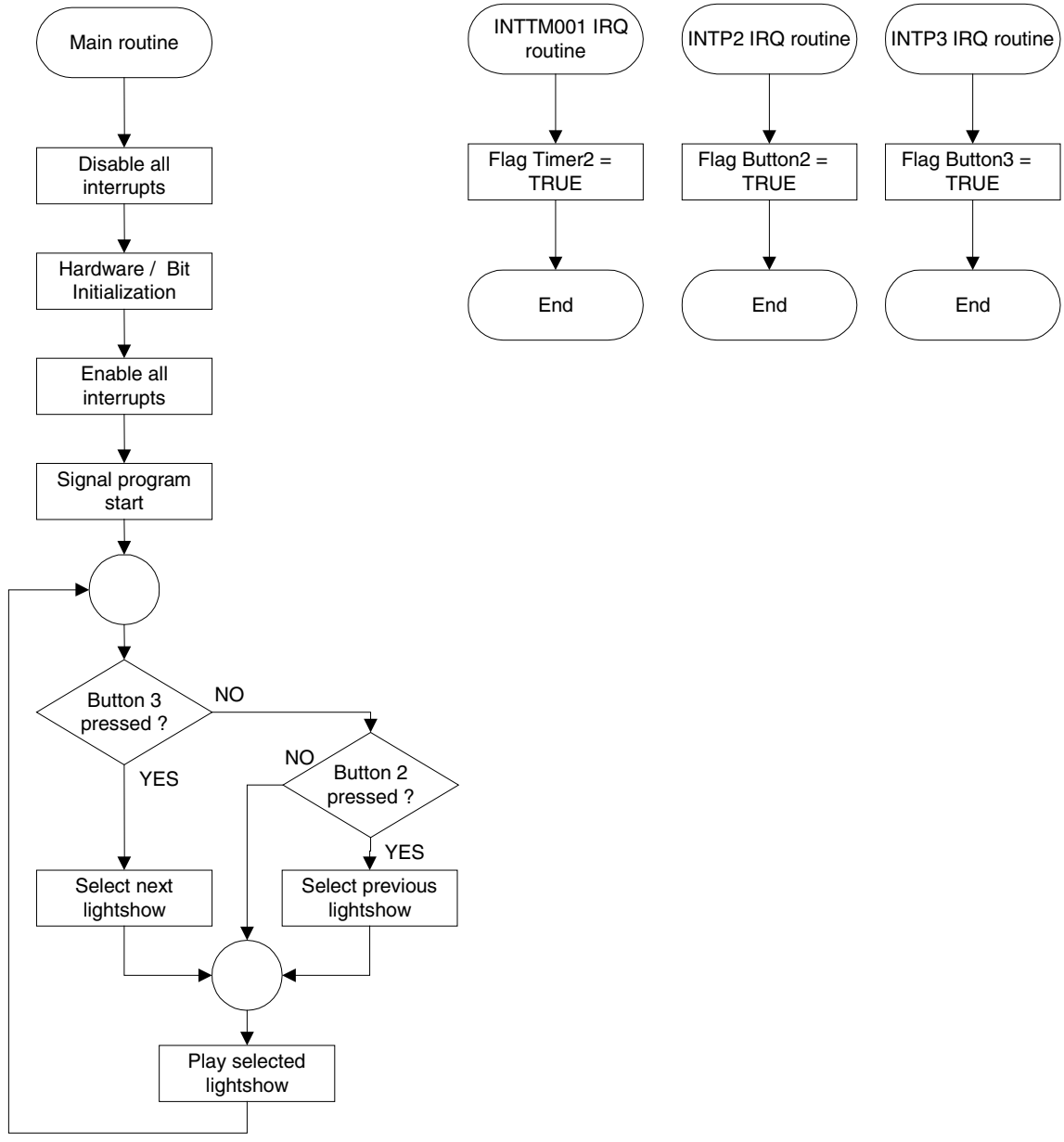
This sample programs plays one of three predefined lightshows. After the program-start-signal, the program plays the first lightshow. By pressing button3 the next show is selected. Button2 selects the previous show. Every show is completed before the next show starts.

Timer01 is working in the modus ‘clear and start on match between TM01 and CR001’. According to selected operating frequency and the value of the compare register CR001 Timer01 generates a 25ms timebase.

Used Internal Peripherals	Used External Parts	Source Modules	
Timer00	LEDs	lightshow.c	Main function
Timer01	Button2	init.c	Hardware and bit initialization
	Button3	interrupt.c	Interrupt functions
		sequences.c	Lightshow sequence definitions

To end the program and return to the download program again please press the START button.

Flowcharts of the main routine and the interrupt functions:



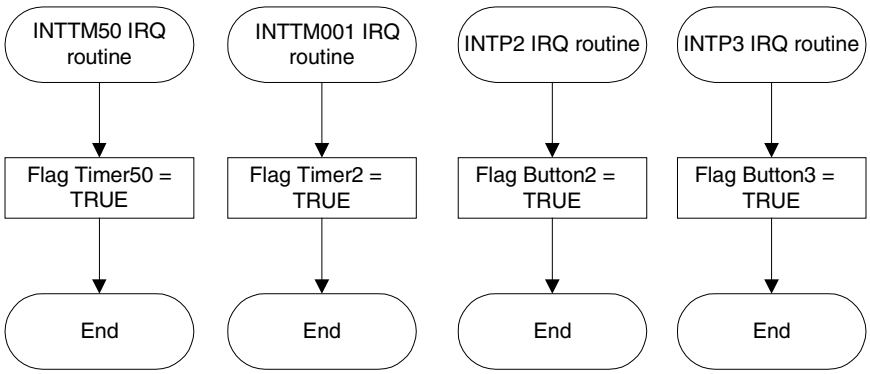
7.5 Reaction time measurement

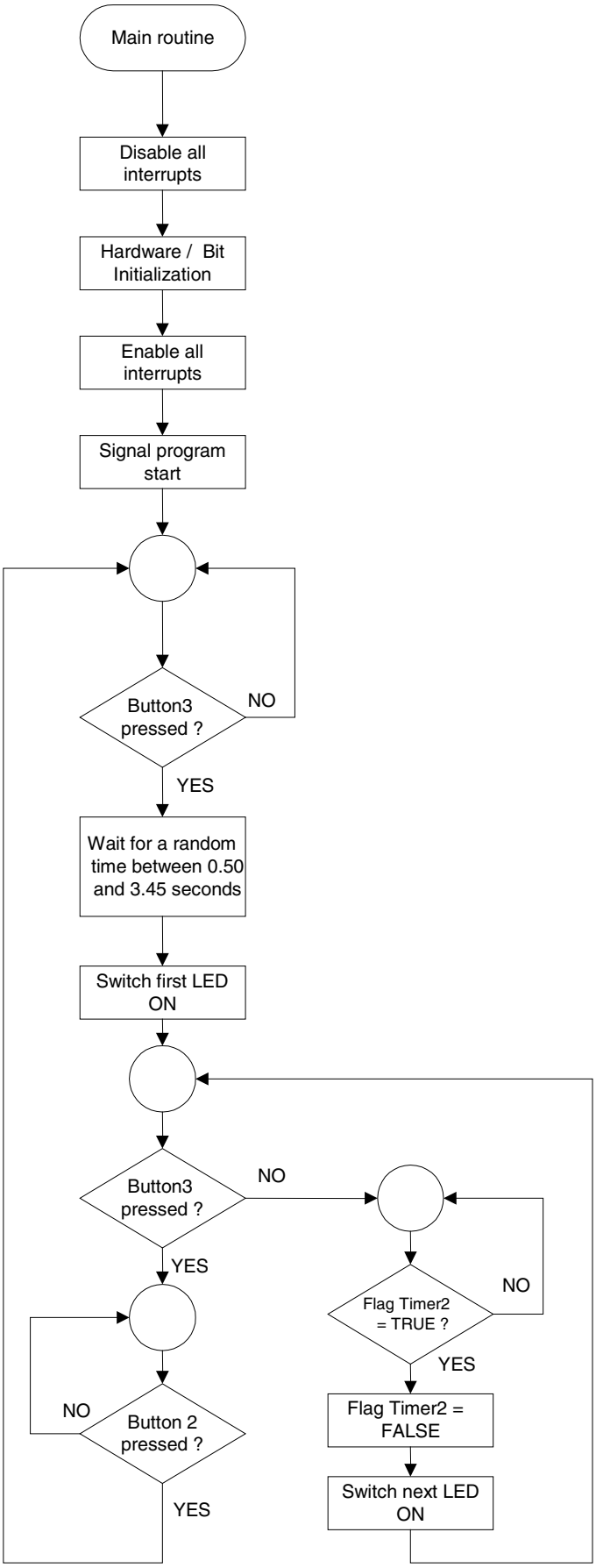
This sample program demonstrates a reaction time measurement. After a press of button3 the application waits for a random time between 0.50 and 3.45 seconds. Then the first LED is switched on and measurement starts. Until the next keystrokes of button 3 every 50 ms a new LED is switched on. Pressing button2 starts a new measuring cycle.
Timer50 is working at 2MHz using a compare value of 64 in the modus 'clear and start on match between TM50 and CR50'. The result is an interrupt repetition time of 31,25 KHz. Timer01 is working in the same modus to generate a 25ms timebase.

Used Internal Peripherals	Used External Parts	Source Modules	
Timer00	LEDs	reactime.c	Main function
Timer01	Button2	init.c	Hardware and bit initialization
Timer50	Button3	interrupt.c	Interrupt functions

To end the program and return to the download program again please press the START button.

Flowcharts of the main routine and the interrupt functions:




Main routine
Disable all interrupts
Hardware / Bit Initialization
Enable all interrupts
Signal program start
Button3 pressed ?
NO
YES
Wait for a random time between 0.50 and 3.45 seconds
Switch first LED ON
Button3 pressed ?
NO
YES
Flag Timer2 = TRUE ?
NO
YES
Flag Timer2 = FALSE
Switch next LED ON
Button 2 pressed ?
NO
YES

7.6 Entrance code checker

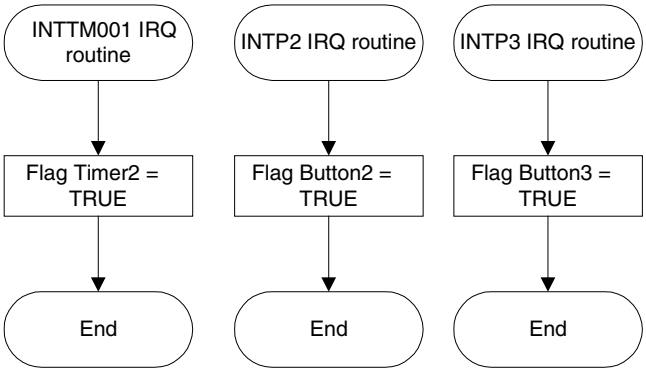
This sample program waits for a sequence of five keystrokes. If the input sequence matches the predefined sequence LED9 and one Port are switched on for 5 seconds. Otherwise, all LED flash five times.
Then the program waits for a new input sequence. The output port is P130 for the 78K0/KF1 module and P00 for the V850ES/KF1 module. The code sequence is stored in the array ucCode. The sequence is Button 3 - Button 3 - Button 2 - Button 3 - Button2. A flash of LED D1 signals an accepted key press.

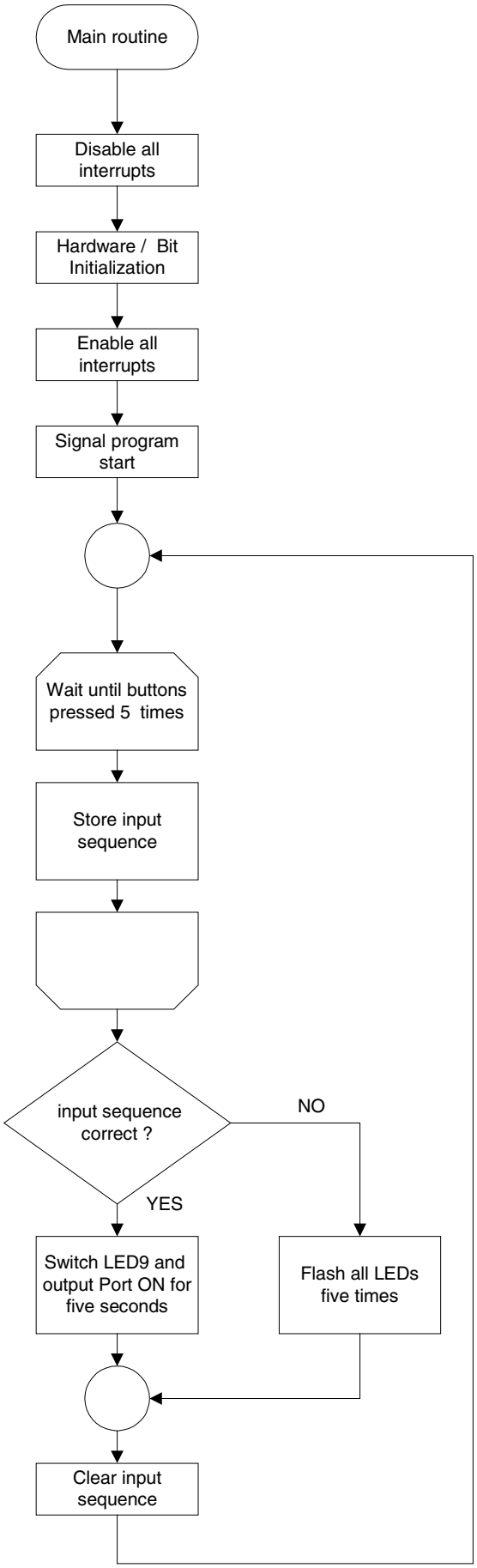
Timer01 is working in the modus ‘clear and start on match between TM01 and CR001’. According to selected operating frequency and the value of the compare register CR001 Timer01 generates a 25ms timebase.

Used Internal Peripherals	Used External Parts	Source Modules	
Timer00	LEDs	codechk.c	Main function
Timer01	Button2	init.c	Hardware and bit initialization
	Button3	interrupt.c	interrupt functions

To end the program and return to the download program again please press the START button.

Flowcharts of the main routine and the interrupt functions:




Main routine
Disable all interrupts
Hardware / Bit Initialization
Enable all interrupts
Signal program start
Wait until buttons pressed 5 times
Store input sequence
input sequence correct ?
NO
YES
Switch LED9 and output Port ON for five seconds
Flash all LEDs five times
Clear input sequence

7.7 Count down timer

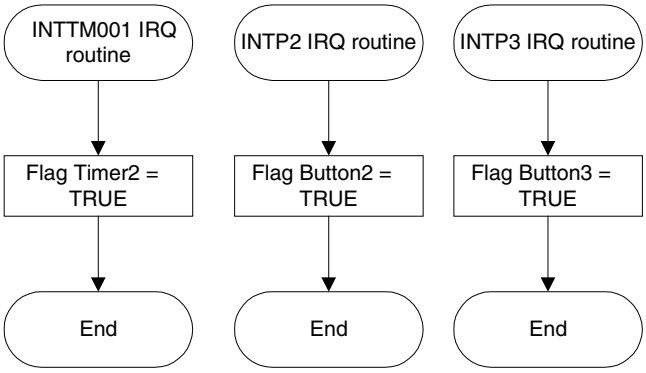
With this sample programs the board can be used as a count down timer. After the signal for program start the program waits for the input of the timer time, which can be set by button3. Each press increases the time by 60 seconds. The current time is shown by the LEDs in units of minutes. A press of button2 starts the timer, which is shown by a flashing LED D9.
After the selected time is finished all LEDs flash for 3 minutes or a key press of the user. Then the program goes to stand by modus. A key press during countdown time or stand-by-modus sets the program to input mode again.

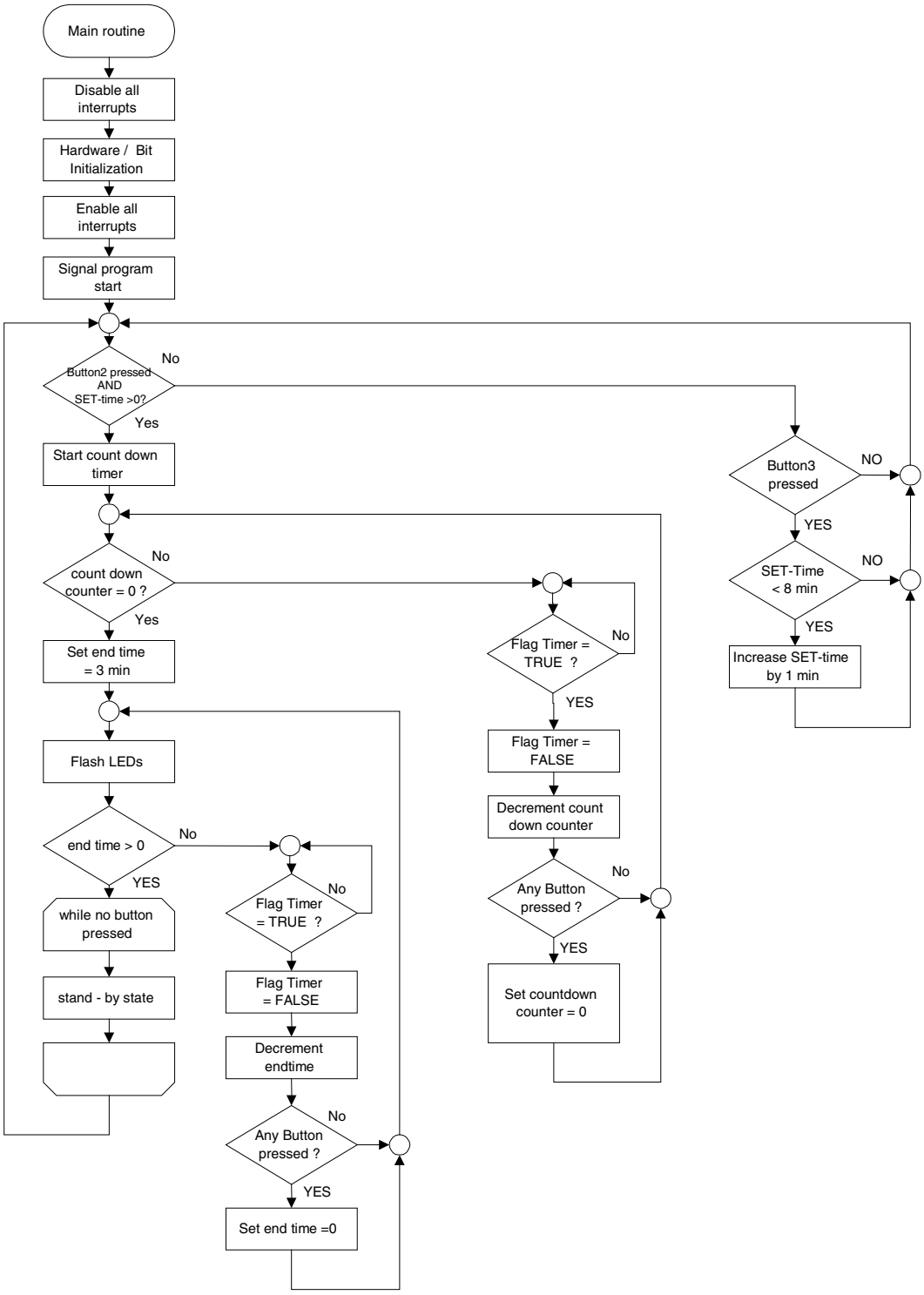
Timer01 is working in the modus 'clear and start on match between TM01 and CR001'. According to selected operating frequency and the value of the compare register CR001 Timer01 generates a 25ms timebase.

Used Internal Peripherals	Used External Parts	Source Modules	
Timer00	LEDs	timer.c	Main function
Timer01	Button2	init.c	Hardware and bit initialization
	Button3	interrupt.c	interrupt functions

To end the program and return to the download program again please press the START button.

Flowcharts of the main routine and the interrupt functions:




Main routine
Disable all interrupts
Hardware / Bit Initialization
Enable all interrupts
Signal program start
Button2 pressed AND SET-time >0?
No
Yes
Start count down timer
count down counter = 0 ?
No
Yes
Set end time = 3 min
Flash LEDs
end time > 0
No
YES
while no button pressed
stand - by state
Flag Timer = TRUE ?
No
Flag Timer = FALSE
Decrement endtime
Any Button pressed ?
No
YES
Set end time =0
Flag Timer = TRUE ?
No
YES
Flag Timer = FALSE
Decrement count down counter
Any Button pressed ?
No
YES
Set countdown counter = 0
Button3 pressed
NO
YES
SET-Time < 8 min
NO
YES
Increase SET-time by 1 min

7.8 Melody maker

This sample programs plays one of eight predefined melodies using an external piezo buzzer. By pressing button3 the next melody is selected. Button2 selects the previous melody. Every melody is completed before the next melody starts.

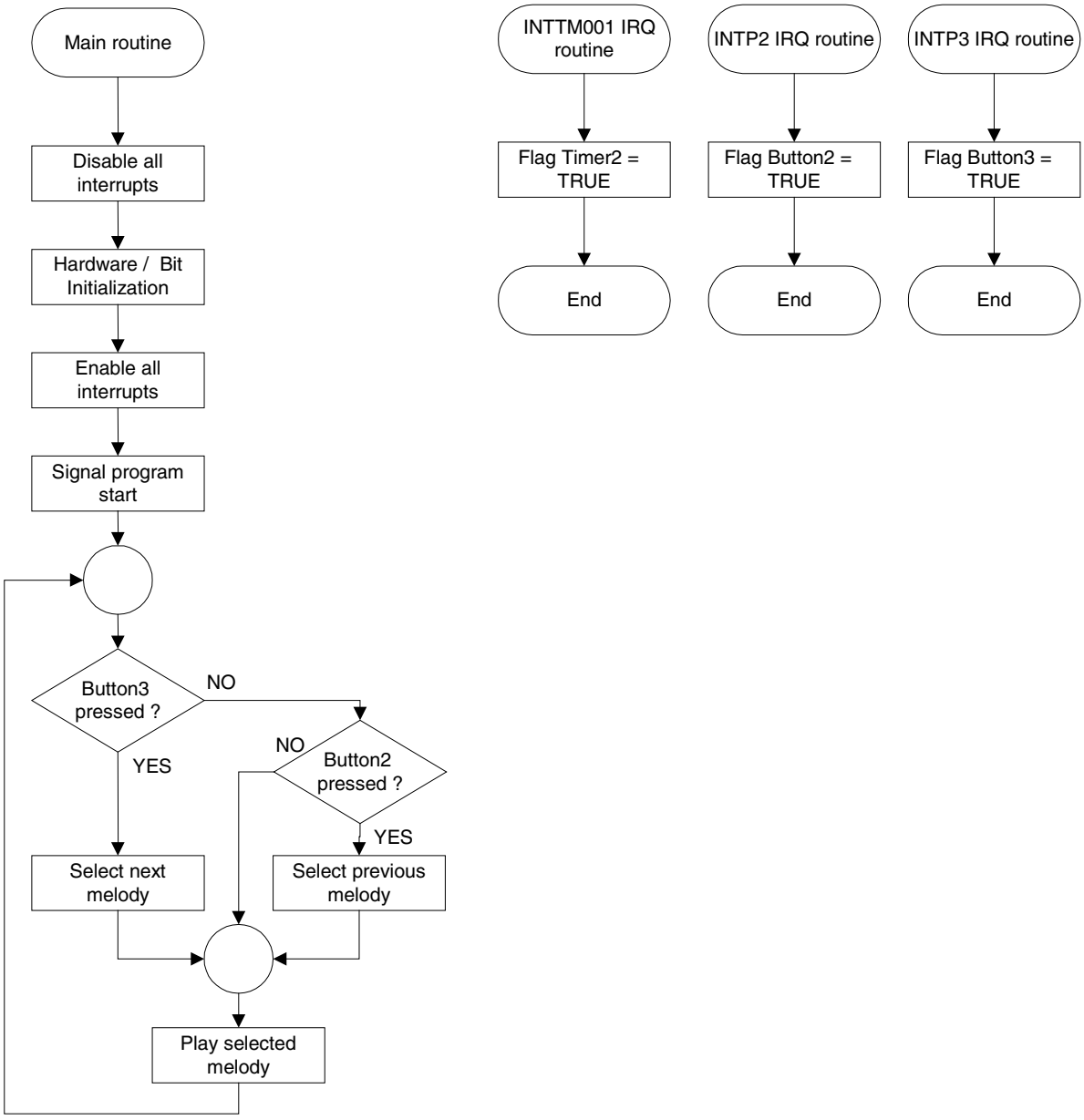
Note: The external buzzer must not exceed the limit of 10 mA current consumption.
It must be corrected between the port pin and V_{CC}.

Timer01 is working in the modus 'clear and start on match between TM01 and CR001'. According to selected operating frequency and the value of the compare register CR001 Timer01 generates a 27.5ms timebase.

Used Internal Peripherals	Used External Parts	Source Modules	
Timer00	LEDs	melody.c	Main function
Timer01	Button2	init.c	Hardware and bit initialization
	Button3	interrupt.c	interrupt functions

To end the program and return to the download program again please press the START button.

Flowcharts of the main routine and the interrupt functions



8. Connectors and Cables

8.1 Serial host connector

Figure 22: Target cable 2

Pin	78K0/KF1	V850ES/KF1	RS232 Signal on *K_Line - Play it!*	Pin	RS232 Signal on PC side
1	NC	NC	---	1	DTR
2	RXD6	RXD0	RxD	2	RxD
3	TXD6	TXD0	TxD	3	TxD
4	NC	NC	DTR	4	DSR
5	NC	NC	GND	5	GND
6	NC	NC	DSR	6	---
7	P17	P33	CTS	7	CTS
8	P16	P32	RTS	8	RTS
9	NC	NC	----	9	---

Figure 23: Serial host connector

9. Schematics

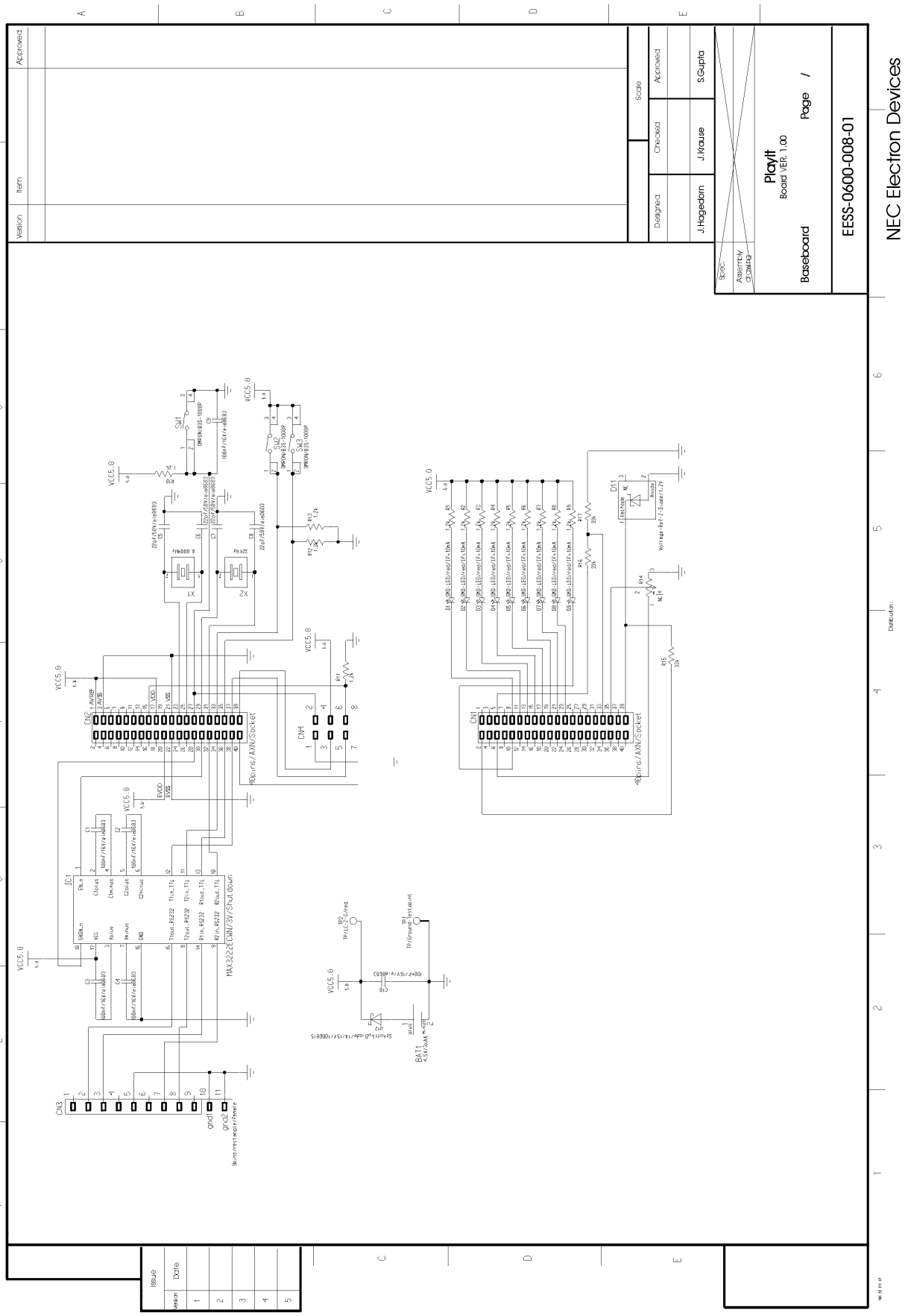


Figure 24: *K_Line - Play it!* baseboard schematics

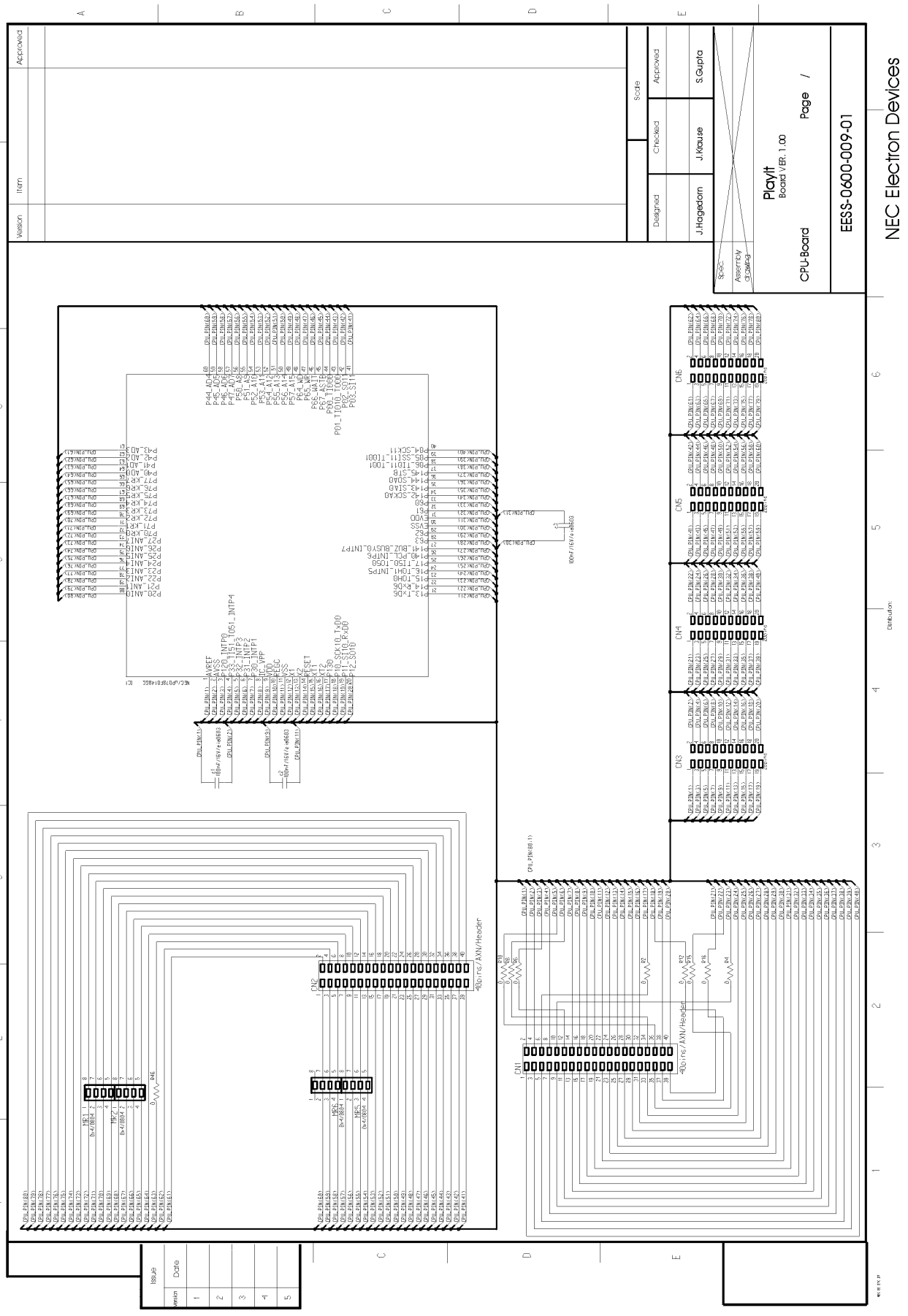


Figure 25: ***K_Line - Play it!*** **78K0/KF1 CPU module schematics**

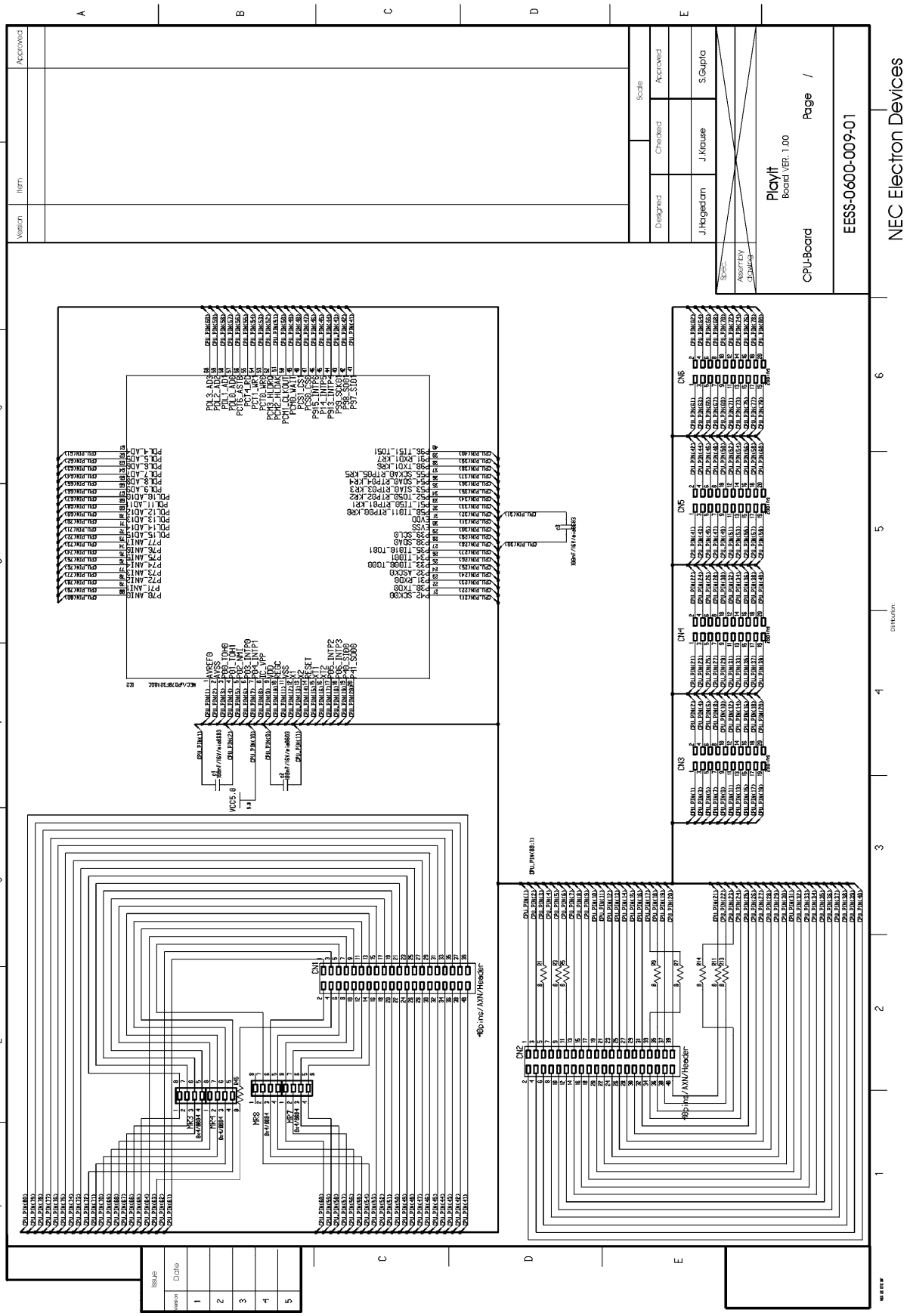


Figure 26: *K_Line - Play it!* V850ES/KF1 CPU module schematics