Microwave Amplifier, Oscillator, and Filter Design

using either common emitter bipolar transistors or common source NMOSFET transistors with bias and stabilization networks. Filters will be designed using microwave passive filter techniques.

EE 414/514 Lab - Fall 2006
Robert J. Weber

The remainder of the laboratory portion of EE 414/514 will consist of a design project. The design project includes the fabrication of an oscillator, amplifier, and filter assembly. The active devices will be an nmos FET and an npn bipolar transistor. The design group chooses either an oscillator with an nmos FET and an amplifier with an npn bipolar transistor or an oscillator with an npn bipolar transistor and an amplifier with an nmos FET.

It is becoming more and more difficult to obtain discrete transistor devices to conduct these design projects since most current technology uses integrated circuits technology. The bipolar and FET devices are old technology but will adequately demonstrate the design techniques that this course seeks to teach. The nmos FET can be used up to about 1 GHz. The npn bipolar can be used up to about 4 GHz. Undergraduate students (EE414) will do their designs in the range of 850 MHz to 1 GHz. Graduate students (EE514) will do their design between 1 and 2 GHz. They will have to determine whether the nmos FET is adequate for their frequency of operation and choose to do both circuits with the npn bipolar if they determine the nmos FET will not work.

EE414 students will use "1206" parts for resistors and capacitors and use "0603" parts for inductors. EE514 students may opt to use "0603" parts for all resistors, capacitors, and inductors but need to be prepared to give a parts list for their components at least one week before the layout is due. Check Appendix E of the text for chip sizes.

It will be necessary to complete the design portion of the assembly by Thanksgiving break in order to allow time to fabricate and test the assembly between Thanksgiving break and final week.

The following schedule from the syllabus is established for the remainder of the semester.

6. Amplifier Design - 3 wks - 9/11, 18, & 9/25
7. Oscillator Design - 2 wks - 10/2 & 10/9
8. Resonator Modeling - 1 wk - 10/16
9. Filter Design - 2 wks - 10/23 & 10/30

These will need to be integrated into the project build and test.

10. Circuit Layout - 2 wks - 11/6 & 11/13
    Laboratory exercise 10 must be done and complete with **layouts completed** before Thanksgiving break!
    This includes off campus students.

11. Project Build & Test (Amp, Osc, and Filter) 11/27 & 12/4

NOTE! The schedule is tight. If you finish the layout of either the amplifier or oscillator early, move on to the filter! You should also take full advantage of any laboratory time this is not scheduled! Use this unscheduled time to advantage. You can run ADS from a UNIX workstation in Coover. You can run ADS at any hour of the day that that laboratory is open and a workstation is free.

Microwave Bipolar Bias Design

EE 414/514 Lab - Fall 2006

Robert J. Weber[1]

Bias Circuits: For dc and rf grounded common emitter devices.

Many common emitter devices become potentially unstable whenever as much as one nH of inductance is put in series with the emitter. For this reason many common microwave and rf devices are rf and dc grounded in the circuits in which they are used. This presents some difficulty in producing a stable bias circuit for the rf device. Several techniques are available to control and stabilize the bias point of an emitter grounded device. Most of these techniques involve sensing collector current via a resistor in the collector bias network of the rf device.

The purpose of this section is to introduce a bias circuit that will effectively compensate for changes in collector current observed in the rf device shown as either a MMBR901 bipolar or a BSS83 NMOS FET. Some causes of collector/drain current changes are such things as temperature effects, component value variations, active parameter variations, and source and output load variations. Figure 1 gives a general block diagram of the rf device with the bias "controller." The controller can be made from a transistor circuit or an op-amp circuit. The discussion to follow describes a transistor circuit. **Graduate students** are to design an op-amp circuit that performs the same task. NOTE: (op-amps that are not rail-to-rail for input common mode require that the voltage drop from the power supplies to the input terminals be larger than a specified voltage.) Note that the control variable for the bipolar is I_b while the control variable for the FET is V_{gs}.

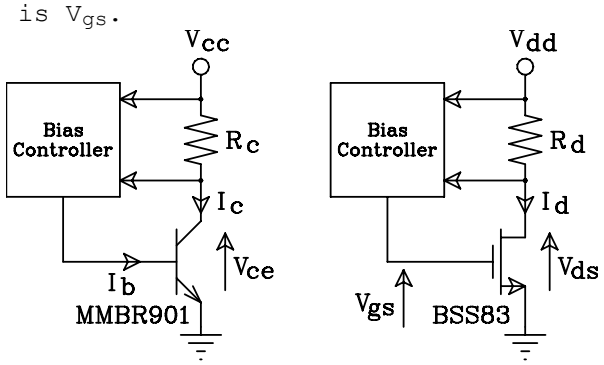


Figure 1: Bias controller block diagram.

The bias controller can use an operational amplifier such as a LM741 (the LM741 is not a rail to rail op-amp!), a rail to rail op-amp, or as shown in Figure 2, a device such as a PNP (MMBT2907A) transistor. The PNP controller circuit shown in Figure 2, senses the collector or drain current across the sensing resistor R_c or R_d. This voltage controls the emitter current of the PNP transistor. For the circuit in Figure 2, a decrease in the MMBR901 collector current or BSS83 drain current will correspond to an increase in the voltage across the MMBR901 or BSS82. An increase of this voltage will cause an increase in the emitter to base voltage ($V_{eb} = -V_{be}$) of the MMBT2907A that in turn causes an increase of PNP base current (thanks to the diode equation) that results in increased MMBT2907A collector current. As the MMBT2907A collector current increases, the base current of the MMBR901 increases or the current through R_{g2} of the BSS83 circuit increases. This causes the MMBR901 collector current or the drain current of the BSS83 to increase due to increased bias control. This increase in collector current or drain current then approximately restores the MMBR901 collector current or BSS83 drain current to its original operating point (Q-point). Assume that the MMBR901 collector current has increased and the MMBR901 V_{ce} has decreased and convince yourself that ultimately the bias controller will work to decrease the MMBR901 collector current to the original operating point. The drain current of the BSS83 is controlled in a similar manner.

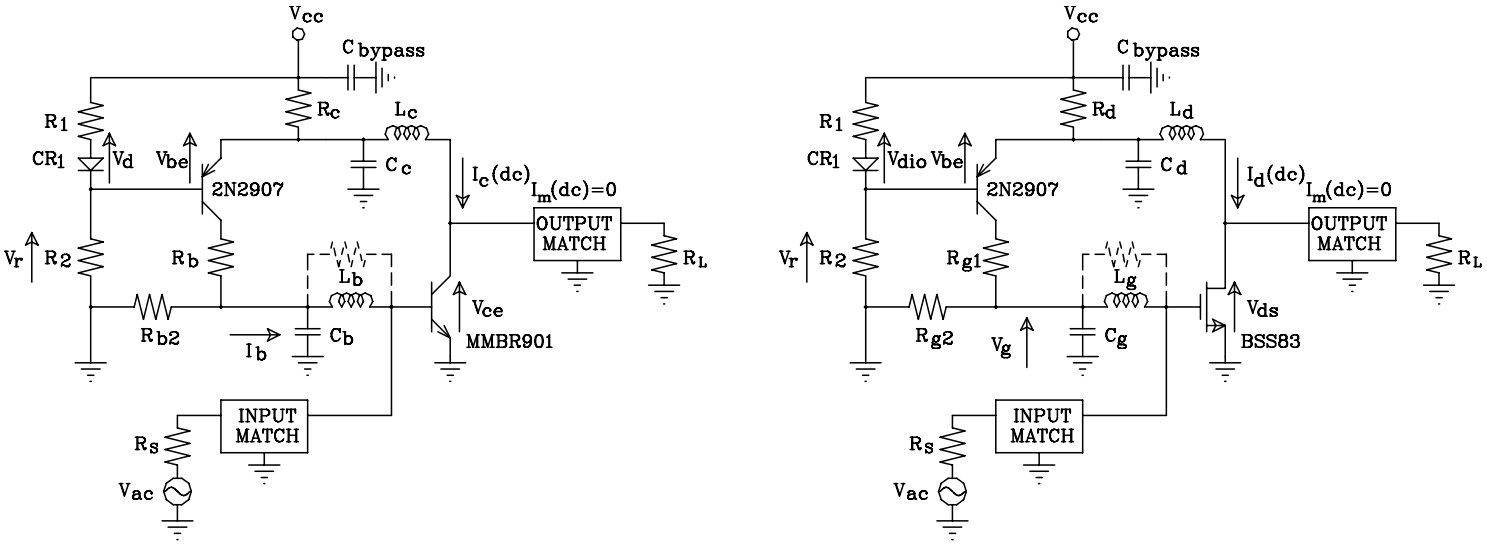


Figure 2: Bias controller implemented with a PNP transistor.
A typical arrangement of rf chokes and bypass capacitors is shown.

The dc design equations for the MMBR901 circuit shown in Figure 2 are given here. A similar set of equations would be used for the BSS83 circuit. For the BSS83 circuit, the gain to source voltage is obtained from the '2907 collector current times R_{g2}. You should use the equations below to arrive at values for the resistors. You are to determine what assumptions were made in order to specify these equations and determine if these assumptions are indeed valid. These equations also assume R_{b2} is infinite for the MMBR901 circuit. You will likely want to let R_{b2} be a reasonable value to limit the control loop gain.

$$V_r = \frac{R_2}{R_1 + R_2}\left(V_{cc} - V_d\right) \qquad (1)$$

$$V_{cc} = I_c R_c + V_{eb} + V_r \qquad (2)$$

$$V_{cc} = I_c R_c + V_{ce} \qquad (3)$$

The following data can be assumed for the initial calculation of component values:

Q-point: Ic=20 mA Vce = 10 V

Unknown Voltages: V_{cc} =12.0 V V_d=0.7 V V_{eb}=0.7 V

Assumed Transistor dc Current Gain: MMBT2907A β=180
MMBR901 β=65

The circuit must work with minimum and maximum β's as specified in the data sheets.

The min/max beta for the MMBT2907A is 100/300 and for the MMBR901 is about 30/200.

One set of values you might possibly choose are:

R_C=100Ω
R_1=100kΩ
R_2=465kΩ

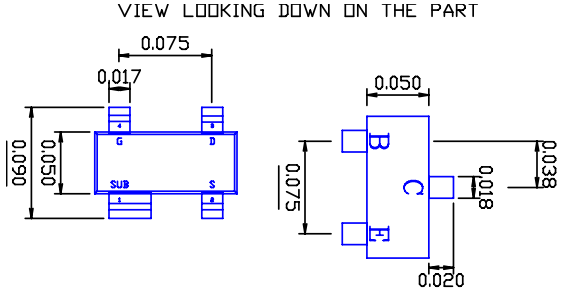
However, R_1 and R_2 are too large for use with minimum transistor β's. (So don't use them.) Why?

For in-circuit operating point adjustments, potentiometers could be used for R_1 and R_C. You would probably place some fixed "dead man" resistors in series with these "pots" to avoid burning out the transistors. The base series resistor, R_b, is used to isolate the PNP collector from the rf circuit and to help prevent oscillation of the PNP-NPN device control loop. Anything from 500 to 1000 ohms should be sufficient. Also 470 pF of capacitance may be needed from the PNP base to the PNP collector and/or from the NPN base to the PNP collector. Run a stability calculation of the circuit ***after*** you complete the rf matches (input and output matches) to determine this! (Don't forget that the input and output matches must not conduct any dc current). The bias controller stability needs to be rechecked after the amplifier matching networks are completed! The diode voltage of CR1 is used to approximately track the emitter to base voltage, V_{eb}, of the PNP device. One method of choosing the current through R1 and R2 is to set the diode voltage equal to the base to emitter voltage of the '2907 transistor. You are not asked to do that for this lab but keep that in mind in an actual application of the circuit.

The amount of power generated in the NPN or FET at this operating point will be about 200 mW. (You will use a MMBR901 in the actual circuit, but you can use a MMBT2222A NPN for a test circuit if you want to check the dc bias control in a student version of PSpice.) This is quite a bit of power for an average ambient temperature of 25 degrees Celsius without a heat sink. The package may therefore be warm or hot to the touch so be careful if you decide to test an actual circuit.

(As a final note, if you use an LM741 as the bias controller, remember that the positive and negative inputs to a LM741 operational amplifier must be kept three volts above and below the negative and positive bias terminals, respectively. The LM741 will probably also need at least a 470 pF capacitor as a feedback integration capacitor for overall loop stability.)

You can check the stability of the bias circuit on an evaluation version of PSPICE^{tm} by using a MMBT2222A (or it may be that the library device is a 2N2222) device in place of the MMBR901 (the MMBR901 is not in the student version library). If a full version of PSPICE^{tm} is in the microwave laboratory it may have a MMBR901 in it depending on the parts library content. Use a transient solution. When the final circuit is completed later in the semester, the complete circuit needs to be tested with a circuit including all rf matches. The circuit should be tested before the rf matches are designed. Try testing the circuit using a large bias inductor (large for 1 GHz, i.e. an impedance greater than 1 k-ohm) and large bypass capacitor (large for 1 GHz, i.e. an impedance smaller than 1 ohm) on both the base and collector leads. Insert a pulsed voltage source in series with the base lead. For example, use a 0.1 V pulse that is 0.2 ms wide positioned about 1 ms from time t=0. If the bias circuit is stable, the collector current will have a transient change in value and then will return to the steady state values. If it does not return to the steady state value, it will either oscillate or some part will go into saturation. First try this on the bias circuit without rf matches but be sure to check it later on the completed circuit. It will save you a lot of grief in the laboratory! Use wires in place of transmission lines when checking low frequency stability. At the low frequencies you will be using for checking bias stability, a transmission line is approximately just a wire. Spice type programs take a time step size that is only one-half of the time delay down the shortest transmission line. Using transmission lines would then causes an extremely long computation time for checking the dc stability of the complete circuit.



Package drawings of the BSS83 (left hand side) and MMBR901 & MMBT2907 (right hand side) Ensure that your layout accommodates these packages. Don't do a layout with leads transposed!

Microwave Amplifier Design

EE 414/514 Lab - Fall 2006

Robert J. Weber[1]

This laboratory design project will be constructed using either the MMBR901 bipolar transistor or the BSS83 NMOS FET for the rf devices. The dc operating point of the transistor will be V_{ce} = 10 volts and I_c = 20 mA or V_{ds} = 10 volts and I_d = 20 mA. There are three separate subsystems to be designed in the complete design project. The three sub-systems are 1) an oscillator, 2) an amplifier, and 3) a filter.
The first sub-system to be designed is the amplifier section.

There are two scattering parameter files used in the MMBR901 design. The first is the high gain set used to establish stability etc. The second lower gain set is used to determine the match and gain after the amplifier part is stabilized using the high gain set. The oscillator will be designed using the low gain set.

AMPLIFIER SPECIFICATIONS

frequency: 1.0 to 1.5 GHz - Undergraduates – bipolar, 0.8 to 1.0 GHz - FET
1.5 to 2.0 GHz - Graduate Students
to be determined first and then
agreed upon by the group and the lab instructor.

bipolar
gain: $20 \log|S_{21}|$ = (16.-6xfreq) min dB at the design frequency
where freq is given in GHz – based on high gain scattering parameters.

FET
gain: $20 \log|S_{21}|$ = (9.-6xfreq) min dB at the design frequency
where freq is given in GHz – based on high gain scattering parameters.

return loss: input: $20 \log|S_{11}|$ = more than 15 dB return loss
output: $20 \log|S_{22}|$ = more than 15 dB return loss.

bandwidth: $f_o \pm 5$ MHz; f_o = design freq.
(Bandwidth is a minimum - it can be wider)

impedance: input and output of amplifier should be matched
using 50 + j0 ohms reference impedances.

stability: the amplifier must be stable from dc (or as low as we measure the transistor) to at least 6 GHz since f_t is at least 6 GHz at I_c = 20 mA. Even mode stability is assured if K>1 and $|\Delta_s|$<1 at all frequencies of interest. This is stability of the completed amplifier including bias circuits - not just the transistor.

Some good advice for the design is to consider how the components will reside on the PC board, tha is, all components must be soldered to copper on the board. That requires small patches of copper that must be included in the model. A standard "solder pad" size to be used in this design is 75 x 75 mils and it is modeled as a microstrip line (MLIN) with length = 75 mils and width = 75 mils. The bipolar transistors have three terminals: base, collector, and emitter, therefore, three pads are required with dimensions as follows: width = 75 mils, length = 75 mils. The NMOS FET has four terminals: drain, gate, source, and body. Periodically stop and sketch or display your circuit as you have modeled it on ADS^{tm} and as it will appear on the board. This will enable you to see redundancies and mistakes more clearly. For example, if a resistor and a capacitor are to be electrically connected, they require a 75 x 75 mil pad between them so that the resistor lead and one end of the chip capacitor end can be soldered to it. The resistor and capacitor DO NOT each require a 75 mil square pad! Be sure to include the parasitics that were measured for the resistor, capacitor, and inductor. For the first cut at the design you may ignore the parasitics, but the parasitics eventually have to be included! You should get started with the impedance matching right away so that you can generate good questions well before the design is too far underway for you to recover in a timely fashion.

P.S. The emitter or source must go directly to ground! DO NOT use an emitter or source resistor to improve dc bias stability - you'll make the circuit rf unstable. Note that when the series oscillator is designed in the next segment of this laboratory exercise (for the undergraduates), the emitter or source is purposely lifted off of ground to provide feedback to generate oscillations.

Microwave Amplifier Design

EE 414/514 Lab - Fall 2006

Robert J. Weber

AMPLIFIER LAB PROCEDURE HINTS

For the lab, here is a procedure you can follow if you are having a difficulty getting started. Your goal: the dB magnitude of S21 is to be greater than (16.-6xfreq-GHz) for the MMBR901 bipolar amplifier and (9.-6xfreq) for the BSS83 NMOS FET amplifier. The dB magnitudes of S11 and S22 need to be more negative than -15 dB.

Step 1 The scattering parameters of the devices are available on the class web site. The MMBR901 and BSS83 scattering parameters were measured with the emitter/source directly shorted to ground with an approximately 0.3 nH inductor. You will likely be adding a solder pad in series with these terminals (don't add another 0.3 nH for the ground impedance since it is already in the scattering parameters). The grounding solder pad will increase the inductance and this is accounted for in ADS when you add the transmission line in series with the common terminal. When you design the oscillator circuit, you may need to consider subtracting this inductance out.

Step 2 Add a 0.075 x 0.075 inch (75 mil x 75 mil) pad to the input and output of the device for bonding/soldering pads. You can only put components on the external end of that pad. Use a transmission line (TLIN in ADS) for the pad. You can use Linecalc for the parameters or easier yet, use the ADS MSUB on your workbench and use a MLIN component. Whenever a component is added later, you will need a minimum area of 0.075 x 0.075 inch to solder to. You will be using 1206 chips for the capacitors and resistors and 0603 chips for the inductors. These are the components measured in lab. The average values from different measurements will be put on the class web site.

Step 3 Stabilize the device at your design frequency. (this is a maximum gain amplifier - not designed for maximum power output but for maximum gain). You may choose to stabilize the amplifier either on the input or the output (why). The K needed is determined by the magnitude of the gain needed (specification given above) and the S21/S12 ratio of the device (see the lecture or text for the equation). The value of the resistor is determined from the CAD program R_VS_K or the equations given on the web site.

Step 4 Calculate the simultaneous conjugate match for the device at the ***output*** of the soldering pads after the device is stabilized. You get the match from ADS or whatever program you are using. If you use Spice, determine the scattering parameters and use the simultaneous match equations from the text or the notes. It will have a simultaneous match after you stabilize it. Synthesize the matches on the input and the output right at the external ends of the pads. You may use a MLIN (in ADS) for the pad. Use a MSUB command on your workbench to establish the board parameters. The board parameters are in the ADS start up guide.

Step 5 Stabilize the device from 10 MHz to 6 GHz (the range of the scattering parameters). You may have to add series LC circuits in parallel with resistors or parallel LC circuit in series with resistors on the input or output of the device. The LC circuits are resonant at your design frequency so they don't affect the match you already determined when the are inserted in your circuit. You will likely need one circuit for the low frequency end and one circuit for the high frequency end. Keep in mind that you will need a dc block at the input and output (shunt L to ground or series C). The part needs to be biased with dc from the bias regulator. Keep that in mind so you can hook up the circuit later without disturbing the match.

Step 6 After the circuit is stabilized and the match is determined, then add pads for the components you need. Each "real" component is a RLC circuit. Each transmission line has an LC circuit. You need to change the values of the matching network components to accommodate the parasitics of the pads and the components. Take one component at a time as you add it and subtract its effect from the values of the matching network components.

After you have the match, stability, and real components in your circuit, congratulate yourself! After this moment of satisfaction, move on to the oscillator design. You should keep your lab TA up to date on your progress. He/she may also be requesting a look at your notebook for your design at some time so please keep one.

Microwave Oscillator Design

(Undergraduate Assignment – graduate assignment, see below)

EE 414/514 Lab - Fall 2006

Robert J. Weber[1]

Maximum Power Conversion Oscillator Design Using Common Terminal Feedback:

The second part of the lab project is the design of an oscillator to drive the amplifier. It will serve as the signal source for the amplifier and will oscillate at the design frequency. A tendency to oscillate at any other frequency is considered a poor design. A program (S3P) written by Robert J. Weber[2] is used to solve for the necessary common terminal feedback reactance, optimum output load, and the input impedance. The power output requirement at 1 GHz is 60 mW (+17.7 dBm) into 50 Ohms and 40 mW (+16 dBm) at 2 GHz. The method we are using should make an output of 80 mW (+19 dBm) realizable at 1 GHz for the bipolar. Approximately 3dB less power would be expected from the BSS83 FET since its highest frequency of oscillation is considerably lower than the bipolar MMBR901.

The design procedure is as follows (refer to Figure 3 for the circuit block diagram):

1. Use either the optimum inductance calculation in the text (page 136) or the opt_ind program to determine the optimum parallel inductance the circuit needs on the collector of the transistor used as an amplifier.

2. Determine the optimum resistive load, R, as given by the following relationship:

$$P_o = \frac{(V_Q - V_{sat})^2}{2R} = \frac{(I_Q - I_{min})^2}{2} R$$

$$R = \frac{V_Q - V_{sat}}{I_Q - I_{min}}$$

where V_Q and I_Q are given at the quiescent operating point of the rf transistor. Then the optimum complex load, Z_{opt}, to be used in the computer program is the above resistance R in parallel with $j\omega L$ from step one. Be sure to change the parallel circuit into the appropriate series combination of R and X.

3. In the S3P program, enter 50 for Zo, 2 for 2-port data and S for the S-parameters of the active device. Enter the S-parameters in MAG/ANG form and the Z_{opt} for the "optimum load" in form required by the program. The program will also ask you for the magnitude of the input reflection coefficients (Γ_{in} for gamma-in) at ports 1 and 3, which are shown in the figure. Remember that a magnitude of one implies that no power is lost in the terminations. Γ_1 (for gamma-source) and Γ_3 (for gamma-common terminal) will be less than one if losses are present (some of the incident power is not reflected). In order for oscillations to occur, the product of the reflection coefficients at any point in the circuit must be one. Therefore, the magnitudes of Γ_{in1}, and Γ_{in3} must be greater than one. Use about 0.95 for the reflection coefficient magnitudes on the common terminal and the input or use circles relating to the series resistance of the component used on the port.

The computer program will generate a solution at this point, that gives you a value for the ground (emitter) impedance, source impedance (base termination), and the oscillator load impedance, Z_{opt}' which are the impedances that you should design with in ADS.

4. Design an output matching network which presents an impedance of Z_{opt}' (as determined by the S3P program) to the output of the transistor--you must include the transistor collector pad, bias choke, etc. in this impedance network.) Design an emitter network that presents the necessary reactance to the emitter at the design frequency---take dc bias into account (a capacitor does not pass dc current!) and include the emitter pad. Design an input network that presents the given source impedance to the base---again, you must include the transistor base pad, bias choke, etc. If you used stabilization resistors in the amplifier design for device stabilization at f_o, eliminate them at the start of the oscillator design. You may need to use other resistors for stabilizing the oscillator at other frequencies. You can use ADS to fine tune and optimize component values just as in the amplifier case.

5. Because the oscillator will actually deliver more power than the amplifier (if the amplifier was designed for maximum gain,) a pad (attenuator) needs to be placed between the oscillator and the amplifier. This will be constructed from three resistors in a tee arrangement or a pi arrangement. The value of the attenuator is determined by assuming the output of the amplifier will be limited to 20 mW. This power is smaller than the oscillator since the oscillator was designed for maximum power conversion and the amplifier was designed for maximum gain. You will know the gain of the amplifier from you analysis and you know the power expected from the oscillator. You can use the design equations from the text (p153) to design the attenuator.

6. Calculate (using ADS) the output impedance of the oscillator. It should have negative resistance only at the design frequency. You could use the negative impedance converter given in the text on page 211 to enable ADS to plot negative impedance on a reflection coefficient chart. If the output impedance has negative resistance at frequencies significantly removed from the design frequency, the oscillator needs to be modified to remove this tendency to oscillate at other frequencies. The base bias circuit is often a problem. If one uses an inductor to bias the base, the series resonance of the inductor with its bypass capacitor might result in the oscillator having negative output impedance at that frequency. Remember that you are raising the emitter off of ground and thus the S parameters of the device are not indicators of the stability of the circuit any more. The effect of the impedance inserted in the emitter is called series feedback.

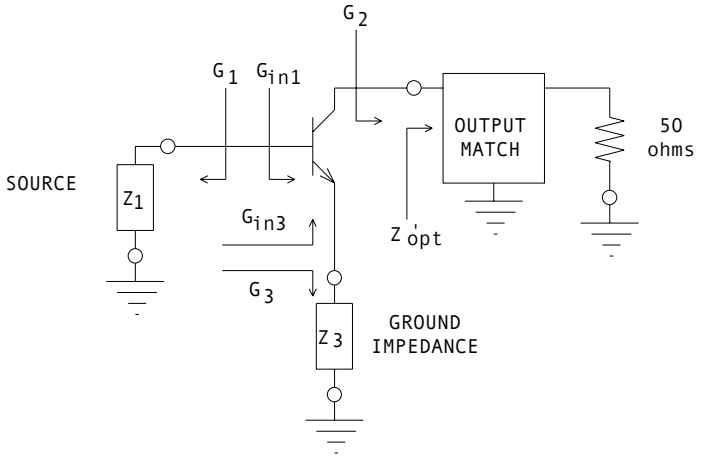


Figure 3: A block diagram depicting basic components of a maximum power conversion, common-terminal feedback oscillator.

Sample Input/Output of the S3P Program

```
                    OSCILLATOR PROGRAMS
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   RESULTING FROM THE USE OR ATTEMPTED USE OF THIS SOFTWARE
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  THIS PROGRAM IS TO BE USED BY A STUDENT ONLY FOR CLASSWORK
             OR RESEARCH WITH ROBERT J. WEBER


        ENTER Y IF YOU AGREE TO THESE CONDITIONS
     ENTER N IF YOU DON'T AGREE TO THESE CONDITIONS


ENTER Z0
      50.000000
ENTER     2    FOR 2 PORT DATA
ENTER     3    FOR 3 PORT DATA
          2
ENTER     S    FOR S PARAMETERS
ENTER     Z    FOR Z PARAMETERS
ENTER     Y    FOR Y PARAMETERS
S
ENTER THE S PARAMETERS IN  VOLT-MAGNITUDE
                           PHASE-DEGREES
ENTER S11,S12,S21,S22
     .8000         135.0
    1.0000E-02     120.0
     2.000         60.00
     .8000        -20.00

ENTER THE OPTIMUM LOAD FOR THE DEVICE
ENTER THE RESISTANCE OF THE SHUNT LOAD
AND THEN THE MAGNITUDE OF THE PARALLEL RESONATING REACTANCE


    O--------------o--------------
                   |              |
                -------        -------
                |     |        |     |
                |     |        |     |
                | jXr |        |Ropt |
                |     |        |     |
                |     |        |     |
                -------        -------
                   |              |
    O--------------o--------------


  Ropt = ?,  Xr = ?
   200        200
```

```
THE OPTIMUM IMPEDANCE IS           (100.000000,100.000000)
CONSISTING OF A PARALLEL RESISTANCE OF      200.000000 AND REACTANCE OF j
    200.000000 OHMS

ENTER DATA FOR GAMMA SOURCE
ENTER THE TYPE OF INPUT YOU WISH

ENTER  QE  FOR EXTERNAL Q
ENTER  QU  FOR UNLOADED Q
ENTER  QL  FOR LOADED Q
ENTER  MA  FOR MAGNITUDE OF GAMMA
ENTER  CR  FOR CENTER AND RADIUS OF CIRCLE
ENTER  RS  FOR SERIES R + jX CIRCLE
ENTER  RP  FOR RP IN PARALLEL WITH + jB CIRCLE

RS
0.5
ENTER THE VALUE OF THE SERIES RESISTANCE
USING A RADIUS OF    9.900990E-01
AT A CENTER OF    9.900990E-03 + j    0.000000E+00

ENTER THE DATA FOR GAMMA COMMON TERMINAL
ENTER THE TYPE OF INPUT YOU WISH

ENTER  QE  FOR EXTERNAL Q
ENTER  QU  FOR UNLOADED Q
ENTER  QL  FOR LOADED Q
ENTER  MA  FOR MAGNITUDE OF GAMMA
ENTER  CR  FOR CENTER AND RADIUS OF CIRCLE
ENTER  RS  FOR SERIES R + jX CIRCLE
ENTER  RP  FOR RP IN PARALLEL WITH + jB CIRCLE

RS
0.5
ENTER THE VALUE OF THE SERIES RESISTANCE
USING A RADIUS OF    9.900990E-01
AT A CENTER OF    9.900990E-03 + j    0.000000E+00
RADIUS FOR 1         1.010101
RADIUS FOR 2     9.900990E-01
CENTER FOR 1,1     (-1.010101E-02,0.000000E+00)
CENTER FOR 1,2      (0.000000E+00,0.000000E+00)
CENTER FOR 2,1      (9.900990E-03,0.000000E+00)
CENTER FOR 2,2      (0.000000E+00,0.000000E+00)
THETA AND PHI1 AND PHI2 ARE       -1.701895        3.403790    3.578802E-08
AMA =        1.951312
CONK =   -5.101644E-01
MAG1 =        1.018024 OR        1.000000
MAG3I=        1.019846 OR        1.000000
MAG3 =    9.805397E-01 OR        1.000000

SOLUTION ONE

REFLECTION COEFFICICIENTS IN MAG AND ANGLE-DEG

   INPUT REFLECTION COEFFICIENT IS    1.018024       141.8389
 2PORT LOAD REFLECT COEFFICIENT IS    .6201737       29.74488
 GROUND INVERSE REF COEFFICIENT IS    1.019846       164.8272

PRESENT THESE REFLECTION COEFFICIENTSTO THE DEVICE \/\/\/
  SOURCE REFLECTION COEFFICIENT IS    .9822952      -141.8389
 3PORT LOAD REFLECT COEFFICIENT IS    .6326987       30.86249
  GROUND REFLECTION COEFFICIENT IS    .9805397      -164.8272
```

```
IMPEDANCES IN REAL AND IMAGINERY FORM

                INPUT IMPEDANCE IS   -.4999991       17.29349
        TWO PORT LOAD IMPEDANCE IS    100.0000       100.0000
OR RES=RP IN PARALLEL WITH REACT XP   200.0000       200.0000
 GAMMA INVERSE GROUND IMPEDANCE IS   -.5000003       6.658674

\/\/\/ PRESENT THESE IMPEDANCES TO THE DEVICE \/\/\/
                SOURCE IMPEDANCE IS    .4999993      -17.29349
      OSCILLATOR LOAD IMPEDANCE IS    95.46526       103.3341
OR RES=RP IN PARALLEL WITH REACT XP   207.3168       191.5297
                GROUND IMPEDANCE IS    .5000001      -6.658674
ENTER CARRIAGE RETURN TO CONTINUE

SOLUTION TWO

REFLECTION COEFFICICIENTS IN MAG AND ANGLE-DEG

   INPUT REFLECTION COEFFICIENT IS    1.000000     -394.71690E-08
 2PORT LOAD REFLECT COEFFICIENT IS    .6201737       29.74488
 GROUND INVERSE REF COEFFICIENT IS    1.000000     -203.02000E-08

PRESENT THESE REFLECTION COEFFICIENTSTO THE DEVICE \/\/\/
  SOURCE REFLECTION COEFFICIENT IS    1.000000      394.71690E-08
 3PORT LOAD REFLECT COEFFICIENT IS    1.000000     -760.94910E-08
  GROUND REFLECTION COEFFICIENT IS    1.000000      203.02000E-08

IMPEDANCES IN REAL AND IMAGINERY FORM

                INPUT IMPEDANCE IS   -50.00000     -145.15660E+07
        TWO PORT LOAD IMPEDANCE IS    100.0000       100.0000
OR RES=RP IN PARALLEL WITH REACT XP   200.0000       200.0000
 GAMMA INVERSE GROUND IMPEDANCE IS   -50.00000     -282.21740E+07

\/\/\/ PRESENT THESE IMPEDANCES TO THE DEVICE \/\/\/
                SOURCE IMPEDANCE IS   -50.00000      145.15660E+07
      OSCILLATOR LOAD IMPEDANCE IS   -50.00000     -752.95160E+06
OR RES=RP IN PARALLEL WITH REACT XP -113.38720E+14 -752.95160E+06
                GROUND IMPEDANCE IS   -50.00000      282.21740E+07
ENTER   G   FOR A DIFFERENT VALUE OF GAMMA
ENTER   Z   FOR A DIFFERENT VALUE OF LOAD
ENTER   N   FOR STOPPING
n
Stop - Program terminated.
```

Microwave Oscillator Design

(Graduate Assignment)
EE 414/514 Lab - Fall 2006
Robert J. Weber[1]

Maximum Power Conversion Oscillator Design Using Loop Feedback

Those students taking EE514 will design a loop oscillator using the design criteria given in Section 8.4.6 in the text. The part inside the oscillator will have a load on it that is the same as in the discussion above for the series feedback oscillator. A one-pole resonator will be inserted in the feedback to help control the frequency. A loop oscillator program is available for student use if they desire.

Microwave Filter Design

(Undergraduate Assignment - graduate assignment, see below)

EE 414/514 Lab - Fall 2006

Robert J. Weber

The third project is the design of a two pole equal element Butterworth, g1=1.414, g2=1.414, quarter wavelength filter at the center frequency fo with a 6 % bandwidth to be put on the output of the amplifier. The center frequency fo is the same as was chosen for the amplifier and oscillator. The design theory is contained in the text and will be covered in the class lectures. The filter will have some loss since the resonators do not have infinite Q. You can estimate the loss you expect by using lossy line analysis in ADS. The figure below shows a typical two-pole quarter wavelength transmission line inverter coupled resonator filter. The filter is often called a comb line filter since each resonator is grounded at the lower end. The configuration looks like the teeth of a comb. For a two-pole filter, there are only two "teeth". However, a filter with many poles would have many "teeth" in the comb. If resonators were coupled differently such that the grounds on adjacent resonators are on opposite sides of the filter, i.e. resonator one is grounded at the bottom, resonator two at the top, etc., then the filter would be called an inter-digital filter with a physical shape similar to interlacing the fingers together from each hand. Fingers are called digits in anatomy.

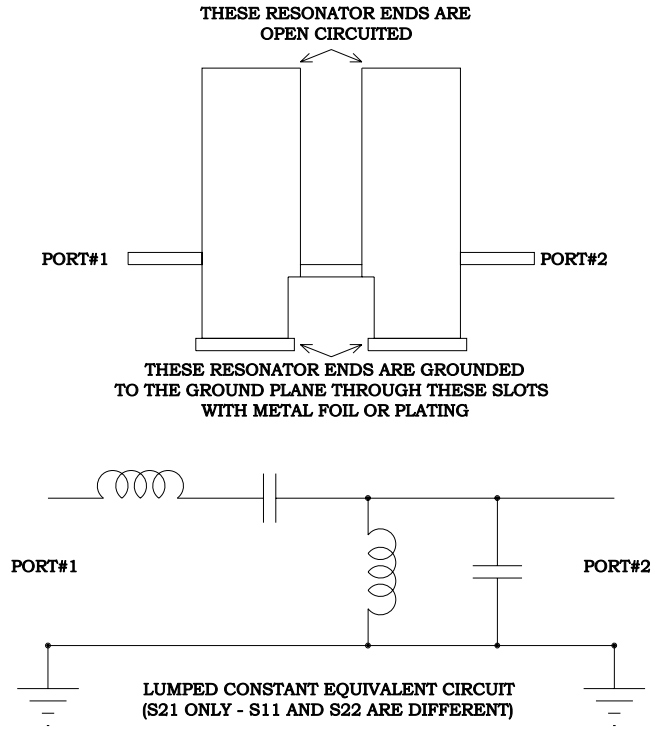

Figure 4: Top view and band pass prototype
of a two pole comb line microstrip filter.

The open circuited ends of the resonator will need to be foreshortened due to fringing capacity (see the text in Section 2.7.7). The short circuited ends of the resonator will need to be foreshortened as well. The ground is on the back side of the printed circuit board, not on the front side. ADS assumes the ground is on the top. The thickness of the board used in this lab is 0.03 inch. The calculations are done without foreshortening. However, when the parts are geometrically layed out, both the open circuited end and the short circuited end of the resonators need to be foreshortened.

Microwave Filter Design

(Graduate Assignment)
EE 414/514 Lab - Fall 2006
Robert J. Weber

The graduate students will design an edge coupled two pole filter on their boards with the same 4% bandwidth. The filter will be a Butterworth filter using the same g values as given in the discussion above.

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(1) This version of the laboratory writeup is a modified versus of older laboratory writeups. The older versions of the laboratory were in part written by Joe Ellerbach and Paul Stucky.

(2) Weber, R. J., "Oscillator Design Using S-Parameters and a Predetermined Source or Load," 45th Annual Symposium on Frequency Control, pp. 364-367, May 1991.