OZ965

High-Efficiency Inverter Controller

FEATURES

- Single-stage power conversion, requiring only a +5v voltage source
- Reduces the number of components and board size by 30% compared with conventional design
- Supports both floating and grounded secondary designs
- 90% efficiency vs. typical 75% efficiency of conventional designs
- Built-in internal open-lamp and short-circuit protections
- Wide dimming range
- Supports multiple CCFL lamps
- Simple and reliable 2-winding transformer design
- Eliminates leakage current when used in a floating secondary design
- Constant-frequency design eliminates interference with LCDs

ORDERING INFORMATION

OZ965G - 16-pin plastic SOP
OZ965R - 16-pin plastic TSSOP
OZ965IG - 16-pin plastic SOP
OZ965IR - 16-pin plastic TSSOP

GENERAL DESCRIPTION

The OZ965 is a single chip, high-efficiency, Cold Cathode Fluorescent Lamp (CCFL) backlight inverter controller whose primary function is to convert +5 volt DC power to approximately 600 VAC. Additionally, the OZ965 performs the lamp dimming function with an analog voltage or low frequency Pulse Width Modulation (PWM) control.

Operating Principle:
The CCFL tube, transformer secondary, and capacitor form a resonant circuit. The OZ965 utilizes the low energy loss resonate mode principle to deliver a very high efficiency inverter.

The OZ965 drives the transformer primary with a variable pulse width voltage directly from the +5v supply. The resultant primary drive current is alternately reversing with zero-voltage-switching. Because of the transformer leakage inductance and the secondary resonant circuit, the secondary voltage and current are approximately sinusoidal. This sinusoid results in very little harmonic emi/rfi emissions.

The OZ965 operates at a single, constant frequency in a PWM mode. Typical operating frequency ranges between 30 KHz to 200 KHz, dependent upon the CCFL and transformer characteristics. Intelligent open-lamp protection provides design flexibility so various transformer models/manufacturers may be used.

Its high driving capability allows the OZ965 to drive high power MOSFETs.

The single stage design results in a low cost, reliable transformer without expensive, less reliable secondary fold-back treatment. The transformer does not require a more expensive center tapped primary.

The OZ965 is available in 16-pin SOP and TSSOP packages. It is specified over the commercial temperature range of 0°C to +70°C, and the industrial temperature range of -40°C to +85°C.

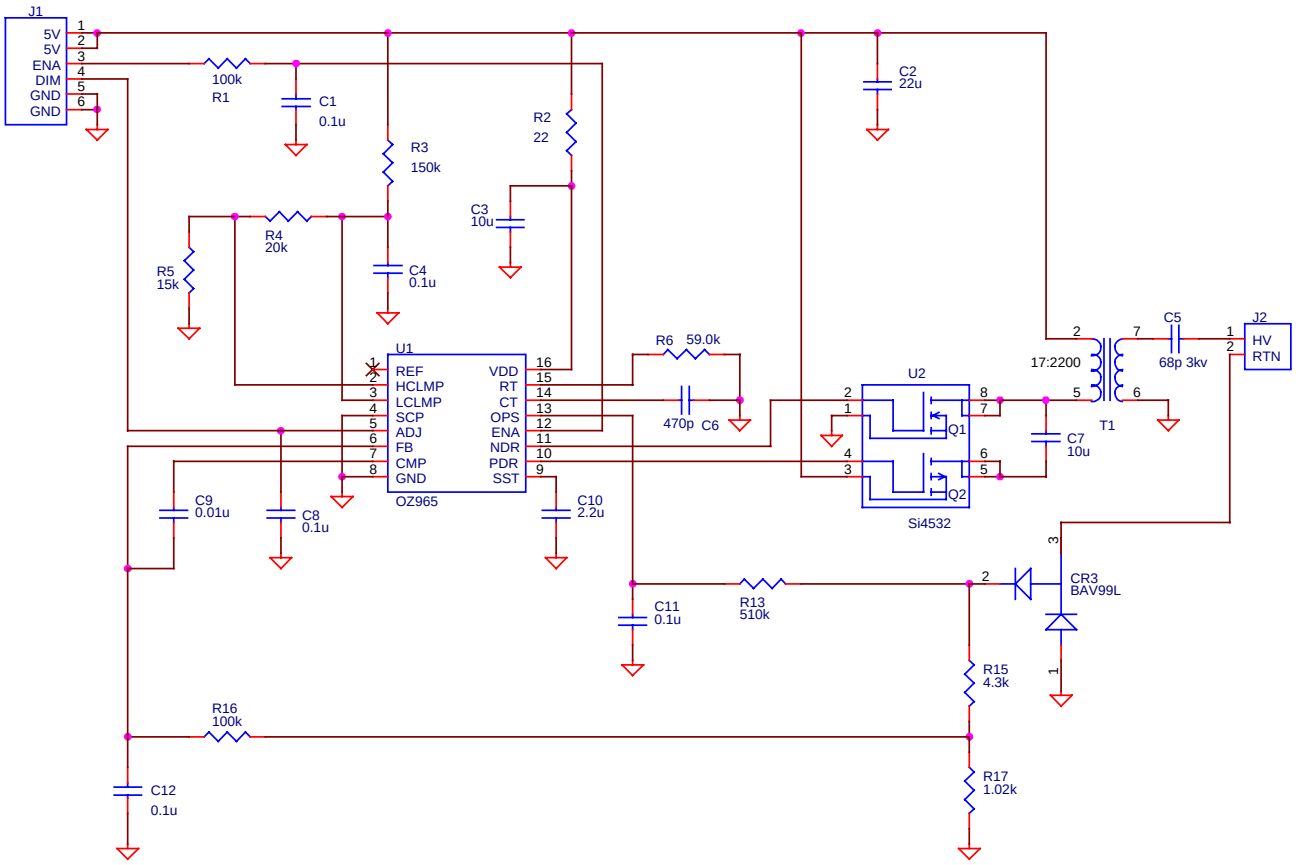


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

Refer to the functional block diagram in Figure 2, below, and the Pin Description Table on page 3.

Power is transferred to the transformer primary by the N-MOSFET, driven by the MOSFET gate driver out of pin NDR. The P-MOSFET resets the primary field, driven by pin PDR. The usual design results in approximately 50% duty cycle at full lamp intensity. Terminating the NDR signal earlier than the full brightness lamp pulse width performs lamp dimming, using the analog dimming. The voltages on pins HCLMP and LCLMP set a threshold voltage for the ramp comparator setting the maximum duty cycle for NDR.

A pulse generator circuit creates the clock signal with the frequency determined by an external, constant current setting resistor (RT) and timing capacitor (CT).

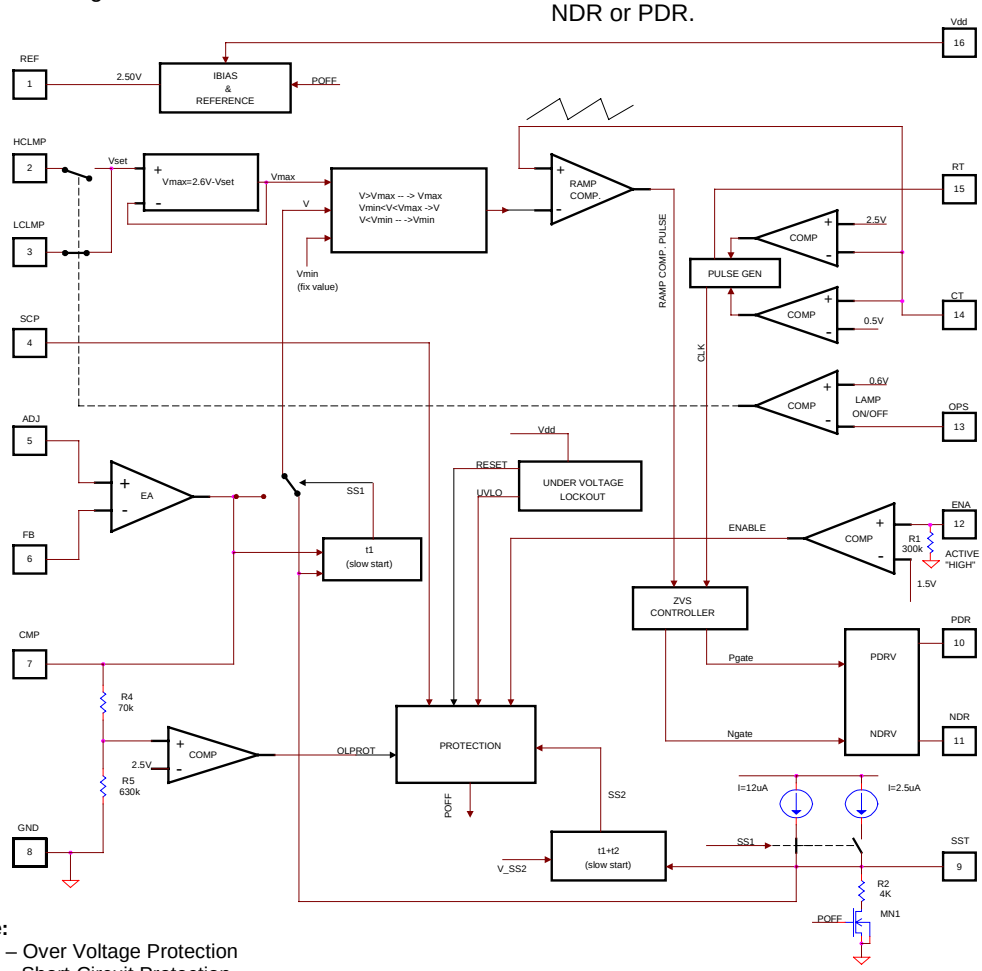
The “soft-start” circuit ensures a reliable and long lamp life starting condition.

“Soft start” gradually increases the energy delivered to the secondary.

When the OZ965 is enabled at pin ENA, the capacitor on pin SST determines the duration of the “soft-start” period, gradually increasing the NDR pulse width to the regulated brightness. The “soft-start” period provides sufficient time for the lamp to ignite.

For system reliability there are several circuit protections provided. To ensure a controlled output, the secondary current is monitored on pin FB and is compared to a reference voltage on pin ADJ. The NDR signal is shortened or lengthened dependent upon this feedback. Protection is provided by the resultant signal, CMP, monitoring for a lamp removal condition. Short circuit protection is provided at pin SCP. The OPS signal selects either HCLMP or LCLMP providing current protection against an “Open Lamp” condition at start-up. The OPS signal also allows adjustment to different transformer models.

To reduce power dissipation, the switch (MOSFET) drive signals are “break-before-make” with a short, fixed off time between activation of NDR or PDR.



Note:
OVP – Over Voltage Protection
SCP – Short-Circuit Protection
UVL – Under Voltage Lockout

Figure 2. Functional Block Diagram

PIN DESCRIPTION

Names	Pin No.	I/O	Description
REF	1	O	Reference voltage output. Nominal voltage is 2.5 V.
HCLMP	2	I	Clamping maximum duty cycle under normal operation.
LCLMP	3	I	Clamping maximum duty cycle under open-lamp condition.
SCP	4	I	Short-circuit protection input (V_{TH}=0.6V)
ADJ	5	I	Reference voltage input for dimming control.
FB	6	I	Current sense feedback.
CMP	7	O	Compensation for the current sense feedback.
GND	8	GND	Ground.
SST	9	I	Soft-start ensures lamp current pulses gradually increases to its normal value
PDR	10	O	Gate drive output for the P-MOSFET.
NDR	11	O	Gate drive output for the N-MOSFET.
ENA	12	I	Enable input, active high (V_{TH}=1.5V)
OPS	13	I	Output current sense (V_{TH}=0.6V)
CT	14	I/O	Timing capacitor. CT and RT set the clock frequency.
RT	15	I/O	Timing resistor. Fosc = 1.91/(Rt • Ct)
VDD	16	PWR	Supply voltage input.

ABSOLUTE MAXIMUM RATINGS

VDD	5.5V
GND	+/- 0.3V
Logic inputs	-0.3 V to VDD+0.3V

	OZ965	OZ965I
Operating temp.	0°C to 70°C	-40°C to 85°C

Operating junction temp.	150°C
Storage temp.	-55°C to 150°C

	OZ965	OZ965I
Power dissipation		
- 16-pin SOP	0.720W	0.580W
- 16-pin TSSOP	0.690W	0.550W
Thermal Impedance (θ_{J-A})		
- 16-pin SOP	111°C/W	111°C/W
- 16-pin TSSOP	115°C/W	115°C/W

RECOMMENDED OPERATING RANGE

VDD	4.75 V to 5.5V *
Fosc	30 KHz to 200 KHz
Rosc	50 k to 150 k

* The VDD range can be extended to 4.5V – 5.5V with all parameters within specification except the shut down function which may not work.

FUNCTIONAL SPECIFICATIONS

Parameter	Symbol	Test Conditions		Limits		Unit
		4.75 V < VDD < 5.25 V	Min	Typ	Max	
Reference Voltage						
Nominal voltage	Vref	I_{load} = 0.1 mA,	2.37	2.50	2.63	V
Line regulation			-	6	-	mV/V
Load regulation		I_{load} = 0.2 mA to 1.0 mA	-	1	-	mV/mA
Oscillator						
Initial accuracy	fosc	Ct = 470 pF, Rt = 49.9 k	76	81	86	KHz
Ramp peak			-	2.54	-	V
Ramp valley			-	0.48	-	V
Temp. stability		TA = -40°C to 85°C	-	-	200	ppm/°C
Error Amplifier						
Input bias current		ADJ = FB = 2.0 V	-	0.25	-	uA
Input offset voltage		VFB = 4.0 V		5	10	mV
Input voltage range			0	-	VDD-1.5	V
Open loop voltage gain			-	65	-	dB
Unity gain bandwidth			-	1.5	-	MHz
Power supply rejection			-	60	-	dB
Under-Voltage Lockout						
Positive-going threshold voltage			**See Table 1, page 5**			
Negative-going threshold voltage			**See Table 1, page 5**			
Supply						
Supply current - Enable Low	I_{OFF}		-	150	200	µA
Supply current - Enable High	I_{ON}	VDD = 5.0 V	-	0.8	2.0	mA
NDR output						
Output high voltage	V_{OH}	Isource = 10 mA, VDD = 5V	-	4.75	-	V
Output low voltage	V_{OL}	Isink = 10 mA, VDD = 5V	-	0.25	0.5	V
Output resistance	R_{OUT}		-	10	-	Ω
PDR output						
Output high voltage	V_{OH}	Isource = 10 mA, VDD = 5V	-	4.7	-	V
Output low voltage	V_{OL}	Isink = 10 mA, VDD = 5V	-	0.5	-	V
Output resistance	R_{OUT}		-	15	-	Ω
Break-Before-Make						
Qn off to Qp on delay	T_{HL}		-	250	-	ns
Qp off to Qn on delay	T_{LH}		-	220	-	ns
High Clamp						
Duty cycle of NDR	HCLMP	OPS=1 V, V_{HCLMP} = 0V	92	94	96	%
		OPS=1 V, V_{HCLMP} = 1.8V	-	14	-	
Low Clamp						
Duty cycle of NDR	LCLMP	OPS=0 V, V_{LCLMP} = 0V	92	94	96	%
		OPS=0 V, V_{LCLMP} = 1.8V	-	14	-	
Max. / Min. Duty cycle						
Duty cycle of NDR			6	-	95	%

		OZ965				OZ965I			
Parameter	**Test Conditions**		**Limits**		**Unit**		**Limits**		**Unit**
	4.75V < VDD < 5.25V	Min	Typ	Max		Min	Typ	Max	
Under-Voltage Lockout									
Positive-going threshold voltage		-	3.9	4.3	V	-	3.9	4.5	V
Negative-going threshold voltage		3.2	3.4	-	V	3.0	3.4	-	V

Table 1. Under-Voltage Lockout for OZ965 and OZ965I (Industrial)

FUNCTIONAL INFORMATION

1. Steady-State Operation

Referring to the schematic shown in Figure 1, the OZ965 operates at a selectable constant frequency through C6 and R6 in pin 14 and Pin 15. It drives one pair of N- and P- power MOSFET switches, Q1 and Q2. These two switches operate in a complementary duty-cycle mode. In other words, Q2 is turned on after Q1 is turned off and vice versa. Figure 2 shows the functional blocks of the OZ965. The OZ965 provides about 250ns of delay for the break-before-make circuit to ensure Q1 and Q2 will never be turned on simultaneously. Figure 1 shows a typical application circuit with input voltage of 5V. The power train circuit includes T1, C7, U2, and C5. The transformer T1 is subjected to a rectangular switching waveform. The current and voltage waveform seen at the CCFL load are quasi-sinusoidal.

Using a large capacitance for C7 allows the steady-state voltage across C7 to assume a dc value of $V_{C7} = -V_{IN} \bullet D/(1-D)$, where D is the turn-on duty cycle of Q1. **Notice that in the OZ965, the minimum duty cycle of Q1 is set at 6%.**

In normal operation, Q1's duty cycle is tuned to 0.5 at a full-load condition. Referring to Figure 3 (on page 6), at the beginning of a positive half-cycle, **t1**, Q2 turns off. Q1 turns on shortly after at **t2**. The magnetizing current, I_M, increases by a rate of V_{IN}/L_M, where L_M is the primary-side magnetizing inductance of the transformer T1. The induced voltage on the secondary winding is positive with respect to the assigned polarity of the transformer. Output current flows from the upper end of the winding through the output capacitor, C5, and into the upper end of the CCFL. While Q1 is on, the transformer transfers energy to the secondary side through a "forward" coupling effect, similar to a forward dc-dc converter. The waveforms and the corresponding timing of the primary winding voltage, magnetizing current, input current, and secondary current are shown in Figure 3, on page 6.

Q1 turns off at the end of the positive half-cycle, **t3**. A portion of the magnetizing current is now diverted to flow through C7 and the intrinsic drain-source diode of Q2. As a result, the voltage applied across the primary winding and the secondary winding both become negative. Meanwhile, the magnetizing current flows from the lower end of the secondary winding into the lower end of the CCFL.

The turn-off of Q1 initiates the negative half-cycle. Q2 turns on shortly after at **t4**. The dc voltage on C7 resets the magnetizing current and the transformer core flux. Q2 turns off at the end of the negative half-cycle, **t5**. This forces the primary current to move from Ground through the intrinsic source-drain diode of Q1, the primary winding, and back into the power source. Shortly after Q2 turns off, Q1 turns on again, starting a new positive half-cycle.

Notice that during the positive half-cycle, the input current is the sum of the magnetizing and reflected output currents, $I_S \bullet N_2/N_1$. During the negative half-cycle, the magnetizing current essentially supports all the output current. In effect, the transformer transfers energy to the secondary side with the same coupled-inductor characteristics as a "flyback" dc-dc converter.

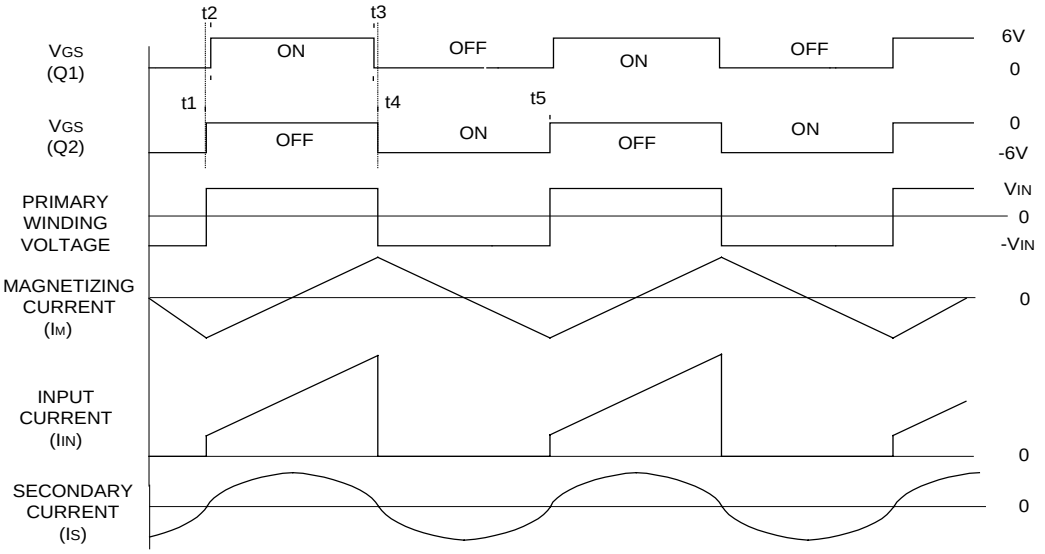


Figure 3. Typical voltage and current waveforms at 50% duty cycle

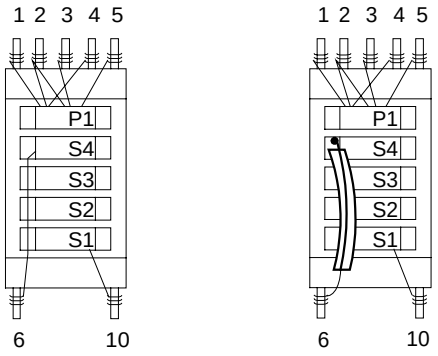
2. Transformer Design

2.1. Transformer in conventional inverter

To support high-voltage ac for driving a CCFL, the transformer's secondary winding typically has a few thousand of turns. Normally, these are divided into a few sections (for a sectioned bobbin). To avoid high voltage crossover, between sections, the maximum voltage differential is limited to less than few hundred Volts. The treatment for the finishing wire is a major engineering challenge. Another type of design is to have the secondary winding wound around a ferrite post. The high voltage differential is made possible by a good-quality manufacturing where the winding layers are properly manipulated.

In the case of sectioned-bobbin transformer, as shown in Figure 4A, the conventional current-fed Royer backlight inverter uses three primary windings sharing the same section P1, occupying 5 pins. The secondary winding is wound over sections S1 to S4. The starting wire of the secondary winding ties to Pin 10. The finishing wire has to cross all secondary-winding sections to finish at Pin 6. Consequently, this fold-back lead wire requires sufficient clearance from the winding surface (see Figure 4A). Alternatively, a layer of Mylar™ or other insulation material may be placed between the fold-back wire and the winding surface of sections S1 to S4, shown in Figure 4B, to avoid high voltage crossover.

The fold-back treatment complicates the transformer manufacturing. In addition, the fold-back structure is prone to arcing failures, particularly with narrow-body transformers.



4A. Fold-back with clearance

4B. Fold-back with insulator

Figure 4. Conventional Transformer structure

2.2. The OZ965 Inverter's transformer structure

The transformer for the OZ965 inverter is much simpler than those in conventional current-fed Royer inverters. There is only one primary winding and one secondary winding, requiring only four pins for termination. Further, the pin-out structure of the bobbin is very flexible. For instance, the primary winding can be wound first and tied to Pin 4 and Pin 5. The secondary is then wound with the starting wire tied to Pin 10, and the finishing wire tied to Pin 1, without applying an insulation tape layer. See Figure 5.

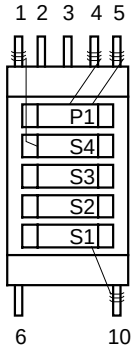


Figure 5. Two-winding structures without fold-back

This simplified bobbin structure and the removal of the fold-back design greatly improve the transformer's reliability and lower manufacturing cost. Further, the overall transformer size is reduced to a minimum with the bobbin and pins' simplification.

3. Stray Capacitance and Quasi-Resonance

A backlight system's stray capacitance partially consists of the inter-winding capacitance from the transformer's secondary winding. Additional stray capacitance from the high-voltage wiring, tube, LCD frame, and foil reflector also adds to the overall amount.

Even a small stray capacitance as little as 10 pF can generate a significant amount of leakage current. To minimize stray capacitance, it is advantageous to integrate the stray capacitance as part of the wave-shaping element.

In general, the high isolation-voltage requirement mandates that primary and secondary windings be wound on separate sections on the bobbin. Consequently, the coupling between the two windings tends to be loose, and leakage inductances high.

When properly utilized, the resonant effect between the transformer's leakage inductance and the stray capacitance can provide sinusoidal voltage and current waveforms even if the transformer is driven by square-wave voltage. By applying this quasi-resonant effect, the OZ965 inverter achieves balanced, sinusoidal drive waveforms while utilizing a constant-frequency, PWM control.

4. Operating Frequency

In general, most CCFLs can operate over a wide frequency range. For notebook computer applications, the recommended operating frequency ranges between 30 KHz and 100 KHz. Operating at a lower frequency will create audible noise and require larger inductive and capacitive components. Operating above 100 KHz, on the other hand, will generate excessive stray capacitance losses. For small LCD panels, operating the inverter at higher frequencies seem to have less impact on the losses.

For OZ965 inverter designs, setting the switching frequency slightly higher than the secondary resonant frequency will result in sinusoidal waveforms over a wide range of lamp current. An efficient design should take into consideration all stray capacitance and leakage inductance.

Notice that for the OZ965, the typical oscillator frequency is determined by the following equation as a reference:

$$Fosc=1.91/(RT \bullet CT)$$

RT is the resistor connected from Pin 15 to ground and CT is the capacitor connected from Pin 14 to ground.

5. Reset Capacitor

The magnetizing inductance of the transformer, L_M, and the reset capacitor, C6, reset each other in a natural manner. Refer to Figure 1. The absolute voltage on C7, V_{C7}, is determined by the following equation to satisfy the balanced-flux of the transformer for each switching cycle.

$$V_{C7} = V_{IN} \bullet D / (1-D)$$

D is the duty cycle of Q1. This capacitor is larger enough to ensure a dc voltage across it.

6. Power MOSFET Selection

The OZ965 is designed to drive high power MOSFETs. For example, the total gate charge of 25nC for both N- and P- MOSFETs can be easily driven through the OZ965. It provides a good solution for high-power applications.

7. Regulation and Dimming Control

In Fig. 1, the current sense resistor, R17, detects the lamp current for each half period. This rectified lamp current is integrated through an error amplifier, which consists of Pins 5, 6 and 7 of the OZ965. Notice that this average voltage at Pin 6 relates to the RMS lamp current through a conversion factor of VFB=(0.45•R17)•I(Lmp). Vary the reference voltage at ADJ, one achieves the dimming control to the CCFL. This reference pin accepts an integrated PWM signal or an analog control signal or another form – potentiometer.

Lately, digital dimming and contrast control using hot keys (Fn keys) are also gaining popularity. Digital controls are more reliable than mechanical potentiometer devices. (For digital dimming control capabilities, please refer to the OZ968, OZ969 SMBus Smart Inverter Controller devices.)

8. Soft-Start Timing

To avoid over-shoot and inrush current problems, a soft start-up function is provided. The driving pulse width increases gradually after the inverter is powered on. The lamp current starts once the striking voltage reached. This lamp current increases as the driving pulse width increases until the regulated current is achieved. The driving pulse follows the error amplifier's command. In the time that the error amplifier's output reaches the SST potential, the soft-start current is reduced to 2.5uA, which increases the ignition time needed for regular LCD panels.

9. Enable

The "Enable" signal applied to the ENA(Pin 12) initiates the starting of the inverter. Internal in IC provides a hysteresis comparator to the ENA signal so as to avoid any bi-stable mode of operation. It is always good practice to filter out any undesired noise at this pin. Notice that during shut-down condition (when ENA pin is low), both Q1 and Q2 are off. The soft-start function is always active every time when the enable signal is asserted "high".

10. Over-Voltage Protection and Short-Circuit Protection

R13 and C11 serve as noise filter for the detected lamp current. When the signal at OPS is greater than 0.6 Volt, it commands the controller to allow a maximum duty cycle determined by the HCLMP potential. On the other hand, if this signal is lower than 0.6 Volt, the LCLMP determines the maximum duty cycle. This provides a high-degree of flexibility to select transformers. High voltage transformers, unlike a well-couple design, possess a high leakage inductance and experience resonance. This resonance, depending upon the quality-factor of the equivalent circuit, generates a very high voltage that may damage the insulation. This can be seen from a practical open-lamp test. The OZ965 provides a user-programmable open-lamp protection circuit. This is to address the different characteristics of the transformers used in the inverters. For each transformer, applying with different operating frequency and different driving pulse width, its output response differs significantly. One is able to determine the optimum driving condition for the transformer and the LCD panels by selecting proper driving duty cycle, which could be determined by the potential at "HCLMP" and "LCLMP" pins. The formula for calculating the maximum duty cycle with respect to the set points is:

$$Dmax = 0.95 - 0.45Vset;\ Vset < 1.8V$$

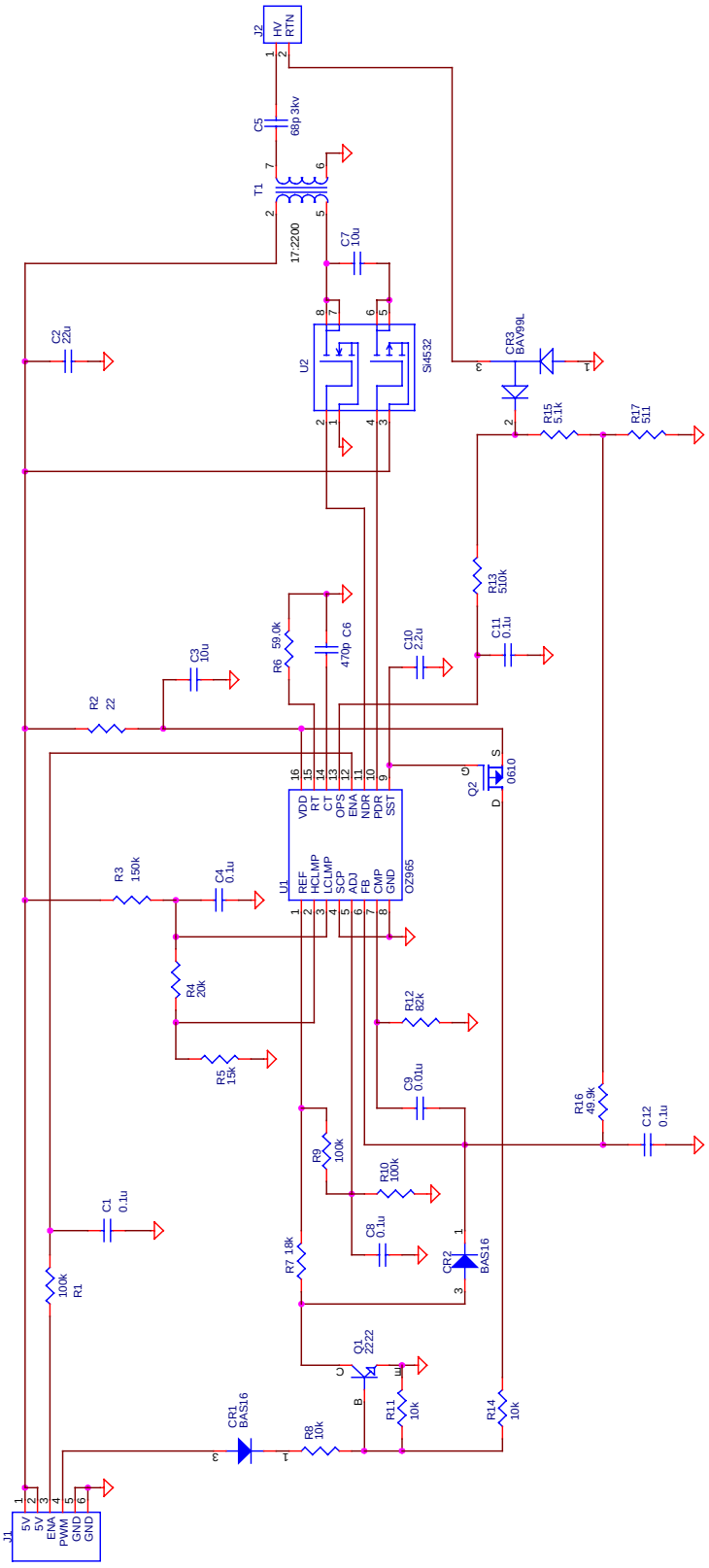
where Vset is the potential at "HCLMP" or "LCLMP". One can adjust these two set points according to the characteristics of the transformer and the loads. In an open-lamp condition, the driving pulse duty cycle is designed to provide sufficient output voltage yet safely operate the transformer. Once the striking period times out under open-lamp condition, the output drive will be terminated and the controller is in a shut-down and latch condition.

In an output short-circuit condition, the input current ramps up rapidly with a high RMS value. The SCP pin (Pin 4) detects an abnormal high potential and executes a shut-down and latch routine. It requires the restart of VDD to resume normal operation.

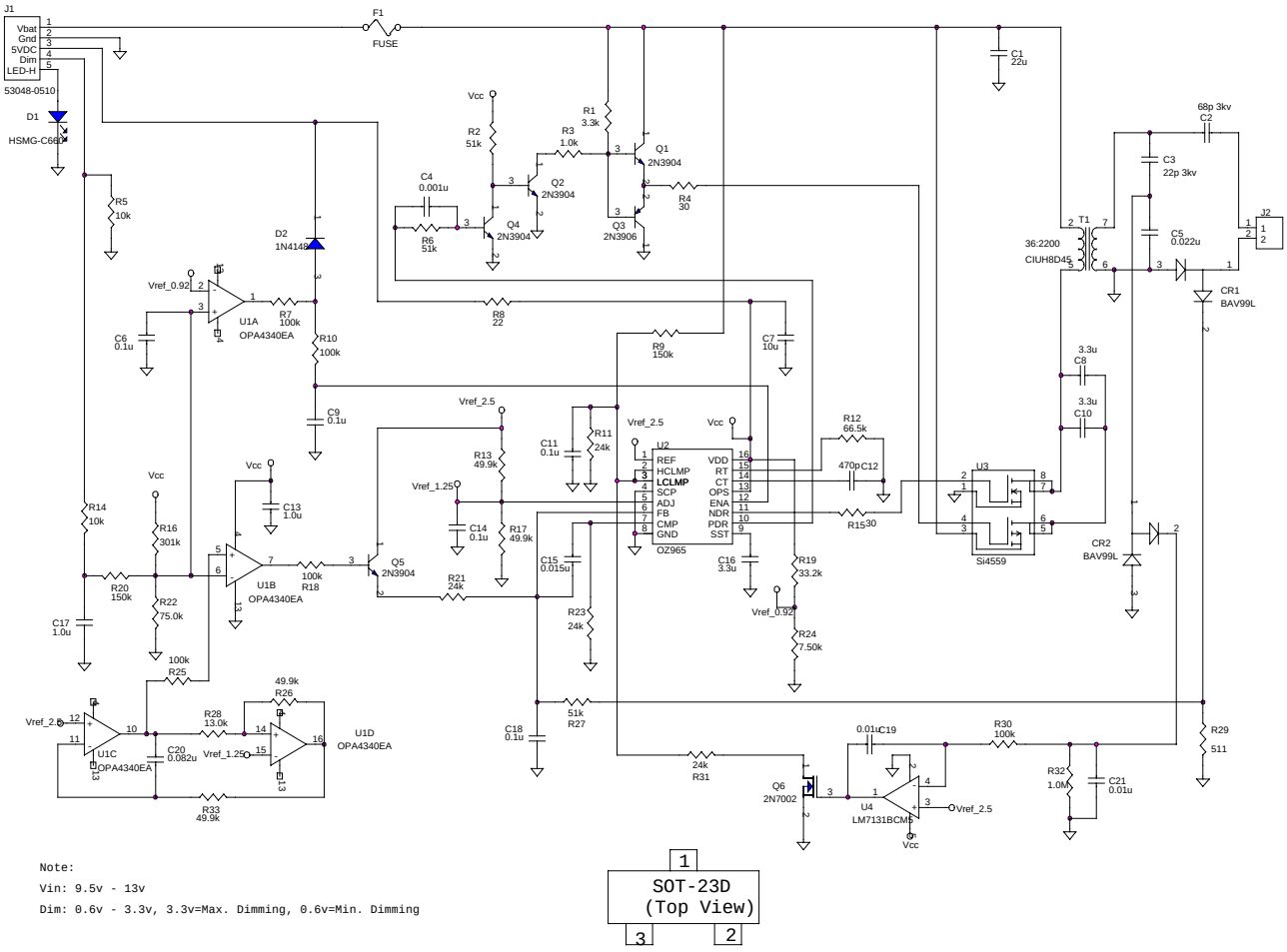
During the start-up stage, both the open-lamp and short-circuit protections are inhibited. In many designs, up to 1 second of soft-start time is required to guarantee sufficient output voltage to ignite the CCFL at low temperatures.

APPLICATION INFORMATION

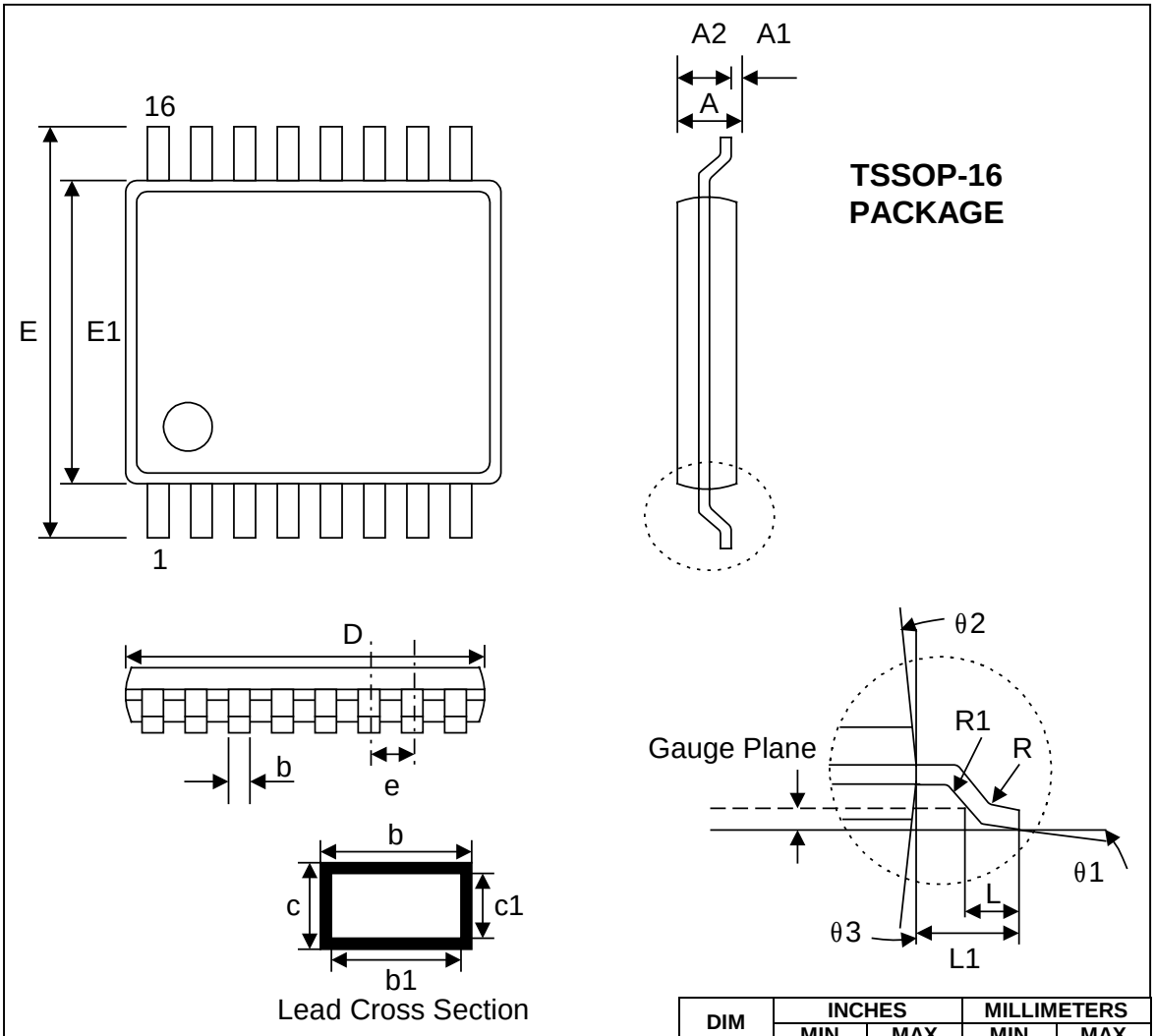
1. Typical Application Circuit with PWM Burst-mode Control



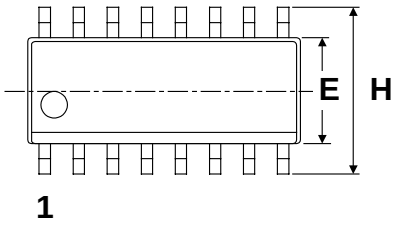
2. Application Circuit with PWM Burst-mode Dimming Control



PACKAGE INFORMATION



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	0.043	-	1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
L	0.020	0.030	0.45	0.75
D	-	-	4.90	5.10
E1	0.169	0.177	4.30	4.50
E	0.252BSC		6.40BSC	
R	0.004	-	0.09	-
R1	0.004	-	0.09	-
b	0.007	0.012	0.19	0.30
b1	0.007	0.010	0.19	0.25
c	0.004	0.008	0.09	0.20
c1	0.004	0.006	0.09	0.16
L1	0.039REF		1.0REF	
e	0.026BSC		0.65BSC	
θ1	0°	8°	0°	8°
θ2	12°REF		12°REF	
θ3	12°REF		12°REF	



SOP-16 PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.0075	0.0098	0.19	0.25
D	0.3859	0.3937	9.80	10.00
E	0.1497	0.1574	3.80	4.00
e	0.050 BCS.		1.27 BCS.	
H	0.2284	0.2440	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°