

深圳市宝安区华威显示厂

HUA WEI DISPLAY SYSTEM ELECTRONICS CO., LTD

Tel: +86-0755-29951125
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**SPECIFICATIONS
FOR
LCD MODULE**

Customer: _____

Model name: HW240320F-0R-0A

Description: LIQUID CRYSTAL DISPLAY MODULE

Date: 2009-08-03

CUSTOMER APPROVAL

Customer Approval	<input type="checkbox"/> Accept <input type="checkbox"/> Reject comment: Approved by: _____
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SUPPLIER APPROVAL

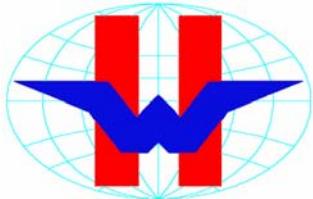
APPROVED	CHECKED	ORGANIZED
何俊光		李峰

1、OTHERS:

APPROVAL FOR SPECIFICATIONS ONLY

APPROVAL FOR SPECIFICATIONS AND SAMPLE

NOTE: VERSION OF SPECIFICATIONS: 00



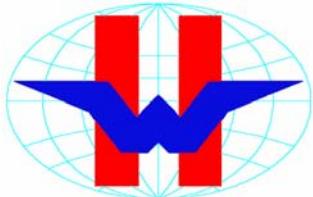
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2. OTHERS:

History of revision

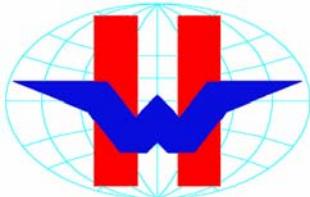


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1. Introduction And General Specifications

Liquid crystal Displays (LCDS) have widely used in many applications such as industrial measurements, office mechanisms, and household electronic–equipment etc. LCM (LCD Module) integrates with LCD and driving circuit that is easily to be interfaced by user. This LCM contains a standard built-in dot –matrix font set.

1.1 Applications of LCM

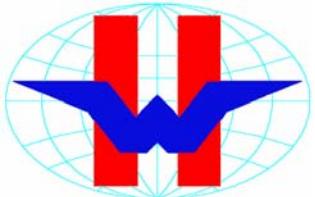
- Telephone
- Faxsimile mechanism
- Electronic Typewriter
- Word processor
- Electronic memo pads
- Remote controller

1.2 Features of LCM

- Compact, thin and light
- Wide view angle
- Low power consumption
- High contrast image
- Wide operating temperature
- High reliability

1.2 General specification

Parameter	Value	Unit
LCD Mode	TFT/ Transmissive	-
Color Depth	262K/65K	-
Display Resolution	240*RGB*320	pixels
Pixel Arrangement	RGB-stripe	-
Viewing Direction	12 o' clock	
Display Mode	Normally white	
LCD Controller/Driver	ILI9325	-
IC Package Type	COG	-
MPU Interface	Standard 8080 system 18 bit/16bit parallel	-
Power Supply Voltage	2.5~3.6	V
Back-light	White LED*4	pcs

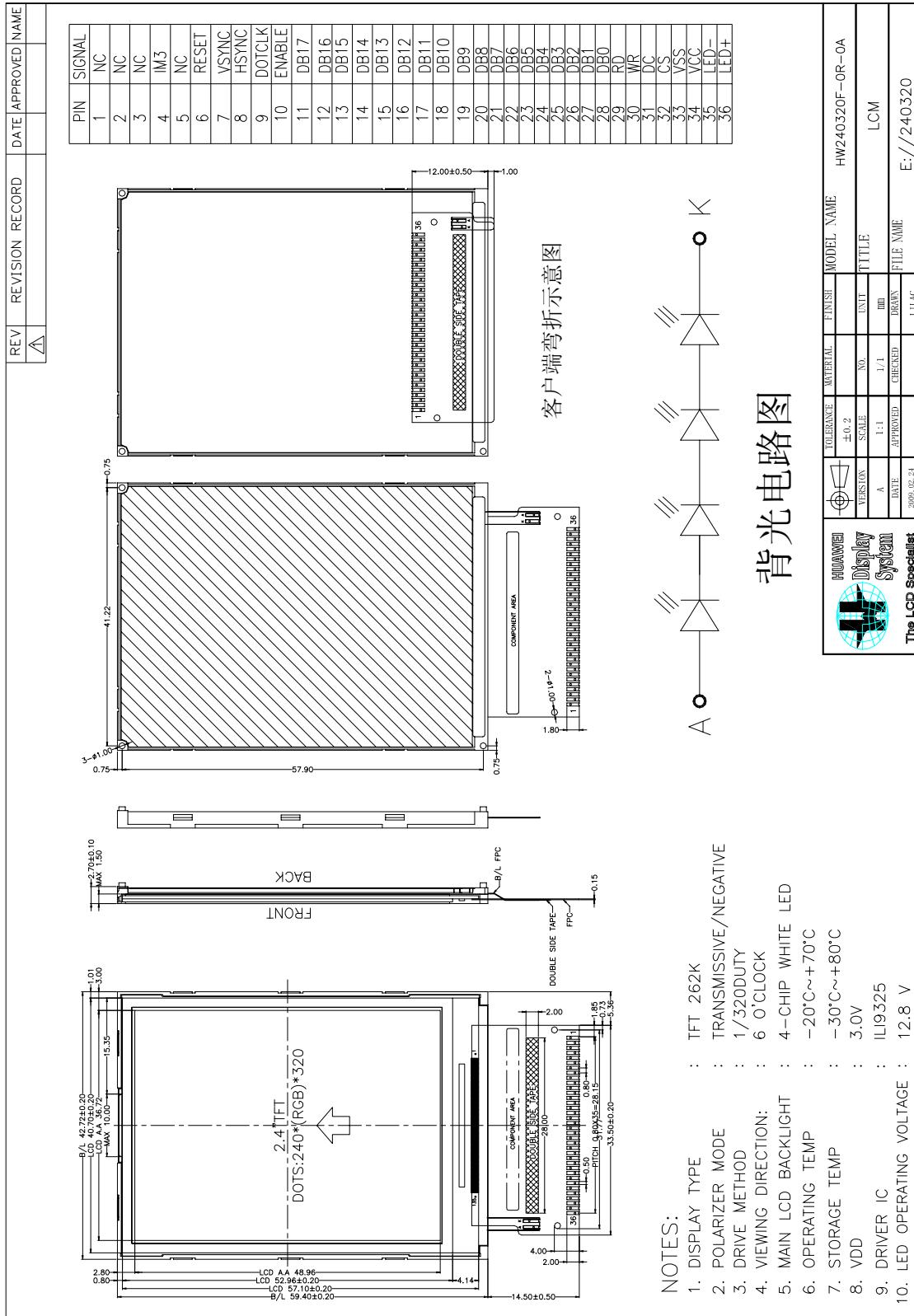


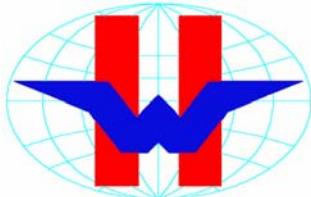
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2. LCD&LCM Outline Drawing





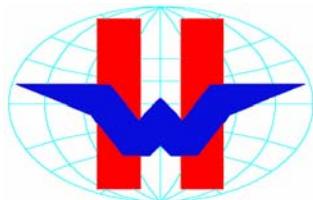
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3. Interface pin Connections Circuit Block Diagram

PIN NO.	SYMBOL	DESCRIPTION
1-3	NC	Not Connect
4	IM3	Select the MPU system interface mode. IM3=L, i80-system 16-bit interface, DB[17:10], DB[8:1]; IM3=H, i80-system 18-bit interface, DB[17:0].
5	NC	Not Connect
6	RESET	This is an active low signal.
7	VSYNC	In external interface mode , served as a vertical synchronize signal input;
8	HSYNC	In external interface mode, served as a horizontal synchronized signal input;
9	DOTCLK	In external interface mode, served as a dot clock signal;
10	ENABLE	Moreover, setting EPL bit can change the polarity of the ENABLE signal;
11-28	DB17-DB0	Data Bas Line
29	RD	Read/Write execution control When /RD is " L ", D0 to D7 are in an output status.
30	WR	Read/Write execution control R/W=" H ":" read R/W=" L ":" write
31	DC	"L":COMMAND DATA , "H":DISPLAY DATA
32	CS	Chip select
33	VSS	Ground
34	VCC	Internal logic power: VCC=2.5V~3.3V,
35	LED-	LED Ground
36	LED+	LED Power

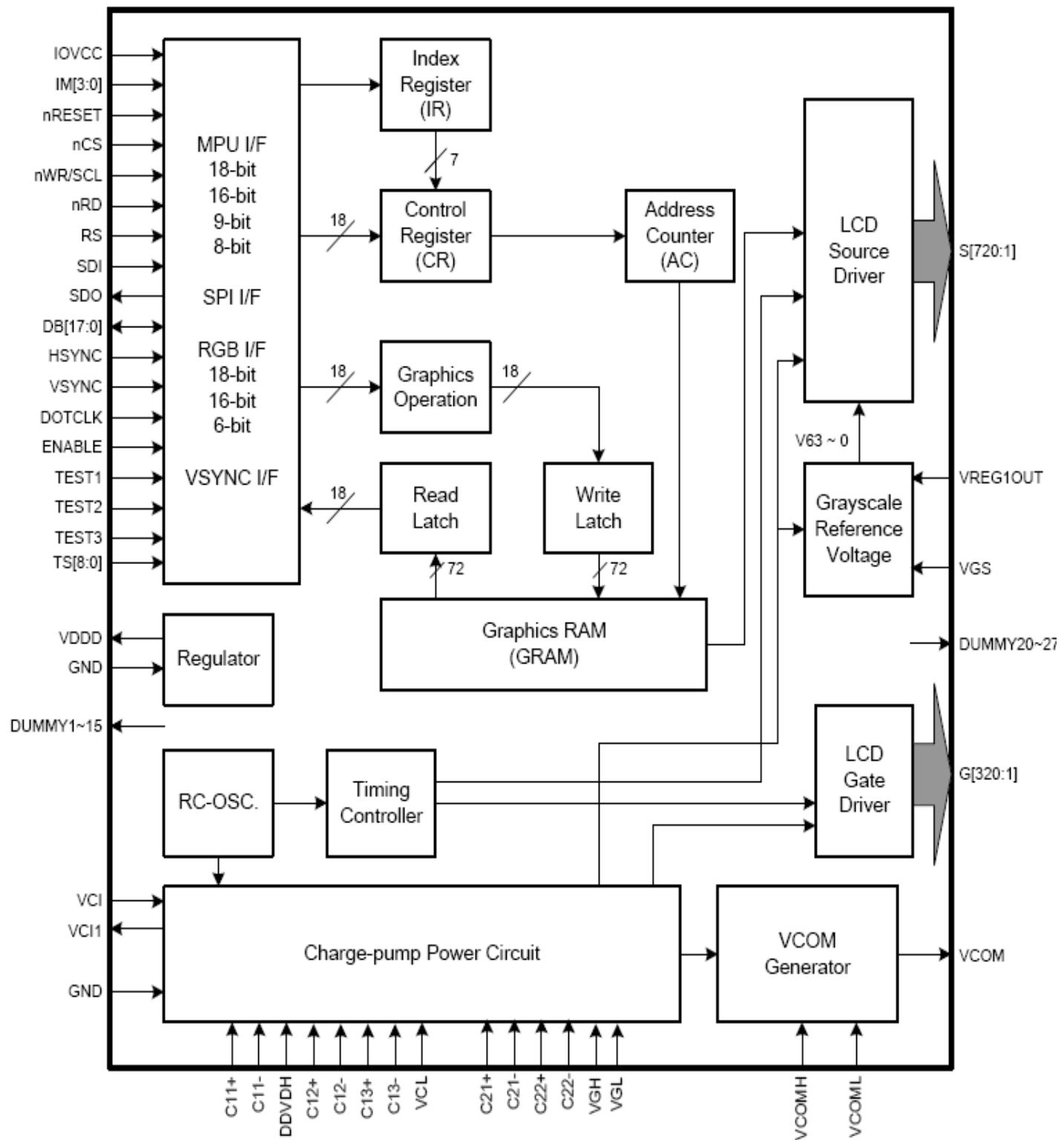


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4. Block diagram





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5. Block description

MPU System Interface

ILI9325 supports three system high-speed interfaces: i80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

ILI9325 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9325 read the first data from the internal GRAM. Valid data are read out after the ILI9325 performs the second read operation.

Registers are written consecutively as the register execution time except starting oscillator takes 0 clock cycle.

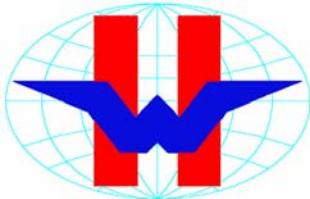
Registers selection by system interface (8-/9-/16-/18-bit bus width)			I80
Function	RS	nWR	nRD
Write an index to IR register	0	0	1
Read an internal status	0	1	0
Write to control registers or the internal GRAM by WDR register.	1	0	1
Read from the internal GRAM by RDR register.	1	1	0

Registers selection by the SPI system interface		
Function	R/W	RS
Write an index to IR register	0	0
Read an internal status	1	0
Write to control registers or the internal GRAM by WDR register.	0	1
Read from the internal GRAM by RDR register.	1	1

Parallel RGB Interface

ILI9325 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the "External Display Interface" section. The ILI9325 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.



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6. System interface

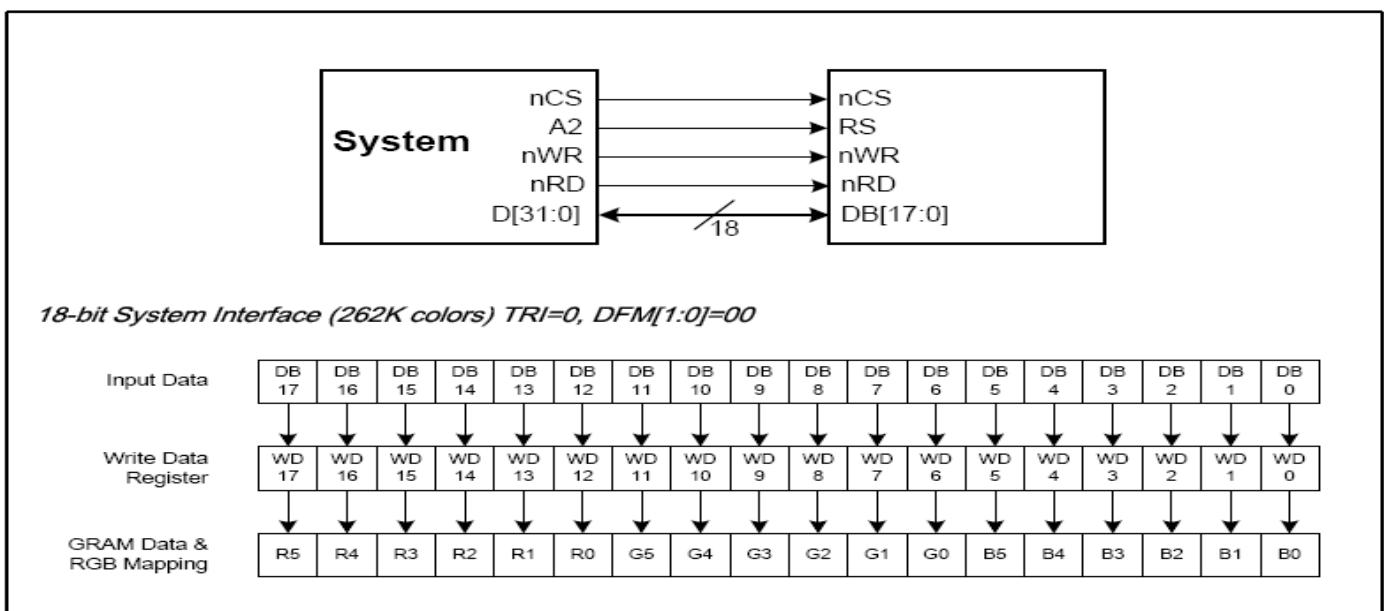
6.1 i80/16-bit system interface

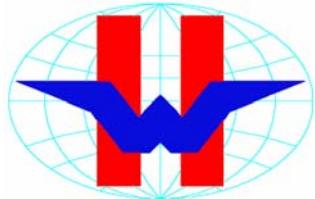
The i80/16-bit system interface is selected by setting the IM[3:0] as "0010" levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1st transfer: 2 bits, 2nd transfer: 16 bits or 1st transfer: 16 bits, 2nd transfer: 2 bits) are necessary for the 16-bit CPU interface.

		16-bit MPU System Interface Data Format																																																																														
TRI	DFM	system 16-bit interface (1 transfers/pixel) 65,536 colors																																																																														
0	*	1st Transfer																																																																														
		<table border="1"> <tr> <td>DB 17</td><td>DB 16</td><td>DB 15</td><td>DB 14</td><td>DB 13</td><td>DB 12</td><td>DB 11</td><td>DB 10</td><td>DB 8</td><td>DB 7</td><td>DB 6</td><td>DB 5</td><td>DB 4</td><td>DB 3</td><td>DB 2</td><td>DB 1</td><td>DB 0</td><td></td><td></td></tr> <tr> <td>R5</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td></td></tr> </table>																		DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0			R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0																								
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R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0																																																															
1	0	80-system 16-bit interface (2 transfers/pixel) 262,144 colors																																																																														
		<table border="1"> <tr> <td>DB 17</td><td>DB 16</td><td>DB 15</td><td>DB 14</td><td>DB 13</td><td>DB 12</td><td>DB 11</td><td>DB 10</td><td>DB 8</td><td>DB 7</td><td>DB 6</td><td>DB 5</td><td>DB 4</td><td>DB 3</td><td>DB 2</td><td>DB 1</td><td>DB 17</td><td>DB 16</td><td></td></tr> <tr> <td>R5</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td></td></tr> </table>																		DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 17	DB 16		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0																								
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		<table border="1"> <tr> <th>1st Transfer</th><th>DB 2</th><th>DB 1</th><th>DB 17</th><th>DB 16</th><th>DB 15</th><th>DB 14</th><th>DB 13</th><th>DB 12</th><th>DB 11</th><th>DB 10</th><th>DB 8</th><th>DB 7</th><th>DB 6</th><th>DB 5</th><th>DB 4</th><th>DB 3</th><th>DB 2</th><th>DB 1</th><th></th></tr> <tr> <td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr> <td></td><td></td><td></td><td>R5</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td></tr> </table>																			1st Transfer	DB 2	DB 1	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1																									R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1
1st Transfer	DB 2	DB 1	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1																																																														
			R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1																																																													

6.2 i80/18-bit system interface

The i80/18-bit system interface is selected by setting the IM[3:0] as "1010" levels.





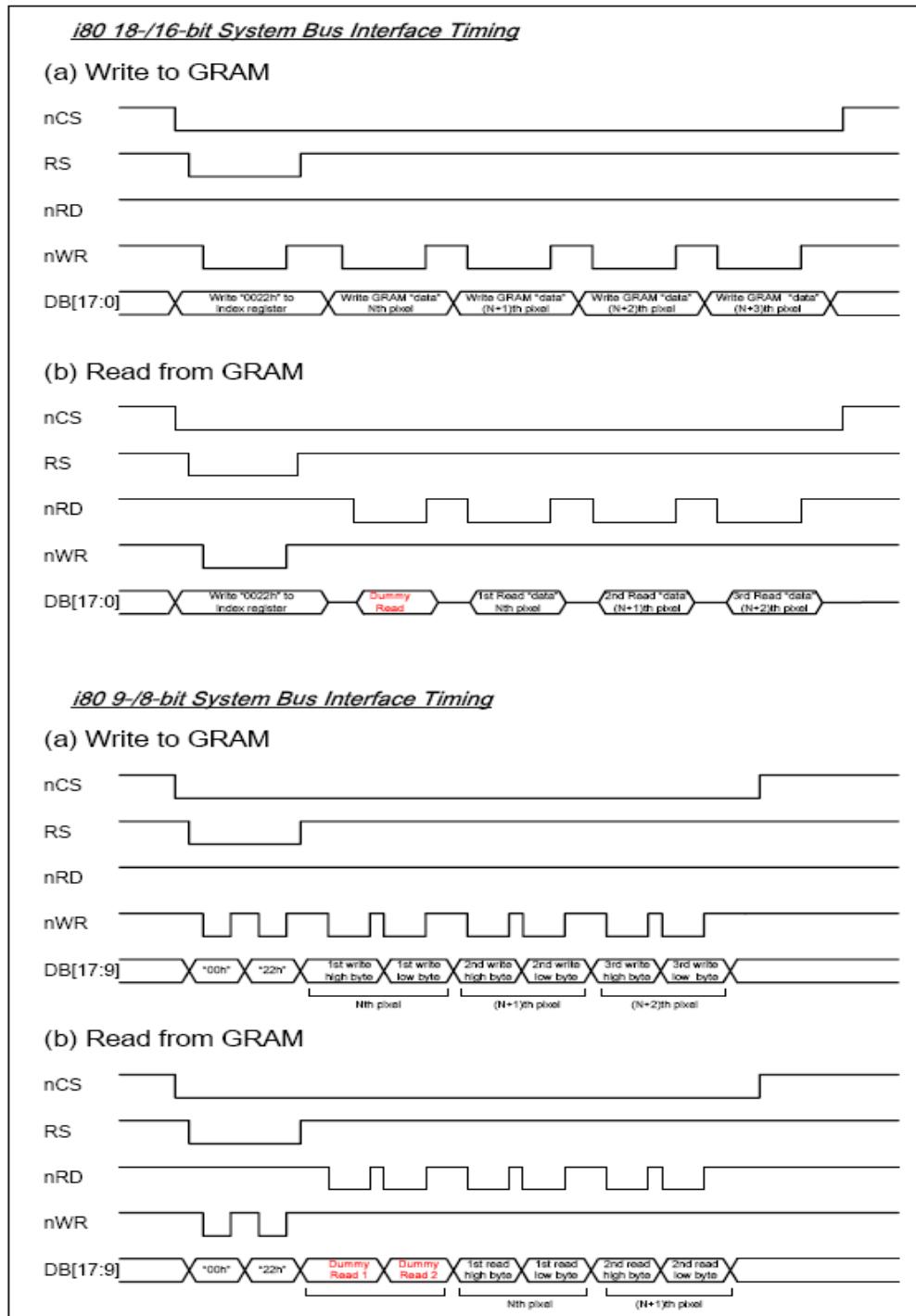
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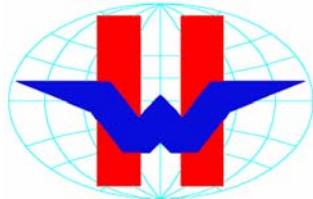
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7. Gram address map & read / write

ILI9325 has an internal graphics RAM (GRAM) of 87,120 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80 system, SPI and RGB interfaces.





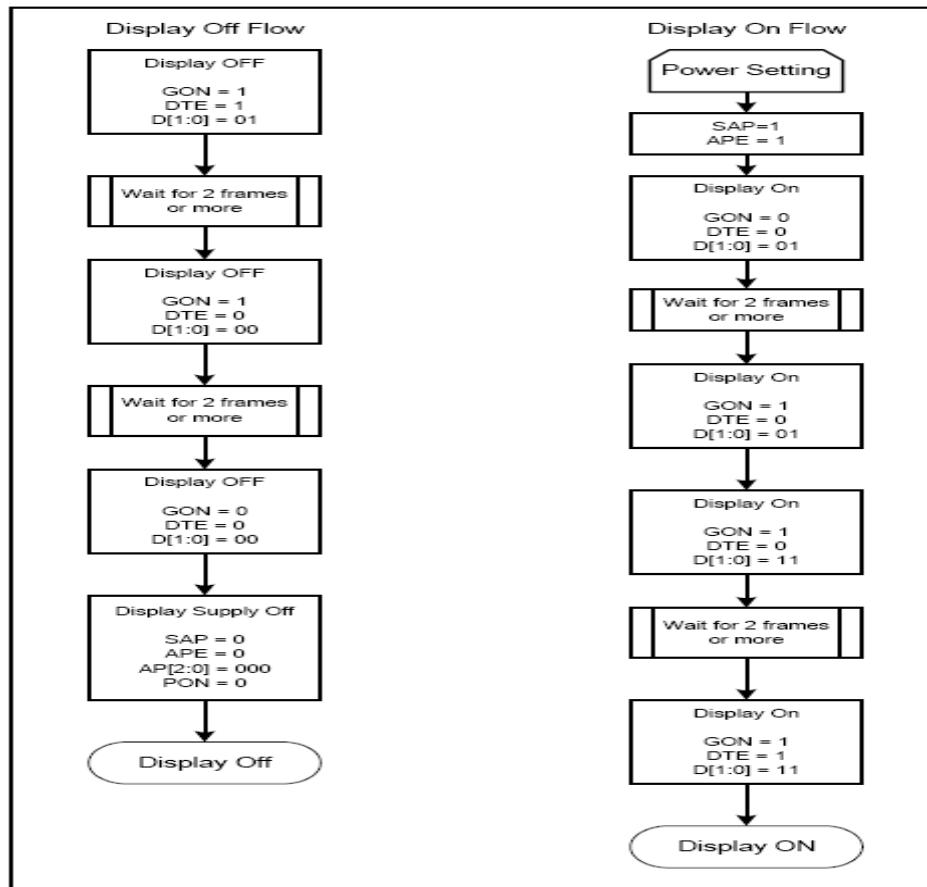
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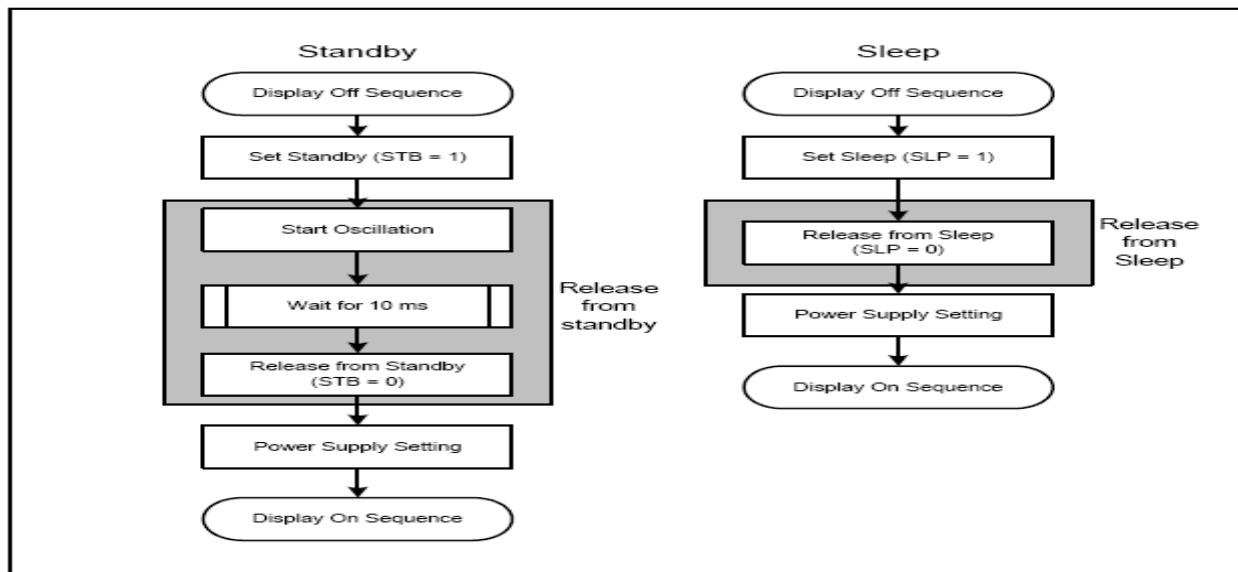
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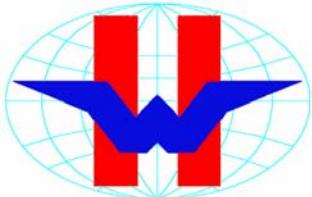
8. Application

8.1 Display ON/OFF sequence



8.2 Standby and sleep





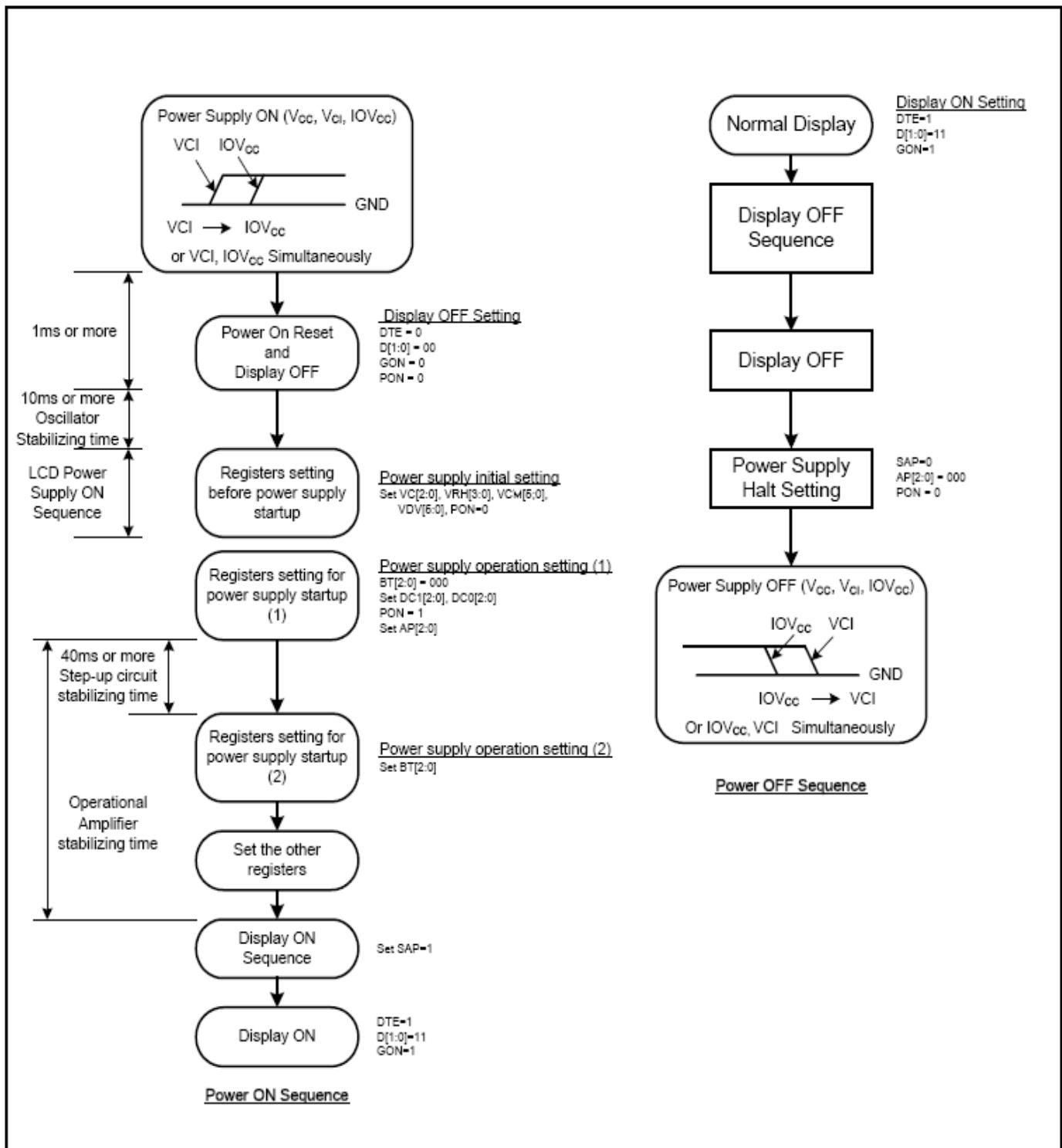
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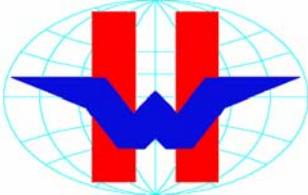
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8.3 Power supply configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.





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9. Initial code

```

// VCI=2.8V
{
    //***** Reset LCD Driver *****/
    LCD_nRESET = 1;
    delayms(1); // Delay 1ms
    LCD_nRESET = 0;
    delayms(10); // Delay 10ms           // This delay time is necessary
    LCD_nRESET = 1;
    delayms(50); // Delay 50 ms

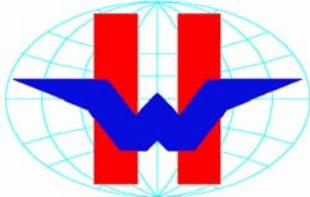
    //***** Start Initial Sequence *****/
    LCD_CtrlWrite_ILI9325(0x00E3, 0x3008); // Set internal timing
    LCD_CtrlWrite_ILI9325(0x00E7, 0x0012); // Set internal timing
    LCD_CtrlWrite_ILI9325(0x00EF, 0x1231); // Set internal timing
    LCD_CtrlWrite_ILI9325(0x0001, 0x0100); // set SS and SM bit
    LCD_CtrlWrite_ILI9325(0x0002, 0x0700); // set 1 line inversion
    LCD_CtrlWrite_ILI9325(0x0003, 0x1030); // set GRAM write direction and BGR=1.
    LCD_CtrlWrite_ILI9325(0x0004, 0x0000); // Resize register
    LCD_CtrlWrite_ILI9325(0x0008, 0x0207); // set the back porch and front porch
    LCD_CtrlWrite_ILI9325(0x0009, 0x0000); // set non-display area refresh cycle ISC[3:0]
    LCD_CtrlWrite_ILI9325(0x000A, 0x0000); // FMARK function
    LCD_CtrlWrite_ILI9325(0x000C, 0x0000); // RGB interface setting
    LCD_CtrlWrite_ILI9325(0x000D, 0x0000); // Frame marker Position
    LCD_CtrlWrite_ILI9325(0x000F, 0x0000); // RGB interface polarity

    //*****Power On sequence *****/
    LCD_CtrlWrite_ILI9325(0x0010, 0x0000); // SAP, BT[3:0], AP, DSTB, SLP, STB
    LCD_CtrlWrite_ILI9325(0x0011, 0x0007); // DC1[2:0], DC0[2:0], VC[2:0]
    LCD_CtrlWrite_ILI9325(0x0012, 0x0000); // VREG1OUT voltage
    LCD_CtrlWrite_ILI9325(0x0013, 0x0000); // VDV[4:0] for VCOM amplitude
    delayms(200); // Dis-charge capacitor power voltage
    LCD_CtrlWrite_ILI9325(0x0010, 0x1290); // SAP, BT[3:0], AP, DSTB, SLP, STB
    LCD_CtrlWrite_ILI9325(0x0011, 0x0227); // DC1[2:0], DC0[2:0], VC[2:0]
    delayms(50); // Delay 50ms
    LCD_CtrlWrite_ILI9325(0x0012, 0x001B); // Internal reference voltage= Vci;
    delayms(50); // Delay 50ms
    LCD_CtrlWrite_ILI9325(0x0013, 0x1700); // Set VDV[4:0] for VCOM amplitude
    LCD_CtrlWrite_ILI9325(0x0029, 0x001E); // Set VCM[5:0] for VCOMH
    LCD_CtrlWrite_ILI9325(0x002B, 0x000D); // Set Frame Rate
    delayms(50); // Delay 50ms
    LCD_CtrlWrite_ILI9325(0x0020, 0x0000); // GRAM horizontal Address
    LCD_CtrlWrite_ILI9325(0x0021, 0x0000); // GRAM Vertical Address

    // ----- Adjust the Gamma Curve -----//
    LCD_CtrlWrite_ILI9325(0x0030, 0x0004);
    LCD_CtrlWrite_ILI9325(0x0031, 0x0007);
    LCD_CtrlWrite_ILI9325(0x0032, 0x0006);
    LCD_CtrlWrite_ILI9325(0x0035, 0x0206);
    LCD_CtrlWrite_ILI9325(0x0036, 0x0408);
    LCD_CtrlWrite_ILI9325(0x0037, 0x0507);
    LCD_CtrlWrite_ILI9325(0x0038, 0x0200);
    LCD_CtrlWrite_ILI9325(0x0039, 0x0707);
    LCD_CtrlWrite_ILI9325(0x003C, 0x0504);
    LCD_CtrlWrite_ILI9325(0x003D, 0x0F02);

    //----- Set GRAM area -----//
    LCD_CtrlWrite_ILI9325(0x0050, 0x0000); // Horizontal GRAM Start Address
    LCD_CtrlWrite_ILI9325(0x0051, 0x00EF); // Horizontal GRAM End Address
    LCD_CtrlWrite_ILI9325(0x0052, 0x0000); // Vertical GRAM Start Address
    LCD_CtrlWrite_ILI9325(0x0053, 0x013F); // Vertical GRAM Start Address
    LCD_CtrlWrite_ILI9325(0x0060, 0xA700); // Gate Scan Line
}

```



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```

LCD_CtrlWrite_ILI9325(0x0061, 0x0001);           // NDL,VLE, REV
LCD_CtrlWrite_ILI9325(0x006A, 0x0000);           // set scrolling line
//----- Partial Display Control -----
LCD_CtrlWrite_ILI9325(0x0080, 0x0000);
LCD_CtrlWrite_ILI9325(0x0081, 0x0000);
LCD_CtrlWrite_ILI9325(0x0082, 0x0000);
LCD_CtrlWrite_ILI9325(0x0083, 0x0000);
LCD_CtrlWrite_ILI9325(0x0084, 0x0000);
LCD_CtrlWrite_ILI9325(0x0085, 0x0000);
//----- Panel Control -----
LCD_CtrlWrite_ILI9325(0x0090, 0x0010);
LCD_CtrlWrite_ILI9325(0x0092, 0x0600);
LCD_CtrlWrite_ILI9325(0x0093, 0x00003);
LCD_CtrlWrite_ILI9325(0x0095, 0x0110);
LCD_CtrlWrite_ILI9325(0x0097, 0x0000);
LCD_CtrlWrite_ILI9325(0x0098, 0x0000);

LCD_CtrlWrite_ILI9325(0x0007, 0x0133);           // 262K color and display ON
}

void LCD_ExitSleep_ILI9325(void)
{
//*****Power On sequence *****/
LCD_CtrlWrite_ILI9325(0x0010, 0x0000);           // SAP, BT[3:0], AP, DSTB, SLP
LCD_CtrlWrite_ILI9325(0x0011, 0x0000);           // DC1[2:0], DC0[2:0], VC[2:0]
LCD_CtrlWrite_ILI9325(0x0012, 0x0000);           // VREG1OUT voltage
LCD_CtrlWrite_ILI9325(0x0013, 0x0000);           // VDV[4:0] for VCOM amplitude
    delayms(200);
LCD_CtrlWrite_ILI9325(0x0010, 0x1290);           // Dis-charge capacitor power voltage
LCD_CtrlWrite_ILI9325(0x0011, 0x0227);           // SAP, BT[3:0], AP, DSTB, SLP, STB
                                                // DC1[2:0], DC0[2:0], VC[2:0]
    delayms(50);
LCD_CtrlWrite_ILI9325(0x0012, 0x001B);           // Internal reference voltage =Vci;
                                                // Delay 50ms
    delayms(50);
LCD_CtrlWrite_ILI9325(0x0013, 0x1700);           // VDV[4:0] for VCOM amplitude
LCD_CtrlWrite_ILI9325(0x0029, 0x001E);           // VCM[5:0] for VCOMH
    delayms(50);
LCD_CtrlWrite_ILI9325(0x0007, 0x0133);           // Delay 50ms
                                                // 262K color and display ON
}

void LCD_EnterSleep_ILI9325(void)
{
LCD_CtrlWrite_ILI9325(0x0007, 0x0131);           // Set D1=0, D0=1
    delayms(10);
LCD_CtrlWrite_ILI9325(0x0007, 0x0130);           // Set D1=0, D0=0
    delayms(10);
LCD_CtrlWrite_ILI9325(0x0007, 0x0000);           // display OFF
//***** Power OFF sequence *****/
LCD_CtrlWrite_ILI9325(0x0010, 0x0000);           // SAP, BT[3:0], APE, AP, DSTB, SLP
LCD_CtrlWrite_ILI9325(0x0011, 0x0000);           // DC1[2:0], DC0[2:0], VC[2:0]
LCD_CtrlWrite_ILI9325(0x0012, 0x0000);           // VREG1OUT voltage
LCD_CtrlWrite_ILI9325(0x0013, 0x0000);           // VDV[4:0] for VCOM amplitude
    delayms(200);
LCD_CtrlWrite_ILI9325(0x0010, 0x0002);           // Dis-charge capacitor power voltage
                                                // SAP, BT[3:0], APE, AP, DSTB, SLP
}

```

10. Notice packing method

Pack the products so that they may not touch each other.

Put the inner cartons containing module into outer carton.

Attach the display label on the visible location on the outer carton.