528-Channel Source Driver with Internal RAM for 262,144-Color Displays

IS2100

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28. Revision History
28.1. Complete Revision from Ver.0.72 to Ver.1.0
28.2. Revised from Ver.1.0 to Ver.1.1
28.3. Revised from Ver.1.1 to Ver.1.52
28.4. Revised from Ver.1.52 to Ver.1.6
28.5. Revised from Ver.1.6 to Ver.1.61

Note: 0/1 are used for setting the registers and L/H are used for setting the pins.

IS2100

528-Channel Source Driver with an Internal RAM for 262,144-Color Displays

1. Outline

The IS2100 LSI supports 262,144-color displays and has a RAM and a controller for 176RGB x 240-dot displays maximum. In combination with the IS2200 gate driver with an internal power supply, the IS2200 can display 176RGB x 240-dot displays.
Best suited for cellular phones that support animated displays.

2. Features

- **Low power design (Power consumption is approx. 2mW in combination with the IS2200 when there is no load to the IS2100/IS2200.)**
- **Super slim chip design—0.96mm x 19.47mm**
- **262,144-color displays**
- 760,320 bits of internal display RAM
- 528-channel LCD drive circuit
- RGB interface circuit for animated displays
- Singular power supply combined with the IS2200 (2.5V - 3.1V)
- 176RGB x 240-dot displays max.
- 18/16/8 bit parallel bus interface and 9/8-bit serial interface
- Incorporates an 8-color display mode
- Window access mode of the internal Display Data RAM
- Gamma correction function
- Internal interface for the IS2200, a gate driver with an on-chip power supply unit

  (Note) Substrate of IS2100 is VSS (GND potential). Remind that substrate of the IS2200 is VSS3 (negative potential).

3. Pin Description

3.1 Power Supply Pins

Bump No.	Symbol	Name	I/O	Description
94 - 101	VCC11	I/O Power Supply	---	I/O Power Supply.
129 - 136	V18	Logic Power Supply	---	2.0V Power Supply for logic. Connect to the V18 pin of the IS2200. Connect the 1uF/10V-capacitor between VSS and this terminal
124 - 128	VDHR	Grayscale power supply for the source driver	---	Grayscale power supply for the source driver
116 - 123	VS	Power supply for the source driver	---	Power supply for the source driver
102 - 115	VSS	Ground pin	---	Ground pin

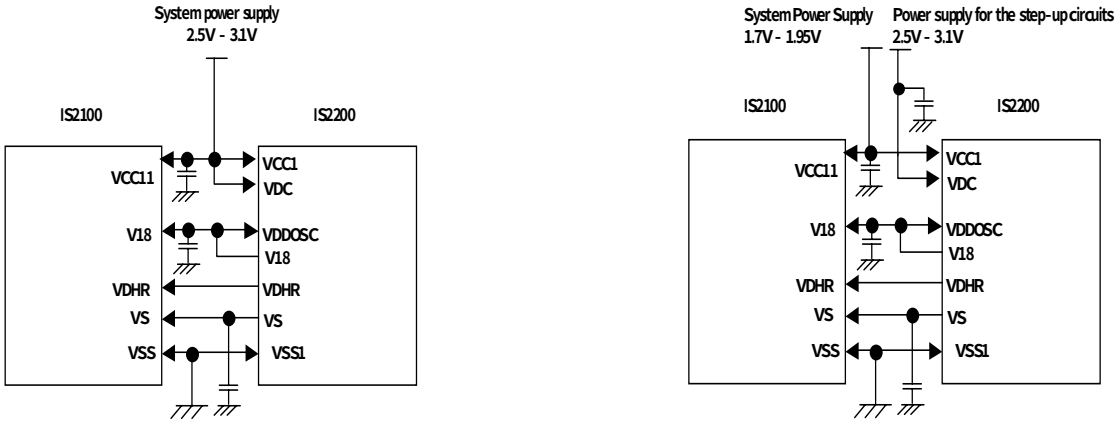


Figure 3-1 Power supply

3.2. Logic I/O Pins

Bump No.	Symbol	Name	I/O	Description
32	BWS2	Bit length selection for the RGB interface circuit.	I	L: 18 bit H: 16 bit (Invalid when the system interface circuit is used.)
30	BWS1	Bit length selection for the system interface circuit.	I	L: 18-bit Parallel; H: 16-bit Parallel; L: 9-bit Serial; H: 8-bit Parallel/ Serial; Invalid when the RGBI/F circuit is in use
28	BWS0		I	L: 18-bit Parallel; L: 16-bit Parallel; H: 9-bit Serial; H: 8-bit Parallel/ Serial; Invalid when the RGBI/F circuit is in use
20	PSX	System interface mode selection	I	L: Parallel interface (only i80/M68 interface) H: Serial interface only
59	/CS	Chip selection	I	Chip selection pin. The L level enables inputting commands and reading/writing data.
60	/RESET	Reset	I	Switching to L initializes internally. Must reset after power is supplied.
63	/RD(E)	Read (Enable)	I	When the i80 series parallel transferred data (/RD) is selected, reading is valid by this signal. L: The data is outputted to the data pins (D17-D0) When the M68 series parallel transferred data (E) is selected, writing/reading is valid. L: Read/Write allowed. H: Read/Write prohibited.
62	/WR (R/W)	Write (Write / Read)	I	When the i80 series parallel transferred data (/WR) is selected, writing is valid by this signal. L: The data are written. When the M68 series parallel transferred data (R/W) and the serially transferred data are selected, writing/reading is valid by this pin. L: Write H: Read
22	C86	Interface selection	I	L: i80 series H: M68 series. Connect to VCC11 or VSS when the serial interface is selected.
39 - 56	D17-D0	Data pins	I/O	18-bit bidirectional pins. When the chip is not selected, D17-D0 become high-impedance. Connect to VSS when the serial interface is selected.
67	SI	Serial input	I	Input pin for the serial interface. Connect to VCC11 when the parallel interface is selected.
69	SO	Serial output	O	Output pin for the serial interface. Set as open when the parallel interface is selected.
68	SCL	Serial clock	O	Serial clock input for the serial interface. Connect to VCC11 when the parallel interface is selected.
36	IF_SHARE	Selection pin for sharing data/RGB interface circuits.	I	H: Use the data pins (D17 - D0) both for the system interface circuit and for the RGB interface circuit. L: Use the data pins (D17 - D0) only for the system interface circuit.
64	RGB./CPU	Switching pin for the data pins.	I	When IF_SHARE is H, the data pins are; L: Used for the system interface circuit. H: Used for the RGB interface circuit.
61	RS	Data / Command selection	I	Selects data or command at data transferring. L: Command H: Display data Set this as H when no data transfer is done.
24	DTX1	Data length selection.	I	Selects bit length of the input display data in 16/8-bit parallel data transfer. L: 1 pixel/16bits H: 1 pixel/18bits (See Fig.6-2)

Bump No.	Symbol	Name	I/O	Description
26	DTX2	16/8 bit parallel data transfer method.	I	Selects a data transfer method in the 16/8-bit parallel interface. (For more details, see Fig.6-2 System interface circuit set-up.)
12	SCLEG0	SCL data signal edge selection.	I	Sets an active edge of the serial clock for the input/output data in the serial interface. (See Table 6-5 Relation between the serial clock and the serial data.)
10	SCLEG1	SCL polarity selection.	I	Selects an active level of the serial clock in the serial interface. L: Low level (Starts in Hi level) H: Hi level (Starts in Low level) (See Table 6-5 Relation between the serial clock and the serial data)
74	Hsync	Horizontal synchronization signal.	I	Horizontal synchronization signal for the RGB interface circuit. Connect to VCC11 or VSS when not in use.
73	Vsync	Vertical synchronization signal.	I	Vertical synchronization signal for the RGB interface circuit. Connect to VCC11 or VSS when not in use.
75	Dotclk	Dot clock.	I	Dot clock for the RGB interface circuit Connect to VCC11 or VSS when not is use.
14	HSEG	Hsync polarity selection.	I	Selects an active level of the horizontal synchronization signal for the RGB interface circuit. L: Low-active H: High-active
16	VSEG	Vsync polarity selection.	I	Selects an active level of the vertical synchronization signal for the RGB interface circuit. L: Low-active H: High-active
18	DCKEG	Dotclk polarity selection.	I	Selects an active level of the Dotclk signal for the RGB interface circuit. L: Low-active H: High-active
93 - 88	RGB25 - RGB20	RGB data pins.	I	Data input pins of the RGB interface circuit. Connect to VCC11 or VSS when not is use.
87 - 82	RGB15 - RGB10			
81 - 76	RGB05 - RGB00			
34	DDS	Selection of the dummy raster-row position.	I	Selects a position of the dummy raster-row. L: The end of the frame H: The top of the frame
38	CSTB	Frame synchronization signal.	O	The same signal provided as GFRM. Usually this signal should not be connected.
174	SYSCLK	System clock.	I	Connects to SYSCLK of the IS2200 to receive approx. 600kHz clock from the IS2200.

3.3. IS2200 Control Pins

Bump No.	Symbol	Name	I/O	Description
176	GCS	Chip selection for communicating with the gate driver	O	Chip selection for communicating with the IS2200. Connect to the GCS pin of the IS2200.
177	GDA	Serial data for communicating with the gate driver	O	Serial data for communicating with the IS2200. Connect to the GDA pin of the IS2200.
178	GOE1	OE1 output for the gate driver	O	L: Fixes the gate output to off level during scanning. Connect to the OE1pin of the IS2200.
179	GOE2	OE2 output for the gate driver	O	L: Turns on all the date raster-rows. Connect to the OE2 pin of the IS2200.
181	GFRM	Frame synchronization signal	O	Frame synchronization signal. Connect to the FRM pin of the IS2200.
180	GCLK	CLK output for the gate driver	O	Shift clock for the gate driver. Connect to the CLK pin of the IS2200.
173	VCOUT2	Rectangular signal output	O	Alternative drive pulse. Connect to the VCIN pin of the IS2200.
175	/GRESET	IS2200 reset pin	O	Connect to the /GRESET pin of the IS2200. Executes a software reset by setting as R34:D0=GRES in order to reset the IS2200.
172	STB	IS2200 oscillation control	O	Controls the oscillation of the IS2200. Connect to the STB pin of the IS2200. L: Normal operations H: Stops oscillation of the IS2200

3.4. Sub-LCD Control Pins

Bump No.	Symbol	Name	I/O	Description
70	/BLCS_I	Selection pin for the sub-LCD panel function	I	Pin for selecting the sub-LCD panel function. L: When this function is in use H: When this function is not in use
3	/BLCS_O	Chip selection for the sub-LCD panel	O	Chip selection signal for the sub-LCD panel controller. Set as open when not in use.
4	BLSCL	Serial clock for the sub-LCD panel	O	Serial clock signal for the sub-LCD panel controller. Set as open when not in use.
5	BLSDA	Serial data for the sub-LCD panel	O	Serial data signal for the sub-LCD panel controller. Set as open when not in use.

(Note: Refer to 6.7)

Drivers

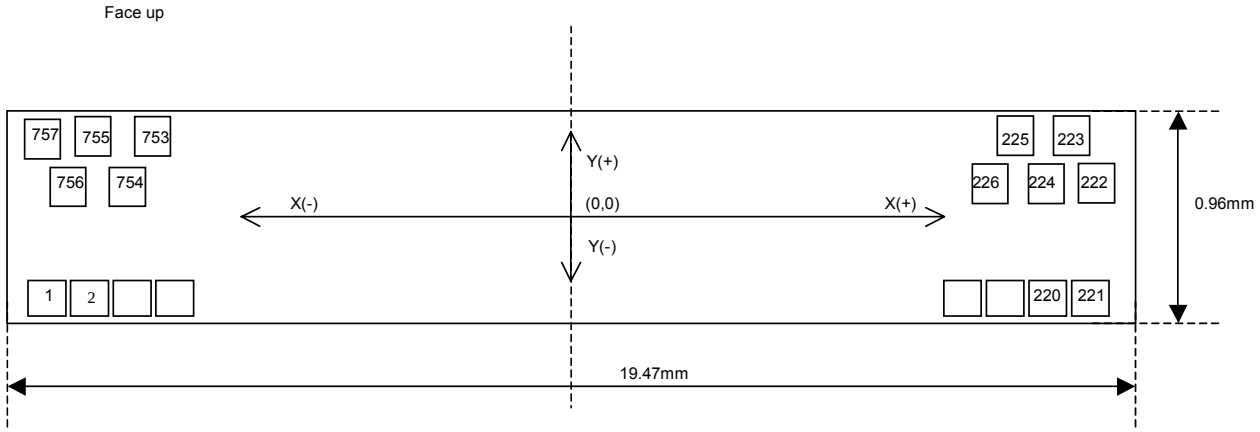
Bump No.	Symbol	Name	I/O	Description
753 - 226	Y1 - Y528	Source output	O	Source output pins.

3.5. Test Pins and Others

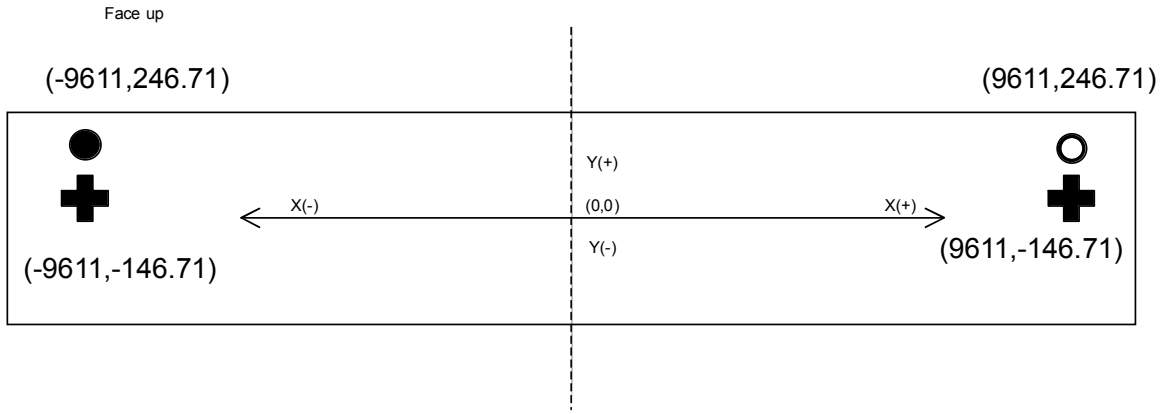
Bump No.	Symbol	Name	I/O	Description
171 170 6 7	TEST3 TEST2 TEST1 TEST0	Test pin	I	Pins for test. Connect to the ground.
1, 137 - 168, 182 - 219, 221,222, 224,755, 757	DUMMY	Dummy pin	---	Dummy pins These are not connected any internal circuits.
2,754, 756	VC1_L	Through pin		Through pin. (For internal wiring, see “4.5. VC1_L and VC1_R Pins”)
220,223, 225	VC1_R	Through pin		Through pin. (For internal wiring, see “4.5. VC1_L and VC1_R Pins”)
9,11,15,19, 23,27,31,35 ,58,66,72	VCC11 (MODE)	Pull-up pin for setting the mode.	---	Pull-up pins for setting the mode.
13,17,21,25 ,29,33,37, 57,65,71 169	VSS (MODE)	Pull-down pin for setting the mode.	---	Pull-down pins for setting the mode.

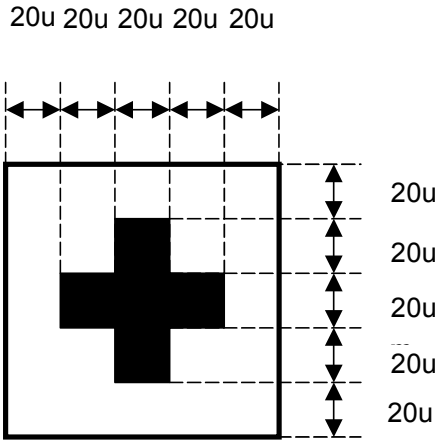
4. Bump Layout

4.1. General



4.2. Alignment Mark

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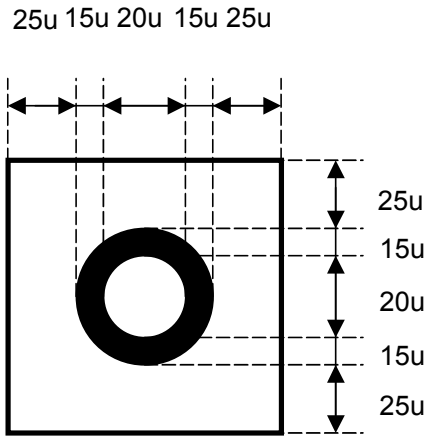
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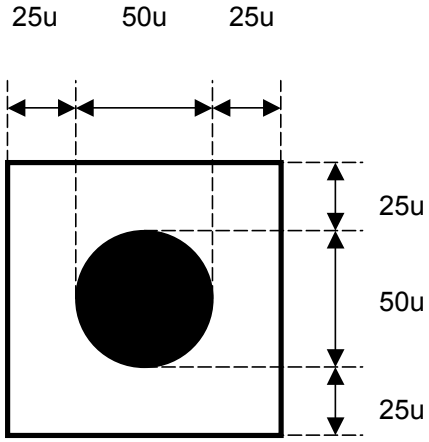
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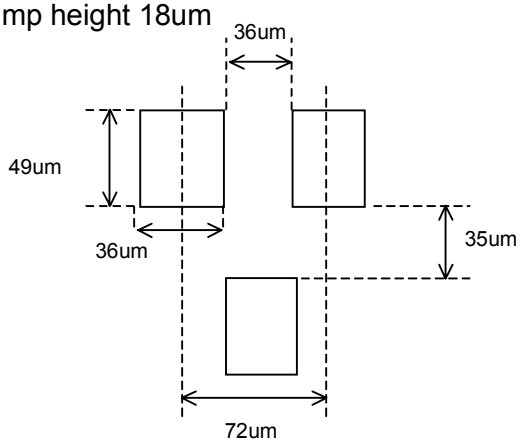
4.3. Bump Specification

4.3.1. Source output side

Bump type A

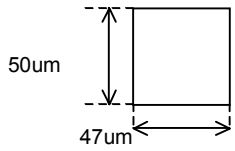
Bump height 18um



4.3.2. IO side

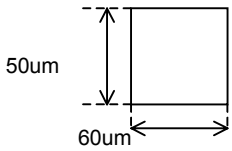
Bump type B

Bump height 18um



Bump type C

Bump height 18um



The height of bump is defined in the Delivery Specification.

4.4. Bump Coordinates

BumpNo.	Name	X (µm)	Y (µm)	Bumptype
1	DUMMY	-9606.92	-400.00	B
2	VC1	-9526.92	-400.00	B
3	/BLCS_O	-9446.92	-400.00	B
4	BLSCL	-9346.92	-400.00	B
5	BLSDA	-9246.92	-400.00	B
6	TEST1	-9146.92	-400.00	B
7	TEST0	-9046.92	-400.00	B
8	VSS(MODE)	-8948.44	-400.00	B
9	VCC11(MODE)	-8868.44	-400.00	B
10	SCLEG1	-8770.77	-400.00	B
11	VCC11(MODE)	-8690.44	-400.00	B
12	SCLEG0	-8592.77	-400.00	B
13	VSS(MODE)	-8512.44	-400.00	B
14	HSEG	-8414.77	-400.00	B
15	VCC11 (MODE)	-8334.44	-400.00	B
16	VSEG	-8236.77	-400.00	B
17	VSS (MODE)	-8156.44	-400.00	B
18	DCKEG	-8058.77	-400.00	B
19	VCC11(MODE)	-7978.44	-400.00	B
20	PSX	-7880.77	-400.00	B
21	VSS (MODE)	-7800.44	-400.00	B
22	C86	-7702.77	-400.00	B
23	VCC11 (MODE)	-7622.44	-400.00	B
24	DTX1	-7524.77	-400.00	B
25	VSS (MODE)	-7444.44	-400.00	B
26	DTX2	-7346.77	-400.00	B
27	VCC11 (MODE)	-7266.44	-400.00	B
28	BWS0	-7168.77	-400.00	B
29	VSS (MODE)	-7088.44	-400.00	B
30	BWS1	-6990.77	-400.00	B
31	VCC11 (MODE)	-6910.44	-400.00	B
32	BWS2	-6812.77	-400.00	B
33	VSS (MODE)	-6732.44	-400.00	B
34	DDS	-6634.77	-400.00	B
35	VCC11 (MODE)	-6554.44	-400.00	B
36	IF_SHARE	-6456.77	-400.00	B
37	VSS (MODE)	-6376.44	-400.00	B
38	CSTB	-6296.44	-400.00	B
39	D17	-6196.44	-400.00	B
40	D16	-6096.44	-400.00	B
41	D15	-5996.44	-400.00	B
42	D14	-5896.44	-400.00	B
43	D13	-5796.50	-400.00	B
44	D12	-5696.44	-400.00	B
45	D11	-5596.44	-400.00	B
46	D10	-5496.44	-400.00	B
47	D9	-5396.44	-400.00	B
48	D8	-5296.44	-400.00	B
49	D7	-5196.44	-400.00	B
50	D6	-5096.44	-400.00	B
51	D5	-4996.44	-400.00	B
52	D4	-4896.44	-400.00	B
53	D3	-4796.44	-400.00	B
54	D2	-4696.44	-400.00	B
55	D1	-4596.44	-400.00	B
56	D0	-4496.44	-400.00	B
57	VSS (MODE)	-4397.96	-400.00	B
58	VCC11 (MODE)	-4317.96	-400.00	B
59	/CS	-4237.96	-400.00	B
60	/RESET	-4137.96	-400.00	B
61	RS	-4037.96	-400.00	B
62	/WR	-3937.96	-400.00	B
63	/RD	-3837.96	-400.00	B
64	RGB/MCPU	-3737.96	-400.00	B
65	VSS (MODE)	-3639.48	-400.00	B
66	VCC11 (MODE)	-3559.48	-400.00	B
67	SI	-3479.48	-400.00	B
68	SCL	-3379.48	-400.00	B
69	SO	-3279.48	-400.00	B
70	/BLCS_I	-3179.48	-400.00	B
71	VSS (MODE)	-3081.00	-400.00	B
72	VCC11 (MODE)	-3001.00	-400.00	B
73	Vsync	-2921.00	-400.00	B
74	Hsync	-2821.00	-400.00	B
75	Dotclk	-2721.00	-400.00	B
76	RGB00	-2621.00	-400.00	B
77	RGB01	-2521.00	-400.00	B
78	RGB02	-2421.00	-400.00	B
79	RGB03	-2321.00	-400.00	B
80	RGB04	-2221.00	-400.00	B
81	RGB05	-2121.00	-400.00	B

BumpNo.	Name	X (µm)	Y (µm)	Bumptype
82	RGB10	-2021.00	-400.00	B
83	RGB11	-1921.00	-400.00	B
84	RGB12	-1821.00	-400.00	B
85	RGB13	-1721.00	-400.00	B
86	RGB14	-1621.00	-400.00	B
87	RGB15	-1521.00	-400.00	B
88	RGB20	-1421.00	-400.00	B
89	RGB21	-1321.00	-400.00	B
90	RGB22	-1221.00	-400.00	B
91	RGB23	-1121.00	-400.00	B
92	RGB24	-1021.00	-400.00	B
93	RGB25	-921.00	-400.00	B
94	VCC11	-820.93	-400.00	B
95	VCC11	-740.93	-400.00	C
96	VCC11	-660.93	-400.00	C
97	VCC11	-580.93	-400.00	C
98	VCC11	-500.93	-400.00	C
99	VCC11	-420.93	-400.00	C
100	VCC11	-340.93	-400.00	C
101	VCC11	-260.93	-400.00	B
102	VSS	-180.93	-400.00	B
103	VSS	-100.93	-400.00	C
104	VSS	-20.93	-400.00	C
105	VSS	59.07	-400.00	C
106	VSS	139.07	-400.00	C
107	VSS	219.07	-400.00	C
108	VSS	299.07	-400.00	B
109	VSS	379.07	-400.00	B
110	VSS	459.07	-400.00	C
111	VSS	539.07	-400.00	C
112	VSS	619.07	-400.00	C
113	VSS	699.07	-400.00	C
114	VSS	779.07	-400.00	C
115	VSS	859.07	-400.00	B
116	VS	939.07	-400.00	B
117	VS	1019.07	-400.00	C
118	VS	1099.07	-400.00	C
119	VS	1179.07	-400.00	C
120	VS	1259.07	-400.00	C
121	VS	1339.07	-400.00	C
122	VS	1419.07	-400.00	C
123	VS	1499.07	-400.00	B
124	VDHR	1579.07	-400.00	B
125	VDHR	1659.07	-400.00	C
126	VDHR	1739.07	-400.00	C
127	VDHR	1819.07	-400.00	C
128	VDHR	1899.07	-400.00	B
129	V18	2003.43	-400.00	B
130	V18	2083.43	-400.00	C
131	V18	2163.43	-400.00	C
132	V18	2243.43	-400.00	C
133	V18	2323.43	-400.00	C
134	V18	2403.43	-400.00	C
135	V18	2483.43	-400.00	C
136	V18	2563.43	-400.00	B
137	DUMMY	2641.28	-400.00	B
138	DUMMY	2721.28	-400.00	B
139	DUMMY	2801.28	-400.00	B
140	DUMMY	2881.28	-400.00	B
141	DUMMY	2961.28	-400.00	B
142	DUMMY	3041.28	-400.00	B
143	DUMMY	3121.28	-400.00	B
144	DUMMY	3201.28	-400.00	B
145	DUMMY	3281.28	-400.00	B
146	DUMMY	3361.28	-400.00	B
147	DUMMY	3441.28	-400.00	B
148	DUMMY	3521.28	-400.00	B
149	DUMMY	3601.28	-400.00	B
150	DUMMY	3681.28	-400.00	B
151	DUMMY	3761.28	-400.00	B
152	DUMMY	3841.28	-400.00	B
153	DUMMY	3921.28	-400.00	B
154	DUMMY	4001.28	-400.00	B
155	DUMMY	4081.28	-400.00	B
156	DUMMY	4161.28	-400.00	B
157	DUMMY	4241.28	-400.00	B
158	DUMMY	4321.28	-400.00	B
159	DUMMY	4401.28	-400.00	B
160	DUMMY	4481.28	-400.00	B
161	DUMMY	4561.28	-400.00	B
162	DUMMY	4641.28	-400.00	B

BumpNo.	Name	X (µm)	Y (µm)	BumpType
163	DUMMY	4721.28	-400.00	B
164	DUMMY	4801.28	-400.00	B
165	DUMMY	4881.28	-400.00	B
166	DUMMY	4961.28	-400.00	B
167	DUMMY	5041.28	-400.00	B
168	DUMMY	5121.28	-400.00	B
169	VSS (MODE)	5201.28	-400.00	B
170	TEST2	5299.76	-400.00	B
171	TEST3	5399.76	-400.00	B
172	STB	5499.76	-400.00	B
173	VCOUT2	5599.76	-400.00	B
174	SYSCLK	5699.76	-400.00	B
175	/GRESET	5799.76	-400.00	B
176	GCS	5899.76	-400.00	B
177	GDA	5999.76	-400.00	B
178	GOE1	6099.76	-400.00	B
179	GOE2	6199.76	-400.00	B
180	GCLK	6299.76	-400.00	B
181	GFRM	6399.76	-400.00	B
182	DUMMY	6479.76	-400.00	B
183	DUMMY	6559.76	-400.00	B
184	DUMMY	6639.76	-400.00	B
185	DUMMY	6719.76	-400.00	B
186	DUMMY	6799.76	-400.00	B
187	DUMMY	6879.76	-400.00	B
188	DUMMY	6959.76	-400.00	B
189	DUMMY	7039.76	-400.00	B
190	DUMMY	7119.76	-400.00	B
191	DUMMY	7199.76	-400.00	B
192	DUMMY	7279.76	-400.00	B
193	DUMMY	7359.76	-400.00	B
194	DUMMY	7439.76	-400.00	B
195	DUMMY	7519.76	-400.00	B
196	DUMMY	7599.76	-400.00	B
197	DUMMY	7679.76	-400.00	B
198	DUMMY	7759.76	-400.00	B
199	DUMMY	7839.76	-400.00	B
200	DUMMY	7919.76	-400.00	B
201	DUMMY	7999.76	-400.00	B
202	DUMMY	8079.76	-400.00	B
203	DUMMY	8159.76	-400.00	B
204	DUMMY	8239.76	-400.00	B
205	DUMMY	8319.76	-400.00	B
206	DUMMY	8399.76	-400.00	B
207	DUMMY	8479.76	-400.00	B
208	DUMMY	8559.76	-400.00	B
209	DUMMY	8639.76	-400.00	B
210	DUMMY	8719.76	-400.00	B
211	DUMMY	8799.76	-400.00	B
212	DUMMY	8879.76	-400.00	B
213	DUMMY	8959.76	-400.00	B
214	DUMMY	9039.76	-400.00	B
215	DUMMY	9119.76	-400.00	B
216	DUMMY	9199.76	-400.00	B
217	DUMMY	9279.76	-400.00	B
218	DUMMY	9359.76	-400.00	B
219	DUMMY	9439.76	-400.00	B
220	VC1	9527.01	-400.00	B
221	DUMMY	9607.01	-400.00	B
222	DUMMY	9630.00	326.21	A
223	VC1	9594.00	410.21	A
224	DUMMY	9558.00	326.21	A
225	VC1	9522.00	410.21	A
226	Y528	9486.00	326.21	A
227	Y527	9450.00	410.21	A
228	Y526	9414.00	326.21	A
229	Y525	9378.00	410.21	A
230	Y524	9342.00	326.21	A
231	Y523	9306.00	410.21	A
232	Y522	9270.00	326.21	A
233	Y521	9234.00	410.21	A
234	Y520	9198.00	326.21	A
235	Y519	9162.00	410.21	A
236	Y518	9126.00	326.21	A
237	Y517	9090.00	410.21	A
238	Y516	9054.00	326.21	A
239	Y515	9018.00	410.21	A
240	Y514	8982.00	326.21	A
241	Y513	8946.00	410.21	A
242	Y512	8910.00	326.21	A
243	Y511	8874.00	410.21	A
244	Y510	8838.00	326.21	A
245	Y509	8802.00	410.21	A
246	Y508	8766.00	326.21	A
247	Y507	8730.00	410.21	A
248	Y506	8694.00	326.21	A

BumpNo.	Name	X (µm)	Y (µm)	BumpType
249	Y505	8658.00	410.21	A
250	Y504	8622.00	326.21	A
251	Y503	8586.00	410.21	A
252	Y502	8550.00	326.21	A
253	Y501	8514.00	410.21	A
254	Y500	8478.00	326.21	A
255	Y499	8442.00	410.21	A
256	Y498	8406.00	326.21	A
257	Y497	8370.00	410.21	A
258	Y496	8334.00	326.21	A
259	Y495	8298.00	410.21	A
260	Y494	8262.00	326.21	A
261	Y493	8226.00	410.21	A
262	Y492	8190.00	326.21	A
263	Y491	8154.00	410.21	A
264	Y490	8118.00	326.21	A
265	Y489	8082.00	410.21	A
266	Y488	8046.00	326.21	A
267	Y487	8010.00	410.21	A
268	Y486	7974.00	326.21	A
269	Y485	7938.00	410.21	A
270	Y484	7902.00	326.21	A
271	Y483	7866.00	410.21	A
272	Y482	7830.00	326.21	A
273	Y481	7794.00	410.21	A
274	Y480	7758.00	326.21	A
275	Y479	7722.00	410.21	A
276	Y478	7686.00	326.21	A
277	Y477	7650.00	410.21	A
278	Y476	7614.00	326.21	A
279	Y475	7578.00	410.21	A
280	Y474	7542.00	326.21	A
281	Y473	7506.00	410.21	A
282	Y472	7470.00	326.21	A
283	Y471	7434.00	410.21	A
284	Y470	7398.00	326.21	A
285	Y469	7362.00	410.21	A
286	Y468	7326.00	326.21	A
287	Y467	7290.00	410.21	A
288	Y466	7254.00	326.21	A
289	Y465	7218.00	410.21	A
290	Y464	7182.00	326.21	A
291	Y463	7146.00	410.21	A
292	Y462	7110.00	326.21	A
293	Y461	7074.00	410.21	A
294	Y460	7038.00	326.21	A
295	Y459	7002.00	410.21	A
296	Y458	6966.00	326.21	A
297	Y457	6930.00	410.21	A
298	Y456	6894.00	326.21	A
299	Y455	6858.00	410.21	A
300	Y454	6822.00	326.21	A
301	Y453	6786.00	410.21	A
302	Y452	6750.00	326.21	A
303	Y451	6714.00	410.21	A
304	Y450	6678.00	326.21	A
305	Y449	6642.00	410.21	A
306	Y448	6606.00	326.21	A
307	Y447	6570.00	410.21	A
308	Y446	6534.00	326.21	A
309	Y445	6498.00	410.21	A
310	Y444	6462.00	326.21	A
311	Y443	6426.00	410.21	A
312	Y442	6390.00	326.21	A
313	Y441	6354.00	410.21	A
314	Y440	6318.00	326.21	A
315	Y439	6282.00	410.21	A
316	Y438	6246.00	326.21	A
317	Y437	6210.00	410.21	A
318	Y436	6174.00	326.21	A
319	Y435	6138.00	410.21	A
320	Y434	6102.00	326.21	A
321	Y433	6066.00	410.21	A
322	Y432	6030.00	326.21	A
323	Y431	5994.00	410.21	A
324	Y430	5958.00	326.21	A
325	Y429	5922.00	410.21	A
326	Y428	5886.00	326.21	A
327	Y427	5850.00	410.21	A
328	Y426	5814.00	326.21	A
329	Y425	5778.00	410.21	A
330	Y424	5742.00	326.21	A
331	Y423	5706.00	410.21	A
332	Y422	5670.00	326.21	A
333	Y421	5634.00	410.21	A
334	Y420	5598.00	326.21	A

BumpNo.	Name	X (µm)	Y (µm)	Bumptype
335	Y419	5562.00	410.21	A
336	Y418	5526.00	326.21	A
337	Y417	5490.00	410.21	A
338	Y416	5454.00	326.21	A
339	Y415	5418.00	410.21	A
340	Y414	5382.00	326.21	A
341	Y413	5346.00	410.21	A
342	Y412	5310.00	326.21	A
343	Y411	5274.00	410.21	A
344	Y410	5238.00	326.21	A
345	Y409	5202.00	410.21	A
346	Y408	5166.00	326.21	A
347	Y407	5130.00	410.21	A
348	Y406	5094.00	326.21	A
349	Y405	5058.00	410.21	A
350	Y404	5022.00	326.21	A
351	Y403	4986.00	410.21	A
352	Y402	4950.00	326.21	A
353	Y401	4914.00	410.21	A
354	Y400	4878.00	326.21	A
355	Y399	4842.00	410.21	A
356	Y398	4806.00	326.21	A
357	Y397	4770.00	410.21	A
358	Y396	4734.00	326.21	A
359	Y395	4698.00	410.21	A
360	Y394	4662.00	326.21	A
361	Y393	4626.00	410.21	A
362	Y392	4590.00	326.21	A
363	Y391	4554.00	410.21	A
364	Y390	4518.00	326.21	A
365	Y389	4482.00	410.21	A
366	Y388	4446.00	326.21	A
367	Y387	4410.00	410.21	A
368	Y386	4374.00	326.21	A
369	Y385	4338.00	410.21	A
370	Y384	4302.00	326.21	A
371	Y383	4266.00	410.21	A
372	Y382	4230.00	326.21	A
373	Y381	4194.00	410.21	A
374	Y380	4158.00	326.21	A
375	Y379	4122.00	410.21	A
376	Y378	4086.00	326.21	A
377	Y377	4050.00	410.21	A
378	Y376	4014.00	326.21	A
379	Y375	3978.00	410.21	A
380	Y374	3942.00	326.21	A
381	Y373	3906.00	410.21	A
382	Y372	3870.00	326.21	A
383	Y371	3834.00	410.21	A
384	Y370	3798.00	326.21	A
385	Y369	3762.00	410.21	A
386	Y368	3726.00	326.21	A
387	Y367	3690.00	410.21	A
388	Y366	3654.00	326.21	A
389	Y365	3618.00	410.21	A
390	Y364	3582.00	326.21	A
391	Y363	3546.00	410.21	A
392	Y362	3510.00	326.21	A
393	Y361	3474.00	410.21	A
394	Y360	3438.00	326.21	A
395	Y359	3402.00	410.21	A
396	Y358	3366.00	326.21	A
397	Y357	3330.00	410.21	A
398	Y356	3294.00	326.21	A
399	Y355	3258.00	410.21	A
400	Y354	3222.00	326.21	A
401	Y353	3186.00	410.21	A
402	Y352	3150.00	326.21	A
403	Y351	3114.00	410.21	A
404	Y350	3078.00	326.21	A
405	Y349	3042.00	410.21	A
406	Y348	3006.00	326.21	A
407	Y347	2970.00	410.21	A
408	Y346	2934.00	326.21	A
409	Y345	2898.00	410.21	A
410	Y344	2862.00	326.21	A
411	Y343	2826.00	410.21	A
412	Y342	2790.00	326.21	A
413	Y341	2754.00	410.21	A
414	Y340	2718.00	326.21	A
415	Y339	2682.00	410.21	A
416	Y338	2646.00	326.21	A
417	Y337	2610.00	410.21	A
418	Y336	2574.00	326.21	A
419	Y335	2538.00	410.21	A
420	Y334	2502.00	326.21	A

BumpNo.	Name	X (µm)	Y (µm)	Bumptype
421	Y333	2466.00	410.21	A
422	Y332	2430.00	326.21	A
423	Y331	2394.00	410.21	A
424	Y330	2358.00	326.21	A
425	Y329	2322.00	410.21	A
426	Y328	2286.00	326.21	A
427	Y327	2250.00	410.21	A
428	Y326	2214.00	326.21	A
429	Y325	2178.00	410.21	A
430	Y324	2142.00	326.21	A
431	Y323	2106.00	410.21	A
432	Y322	2070.00	326.21	A
433	Y321	2034.00	410.21	A
434	Y320	1998.00	326.21	A
435	Y319	1962.00	410.21	A
436	Y318	1926.00	326.21	A
437	Y317	1890.00	410.21	A
438	Y316	1854.00	326.21	A
439	Y315	1818.00	410.21	A
440	Y314	1782.00	326.21	A
441	Y313	1746.00	410.21	A
442	Y312	1710.00	326.21	A
443	Y311	1674.00	410.21	A
444	Y310	1638.00	326.21	A
445	Y309	1602.00	410.21	A
446	Y308	1566.00	326.21	A
447	Y307	1530.00	410.21	A
448	Y306	1494.00	326.21	A
449	Y305	1458.00	410.21	A
450	Y304	1422.00	326.21	A
451	Y303	1386.00	410.21	A
452	Y302	1350.00	326.21	A
453	Y301	1314.00	410.21	A
454	Y300	1278.00	326.21	A
455	Y299	1242.00	410.21	A
456	Y298	1206.00	326.21	A
457	Y297	1170.00	410.21	A
458	Y296	1134.00	326.21	A
459	Y295	1098.00	410.21	A
460	Y294	1062.00	326.21	A
461	Y293	1026.00	410.21	A
462	Y292	990.00	326.21	A
463	Y291	954.00	410.21	A
464	Y290	918.00	326.21	A
465	Y289	882.00	410.21	A
466	Y288	846.00	326.21	A
467	Y287	810.00	410.21	A
468	Y286	774.00	326.21	A
469	Y285	738.00	410.21	A
470	Y284	702.00	326.21	A
471	Y283	666.00	410.21	A
472	Y282	630.00	326.21	A
473	Y281	594.00	410.21	A
474	Y280	558.00	326.21	A
475	Y279	522.00	410.21	A
476	Y278	486.00	326.21	A
477	Y277	450.00	410.21	A
478	Y276	414.00	326.21	A
479	Y275	378.00	410.21	A
480	Y274	342.00	326.21	A
481	Y273	306.00	410.21	A
482	Y272	270.00	326.21	A
483	Y271	234.00	410.21	A
484	Y270	198.00	326.21	A
485	Y269	162.00	410.21	A
486	Y268	126.00	326.21	A
487	Y267	90.00	410.21	A
488	Y266	54.00	326.21	A
489	Y265	18.00	410.21	A
490	Y264	-18.00	326.21	A
491	Y263	-54.00	410.21	A
492	Y262	-90.00	326.21	A
493	Y261	-126.00	410.21	A
494	Y260	-162.00	326.21	A
495	Y259	-198.00	410.21	A
496	Y258	-234.00	326.21	A
497	Y257	-270.00	410.21	A
498	Y256	-306.00	326.21	A
499	Y255	-342.00	410.21	A
500	Y254	-378.00	326.21	A
501	Y253	-414.00	410.21	A
502	Y252	-450.00	326.21	A
503	Y251	-486.00	410.21	A
504	Y250	-522.00	326.21	A
505	Y249	-558.00	410.21	A
506	Y248	-594.00	326.21	A

BumpNo.	Name	X (µm)	Y (µm)	BumpType
507	Y247	-630.00	410.21	A
508	Y246	-666.00	326.21	A
509	Y245	-702.00	410.21	A
510	Y244	-738.00	326.21	A
511	Y243	-774.00	410.21	A
512	Y242	-810.00	326.21	A
513	Y241	-846.00	410.21	A
514	Y240	-882.00	326.21	A
515	Y239	-918.00	410.21	A
516	Y238	-954.00	326.21	A
517	Y237	-990.00	410.21	A
518	Y236	-1026.00	326.21	A
519	Y235	-1062.00	410.21	A
520	Y234	-1098.00	326.21	A
521	Y233	-1134.00	410.21	A
522	Y232	-1170.00	326.21	A
523	Y231	-1206.00	410.21	A
524	Y230	-1242.00	326.21	A
525	Y229	-1278.00	410.21	A
526	Y228	-1314.00	326.21	A
527	Y227	-1350.00	410.21	A
528	Y226	-1386.00	326.21	A
529	Y225	-1422.00	410.21	A
530	Y224	-1458.00	326.21	A
531	Y223	-1494.00	410.21	A
532	Y222	-1530.00	326.21	A
533	Y221	-1566.00	410.21	A
534	Y220	-1602.00	326.21	A
535	Y219	-1638.00	410.21	A
536	Y218	-1674.00	326.21	A
537	Y217	-1710.00	410.21	A
538	Y216	-1746.00	326.21	A
539	Y215	-1782.00	410.21	A
540	Y214	-1818.00	326.21	A
541	Y213	-1854.00	410.21	A
542	Y212	-1890.00	326.21	A
543	Y211	-1926.00	410.21	A
544	Y210	-1962.00	326.21	A
545	Y209	-1998.00	410.21	A
546	Y208	-2034.00	326.21	A
547	Y207	-2070.00	410.21	A
548	Y206	-2106.00	326.21	A
549	Y205	-2142.00	410.21	A
550	Y204	-2178.00	326.21	A
551	Y203	-2214.00	410.21	A
552	Y202	-2250.00	326.21	A
553	Y201	-2286.00	410.21	A
554	Y200	-2322.00	326.21	A
555	Y199	-2358.00	410.21	A
556	Y198	-2394.00	326.21	A
557	Y197	-2430.00	410.21	A
558	Y196	-2466.00	326.21	A
559	Y195	-2502.00	410.21	A
560	Y194	-2538.00	326.21	A
561	Y193	-2574.00	410.21	A
562	Y192	-2610.00	326.21	A
563	Y191	-2646.00	410.21	A
564	Y190	-2682.00	326.21	A
565	Y189	-2718.00	410.21	A
566	Y188	-2754.00	326.21	A
567	Y187	-2790.00	410.21	A
568	Y186	-2826.00	326.21	A
569	Y185	-2862.00	410.21	A
570	Y184	-2898.00	326.21	A
571	Y183	-2934.00	410.21	A
572	Y182	-2970.00	326.21	A
573	Y181	-3006.00	410.21	A
574	Y180	-3042.00	326.21	A
575	Y179	-3078.00	410.21	A
576	Y178	-3114.00	326.21	A
577	Y177	-3150.00	410.21	A
578	Y176	-3186.00	326.21	A
579	Y175	-3222.00	410.21	A
580	Y174	-3258.00	326.21	A
581	Y173	-3294.00	410.21	A
582	Y172	-3330.00	326.21	A
583	Y171	-3366.00	410.21	A
584	Y170	-3402.00	326.21	A
585	Y169	-3438.00	410.21	A
586	Y168	-3474.00	326.21	A
587	Y167	-3510.00	410.21	A
588	Y166	-3546.00	326.21	A
589	Y165	-3582.00	410.21	A
590	Y164	-3618.00	326.21	A
591	Y163	-3654.00	410.21	A
592	Y162	-3690.00	326.21	A

BumpNo.	Name	X (µm)	Y (µm)	BumpType
593	Y161	-3726.00	410.21	A
594	Y160	-3762.00	326.21	A
595	Y159	-3798.00	410.21	A
596	Y158	-3834.00	326.21	A
597	Y157	-3870.00	410.21	A
598	Y156	-3906.00	326.21	A
599	Y155	-3942.00	410.21	A
600	Y154	-3978.00	326.21	A
601	Y153	-4014.00	410.21	A
602	Y152	-4050.00	326.21	A
603	Y151	-4086.00	410.21	A
604	Y150	-4122.00	326.21	A
605	Y149	-4158.00	410.21	A
606	Y148	-4194.00	326.21	A
607	Y147	-4230.00	410.21	A
608	Y146	-4266.00	326.21	A
609	Y145	-4302.00	410.21	A
610	Y144	-4338.00	326.21	A
611	Y143	-4374.00	410.21	A
612	Y142	-4410.00	326.21	A
613	Y141	-4446.00	410.21	A
614	Y140	-4482.00	326.21	A
615	Y139	-4518.00	410.21	A
616	Y138	-4554.00	326.21	A
617	Y137	-4590.00	410.21	A
618	Y136	-4626.00	326.21	A
619	Y135	-4662.00	410.21	A
620	Y134	-4698.00	326.21	A
621	Y133	-4734.00	410.21	A
622	Y132	-4770.00	326.21	A
623	Y131	-4806.00	410.21	A
624	Y130	-4842.00	326.21	A
625	Y129	-4878.00	410.21	A
626	Y128	-4914.00	326.21	A
627	Y127	-4950.00	410.21	A
628	Y126	-4986.00	326.21	A
629	Y125	-5022.00	410.21	A
630	Y124	-5058.00	326.21	A
631	Y123	-5094.00	410.21	A
632	Y122	-5130.00	326.21	A
633	Y121	-5166.00	410.21	A
634	Y120	-5202.00	326.21	A
635	Y119	-5238.00	410.21	A
636	Y118	-5274.00	326.21	A
637	Y117	-5310.00	410.21	A
638	Y116	-5346.00	326.21	A
639	Y115	-5382.00	410.21	A
640	Y114	-5418.00	326.21	A
641	Y113	-5454.00	410.21	A
642	Y112	-5490.00	326.21	A
643	Y111	-5526.00	410.21	A
644	Y110	-5562.00	326.21	A
645	Y109	-5598.00	410.21	A
646	Y108	-5634.00	326.21	A
647	Y107	-5670.00	410.21	A
648	Y106	-5706.00	326.21	A
649	Y105	-5742.00	410.21	A
650	Y104	-5778.00	326.21	A
651	Y103	-5814.00	410.21	A
652	Y102	-5850.00	326.21	A
653	Y101	-5886.00	410.21	A
654	Y100	-5922.00	326.21	A
655	Y99	-5958.00	410.21	A
656	Y98	-5994.00	326.21	A
657	Y97	-6030.00	410.21	A
658	Y96	-6066.00	326.21	A
659	Y95	-6102.00	410.21	A
660	Y94	-6138.00	326.21	A
661	Y93	-6174.00	410.21	A
662	Y92	-6210.00	326.21	A
663	Y91	-6246.00	410.21	A
664	Y90	-6282.00	326.21	A
665	Y89	-6318.00	410.21	A
666	Y88	-6354.00	326.21	A
667	Y87	-6390.00	410.21	A
668	Y86	-6426.00	326.21	A
669	Y85	-6462.00	410.21	A
670	Y84	-6498.00	326.21	A
671	Y83	-6534.00	410.21	A
672	Y82	-6570.00	326.21	A
673	Y81	-6606.00	410.21	A
674	Y80	-6642.00	326.21	A
675	Y79	-6678.00	410.21	A
676	Y78	-6714.00	326.21	A
677	Y77	-6750.00	410.21	A
678	Y76	-6786.00	326.21	A

BumpNo.	Name	X (µm)	Y (µm)	Bumptype
679	Y75	-6822.00	410.21	A
680	Y74	-6858.00	326.21	A
681	Y73	-6894.00	410.21	A
682	Y72	-6930.00	326.21	A
683	Y71	-6966.00	410.21	A
684	Y70	-7002.00	326.21	A
685	Y69	-7038.00	410.21	A
686	Y68	-7074.00	326.21	A
687	Y67	-7110.00	410.21	A
688	Y66	-7146.00	326.21	A
689	Y65	-7182.00	410.21	A
690	Y64	-7218.00	326.21	A
691	Y63	-7254.00	410.21	A
692	Y62	-7290.00	326.21	A
693	Y61	-7326.00	410.21	A
694	Y60	-7362.00	326.21	A
695	Y59	-7398.00	410.21	A
696	Y58	-7434.00	326.21	A
697	Y57	-7470.00	410.21	A
698	Y56	-7506.00	326.21	A
699	Y55	-7542.00	410.21	A
700	Y54	-7578.00	326.21	A
701	Y53	-7614.00	410.21	A
702	Y52	-7650.00	326.21	A
703	Y51	-7686.00	410.21	A
704	Y50	-7722.00	326.21	A
705	Y49	-7758.00	410.21	A
706	Y48	-7794.00	326.21	A
707	Y47	-7830.00	410.21	A
708	Y46	-7866.00	326.21	A
709	Y45	-7902.00	410.21	A
710	Y44	-7938.00	326.21	A
711	Y43	-7974.00	410.21	A
712	Y42	-8010.00	326.21	A
713	Y41	-8046.00	410.21	A
714	Y40	-8082.00	326.21	A
715	Y39	-8118.00	410.21	A
716	Y38	-8154.00	326.21	A
717	Y37	-8190.00	410.21	A
718	Y36	-8226.00	326.21	A
719	Y35	-8262.00	410.21	A
720	Y34	-8298.00	326.21	A
721	Y33	-8334.00	410.21	A
722	Y32	-8370.00	326.21	A
723	Y31	-8406.00	410.21	A
724	Y30	-8442.00	326.21	A
725	Y29	-8478.00	410.21	A
726	Y28	-8514.00	326.21	A
727	Y27	-8550.00	410.21	A
728	Y26	-8586.00	326.21	A
729	Y25	-8622.00	410.21	A
730	Y24	-8658.00	326.21	A
731	Y23	-8694.00	410.21	A
732	Y22	-8730.00	326.21	A
733	Y21	-8766.00	410.21	A
734	Y20	-8802.00	326.21	A
735	Y19	-8838.00	410.21	A
736	Y18	-8874.00	326.21	A
737	Y17	-8910.00	410.21	A
738	Y16	-8946.00	326.21	A
739	Y15	-8982.00	410.21	A
740	Y14	-9018.00	326.21	A
741	Y13	-9054.00	410.21	A
742	Y12	-9090.00	326.21	A
743	Y11	-9126.00	410.21	A
744	Y10	-9162.00	326.21	A
745	Y9	-9198.00	410.21	A
746	Y8	-9234.00	326.21	A
747	Y7	-9270.00	410.21	A
748	Y6	-9306.00	326.21	A
749	Y5	-9342.00	410.21	A
750	Y4	-9378.00	326.21	A
751	Y3	-9414.00	410.21	A
752	Y2	-9450.00	326.21	A
753	Y1	-9486.00	410.21	A
754	VC1	-9522.00	326.21	A
755	DUMMY	-9558.00	410.21	A
756	VC1	-9594.00	326.21	A
757	DUMMY	-9630.00	410.21	A

4.5. VC1_L and VC1_R Pins

VC1_L (PAD2, PAD756, PAD754) and VC1_R (PAD220, PAD225, PAD223) are connected in the LSI as shown in Fig4-1. These pins are used to send the VCOM output of the IS2200, from the lower input side to the upper output side of the IS2100.

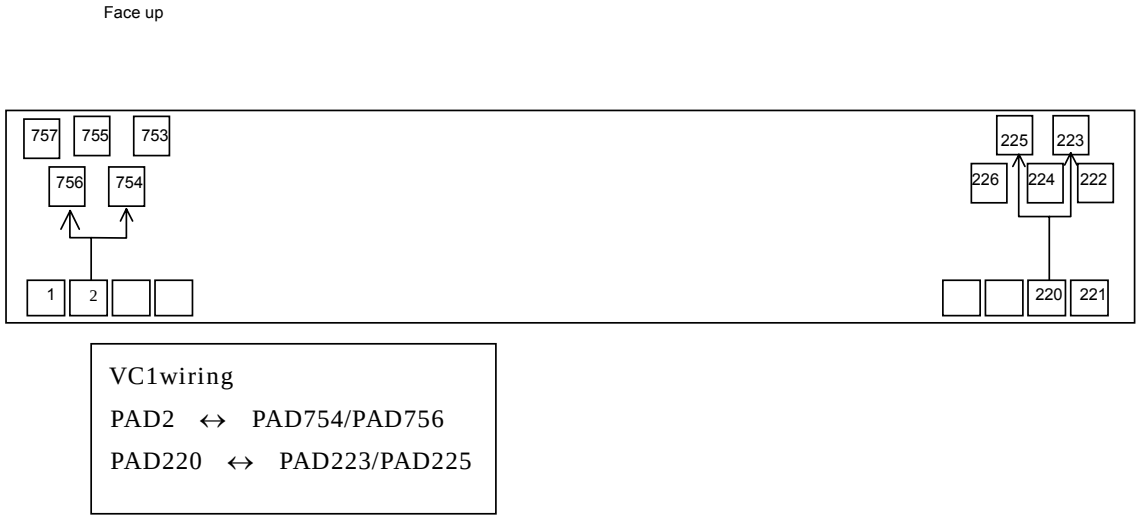


Fig. 4-1 Internal wiring of VC1

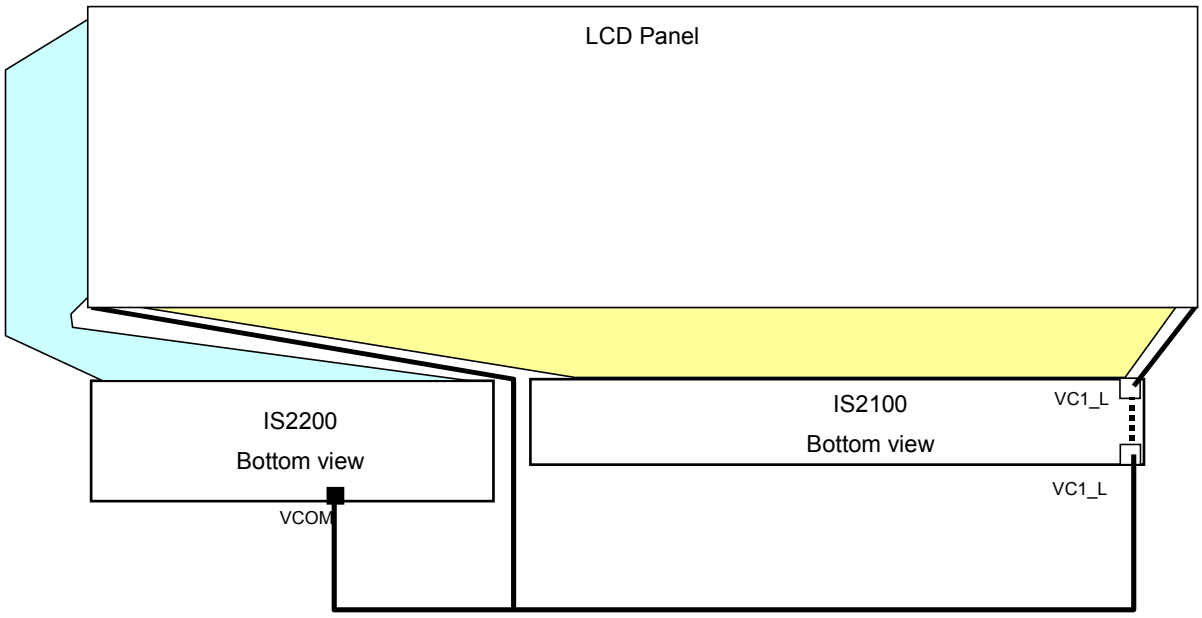
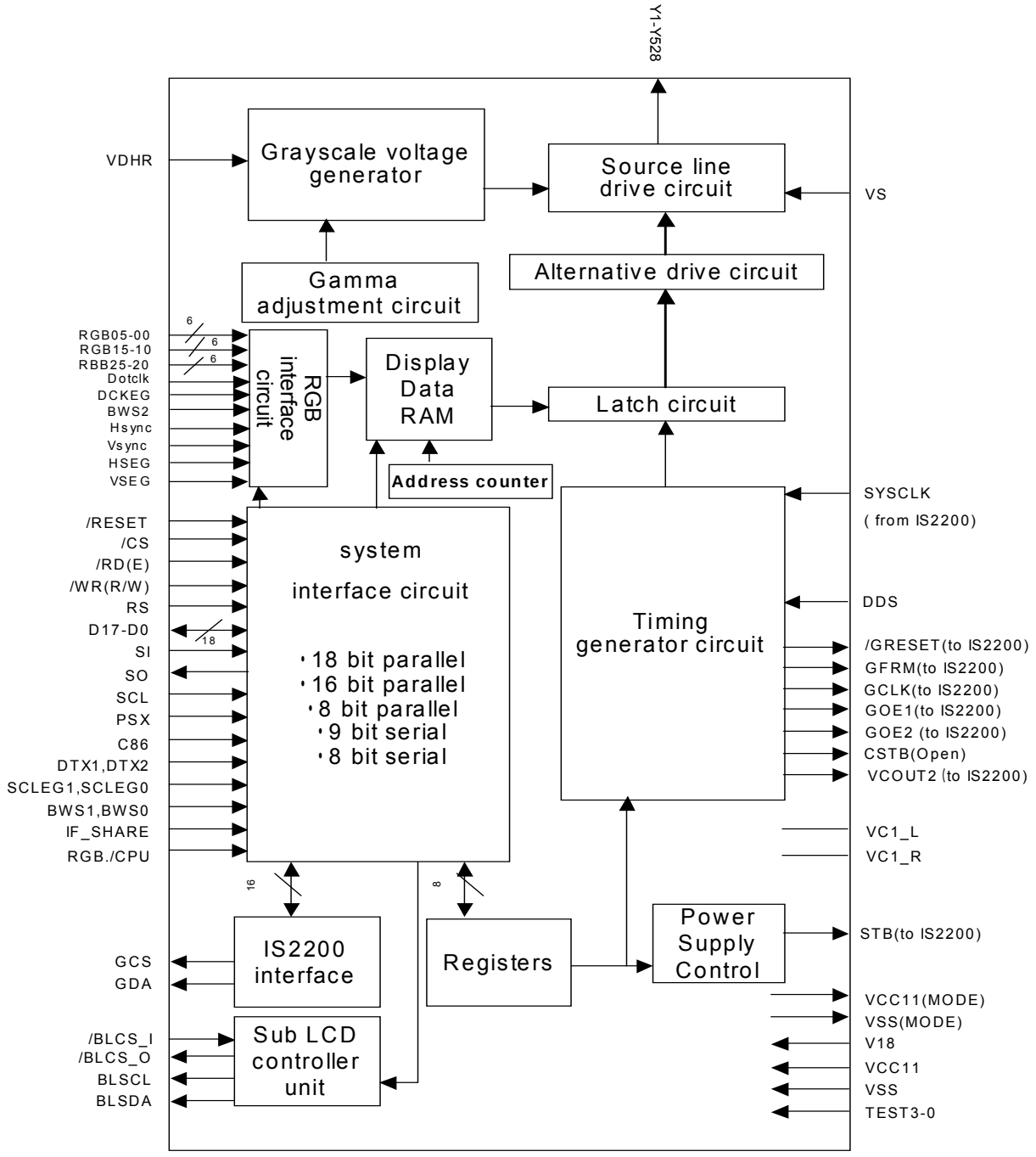


Fig. 4-2 VCOM wiring (e.g.)

5. Block Diagram



6. Interface

The IS2100 has a system interface circuit and an RGB interface circuit. As for the data bus, the IS2100 has data pins (D17-D0) for the CPU connection and RGB pins (RGB25-00) for animated displays. Since the data bus (D17-D0) can be shared with the data bus for the RGB interface circuit, the IS2100 can provide the animated display interface with less wiring.
To select an interface, please refer to Table 6-1.

Pin			Interface circuit		
PSX	IF_SHARE	PGB. /CPU	SI, SO, SCLK	D17 - 0	RGB25 - 00
L	L	L	-	System interface circuit	RGB interface circuit
L	L	H	-	System interface circuit	RGB interface circuit
L	H	L	-	System interface circuit / RGB interface circuit (＊1)	-
L	H	H	-	RGB interface circuit	-
H	L	L	System interface circuit	-	RGB interface circuit
H	L	H	System interface circuit		RGB interface circuit
H	H	L	System interface circuit	RGB interface circuit	-
H	H	H	-	RGB interface circuit	-

Table 6-1 Interface type

Note: System interface circuit is not available when IF_SHARE=H and RGB./CPU=H.
(Parallel and serial transfers are not available.)

*: Both of circuits are available when Dotclk, /CS, /WR, /RD are inputted simultaneously.
RGB interface circuit: Display data transfer
System interface circuit: Command

6.1. System Interface Circuit

The IS2100 has the 18/16/8-bit parallel interface circuits for i80, and
the 18/16/8-bit parallel interface circuits
and the 9/8-bit serial interface circuits for M68.

To select an interface, please refer to Table 6-2.

Interface Mode	Terminal					Interface Mode	Number of data in a dot	Transferring method of one dot data	Transferring method of one command data
	PSX	BWS1	BWS0	DTX2	DTX1				
MPU1	L	L	L	X	X	18-bit parallel	18 bits	18-bit collective	16-bit collective
MPU2	L	H	L	L	H	16-bit parallel	18 bits	9-bit twice	
MPU3	L	H	L	H	H			16-bit + 2-bit	
MPU4	L	H	L	L	L		16 bits	16-bit collective	
MPU5	L	H	H	L	H	8-bit parallel	18 bits	6-bit 3 times	8-bit twice
MPU6	L	H	H	H	H			8-bit + 8-bit + 2-bit	
MPU7	L	H	H	H	L		16 bits	8-bit twice	
MPU8	H	L	H	X	X	9-bit serial	18 bits	9-bit twice	9-bit twice
MPU9	H	H	H	X	X	8-bit serial	16 bits	8-bit twice	8-bit twice

Table 6-2 System interface circuit set-up

6.1.1. Parallel interface circuit

When /CS=L, the IS2100 becomes active and can communicate with the parallel interface circuit.

C86=L → i80 series CPU
C86=H → M68 series CPU

The i80/M68 series distinguish the data bus (D17-D0) conditions with the combinations of RS, /RD (E) and /WR (R/W) instruction as listed in Table 6-3 and 6-4.

RS	/RD (E)	/WR (R/W)	Function
H	L	H	Read display data
H	H	L	Write display data
L	L	H	Read registers
L	H	L	Write command

Table 6-3 i80series data bus selection

RS	/RD (E)	/WR (R/W)	Function
H	H	H	Read display data
H	H	L	Write display data
L	H	H	Read registers
L	H	L	Write command

Table 6-4 M68series data bus selection

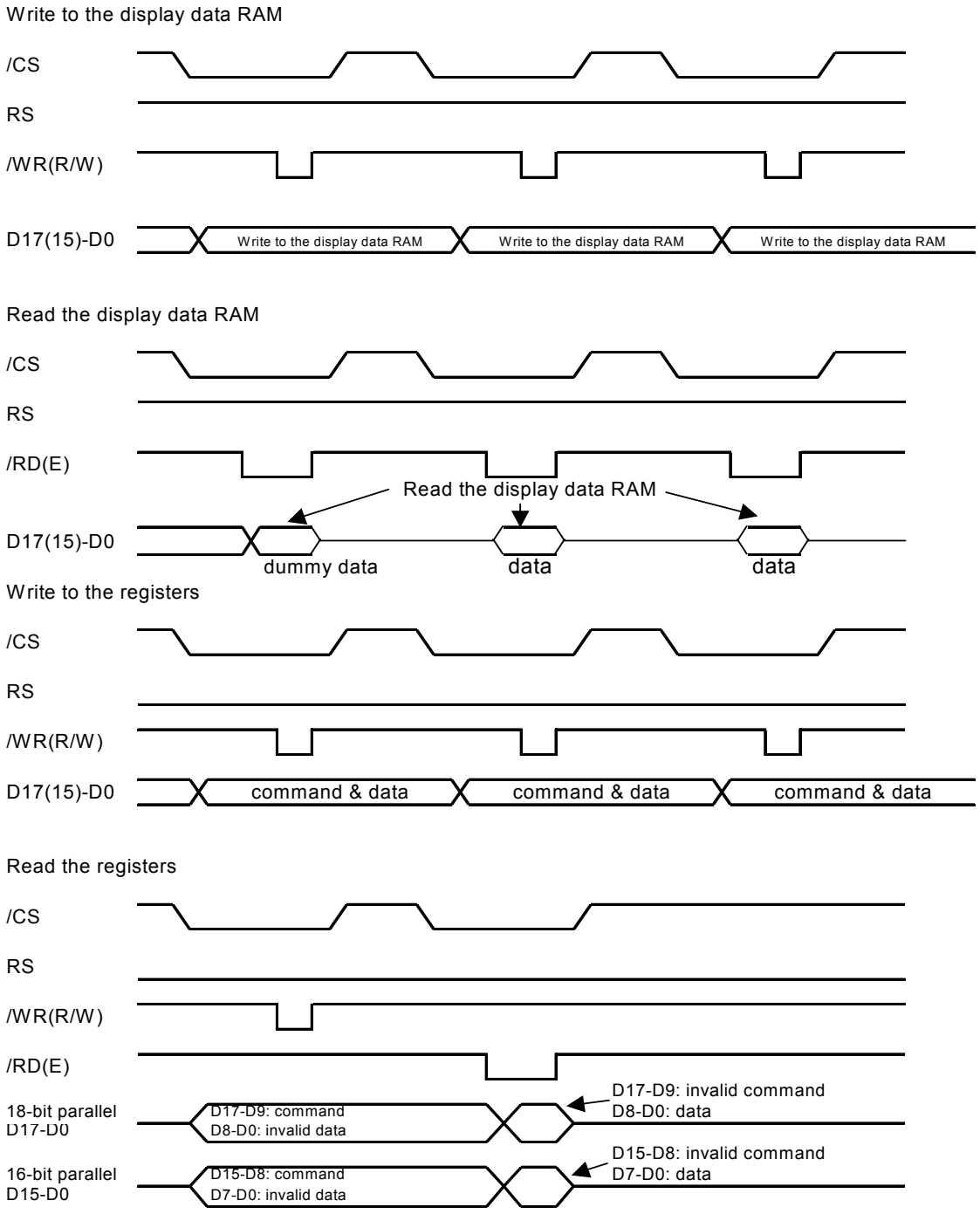


Fig. 6-1 18/16-bit parallel interface timing (for i80-series)

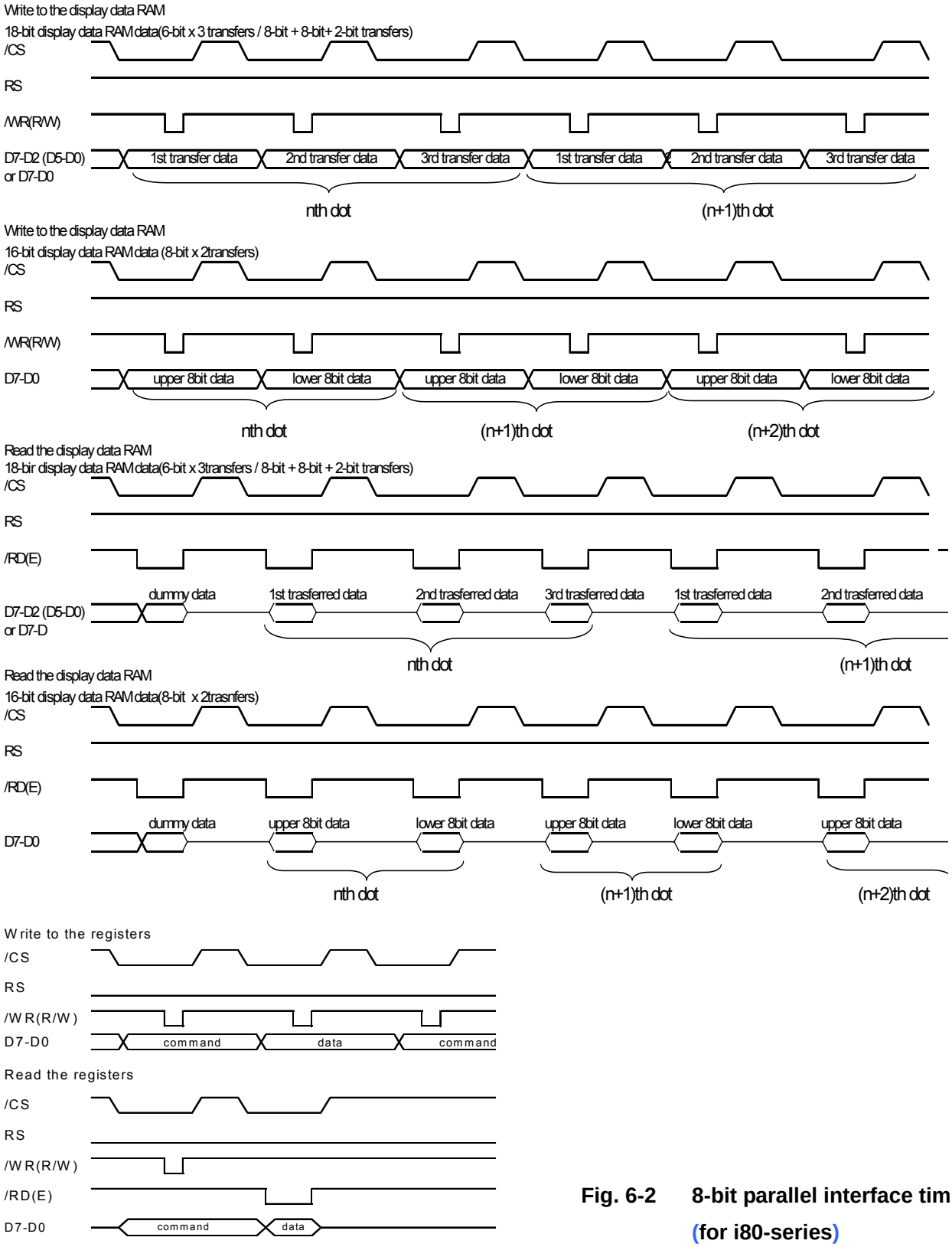


Fig. 6-2 8-bit parallel interface timing (for i80-series)

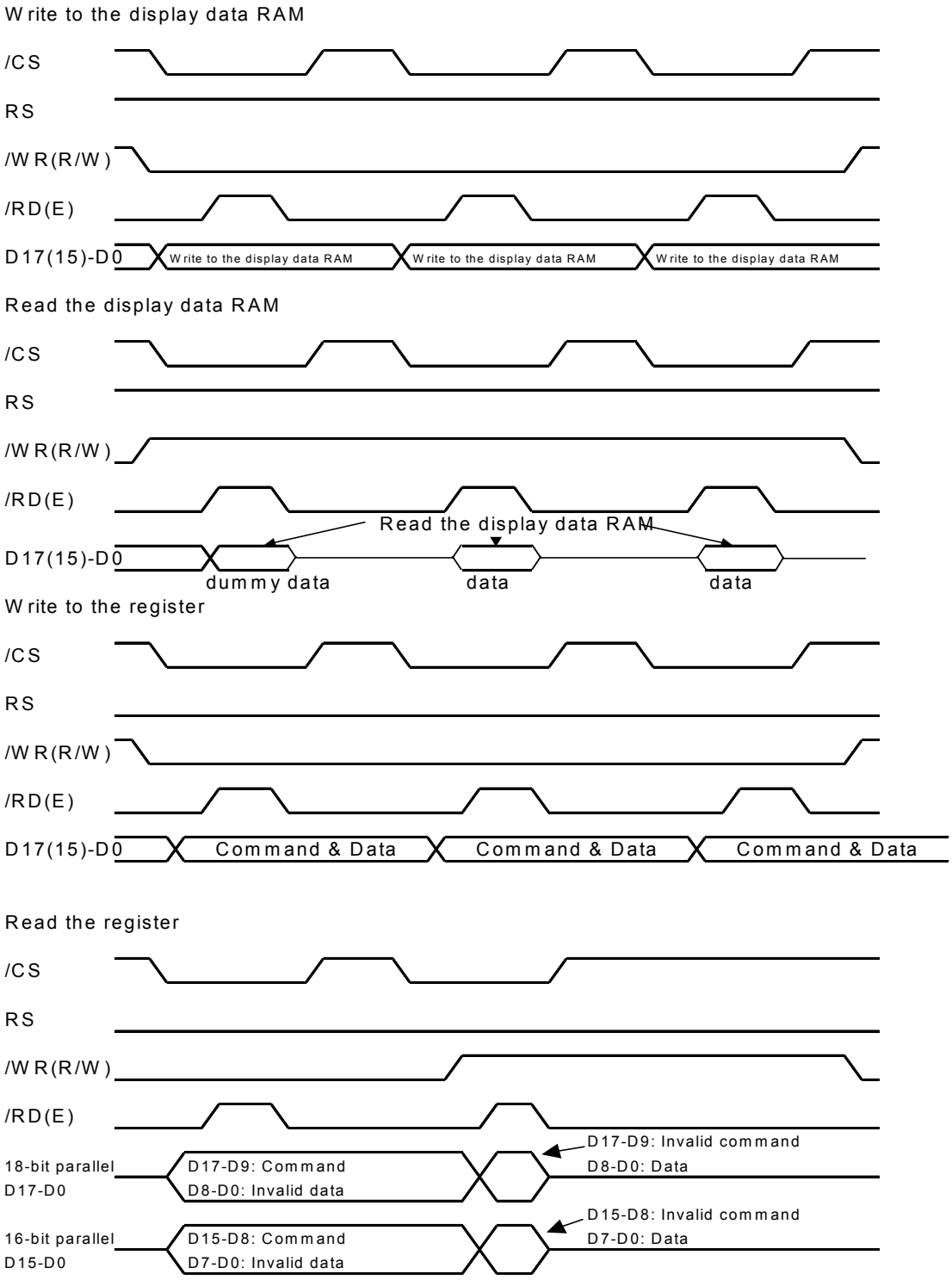


Fig. 6-3 18/16-bit parallel interface timing (for M68-series)

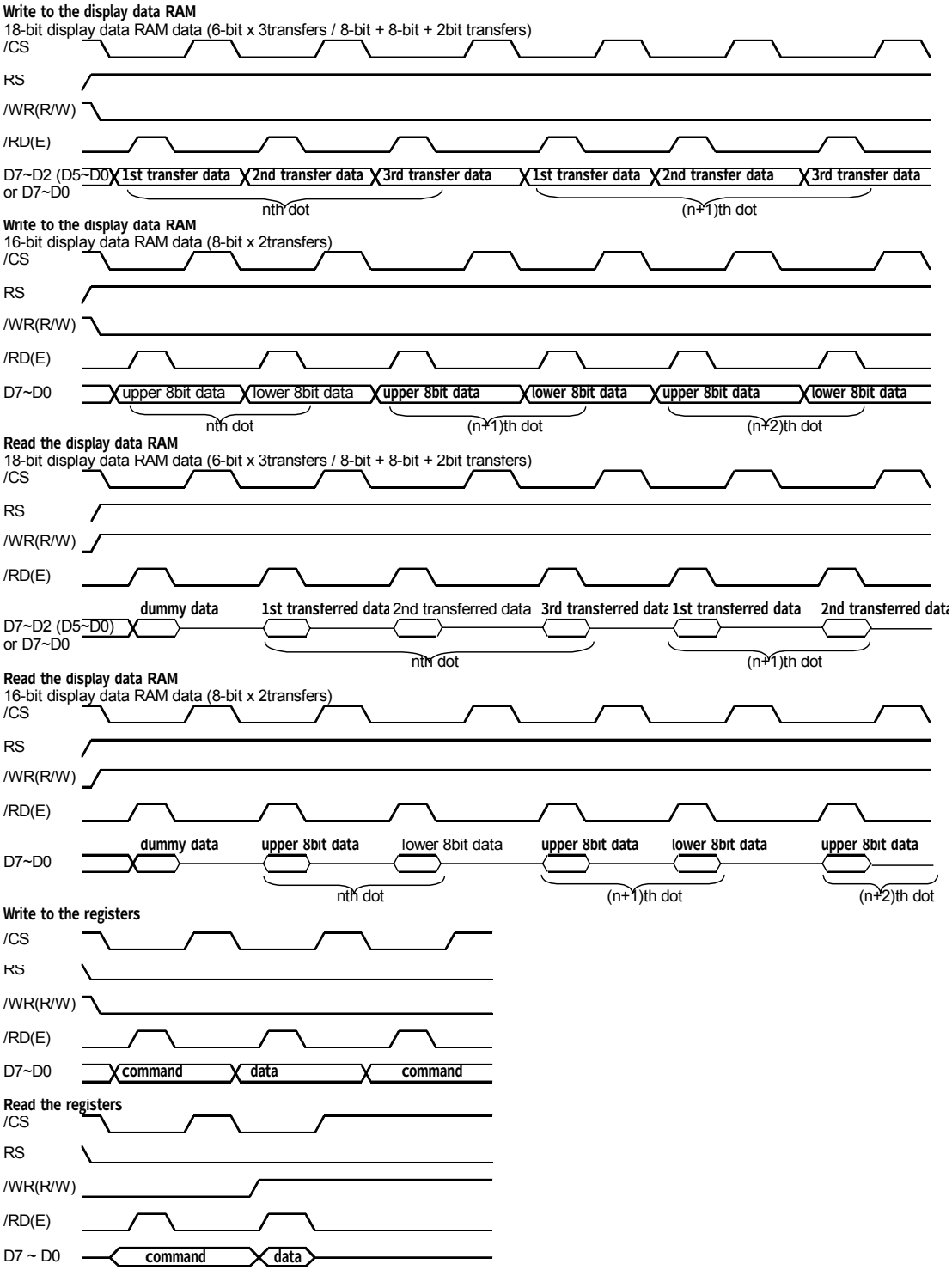


Fig. 6-4 8-bit parallel interface timing (for M68-series)

6.1.2. Serial interface circuit

When /CS=L, the IS2100 becomes active and can communicate with a serial interface circuit. Also, the serial data input (SI), the serial data output (SO), and the serial clock become on stand-by. The selection of read/write data operation is made with the R/W pin.

Please remember to finish this operation in 16-clock unit when the 8-bit serial interface circuit is in use, and in 18-clock unit when the 9-bit serial interface circuit is in use.

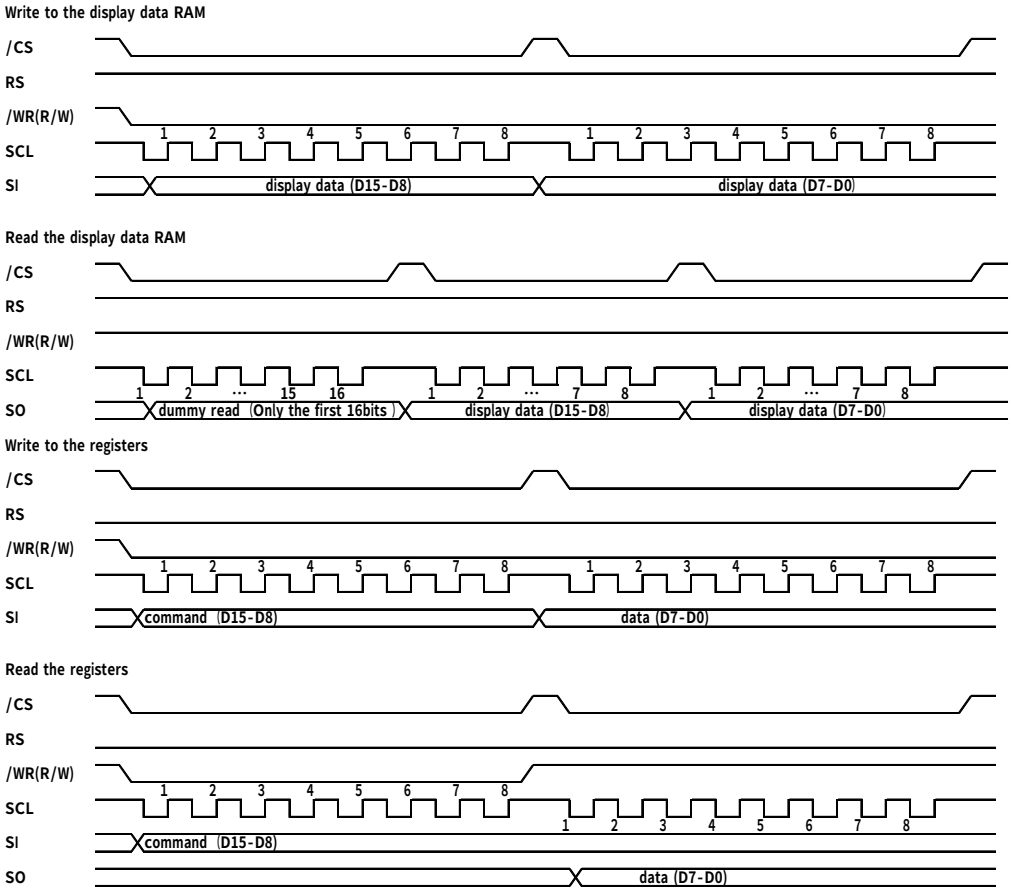


Fig. 6-5 8-bit serial interface timing (SCLEG1=SCLEG0=L)

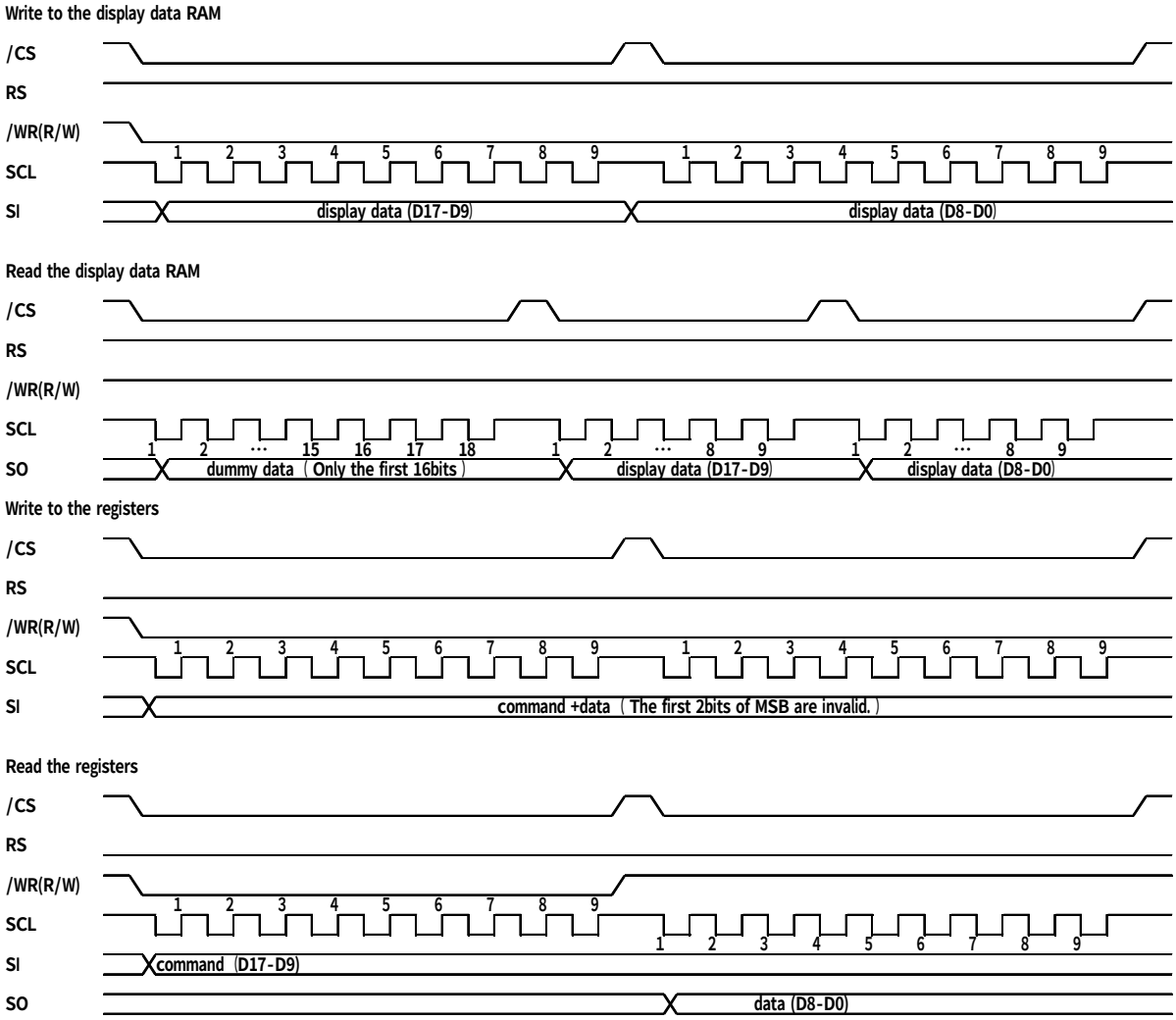


Fig. 6-6 9-bit serial interface timing (SCLEG1=SCLEG0=L)

The setting of the SCLEG1 and SCLEG0 pins specify an effective edge of the serial clock signal and I/O data, and an active level of the serial clock signal.

SCLEG1	SCLEG0	Active level of the serial clock	Latch timing of serial data	Output timing of serial data
L	L	Low level	Rising edge of the serial clock	Falling edge of the serial clock
L	H	Low level	Falling edge of the serial clock	Rising edge of the serial clock
H	L	High level	Falling edge of the serial clock	Rising edge of the serial clock
H	H	High level	Rising edge of the serial clock	Falling edge of the serial clock

Table 6-5 Relation between the serial clock and the serial data

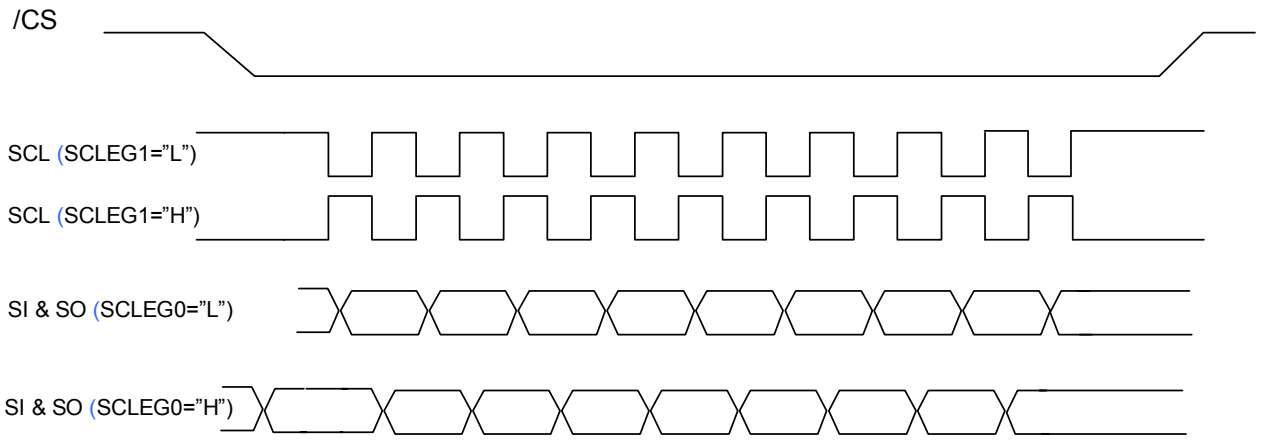


Fig.6-7 9-bit serial interface (example)

6.2. RGB Interface Circuit

The IS2100 incorporates the RGB interface circuit for reproducing animated displays. The IF_SHARE pin selects either L: sharing data pins (D17-D0) or R: using RGB pins (RGB25-00) as input for the RGB interface circuit

IF_SHARE pin	Description
L	The data pins aren't shared with the RGB pins. RGB25-RGB00 pins are used for the RGB interface circuit.
H	The data pins are used as the input to the RGB interface circuit.

Table 6-6 IF_SHARE pin set up

When the data pins are shared as inputs to the RGB interface circuit, bit allocations are applied as below.

Data bus	RGB bus
D17-D12	RGB25-RGB20
D11-D6	RGB15-RGB10
D5-D0	RGB05-RGB00

Table 6-7 Bit allocation at using for the RGB pins

When data pins are shared with input pins for the RGB interface circuit, RGB./CPU pin selects which circuit should be used for data pins.

- RGB./CPU =H: Data pins are used as inputs to the system interface circuit.
- RGB./CPU =L: Data pins are used as inputs to the RGB interface circuit.

The IS2100 has two interface modes as shown below when RGB interface is used.
You can choose the number of the data bits per dot by using the BWS2 pin. The 16-bit interface mode (BWS2=H) 65,536 colors display with expanding 16-bit data to 18-bit data as shown in Fig.6-8.

Interface type	Pin	Register	Interface mode	Number of the data per dot	Transferring method of 1 dot
	BWS2	MSBF (R157:D0)			
RGB1	L	L	18-bit	18-bit	18-bit corrective
RGB2	H	L	16-bit	16-bit	16-bit corrective

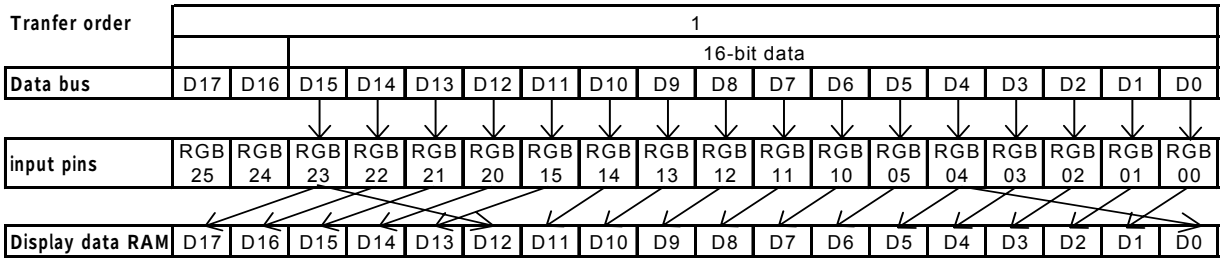


Fig.6-8 RGB2 type

6.3. Data Distinction

The RS pin specifies an access direction either to the registers or to the display data RAM.

RS	Input data
L	Command
H	Display data

Table 6-8 Distinction of input data

6.4. The Composition of the Register

The register consists of 16 bits. Upper 8 bits (D15-D8) are for the addresses and lower 8 bits (D7-D0) are for the data.

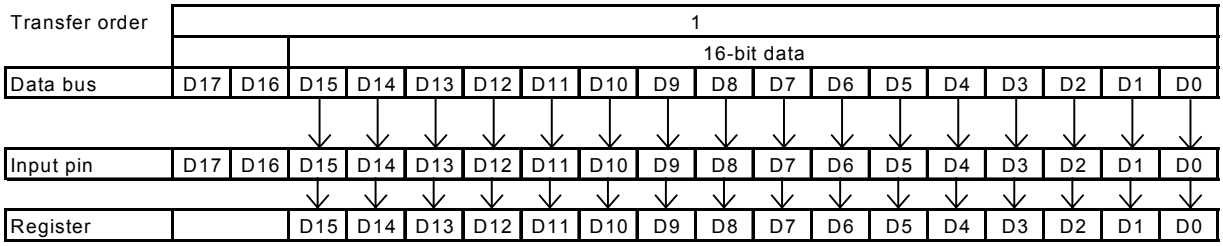
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Addresses								Data							

Table 6-9 The composition of the register

6.5. Relation between Bus Data and the Registers

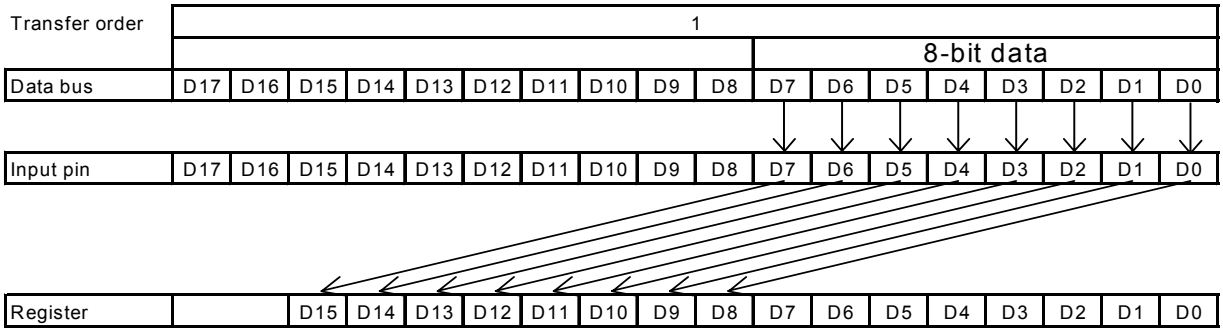
The following shows the display data allocation of each MPU type.

6.5.1. MPU1, MPU2, MPU3, MPU4 Type

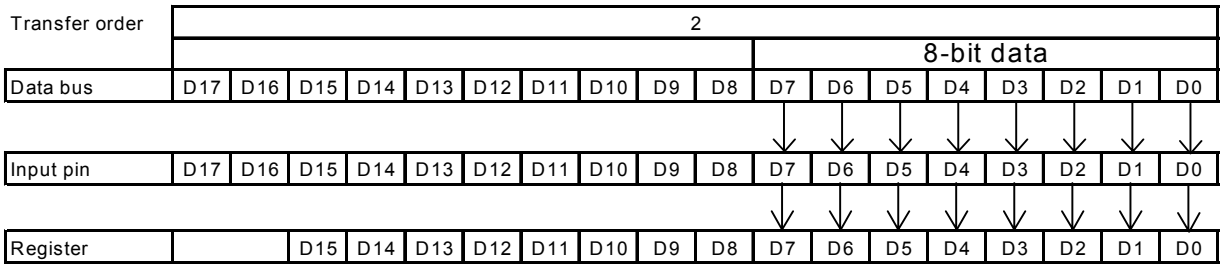


6.5.2. MPU5, MPU6, MPU7 Type

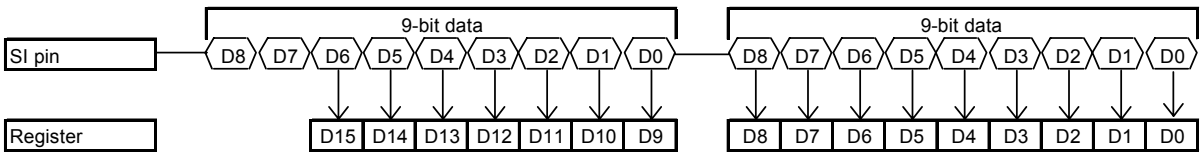
1st transfer



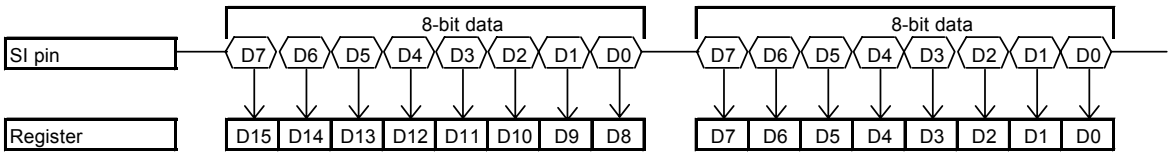
2nd transfer



6.5.3. MPU8 Type



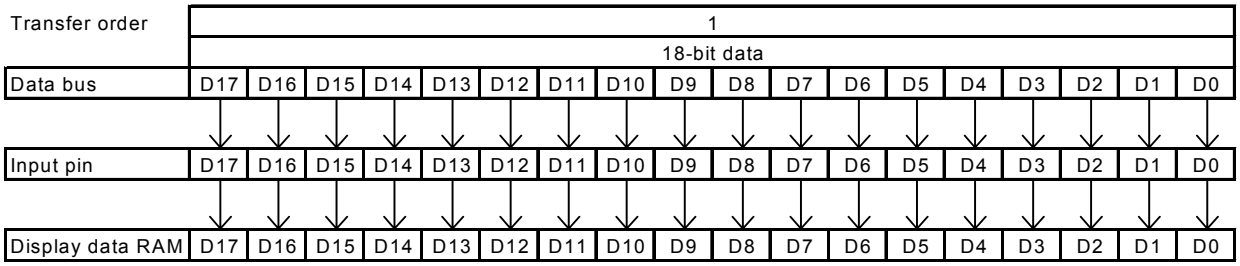
6.5.4. MPU9 Type



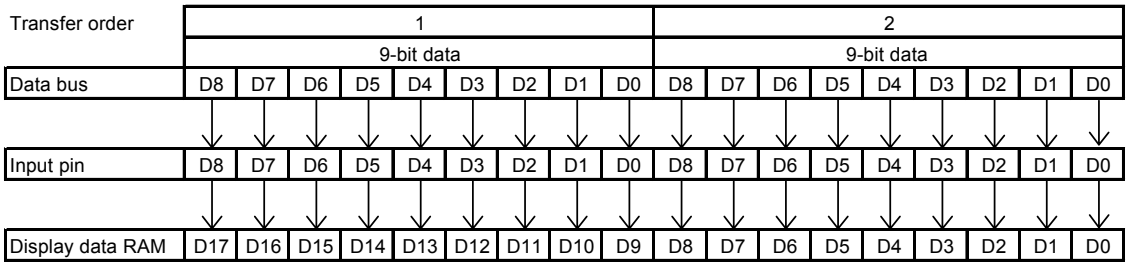
6.6. Relation between Bus Data and the Display Data RAM

The following shows the display data allocation of each MPU type.

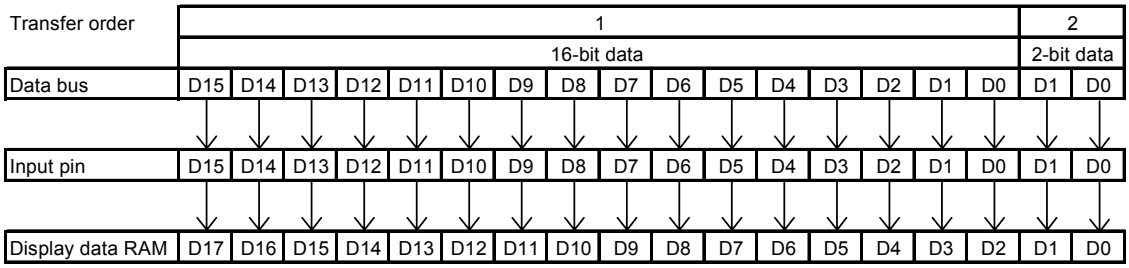
6.6.1. MPU1 Type



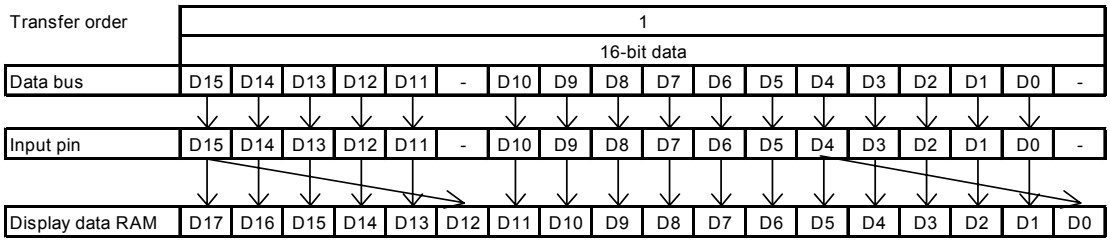
6.6.2 MPU2 Type



6.6.3. MPU3 Type



6.6.4. MPU4 Type

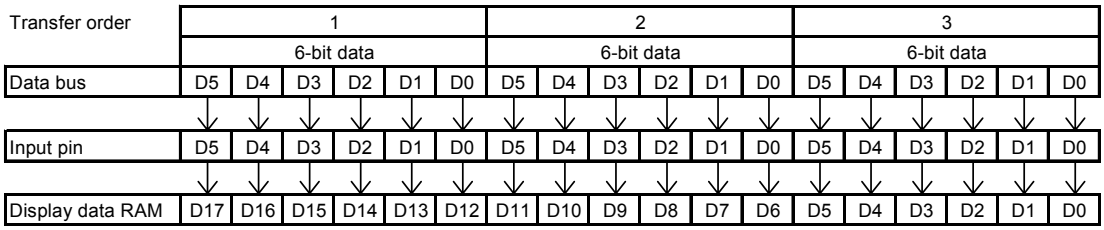


D12 of the display data RAM is compensated by the data from D15, and D0 of the display data RAM is compensated by the data from D4. (The 16-bit data is expanded to 18-bit data.)

6.6.5. MPU5 Type

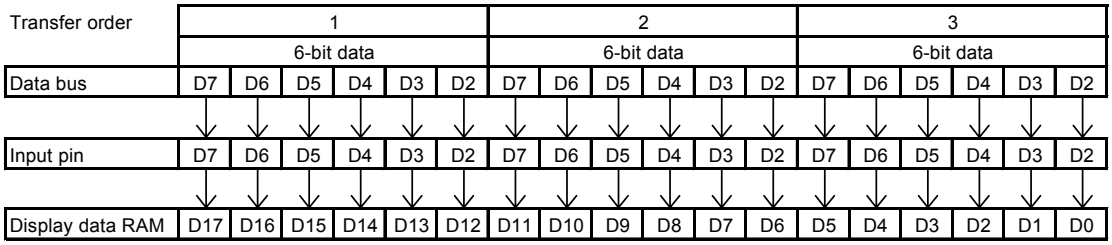
MPU5 type can change the location of invalid bits according to the MSBF configuration of R157 register.

MPU5 type A (MSBF=0)



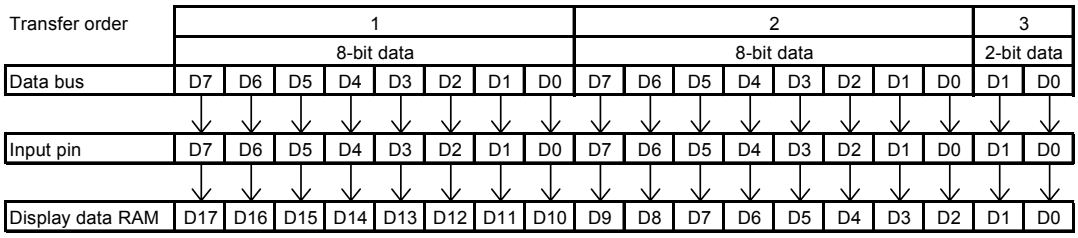
Data D7 and D6 are invalid.

MPU5 type B (MSBF=1)

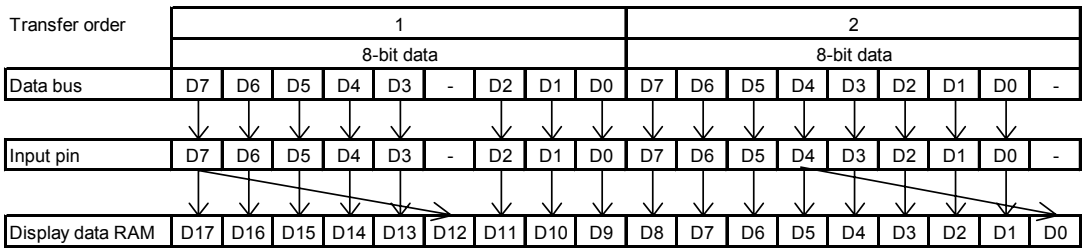


Data D1 and D0 are invalid.

6.6.6. MPU6 Type

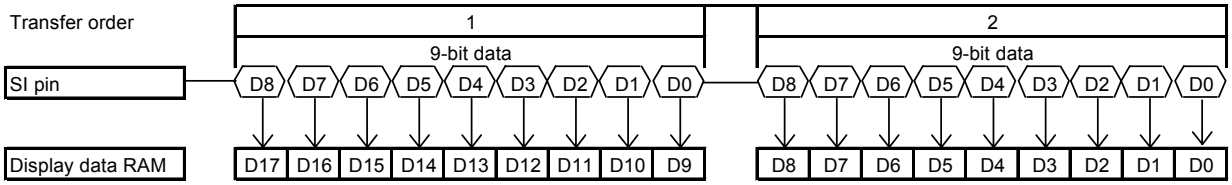


6.6.7. MPU7 Type

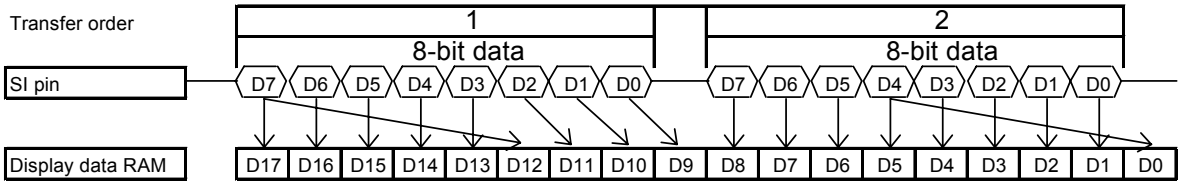


D12 of the display data RAM is compensated by the data from D7 in the first transfer, and D0 of the display data RAM is compensated by the data from D4 in the second transfer. (The 16-bit data is expanded to 18-bit data.)

6.6.8. MPU8 Type



6.6.9. MPU9 Type



D12 of the display data RAM is compensated by the data from D7 in the first transfer, and D0 of the display data RAM is compensated by the data from D4 in the second transfer.
(The 16-bit data is expanded to 18-bit data.)

(Special Note) Switching between the MPU4 and the MPU2 types

We assure the proper switching operation as long as the following program is performed.

Initialize
Set “MPU2 MODE”
Write to the display data RAM

390nS

Set “MPU4 MODE” (switching from MPU2 to MPU4)
R6 X register setting
R7 X register setting
Write to the display data RAM

390nS
Set ”MPU2 MODE” (switching from MPU4 to MPU2)
Set R6 X register
Set R7 X register
Write to the display data RAM

6.7. Serial Interface for Sub-LCD

When /BLCS_I=L, the sub-LCD panel function is valid. The serially transferred date from the MPU can be sent to the sub-LCD module via the IS2100. The interfaces for the IS2100 and the MPU require the setting of SCLEG1 and SCLEG0 as listed in Table 6-5. When /BLCS is L, the clock signal of falling edge has priority and outputted from BLSCL, regardless of the SCLEG1/SCLEG0 setting of the IS2100's SCL and the specification of falling/rising edge. Data will be outputted in synchronization with this falling edge.

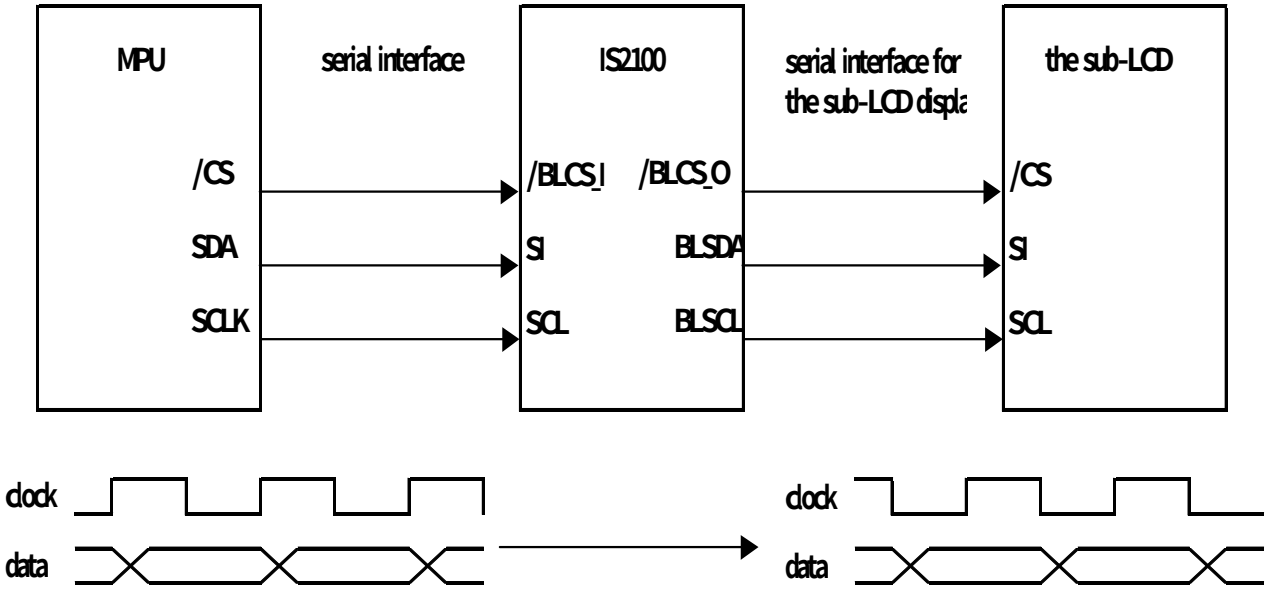


Fig. 6-9 An image of the sub-LCD display

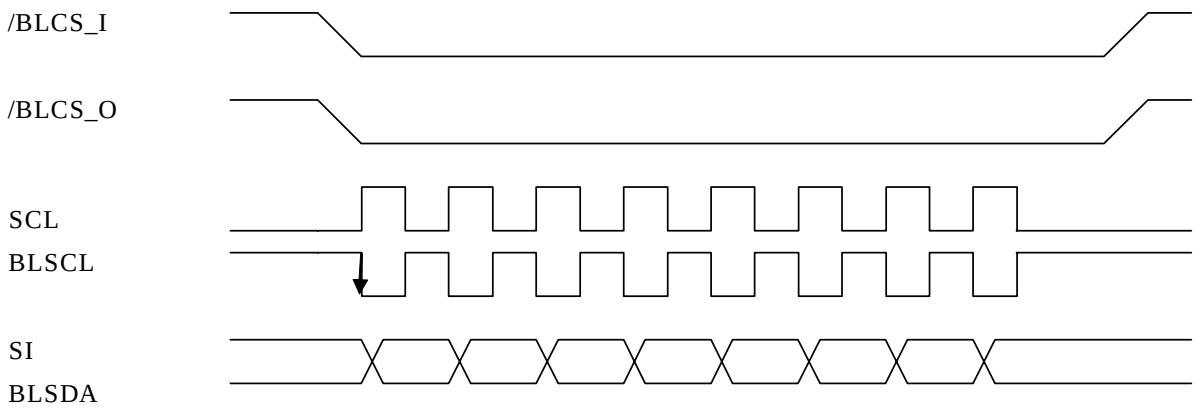


Fig. 6-10 The 8-bit serial operation

Note1: When the sub-LCD serial interface is in use, the system interface circuit can only communicate through the parallel interface.

Note 2: When the serial clock is inputted, please do not repeatedly switch the chip select pin (/BLCS_I) between active and inactive.

Note 3: While transferring data, please make sure to set the chip select pin (/BLCS_I) as inactive at every transfer (every 8bits or 9 bits).

7. Access to the Display Data RAM

7.1. X Address of the Display Data RAM and Reading/Writing of the Display Data RAM

The IS2100 has an internal 18-bit bus RAM for 176RGBX240-dot displays. You can access the arbitrary address by specifying X and Y addresses. One address of X address equals to one dot.

Bit	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Dot allocation	Pixel 1						Pixel 2						Pixel 3					
	1 dot																	

Table 7-1 Bit configuration of the display RAM

Setting the RS pin as H enables the access from the data bus to the display data RAM. The display data RAM data will be written at the X and Y addresses which are specified by the R6 and R7 registers. Every time the IS2100 operates writing/reading of the display data, the X address increases up to 175. When the X address reaches 175, it restarts down from 0, while the Y address increases. Also when the Y address reaches 239, it restarts down from 0. You can select the address increment direction, either from X or Y, by using the D2=INC bit of the R5 register.

*Note: Provided that this setting is prohibited when RGB interface circuit is in use.

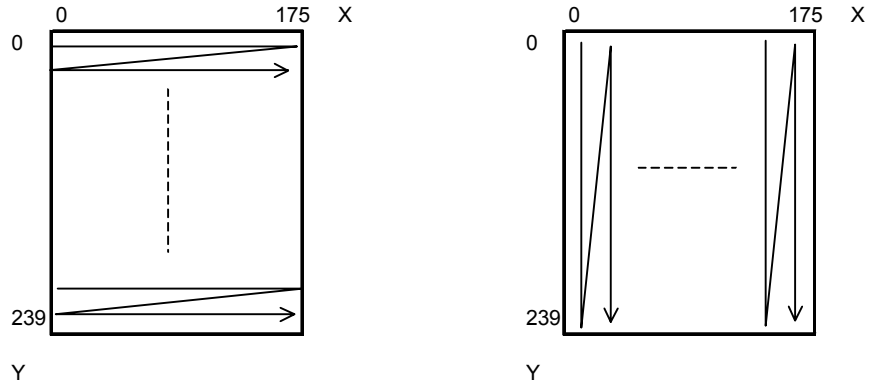


Fig. 7-1 The address increment direction

D7=ADX and D6=ADR of R1 register decides the addressing direction of X and Y.

ADX=0: X0→X175 ADR=0: Y0→Y239

ADX=1: X175→X0 ADR=1: Y239→Y0

This operation is prohibited when the RGB interface circuit is in use.

(Only the setting of ADX=ADR=0 is available in case that the RGB interface circuit is used.)

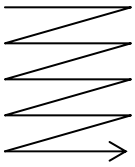
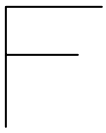
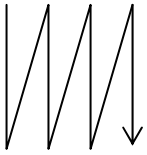
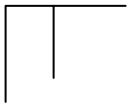
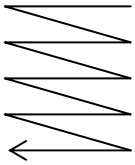
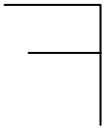
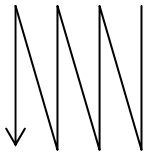
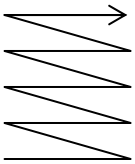
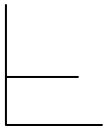
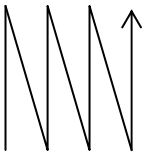
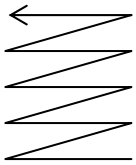
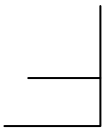
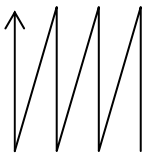
	INC=0		INC=1	
	Address increment direction	Display image	Address increment direction	Display image
ADX=0 ADR=0				
ADX=1 ADR=0				
ADX=0 ADR=1				
ADX=1 ADR=1				

Fig.7-2 The memory increment and display images

Setting the start-address when writing to the RAM

1. When the data access control register (R5) is D4=WAS=0. (Normal writing mode)

ADX	ADR	R6 value	R7 value
0	0	0	0
0	1	0	EFH
1	0	AFH	0
1	1	AFH	EFH

2. When the data access control register (R5) is D4=WAS=1. (Window access mode)

ADX	ADR	R6 value	R7 value	
0	0	XMIN	YMIN	XMIN: The value set in the R8 register
0	1	XMIN	YMAX	XMAX: The value set in the R9 register
1	0	XMAX	YMIN	YMIN: The value set in the R10 register
1	1	XMAX	YMAX	YMAX: the value set in the R11register

7.2. Relation between X address of the Display Data RAM and the LCD panel

Table 7-2 shows the relation between the display data RAM and the LCD panel. By setting D5=ADC of the control register (R0) as 1, the relation between the LCD panel and the display data RAM address changes. In order to display pictures in reverse when D5=ADC of the control register (R0) is set as 1, the display data in the display data RAM should be written in reverse.

ADX=0														
Source output	ADC=0	Y1	Y2	Y3	Y4	Y5	Y6	--------	Y523	Y524	Y525	Y526	Y527	Y528
	ADC=1	Y528	Y527	Y526	Y525	Y524	Y523	--------	Y6	Y5	Y4	Y3	Y2	Y1
X address		00H			01H			--------	AEH			AFH		
Bit allocation		17-12	11-6	5-0	17-12	11-6	5-0	--------	17-12	11-6	5-0	17-12	11-6	5-0
Dot		Dot 1			Dot 2				Dot 175			Dot 176		

ADX=1														
Source Output	ADC=0	Y1	Y2	Y3	Y4	Y5	Y6	--------	Y523	Y524	Y525	Y526	Y527	Y528
	ADC=1	Y528	Y527	Y526	Y525	Y524	Y523	--------	Y6	Y5	Y4	Y3	Y2	Y1
X address		AFH			AEH			--------	01H			00H		
Bit allocation		17-12	11-6	5-0	17-12	11-6	5-0	--------	17-12	11-6	5-0	17-12	11-6	5-0
Dot		Dot 1			Dot 2				Dot 175			Dot 176		

Table 7-2: The relation between the Display Data RAM and the LCD panel

7.3. Arbitrary Address Area Access (Window Access Mode)

You can access the rectangular area that is formed by a diagonal line of the two Display Data RAM arbitrary points, with one point as the start point and the other as the end point. The start point is specified by the R8 and R10 registers. The end point is specified by the R9 and R11 registers. By setting D4=WAS of the register as 1, this arbitrary address area access will be available. The window access mode is active when R2: D0=NWRGB=1 despite of this D4=WAS setting. You can either specify the rectangular area first or set the D4=WAS of the R5 register first to start the window access mode.

In this mode, an address scanning is also valid as well as in the usual writing mode. Also by specifying the R6 and R7 registers, it is possible to write data from the arbitrary address. Please be sure to set the address for the R6 and R7 registers within the rectangular area. This function can be used in both of usual access and the high-speed RAM-write modes.

*Note: R6 and R7 are prohibited to use when RGB interface is in use.

Address	Address relation
X address	00H≦MIN X address ≦X address ≦MAX X address ≦AFH
Y address	00H≦MIN Y address ≦Y address ≦ MAX Y address ≦EFH

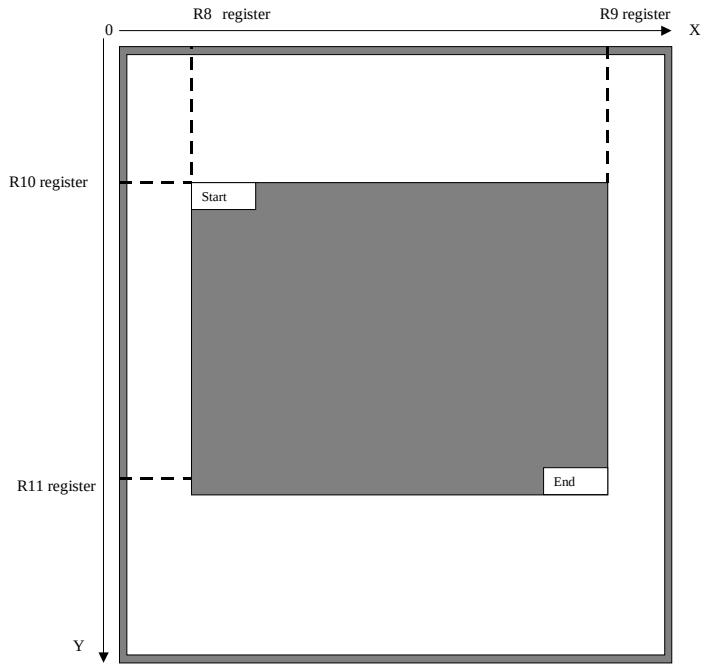


Fig. 7-3 The address of the arbitrary address area access

7.4. High-speed RAM-Write Mode (Burst Transfer Mode)

The IS2100 has two ways to access the display data RAM. In addition to the standard display data RAM-write mode, the IS2100 has a high-speed RAM-write mode. The speed of the high-speed RAM-write mode is twice as fast as that of the standard display data RAM-write mode. This mode is especially suited for applications, which require the high-speed rewriting of the display data, such as display of color- animations, etc.

By setting D6=BSTR of the data access control register (R5) as 1, this high-speed RAM-write mode become available. When the high-speed RAM-write mode is selected, the data for two dots, which equals to 36 bits for writing to the display data RAM, is once stored to the IS2100 internal register (if the data is 16 bits per dot, the 16-bit data will be expanded to 18-bit data.) and then is sent to the display data RAM. In this way, the IS2100 achieves to double the speed of the standard RAM-write mode. However, if the data length falls short of less than 2 dots, they will not be sent to the display data RAM. So please be sure to send data per two dots. This high-speed RAM-write mode has restrictions for specifying those addressed listed below.

Register	Register name	Restrictions
R5	Data access control register D2= INC	Only 0 is valid
R6	X address register	2n-2(n=1 - 88)

Register	Register name	Restrictions
R8	MIN X address register	2n-2(n=1 - 88)
R9	MAX X address register	

Table 7-3 Address setting restrictions at the high-speed RAM-write

(Note)

(ADC=1, ADX=1), (ADC=0, ADX=0): Valid

(ADC=1, ADX=0), (ADC=0, ADX=1): Prohibited to use

8. Input and Synchronization Display Mode

The IS2100 has two writing modes to write display data to the display data RAM via the RGB interface circuit as listed below.

(1) The capture mode is a mode in which display data is written to the display data RAM and the data from the display data RAM is displayed.

(2) The override mode is a mode in which RGB pins are not available to input display data. The system interface circuit will be used to input display data.

Also the IS2100 has two synchronization display mode as listed below,

(1) The internal synchronization display mode that is synchronized with the internal clock and shows displays.

(2) The externally synchronization display mode that is synchronized with the vertical synchronization signal (Vsync) and the horizontal synchronization signal (Hsync), and shows displays.

To select one of these modes, set D2=RGBS, D1=DISPCK, D0=NWRGB of the RGB control register (R2).

Table 8-1 shows the combinations of these modes. When switching modes, IS2100 can display correct pictures only after finish displaying the present frame.

R2 register			RGB mode	Data Input pin	Used Interface circuit	Signal used to write to the display data RAM	Display data RAM -> Display	
D2	D1	D0						
RGBS	DISPCK	NWRGB					Mode name	Signal used to display
0	1	1	Capture mode	RGBx5-x0 /D17-D0 (*1)	RGB interface circuit	Vsync, Hsync Dotclk	Externally synchronized display mode	Vsync, Hsync, Dotclk
							Refer t o “8.1.1.”	
0	0	1	Capture mode	RGBx5-x0 /D17-D0 (*1)	RGB interface circuit	Vsync, Hsync Dotclk	Internally synchronized display mode	SYSCLK (*2)
							Refer to “8.1.2.”	
1	0	0	Override RGB mode	D17~D0	System interface circuit	/CS, /RD (E), /WR (RW) (*3)	Internally synchronized display mode	SYSCLK (*2)
							Refer to “8.1.3.”	
1	1	0	Override RGB mode	D17~D0	System interface circuit	/ CS, /RD (E), /WR (RW) (*3)	Externally synchronized display mode	Vsync, Hsync, Dotclk
							Refer to “8.1.4.”	

Table 8-1 Display mode set up

*1: By setting IF_SHARE and RGB. /CPU pins, D17-D0 can be used for the data input pins.

*2: SYSCLK: a system clock signal inputted via the SYSCLK pin.

*3: Serial interface pins are also available.

8.1. The operation of the RGB Interface

By setting D0=NWRGB of the RGB interface register (R2) as 1, the IS2100 can write the display data from the RGB interfaced circuit to the display data RAM. When the RGB interface circuit is in use, the IS2100 takes in the display data synchronized with the vertical synchronization signal (Vsync), the horizontal synchronization signal (Hsync), and the dot clock (Dotclk) from the RGB bus (RGB25-RGB00) or the data bus (D17-D0), and then writes to the display data RAM.

8.1.1. Externally synchronized display mode + capture mode

By setting D2, D1 and D0 of the RGB interface register (R2) as “011”, the IS2100 enters “externally synchronized display mode + capture mode”. In this mode, display data is written to the display data RAM first and then displayed in synchronization with Vsync, Hsync and Dotclk by reading the display data from the display data RAM in the same frame. The area you can capture is defined by the window access mode.

The data of other areas, which are not included in the window access area, is not updated in this mode so the same data is displayed in those areas.

D0=NWRGB of the RGB interface register (R2) must be set as “0” when needing to update display data of the areas which are not specified by the window access mode. Also the display data must be inputted via the system interface pins. See “6. Interface” section for more information.

In this mode, the blanking period is defined with the RGB back porch register (R62). D7-4=HBP3-0 of the RGB back porch register (R62) specifies the horizontal back porch period, and D3-0=VBP3-0 of the RGB back porch register (R62) specifies the vertical back porch period. See also Fig.8-1.

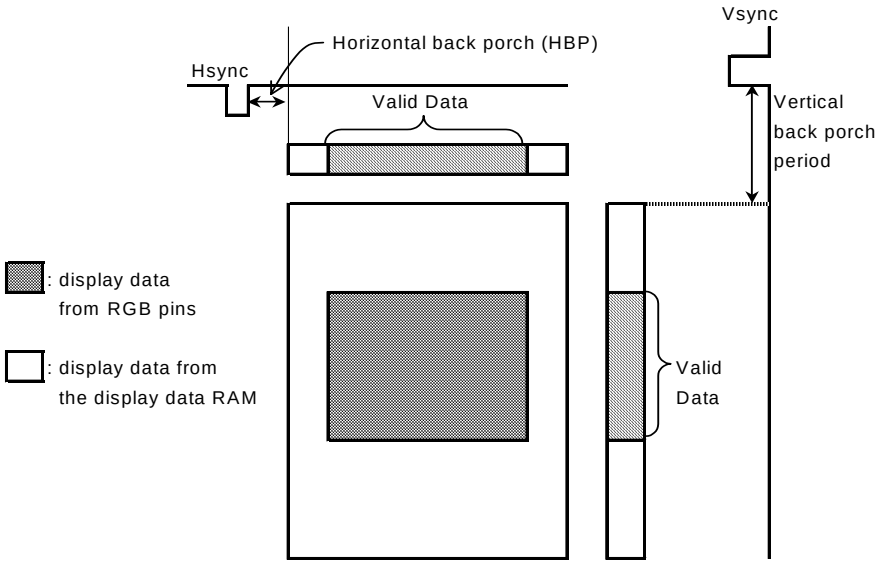


Fig. 8-1 An example of “externally synchronized display mode + capture mode”

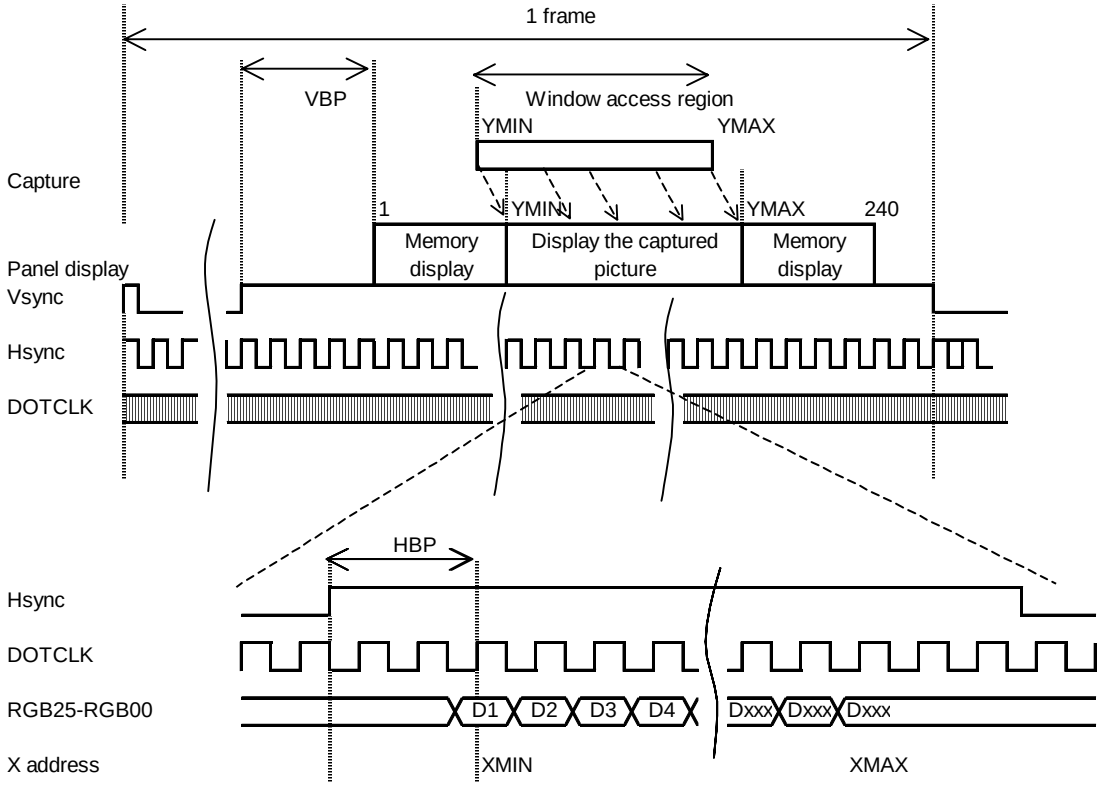


Fig. 8-2 Timing generation of “externally synchronized display mode + capture mode”

8.1.2. Internally synchronized display mode + capture mode

By setting D2, D1 and D0 of the RGB interface register (R2) as “001”, the IS2102 enters “internally synchronized display mode + capture mode”. In this mode, display data is written to the display data RAM first and then displayed by reading the data from the display data RAM. Write operation is performed in synchronization with Vsync, Hsync and Dotclk. On the other hand, display operation is performed in synchronization with SYSCLK (a system clock signal inputted via the SYSCLK pin). The area you can capture is defined by the window access mode. The data of other areas, which are not included in the window access area is not updated in this mode, so the same data is displayed in those areas.

D0=NWRGB of the RGB interface register (R2) must be set as “0” in order to update display data of the areas which are not specified by the window access mode. Also the display data must be inputted via the system interface pins. See “6 Interface” section for more information.

In this mode, 1H period must be defined by SYSCLK instead of Hsync. Please refer to “8.2. Horizontal Raster-Row Cycle Adjustment in the Internally Synchronized Display Mode”.

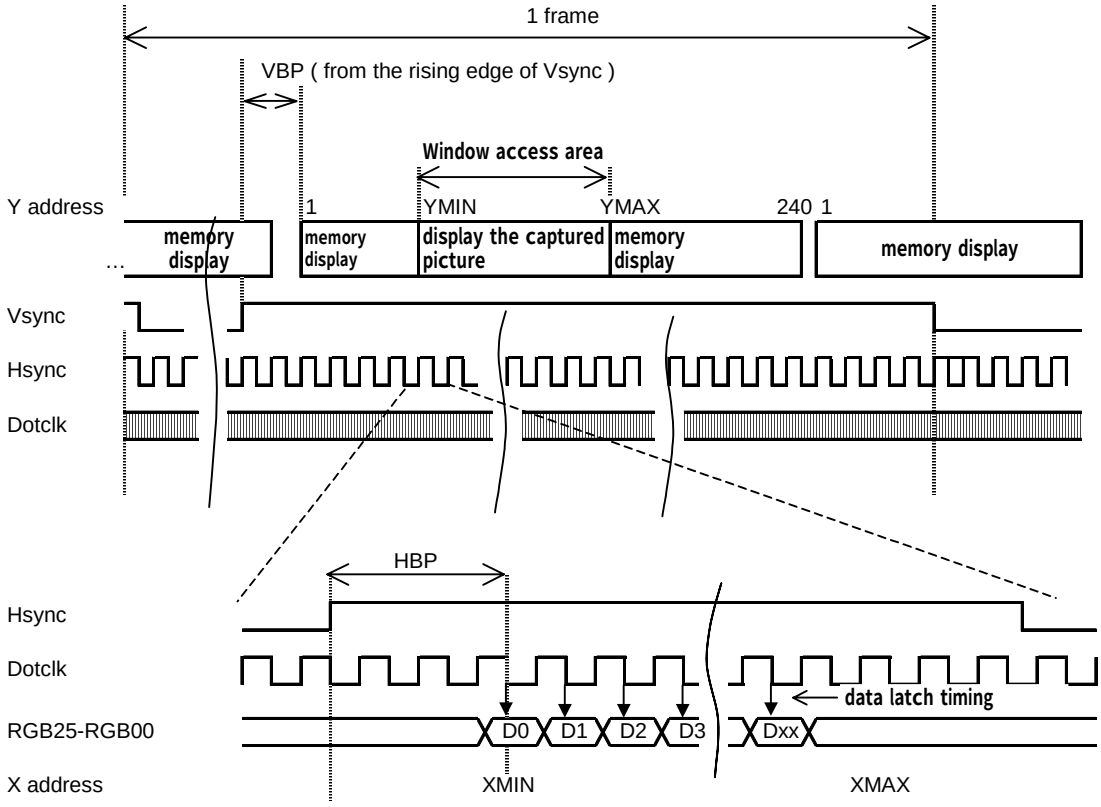


Fig. 8-3 Timing generation of internal synchronize mode + capture mode

8.1.3. Internally synchronized display mode + override RGB mode

By setting D2, D1 and D0 of the RGB interface register (R2) as “x00” (x: 0 or 1), the IS2102 enters “internally synchronized display mode + override RGB mode”. In this mode, display data is inputted via data pins (D17-D0) or serial interface pins, not via RGB pins. The system interface circuit is used to write display data to the display data RAM. But display operation is performed in synchronization with SYSCLK (a system clock signal inputted via the SYSCLK pin).

In this mode, 1H period must be defined using SYSCLK. Please refer to “8.2. Horizontal Raster-Row Cycle Adjustment in the Internally Synchronized Display Mode”.

8.1.4. Externally synchronized display mode + override RGB mode

By setting D2, D1 and D0 of the RGB interface register (R2) as “x10” (x: 0 or 1), the IS2102 enters “Externally synchronized display mode + override RGB mode”. In this mode, display data is inputted via data pins (D17-D0) or serial interface pins, not via RGB pins. The system interface circuit is used to write display data to the display data RAM. Display operation is performed in synchronization with Vsync, Hsync and Dotclk. In this mode, the blanking period is defined with the RGB back porch register (R62). D7-4=HBP3-0 of the RGB back porch register (R62) specifies the horizontal back porch period, and D3-0=VBP3-0 of the RGB back porch register (R62) specifies the vertical back porch period. See also Fig.8-1.

8.1.5. Restrictions on RGB

When the capture mode is in use, constant Dotclk supply is need and data input is required for each frame cycle. In the internal synchronization mode, however, the IS2100 rewrite the reserved area, which is defined in the window access mode, by setting D3=WNRGB of the register R2 as 1,

8.2. Horizontal Raster-Row Cycle Adjustment in The Internally Synchronized Display Mode

The IS2100 receives SYSCLK from the IS2200. The clock number of SYSCLK defines the horizontal raster-row cycle in the internally synchronized display mode. The horizontal raster-row cycle can be adjusted by two ways. One is by calibration and the other is by setting the clock number of one horizontal period in the register. This horizontal cycle adjustment is done by D0=CLKM of the raster-row cycle control mode register (R141).

Raster-row cycle control mode register R141

D0=CLKM	Configuration
L	Calibration
H	Register set up

Fig. 8-4 Line frequency set up

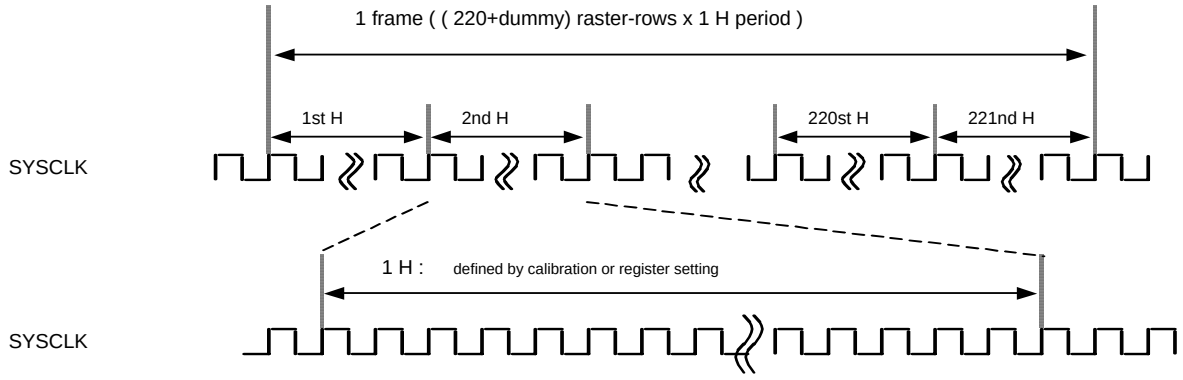


Fig.8-5 Timing of internal clock mode with IS2200 (220-raster-row mode)

8.2.1. Horizontal raster-row cycle adjustment by calibration

By setting D0=OC of the calibration register (R45) as 0, calibration will start. The calibration starts from the first positive edge of SYSCLK after D0=OC is set. The IS2100 counts the number of positive edges of SYSCLK (tcal) until D0=OC becomes 1. Then the IS2100 writes the number of positive edges of SYSCLK in the raster-row clock register (R139). When D1=LTS of the control register 2 (R1) is 1, the IS2100 sets double the number of the counted positive edges (tcal).

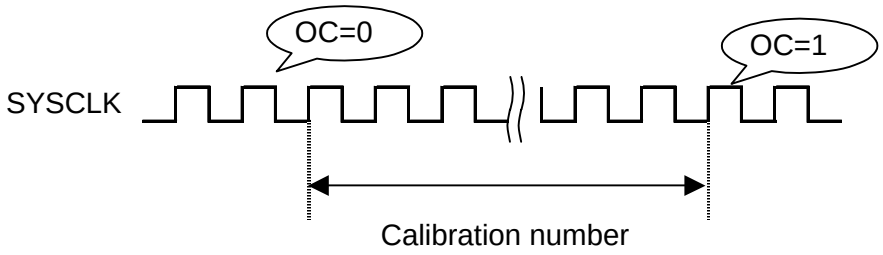


Fig. 8-6 Calibration (220 raster-row mode)

8.2.2. Horizontal raster-row cycle adjustment by register set-up.

First you need to specify the target frame frequency that drives the LCD (60 Hz normally.)

Next using the formula below, calculate the integer of HCK, which is close to the target frame frequency.

SYSCLK: System clock frequency (the clock frequency supplied from the IS2200)

HCK: Raster-row clock number which will be set in the raster-row clock register

GL+1: Gate drive number (220/240) + 1 (dummy output)

e.g. Target frame frequency=60Hz: SYSCLK= 600KHz: GL=220

600KHz÷(HCK＋1)÷(220＋1)=60Hz HCK=45.2

Please determine the figure around HCK=45 while looking at the LCD panel.

*Note: HCK setting is invalid without setting CLKM=1, therefore the default setting of HCK=25H stays effective.

The IS2100 sends the clock to the IS2100 and the clock frequency accuracy is between -40% and +30%. If the accurate horizontal cycle is needed in the internally synchronized display mode, please use the calibration function.

9. Display Operation

IS2100 can control the step-up time to the panel shown below.

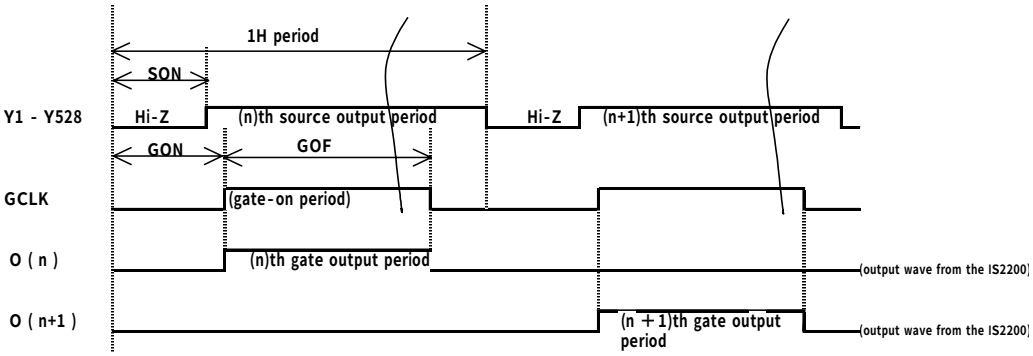


Fig. 9-1 Horizontal timing

9.1. Control Registers for Source Lines/Gate Raster-rows

9.1.1. Source on register (R136)

D7	D6	D5	D4	D3	D2	D1	D0
SON7	SON6	SON5	SON4	SON3	SON2	SON1	SON0

The clock number of SYSCLK defines SON.

Set up the timing to start the source output.

Configuration is prohibited on 00H-01H.

The source output shuts off automatically after 1H. After SON process, it switches to the source output of the next raster-row.

9.1.2. Gate-on register (R137)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
GON7	GON6	GON5	GON4	GON3	GON2	GON1	GON0

The clock number of SYSCLK defines GON.

Set up the timing to turn on the gate line.

Configuration is prohibited on 00H-02H.

In addition, the configuration on 00H-04H is prohibited in the skip1C mode.

And the configuration on 00H-05H is prohibited in the skip2B mode.

9.1.3. Raster-row cycle adjusting mode register (R141)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
GOF6	GOF5	GOF4	GOF3	GOF2	GOF1	GOF0	CLKM

The clock number of SYSCLK defines GOF.

Set up the period of the gate raster-row being on.

R137, R141 setting restrictions

(GON+GOF)=<(HCK-2)

9.2. All 0/1 Display

IS2102 can display 0 or 1 data on the whole screen in spite of the data in the display data RAM by the setting of D7=DISP1 or D6=DISP0 of the control register1 (R0).

(The data in the display data RAM is retained.)

Control resiter 1 (R0)

D7	D6	D5	D4	D3	D2	D1	D0
DISP1	DISP0	ADC	DTY	STBY	COLOR		GSM

DISP1	DISP0	Display
0	0	display the data from display data RAM
0	1	display "0" regardless of the data in display data RAM
1	0	display "1" regardless of the data in display data RAM
1	1	display "1" regardless of the data in display data RAM

9.3. Stop Gate Scanning

You can stop gate scanning by setting D0=GOE1ON of the GOE 1 output control register (R59) as “0”. In this case, all gate scans will be stopped. However, the frame frequency doesn’t change.

GOE 1 output control register (R59)

D7	D6	D5	D4	D3	D2	D1	D0
							GOE1ON

10. Display Control

10.1. Power-on Sequence

For the power supply configuration of the IS2200, please refer to the IS2200 specification.

10.2. Stand-by Sequence

The IS2100 goes into stand-by mode by D3=STBY of the control register (R0) and D0=OSCSTBY of the control register2 (R1). Contents of the display data RAM and all registers will be reserved in this stand-by mode.

When the STBY is set as 1, the source output (Y1-Y528) is fixed to VSS. After scanning the frame in display, GOB2 becomes LOW automatically (GOE1 also becomes LOW), turns on all the gate outputs (O1-O240). This discharges the electric charge of the panel. After tOE2RG period, of which the panel completes discharging (specify according to the panel's characteristics), you can stop the VS regulators by setting RGON of the power supply system control register 4 (R27) as 0, and by setting COMHI of the power supply system control register 7 (R30), the output of VCOM becomes Hi-Z. Then stop the VR regulator by setting RGONR of the power supply system control register 1(R24). And by setting D6, D4-D0 of the power supply system control register1 (R24) as 0, the DC/DC converter will be stopped. By this operation, all the gate outputs (O1-O240) become VSS. Next, if you set OSCSTBY of the control register 2 (R1) as 1, the IS2200 will stop the oscillation.

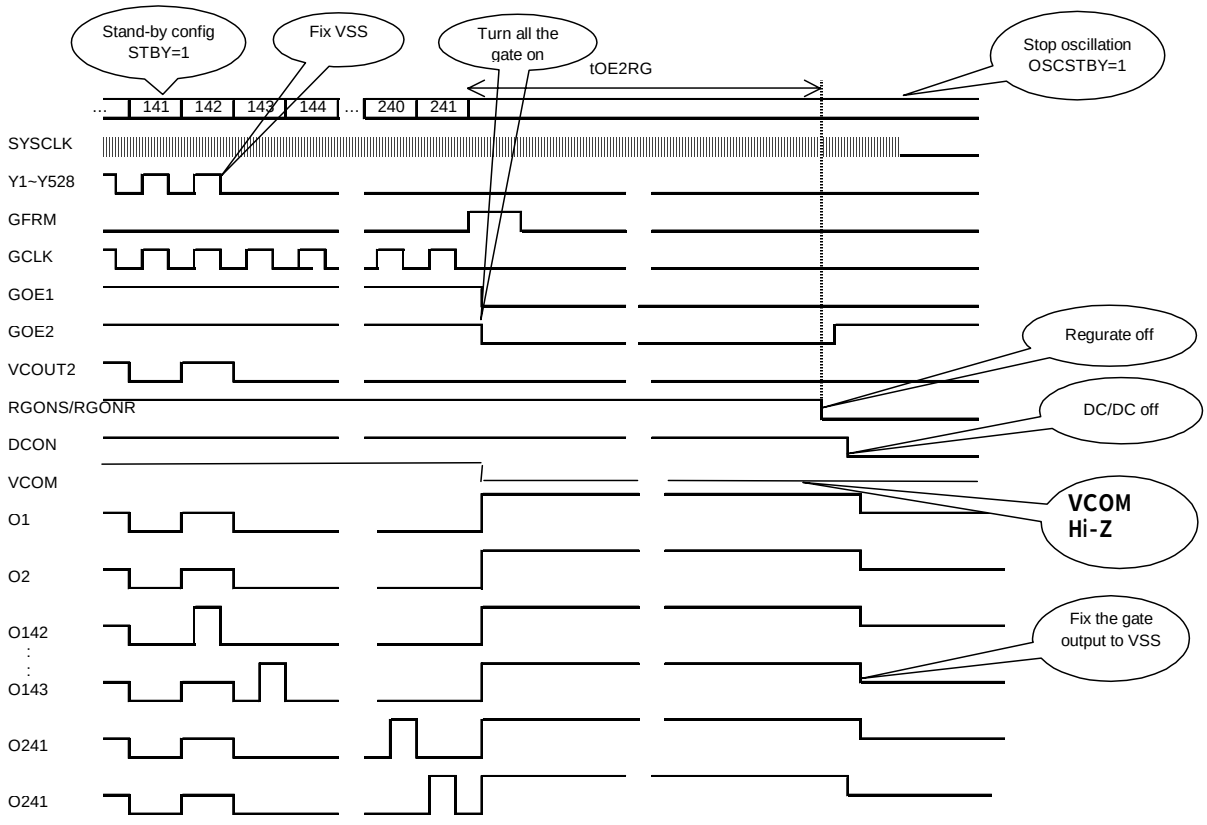


Fig. 10-1 Stand-by sequence

10.3. Stand-by Release Sequence

The IS2100 will start oscillation by setting OSCSTBY of the control register2 (R2) as 0. After the oscillation is stabilized, the IS2100 will operate the power-supply-on-sequence and restart displaying.

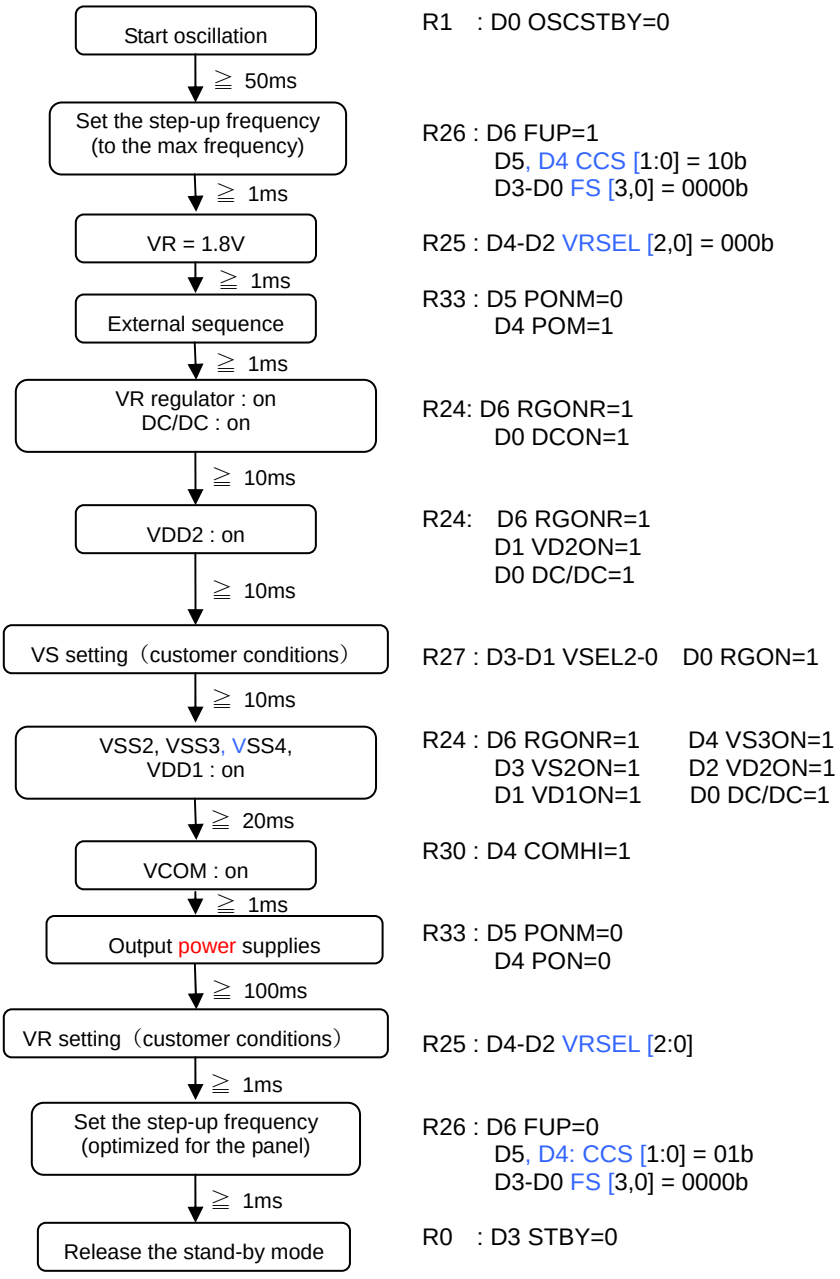
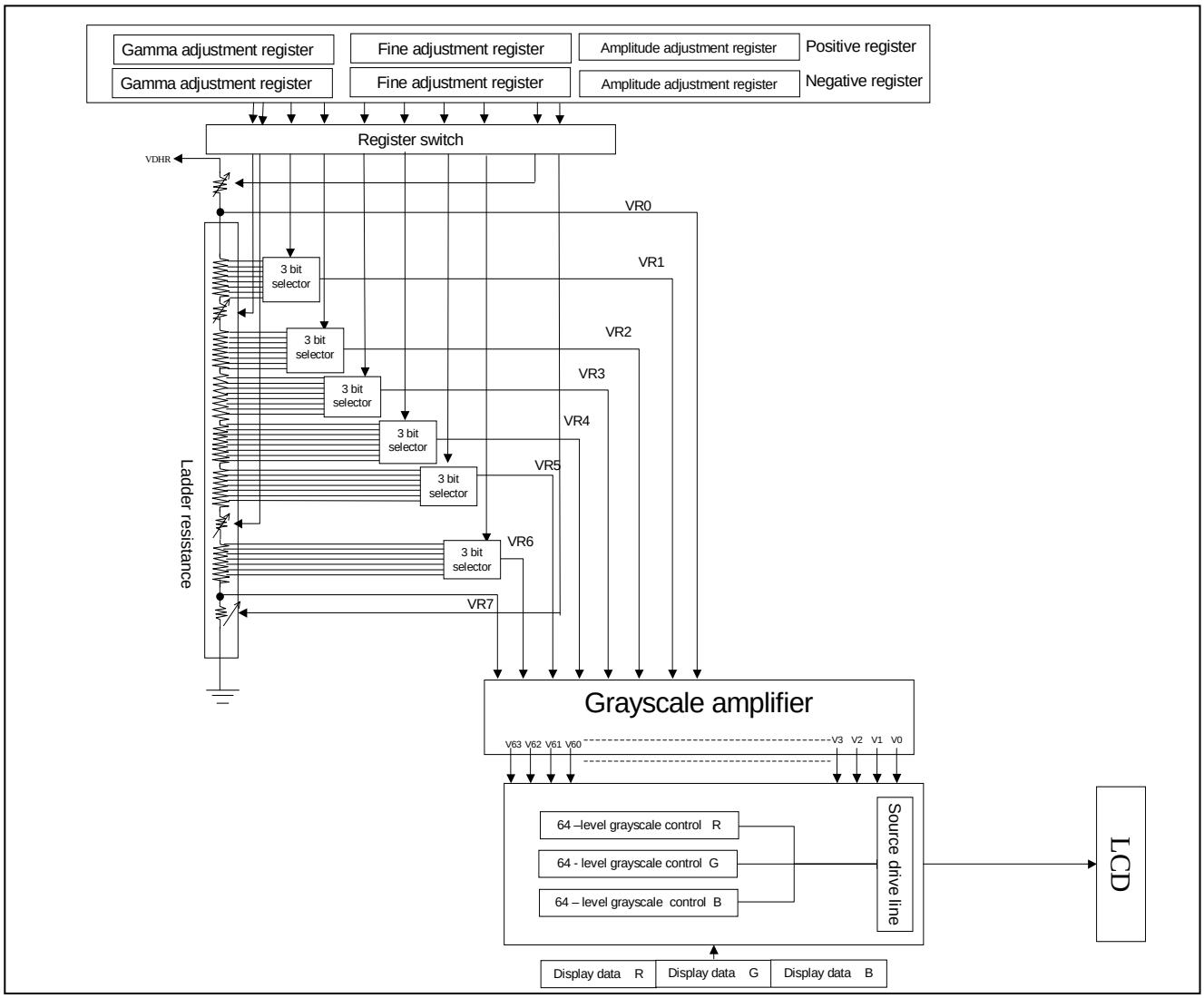


Fig.10-2 The stand-by release sequence

11. Gamma Correction Function

The IS2100 incorporates a gamma correction function to simultaneously display 262,144 colors. The gamma correction function is operated with the gamma-correction registers. The gamma-correction registers have switches for gradient, amplitude and fine corrections. Each switch is separated into positive and negative ones, so the polarity of each register can be specified independently. However, these registers for R, G and B are common.

Fig. 11-1 The gamma condition block and the grayscale controls



11.1. Gradient Adjustment

The gradient adjustment registers (R148, R154) are used to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range.

(See Fig. 11-2 A Gradient adjustment)

11.2. Amplitude Adjustment

The amplitude adjustment registers (R143, R144, R149, R150) are used to adjust the amplitude.

(See Fig. 11-2 B1, B2 Amplitude adjustment)

If you set D4=GSEL of the control register 2 (R1) as 0, the amplitude registers are fixed as V0=VDHR, V63=VSS regardless of those values.

11.3. Fine Adjustment

The fine adjustment registers are to make fine adjustment of the grayscale voltage level.

(See Fig. 11-2 C Fine adjustment)

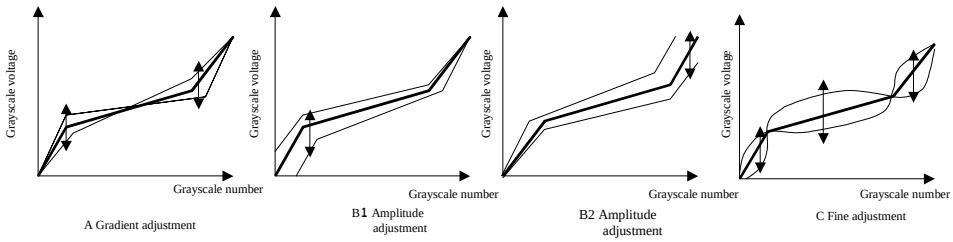


Fig. 11-2 The grayscale number - grayscale characteristics for the voltage

11.4. Gamma Curve Correction Circuit

All the conditioning registers have pins for the positive polarity and the negative polarity; R143 through R148 are for the positive and R149 through R154 are for the negative.

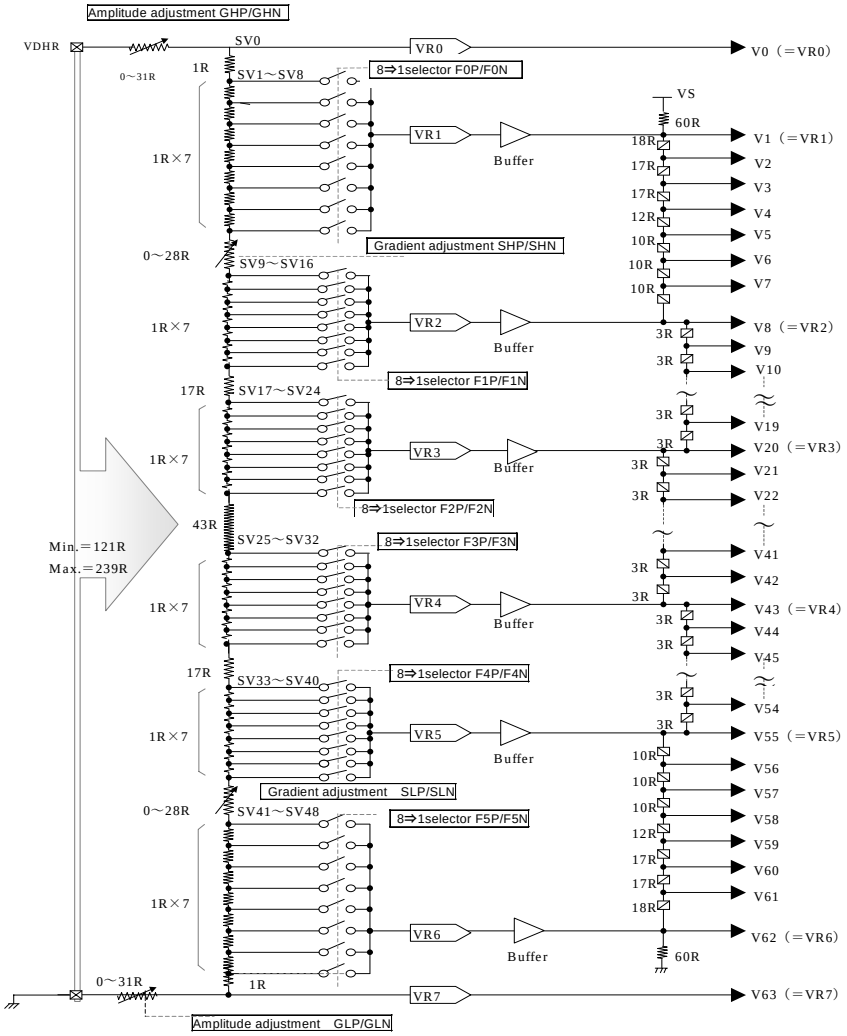


Fig. 11-3 Gamma curve correction circuit

Register		Default	Range	D7	D6	D5	D4	D3	D2
R143	Gamma adjustment register 1 (Upper amplitude – positive)	**05H**	0 - 31R			GHP5	GHP4	GHP3	GHP2
R144	Gamma adjustment register 2 (Lower amplitude – positive)	**05H**	0 - 31R			GLP5	GLP4	GLP3	GLP2
R145	Gamma adjustment register 3 (Fine F1, F0 – positive)	**44H**	(0 - 7R)/F*P		F1P2	F1P1	F1P0		F0P2
R146	Gamma adjustment register 4 (Fine F3, F2 – positive)	**44H**	(0 - 7R)/F*P		F3P2	F3P1	F3P0		F2P2
R147	Gamma adjustment register 5 (Fine F5, F4 – positive)	**44H**	(0 - 7R)/F*P		F5P2	F5P1	F5P0		F4P2
R148	Gamma adjustment register 6 (Lower, upper gradient – positive) (A)	**33H**	(0 - 7R)/F*P		SLP2	SLP1	SLP0		SHP2
R149	Gamma adjustment register 7 (Upper amplitude – negative)	**05H**	(0 - 31R)			GHN5	GHN4	GHN3	GHN2
R150	Gamma adjustment register 8 (Lower amplitude – negative)	**05H**	(0 - 31R)			GLN5	GLN4	GLN3	GLN2
R151	Gamma adjustment register 9 (Fine F1, F0 – negative)	**44H**	(0 - 7R)/F*P		F1N2	F1N1	F1N0		F0N2
R152	Gamma adjustment register 10 (Fine F3, F2 – negative)	**44H**	(0 - 7R)/F*P		F3N2	F3N1	F3N0		F2N2
R153	Gamma adjustment register 11 (Fine F5, F4 – negative)	**44H**	(0 - 7R)/F*P		F5N2	F5N1	F5N0		F4N2
R154	Gamma adjustment register 12 (Lower, upper gradient – negative) (A)	**33H**	(0 - 7R)/F*P		SLN2	SLN1	SLN0		SHN2

(A): 1=4R 00110100=>SLP, SLN=3x4R=12R SHP, SHN=4x4R=16R

Table 11-1 Register table for gamma curve correction

Note 1. When the power is supplied, D4=GSEL of the register R1 is set as 0.

2. Please set D4=GSEL of the register R1 as 1 after setting the R143, R149, R144, R150.
(Contents of the R143, R149, R144, R150 are retained if D4=GSEL is set as 0 after setting the R143, R149, R144, R150.)

11.5. Grayscale Voltage Calculation Formula

Voltage	Formula	Fine adjustment register-positive	Fine adjustment register-negative	Reference voltage
SV0	VDHR – VDHR x {GH /(SUMR+GH)}	GHP5 - GHP0	GHN5 -GHN0	VR0
SV1	VR0 – VR0 x 1R / SUMR	F0P2 - F0P0='111'	F0N2 - F0N0='111'	VR1
SV2	VR0 – VR0 x 2R / SUMR	F0P2 - F0P0='110'	F0N2 - F0N0='110'	
SV3	VR0 – VR0 x 3R / SUMR	F0P2 - F0P0='101'	F0N2 - F0N0='101'	
SV4	VR0 – VR0 x 4R / SUMR	F0P2 - F0P0='100'	F0N2 - F0N0='100'	
SV5	VR0 – VR0 x 5R / SUMR	F0P2 - F0P0='011'	F0N2 - F0N0='011'	
SV6	VR0 – VR0 x 6R / SUMR	F0P2 - F0P0='010'	F0N2 - F0N0='010'	
SV7	VR0 – VR0 x 7R / SUMR	F0P2 - F0P0='001'	F0N2 - F0N0='001'	
SV8	VR0 – VR0 x 8R / SUMR	F0P2 - F0P0='000'	F0N2 - F0N0='000'	
SV9	VR0 – VR0 x (8R + SH) / SUMR	F1P2 - F1P0='111'	F1N2 - F1N0='111'	VR2
SV10	VR0 – VR0 x (9R + SH) / SUMR	F1P2 - F1P0='110'	F1N2 - F1N0='110'	
SV11	VR0 – VR0 x (10R + SH) / SUMR	F1P2 - F1P0='101'	F1N2 - F1N0='101'	
SV12	VR0 – VR0 x (11R + SH) / SUMR	F1P2 - F1P0='100'	F1N2 - F1N0='100'	
SV13	VR0 – VR0 x (12R+ SH) / SUMR	F1P2 - F1P0='011'	F1N2 - F1N0='011'	
SV14	VR0 – VR0 x (13R + SH) / SUMR	F1P2 - F1P0='010'	F1N2 - F1N0='010'	
SV15	VR0 – VR0 x (14R + SH) / SUMR	F1P2 - F1P0='001'	F1N2 - F1N0='001'	
SV16	VR0 – VR0 x (15R + SH) / SUMR	F1P2 - F1P0='000'	F1N2 - F1N0='000'	
SV17	VR0 – VR0 x (32R + SH) / SUMR	F2P2 - F2P0='111'	F2N2 - F2N0='111'	VR3
SV18	VR0 – VR0 x (33R + SH) / SUMR	F2P2 - F2P0='110'	F2N2 - F2N0='110'	
SV19	VR0 – VR0 x (34R + SH) / SUMR	F2P2 - F2P0='101'	F2N2 - F2N0='101'	
SV20	VR0 – VR0 x (35R + SH) / SUMR	F2P2 - F2P0='100'	F2N2 - F2N0='100'	
SV21	VR0 – VR0 x (36R + SH) / SUMR	F2P2 - F2P0='011'	F2N2 - F2N0='011'	
SV22	VR0 – VR0 x (37R + SH) / SUMR	F2P2 - F2P0='010'	F2N2 - F2N0='010'	
SV23	VR0 – VR0 x (38R + SH) / SUMR	F2P2 - F2P0='001'	F2N2 - F2N0='001'	
SV24	VR0 – VR0 x (39R + SH) / SUMR	F2P2 - F2P0='000'	F2N2 - F2N0='000'	
SV25	VR0 – VR0 x (82R + SH) / SUMR	F3P2 - F3P0='111'	F3N2 - F3N0='111'	VR4
SV26	VR0 – VR0 x (83R + SH) / SUMR	F3P2 - F3P0='110'	F3N2 - F3N0='110'	
SV27	VR0 – VR0 x (84R + SH) / SUMR	F3P2 - F3P0='101'	F3N2 - F3N0='101'	
SV28	VR0 – VR0 x (85R + SH) / SUMR	F3P2 - F3P0='100'	F3N2 - F3N0='100'	
SV29	VR0 – VR0 x (86R + SH) / SUMR	F3P2 - F3P0='011'	F3N2 - F3N0='011'	
SV30	VR0 – VR0 x (87R + SH) / SUMR	F3P2 - F3P0='010'	F3N2 - F3N0='010'	
SV31	VR0 – VR0 x (88R + SH) / SUMR	F3P2 - F3P0='001'	F3N2 - F3N0='001'	
SV32	VR0 – VR0 x (89R + SH) / SUMR	F3P2 - F3P0='000'	F3N2 - F3N0='000'	
SV33	VR0 – VR0 x (106R + SH) / SUMR	F4P2 - F4P0='111'	F4N2 - F4N0='111'	VR5
SV34	VR0 – VR0 x (107R + SH) / SUMR	F4P2 - F4P0='110'	F4N2 - F4N0='110'	
SV35	VR0 – VR0 x (108R + SH) / SUMR	F4P2 - F4P0='101'	F4N2 - F4N0='101'	
SV36	VR0 – VR0 x (109R + SH) / SUMR	F4P2 - F4P0='100'	F4N2 - F4N0='100'	
SV37	VR0 – VR0 x (110R + SH) / SUMR	F4P2 - F4P0='011'	F4N2 - F4N0='011'	
SV38	VR0 – VR0 x (111R + SH) / SUMR	F4P2 - F4P0='010'	F4N2 - F4N0='010'	
SV39	VR0 – VR0 x (112R + SH) / SUMR	F4P2 - F4P0='001'	F4N2 - F4N0='001'	
SV40	VR0 – VR0 x (113R + SH) / SUMR	F4P2 - F4P0='000'	F4N2 - F4N0='000'	
SV41	VR0 – VR0 x (113R + SH + SL) / SUMR	F5P2 - F5P0='111'	F5N2 - F5N0='111'	VR6
SV42	VR0 – VR0 x (114R + SH + SL) / SUMR	F5P2 - F5P0='110'	F5N2 - F5N0='110'	
SV43	VR0 – VR0 x (115R + SH + SL) / SUMR	F5P2 - F5P0='101'	F5N2 - F5N0='101'	
SV44	VR0 – VR0 x (116R + SH + SL) / SUMR	F5P2 - F5P0='100'	F5N2 - F5N0='100'	
SV45	VR0 – VR0 x (117R + SH + SL) / SUMR	F5P2 - F5P0='011'	F5N2 - F5N0='011'	
SV46	VR0 – VR0 x (118R + SH + SL) / SUMR	F5P2 - F5P0='010'	F5N2 - F5N0='010'	
SV47	VR0 – VR0 x (119R + SH + SL) / SUMR	F5P2 - F5P0='001'	F5N2 - F5N0='001'	
SV48	VR0 – VR0 x (120R + SH + SL) / SUMR	F5P2 - F5P0='000'	F5N2 - F5N0='000'	
SV49	VDHR x {GL /(SUMR+GH)}	GPL5 - GPL0	GNL5 - GNL0	VR7

SUMR: {ladder resistance sum(GH+GL+SH+SL+121)-GH}✕R
GH: (GHP, GHN selected value) x R
GL: (GLP, GLN selected value) x R
SH: (SHP, SHN selected value) X 4R
SL: (SLP, SLN selected value) X 4R

Table. 11-2 Formulas for the reference voltage

Voltage for the grayscale	Formula
V0	VR0
V1	VR1
V2	V8+(V1-V8)*(76/94)
V3	V8+(V1-V8)*(59/94)
V4	V8+(V1-V8)*(42/94)
V5	V8+(V1-V8)*(30/94)
V6	V8+(V1-V8)*(20/94)
V7	V8+(V1-V8)*(10/94)
V8	VR2
V9	V20+(V8-V20)*11/12
V10	V20+(V8-V20)*10/12
V11	V20+(V8-V20)*9/12
V12	V20+(V8-V20)*8/12
V13	V20+(V8-V20)*7/12
V14	V20+(V8-V20)*6/12
V15	V20+(V8-V20)*5/12
V16	V20+(V8-V20)*4/12
V17	V20+(V8-V20)*3/12
V18	V20+(V8-V20)*2/12)
V19	V20+(V8-V20)*1/12
V20	VR3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(13/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VR4
V44	V55+(V43-V55)*11/12
V45	V55+(V43-V55)*10/12
V46	V55+(V43-V55)*9/12)
V47	V55+(V43-V55)*8/12
V48	V55+(V43-V55)*7/12
V49	V55+(V43-V55)*6/12
V50	V55+(V43-V55)*5/12
V51	V55+(V43-V55)*4/12
V52	V55+(V43-V55)*3/12
V53	V55+(V43-V55)*2/12
V54	V55+(V43-V55)*1/12
V55	VR5
V56	V62+(V55-V62)*(84/94)
V57	V62+(V55-V62)*(74/94)
V58	V62+(V55-V62)*(64/94)
V59	V62+(V55-V62)*(52/94)
V60	V62+(V55-V62)*(35/94)
V61	V62+(V55-V62)*(18/94)
V62	VR6
V63	VR7

Table 11-3 The voltage for (V0-V63) formula

Note!!

1) If you set GHP/GHN and GLP/GLN other than as 0, please make sure to set as follows; V0≤VS-0.2V, V63≥VSS+0.2V. (Refer to “23. DC Characteristics”)

2) If you set GHP/GHN as 0, V0 equals to VS. Please make sure to set as V1≤VS-0.2V.
If you set GLP/GLN as 0, V63 equals to VSS. Please make sure to set as V62≥VSS+0.2V.

11.6. The Voltage for Grayscale and the Data of the Display Data RAM

The relationship between the grayscale output (V0-V63) and the display data RAM is as follows.

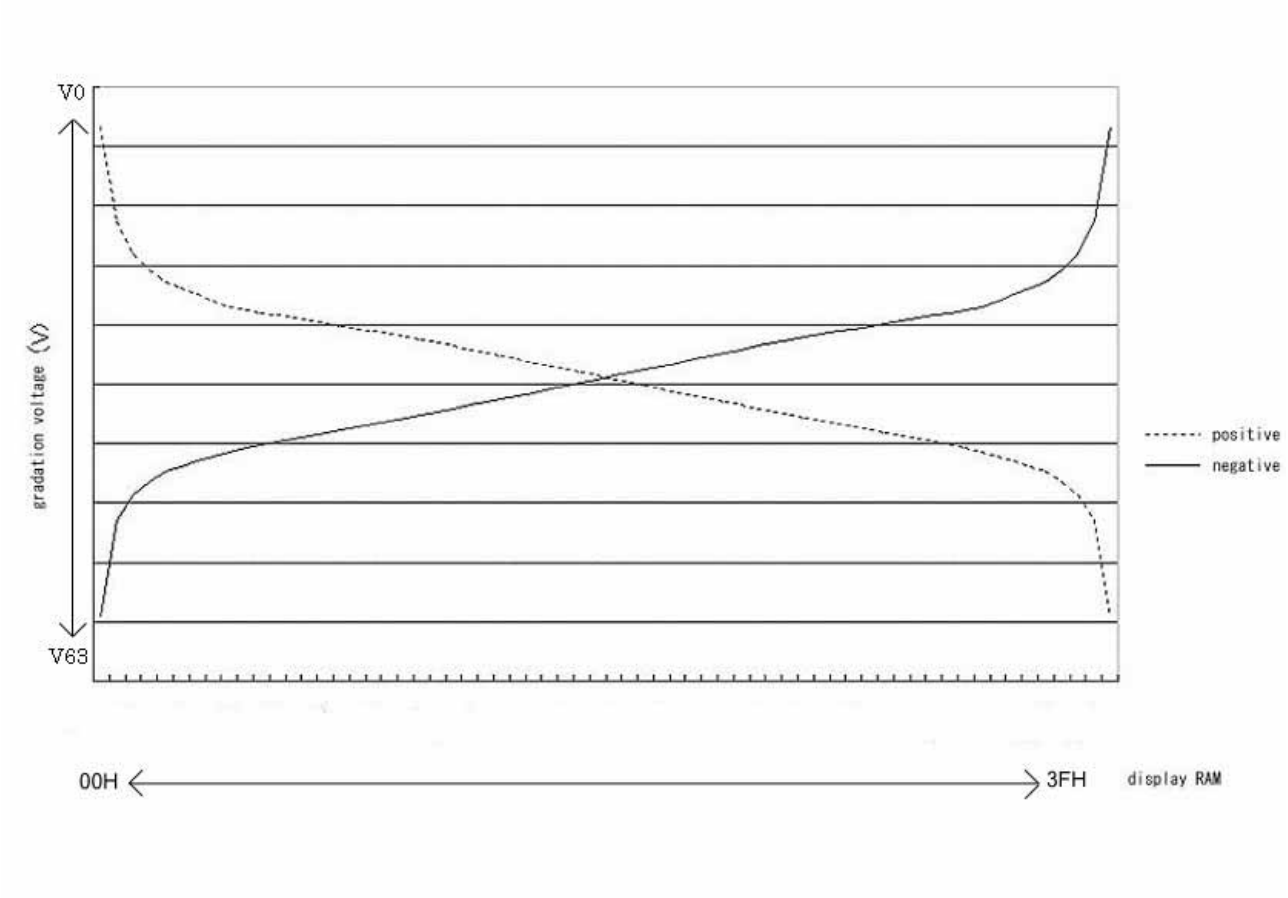


Fig. 11-4 The relationship between the grayscale output (V0-V63) and the display data RAM

12. Eight-color Display Mode

You can start an 8-color display mode by setting D2=COLOR of the control register 1 (R0) as 1. The grayscale levels to be used are only V0 and V63, and the circuits for other levels (V1-V62) are disabled. This, therefore, achieves to reduce the power consumption.

In the eight-color mode, the gamma correction function is invalid. However, the configuration for the gamma correction registers will be maintained.

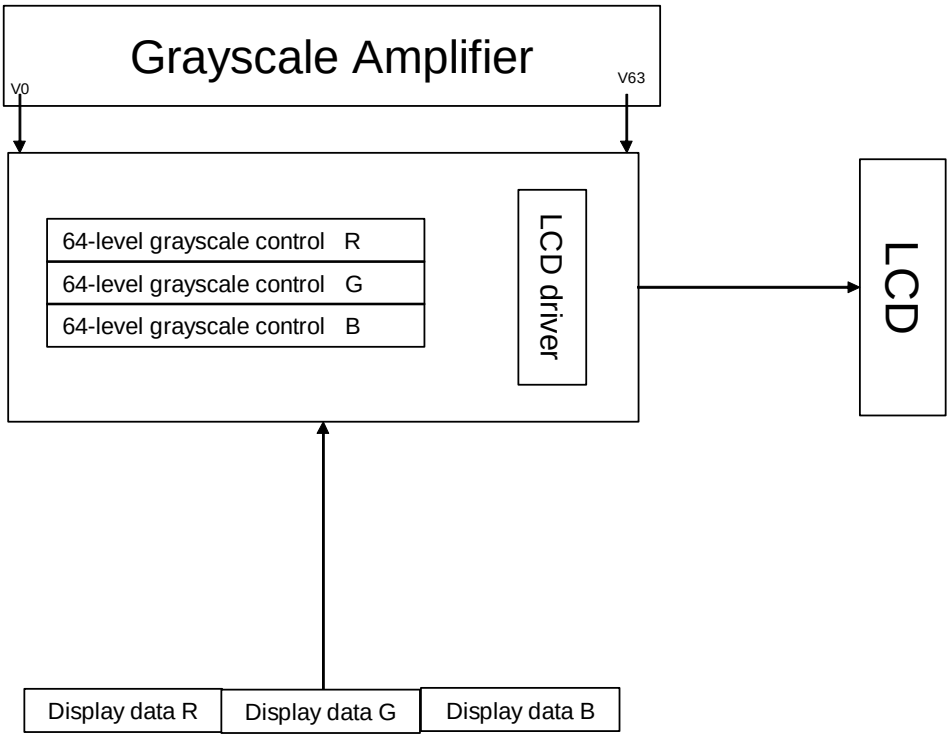


Fig. 12-1 Grayscale control for the eight-color display mode

13. Partial Display Function

The partial display mode is available by setting D4=DTY of the control register 1 (R0) as 1. The IS2100 can drive one or two screens of any size at any position by setting the partial display control register (R18-R23). The colors of the non-display areas can be specified by D0=PSEL of the partial-off area color register 1 (R18) and D2=PGR, D1=PGG, D0=PGB of the partial-off area color register 2 (R19).
This function does not reduce the power consumption.

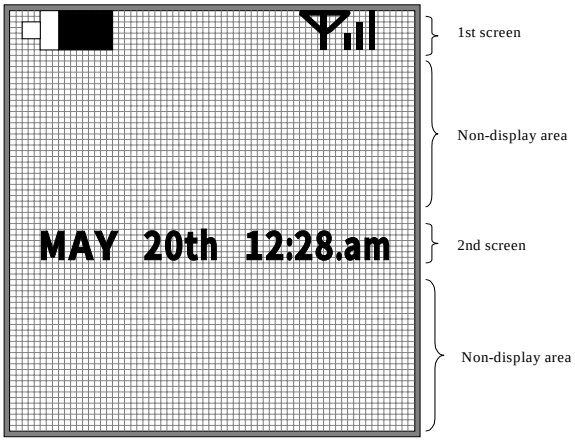


Fig. 13-1 Two screen partial drive

13.1. Partial Display Area Set-up

To specify a partial display area, first you need to specify the raster-row number, where you would like to start the partial display from, in the partial area start registers (R20, R21). (The start raster-rows are “1+R20”, “1+R21”.) The number of raster-rows for partial display areas is specified with partial 1-/2-display area raster-row number registers (R22, R23). Please make sure that the partial display areas 1 and 2 don’t overlap each other.

Partial 1 display area starting register (R20)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P1SL7	P1SL6	P1SL5	P1SL4	P1SL3	P1SL2	P1SL1	P1SL0

Partial 2 display area starting register (R21)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2SL7	P2SL6	P2SL5	P2SL4	P2SL3	P2SL2	P2SL1	P2SL0

Partial 1 display area raster-row number register (R22)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P1AW7	P1AW6	P1AW5	P1AW4	P1AW3	P1AW2	P1AW1	P1AW0

Partial 2 display area raster-row number register (R23)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2AW7	P2AW6	P2AW5	P2AW4	P2AW3	P2AW2	P2AW1	P2AW0

13.2. Display Color Selection in The Non-Display Areas

The output of the non-display areas can be specified by the partial-off area color register1 and the partial-off area color register 2.

Partial off area color register 1(R18)	Display color selection
D0=PSEL; 0	The color specified by the partial off area color register 2 (R19)
D0=PSEL; 1	The color specified by 0 or 1 of the upper bit of each pixel of the Display Data RAM

R19			Output voltage for each pixel			When Pixel 1= R 2= G 3= B
D 2	D 1	D 0				
PGR	PGG	PGB	Pixel 1	Pixel 2	Pixel 3	
0	0	0	Vo	Vo	Vo	Black
0	0	1	Vo	Vo	V63	Blue
0	1	0	Vo	V63	Vo	Green
0	1	1	Vo	V63	V63	Cyan
1	0	0	V63	Vo	Vo	Red
1	0	1	V63	Vo	V63	Magenta
1	1	0	V63	V63	Vo	Yellow
1	1	1	V63	V63	V63	White

13.3 Gate Scan in the Non-display Area

You can choose a gate scan method in the non-display area from these two listed below.

1. Arbitrary frame cycle
2. Reversed frame or reversed n-raster-row when the partial display areas are driven by n-raster-row reverse.

13.3.1. Arbitrary frame cycles

Arbitrary frame cycles can be available when reversed frame or reversed n-raster-row is selected as a gate scan of display areas. By setting D0=GSM of the control register 1 (R0) as “1”, this gate scan will be available. D7-D0=GSMLN7-GSMLN0 of the partial gate register 1 (R52) are used to define the number of frames where gate scan will be performed. For example, if GSMLN7-GSMLN0 are set as 02H, the gate scan will be done in one frame per every 3 frames and all gate outputs in the partial-off display areas will be “OFF” in the other two frames.

When set GSMLN7-GSMLN0 as 00H, no gate scan will be performed in the non-display areas.

Note: Prohibited to set the odd numbers to R52. (DC voltage will be applied to the panel.)

Partial gate register 1 (R52)

D7	D6	D5	D4	D3	D2	D1	D0
GSMLN7	GSMLN6	GSMLN5	GSMLN4	GSMLN3	GSMLN2	GSMLN1	GSMLN0

13.3.2. Reversed frame or n-raster-row reverse when the partial display area is driven with the n-raster-row reverse

When the partial display area is driven by the n-raster-row reverse, the IS2100 can drive the non-display areas by the frame reverse by setting D0=PNFRM of the partial gate register 2 (R53) is set as “1”.

Note: PNFRM has to be set as 0 when normal display mode is selected (R0:D4=DTY=0).

Partial gate register 2 (R53)

D7	D6	D5	D4	D3	D2	D1	D0
							PNFRM

14. Vertical Scroll Function

The IS 2100 incorporates a scroll display function. Since this scroll function does not perform automatically, please follow the instruction below to manually operate this function.

First specify the number of the raster-row to assign where to start the scrolling in the scroll area start register (R15). Next, define the number of raster-rows for the scroll area in the scroll area raster-row number register (R16).

If you specify an amount of scroll (e.g. 2 steps) in the scroll step number register (R17), the displayed picture will scroll up from the next frame by the specified amount (e.g. 2 steps) and maintain its displayed picture. Also if you want the picture to scroll up (e.g. 2 steps) further, please set (2＋2=4) in the R17. Accordingly, if you want the picture to scroll up (e.g. 2 steps) further again, please set (2＋2＋2=6) in the R17. When value of R17 exceeds value of R16, please reset the value of R17 with the value less than R16.

To stop this scroll function, please set 0 in the scroll step number register (R17).

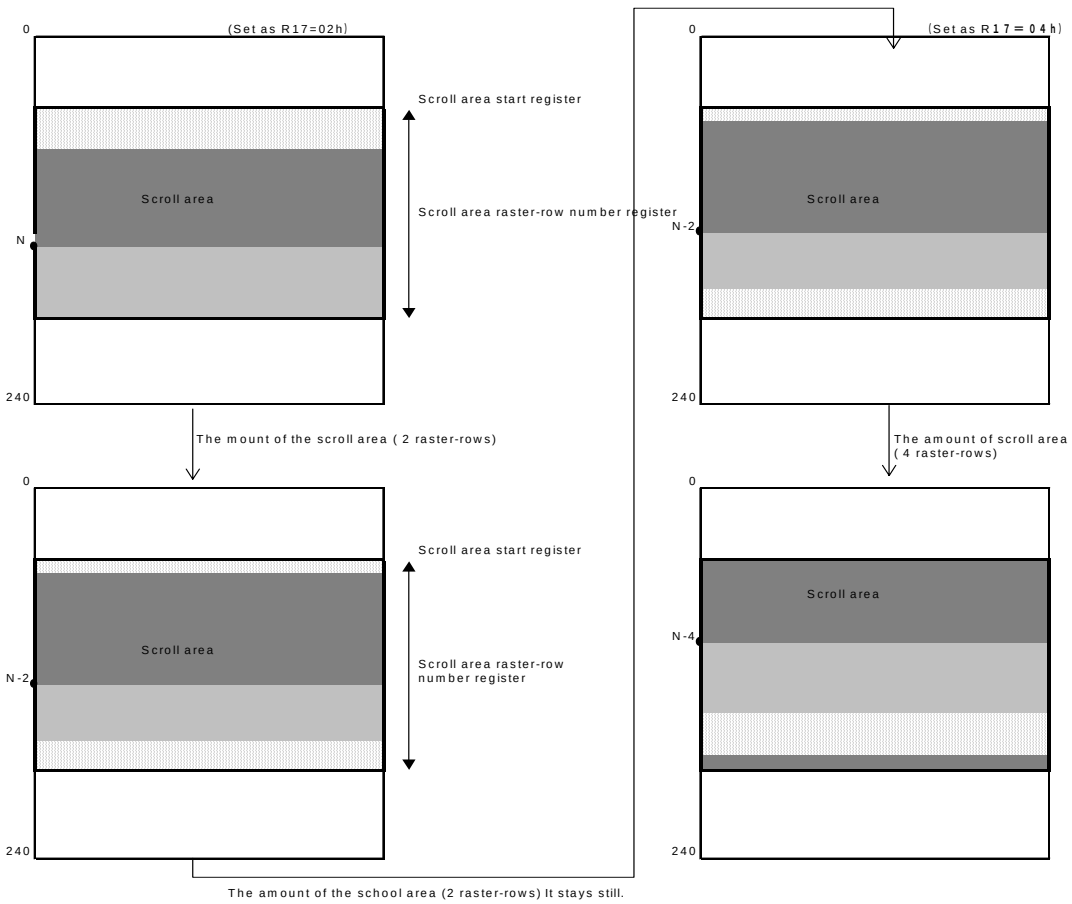


Fig. 14-1 Image that the display start line is the second line

14.1. Registers for The Scroll Control

14.1.1. Scroll area start register (R15)

D7	D6	D5	D4	D3	D2	D1	D0	Start raster-row Y address
SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0	
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
								:
1	1	1	0	1	1	0	1	237
1	1	1	0	1	1	1	0	238
1	1	1	0	1	1	1	1	239

14.1.2. Scroll area line number register (R16)

D7	D6	D5	D4	D3	D2	D1	D0	Scroll area raster-row number
SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0	
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
								:
1	1	1	0	1	1	0	1	238
1	1	1	0	1	1	1	0	239
1	1	1	0	1	1	1	1	240

14.1.3. Scroll step number register (R17)

D7	D6	D5	D4	D3	D2	D1	D0	Scroll step raster-row number
SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	
0	0	0	0	0	0	0	0	No scroll
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
								:
1	1	1	0	1	1	0	1	237
1	1	1	0	1	1	1	0	238
1	1	1	0	1	1	1	1	239

15. Interface for Setting up the IS2200

The IS2100 has an internal serial interface for setting up the gate-driver IS2200 with an internal power supply. Writing to the registers in the IS2100 starts the serial communication automatically. Under the serial communication, the automatic transfer is not available even if you write to the registers for the IS2200. Please write to the next register after the serial communication is finished. Please remember to keep distance of 50 μs or more when you write to the IS2200 register continuously.

Refer to the IS2200'S specification for further details.

16. Gate Raster-Row Drive

The IS2100 incorporates an n-raster-row reversed drive and a frame reversed drive. Please set them up according to the panel's characteristics.

Always operate the reversed frame drive for at least one frame before performing the Skip Reverse 2B.

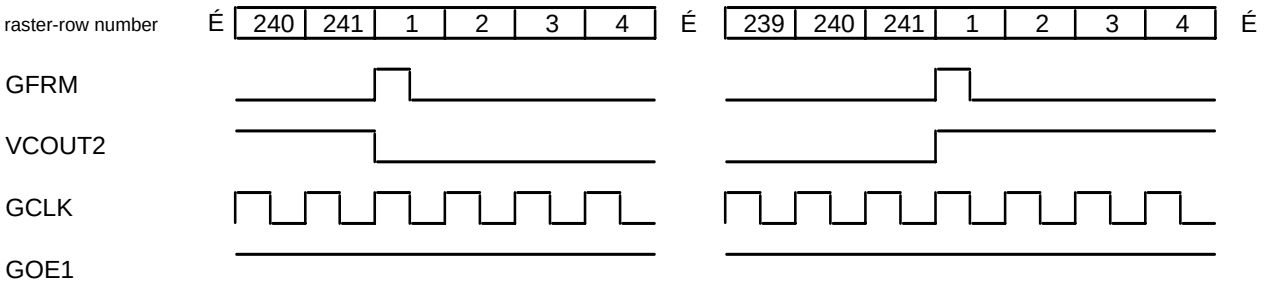
The configuration of 00H-04H in the R137 register is invalid when the Skip Reversed 2B or IC is in use.

R55			Scan mode	Description
D2	D1	D0		
GSCAN2	GSCAN1	GSCAN0		
0	0	0	Reversed frame	Reverse operation is performed every frame.
0	0	1	Reversed n-raster-row	Reverse operation is performed every configured raster-row number (01H-78H) set in the R51 register.
0	1	0	Skip reverse 1 A	The gate output repeats ON/OFF and the common output reverses every 2-raster-row. The frame frequency does not change.
0	1	1	Skip reverse 1 B	The gate output repeats ON/OFF and the common output reverses every 2-raster-row. After displaying one frame, the frame reverses. The frame frequency is not changed.
1	0	0	Skip reverse 1 C	2 raster-row interlaced drive Only available in the internally synchronized display mode.
1	0	1	Skip reverse 2 A	The gate output repeats ON/OFF/OFF and the common output operates the frame reverse. The frame frequency is not changed.
1	1	0	Skip reverse 2 B	The gate output repeats ON/OFF/OFF and the common output operates the frame reverse. 3 raster-row-interlace Only available in the internally synchronized display mode.

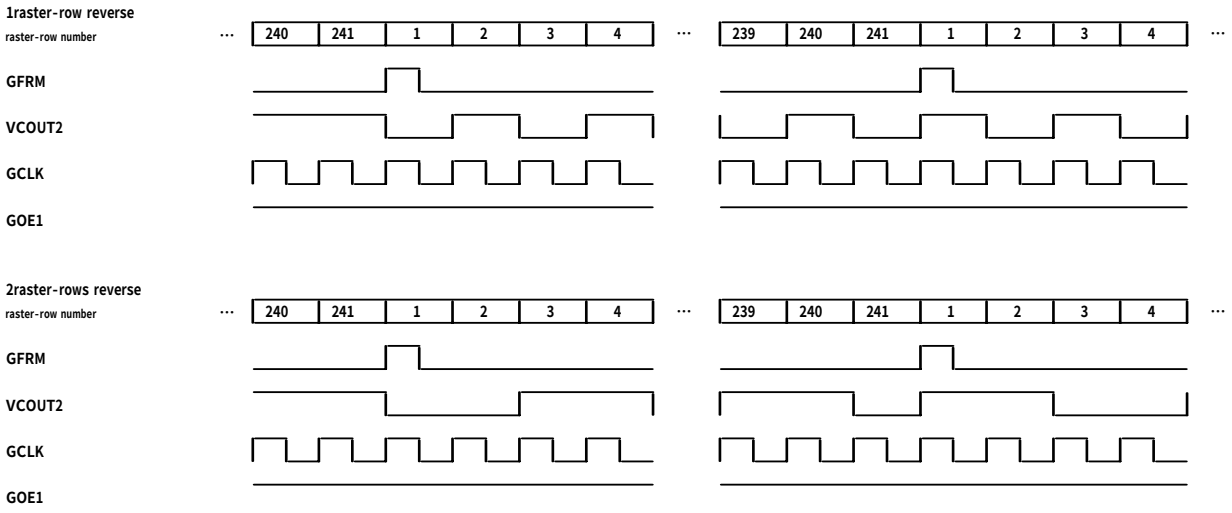
Fig. 16-1 Reversed AC drive display configuration

16.1. Reversed Frame Display

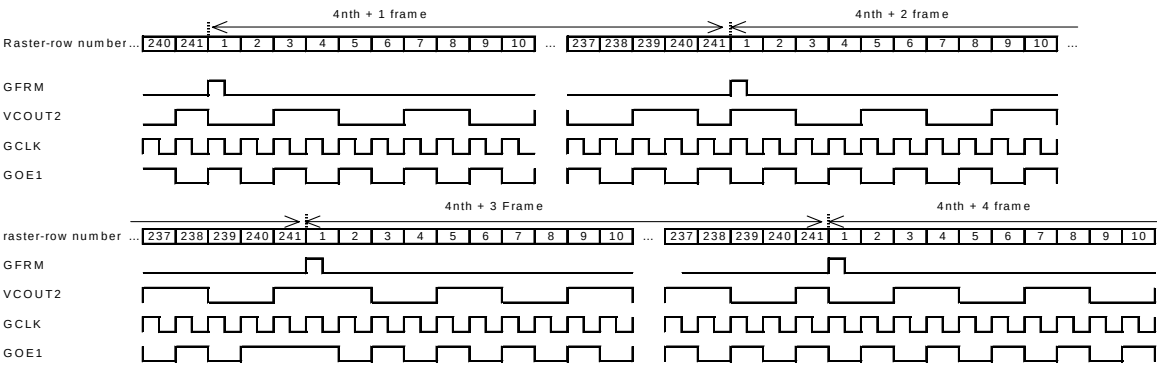
Frame reverse



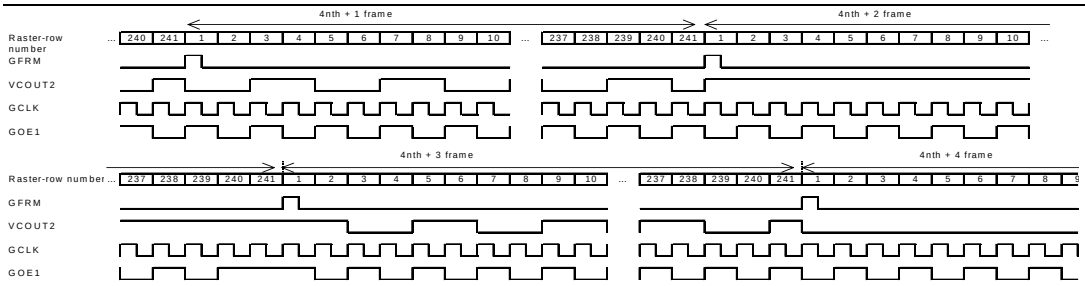
16.2. n Raster-Row Reversed Display



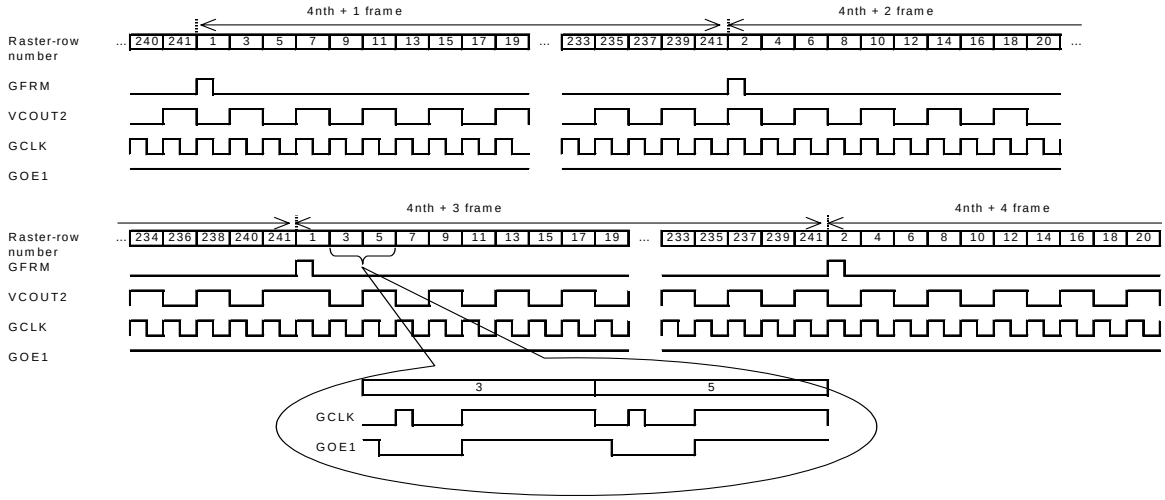
16.3. Skip Reverse 1 A



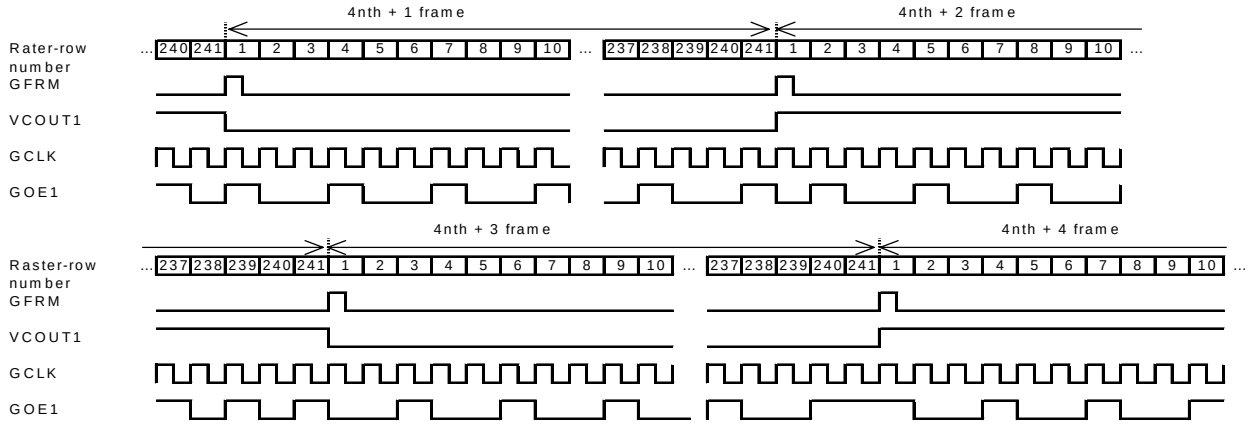
16.4. Skip Reverse 1 B



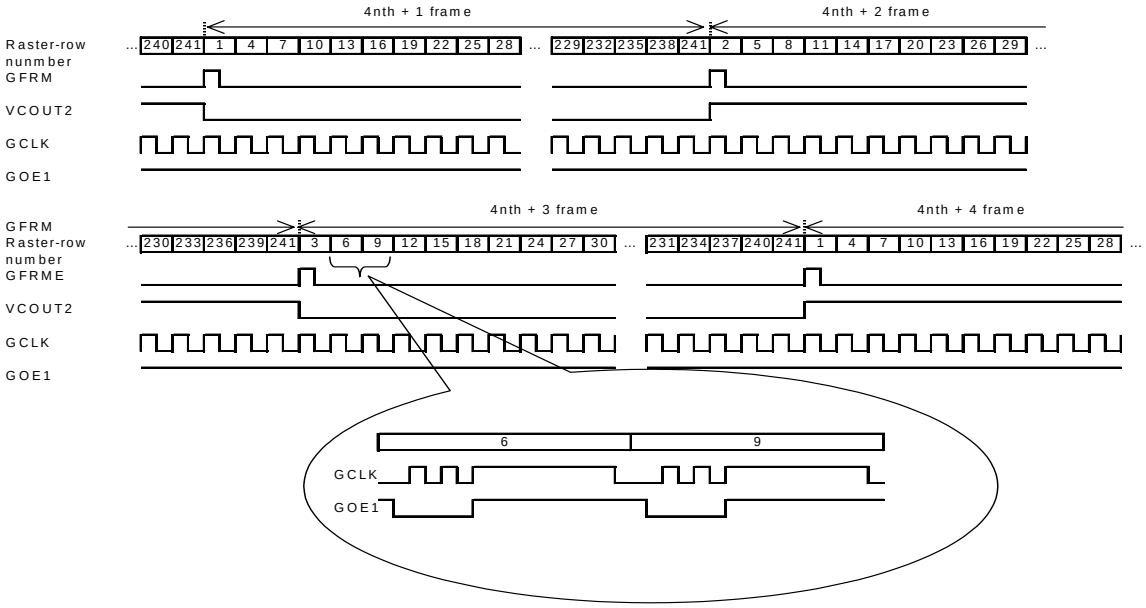
16.5. Skip Reverse 1C



16.6. Skip Reverse 2A



16.7. Skip Reverse 2B



17. Gate Driver IS2200 Output Control

17.1. Set The Number of Gate Drive Raster-Rows

The number of the gate raster-rows is defined with D0=NGO0 of the display size setting register (R13).

Display size setting register (R13)

R13 D0=NGO0	Number of the gate output
0	240 outputs
1	220 outputs

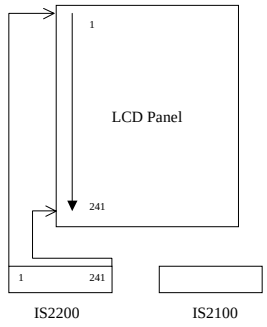
17.2. Scan Pattern

There are multiple ways (modes) to mount this LSI on the panel (shown on the next page). Please choose one preferred mode for you panel and set D2 - D0 of the power supply system control register 5 (R29) and the R/L pin of the IS2200 using the table below. For more information of the blanking period and the dummy raster-rows, please refer to Chapter 17.3 and 17.4.

R/L	SCN2	SCN1	SCN0	Scan mode
H	1	1	1	MODE1R
L	1	1	1	MODE1L
H	0	1	1	MODE2R
L	0	1	1	MODE2L
H	1	0	1	MODE3R
L	1	0	1	MODE3L
H	0	0	1	MODE4R
L	0	0	1	MODE4L
H	X	X	0	MODE5R
L	X	X	0	MODE5L

*All the figures below are when the output is 240. For 220 outputs, please refer to the Table 17-2.

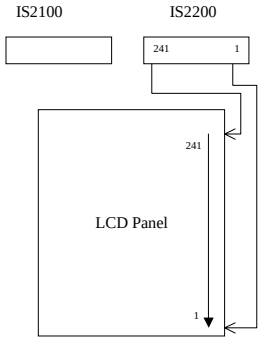
MODE1R



Scanning order
O1→O241

SCN2=1
SCN1=1
SCN0=1
R/L=H

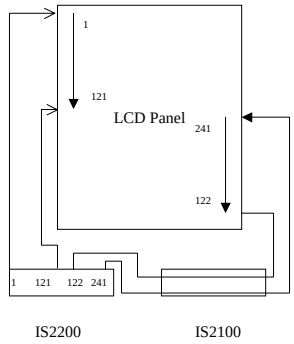
MODE1L



Scanning order
O241→O1

SCN2=1
SCN1=1
SCN0=1
R/L=L

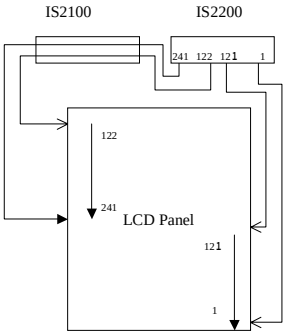
MODE2R



Scanning order
O1→O2→…O121
O241→O122

SCN2=0
SCN1=1
SCN0=1
R/L=H

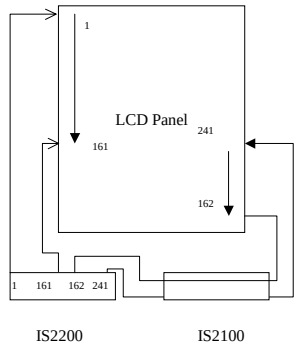
MODE2L



Scanning order
O122→O123…
→O241→O121…
→O1

SCN2=0
SCN1=1
SCN0=1
R/L=L

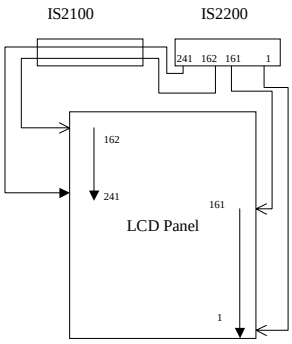
MODE3R



Scanning order
O1→O2→…O161→
O241→O162

SCN2=1
SCN1=0
SCN0=1
R/L=H

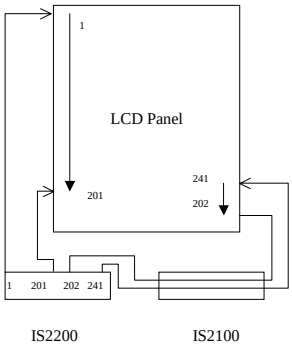
MODE3L



Scanning order
O162 → O163 …
→ O241 → O161…
→ O1

SCN2=1
SCN1=0
SCN0=1
R/L=L

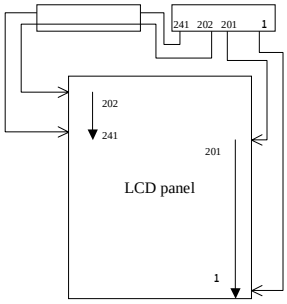
MODE4R



Scanning order
O1→O2→…O201→
O241→O202

SCN2=0
SCN1=0
SCN0=1
R/L=H

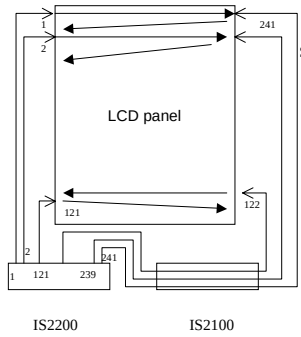
MODE4L



Scanning order
O202→O203…
→O241→O201…
→O1

SCN2=0
SCN1=0
SCN0=1
R/L=L

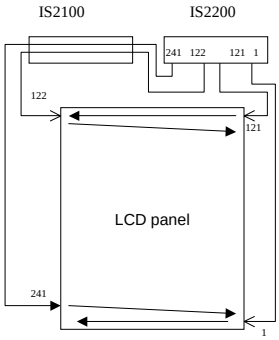
MODE5R



Scanning order
O1 → O241 → O2 →
O240…O122 → O121

SCN2=X
SCN1=X
SCN0=0
R/L=H

MODE5L



Scanning order
O121 → O122 →
O120 → O123…
→ O2 → O2 41→ O1

SCN2=X
SCN1=X
SCN0=0
R/L=L

17.3. Gate Output Order Classified by Mode

Scanning mode	DDS terminal	Dummy output terminal	Scanning order	Reserved pins
MODE1R	L	O241	O1 -> O2-> O3 ->...-> O239 -> O240 -> (dummy)	---
	H	O1	(Dummy) -> O2-> O3 ->...-> O239 -> O240 -> O241	---
MODE1L	L	O1	O241 -> O240 -> O239 ->...-> O3 -> O2 -> (dummy)	---
	H	O241	(Dummy) -> O240 -> O239 -> ...-> O3 -> O2 -> O1	---
MODE2R	L	O122	O1->O2-> ... ->O120->O121->O241 ->O240->O239-> ... ->O123->(dummy)	---
	H	O1	(Dummy)->O2-> ... ->O120->O121-> O241->O240-> ... ->O123->O122	---
MODE2L	L	O1	O122->O123->O124->...->O240->O241 ->O121->O120->...->O3->O2->(dummy)	---
	H	O122	(Dummy)->O123->O124-> ... ->O241 ->O121->O120->...->O3->O2->O1	---
MODE3R	L	O162	O1->O2->O3-> ... ->O160->O161-> O241->O240-> ... ->O163->(dummy)	---
	H	O1	(Dummy)->O2->O3-> ... ->O161-> O241->O240-> ... ->O163->O162	---
MODE3L	L	O1	O162->O163->...->O240->O241->O161->O160->...->O2->(dummy)	---
	H	O162	(Dummy)->O163->...->O240->O241->O161->O160->...->O2->O1	---
MODE4R	L	O202	O1->O2->...->O200->O201 ->O241->O240->...->O203->(dummy)	---
	H	O1	(Dummy)->O2->...->O200->O201 ->O241->O240->...->O203->O202	---
MODE4L	L	O1	O202->O203->...->O240->O241->O201->O200->...->O2->(dummy)	---
	H	O202	(Dummy)->O203->...->O240->O241->O201 -> O200 -> ... -> O2 -> O1	---
MODE5R	L	O121	O1->O241->O2->O240->...->O119->O123->O120->O122->(dummy)	---
	H	O1	(Dummy)->O241->O2->O240->...->O119->O123->O120->O122->O121	---
MODE5L	L	O1	O121->O122->O120->O123->...->O3->O240->O2->O241->(dummy)	---
	H	O121	(Dummy)->O122->O120->O123->...->O3->O240->O2->O241->O1	---

Table 17-1 The number of raster-rows --- 240 lines

Scanning mode	DDS terminal	Dummy output terminal	Scanning order	Reserved pins
MODE1R	L	O221	O1 -> O2-> O3 -> …-> O219 -> O220 -> (dummy)	O222 - O241
	H	O1	(Dummy) -> O2-> O3 ->…-> O219 -> O220 -> O221	O222 - O241
MODE1L	L	O21	O241 -> O240 -> O239 -> … -> O23 -> O22 -> (dummy)	O1 - O20
	H	O241	(Dummy) -> O240 -> O239 -> … -> O23 -> O22 -> O21	O1 - O20
MODE2R	L	O142	O1->O2-> … ->O120->O121->O241->O240->O239->…->O143->(dummy)	O122 - O141
	H	O1	(Dummy)->O2-> … ->O120->O121->O241->O240-> … ->O143->O142	O122 - O141
MODE2L	L	O21	O122->O123->O124->…->O240->O241->O121->O120-> … ->O22->(dummy)	O1 - O20
	H	O122	(Dummy)->O123->O124-> … ->O241->O121->O120-> … ->O23->O22->O21	O1 - O20
MODE3R	L	O162	O1->O2->O3-> … ->O140->O141-> O241->O240-> … ->O163->(dummy)	O142 - O161
	H	O1	(Dummy)->O2->O3-> … ->O141-> O241->O240-> … ->O163->O162	O142 - O161
MODE3L	L	O1	O162->O163->…->O240->O241->O141->O140->…->O2->(dummy)	O142 - O161
	H	O162	(Dummy)->O163->…->O240->O241->O141->O140->…->O2->O1	O142 - O161
MODE4R	L	O202	O1->O2->…->O180->O181 ->O241->O240->…->O203->(dummy)	O182 - O201
	H	O1	(Dummy)->O2->…->O180->O181 ->O241->O240->…->O203->O202	O182 - O201
MODE4L	L	O1	O202->O203->…->O240->O241->O181->O180->…->O2->(dummy)	O182 - O201
	H	O202	(Dummy)->O203->…->O240->O241->O181 -> O180 -> … -> O2 -> O1	O182 - O201
MODE5R	L	O111	O1->O241->O2->O240-> …->O109->O133->O110->O132->(dummy)	O112 - O131
	H	O1	(Dummy)->O241->O2->O240->…->O109->O133->O110->O132->O111	O112 - O131
MODE5L	L	O11	O121->O122->O120->O123-> …->O13->O230->O12->O231->(dummy)	O1 - O10 O232 - O241
	H	O121	(Dummy)->O122->O120->O123->…->O13->O230->O12->O231->O11	O1 - O10 O232 - O241

Table 17-2 The number of raster-rows --- 220 lines

17.4. Blanking Period and Dummy Raster-Row

The dummy line number selection register (R118) is for setting the blanking period. Also you can select either to put the blanking period and the dummy raster-row at the top of the frame or the end by the DDS pin of the IS2100.

17.4.1. Dummy line number selection register (R118)

D7	D6	D5	D4	D3	D2	D1	D0
							DMYSEL

DMYSEL: Select the blanking period

0: 1 dummy line scan for one raster-row

(The last display data gets output from the source output.)

1: above ＋7 blanking period (in the blanking period, AC reversed drive of the gate-output OFF)

17.4.2 DDS pin set up

DDS pin	Dummy line
L	End: 1 frame scan ＋dummy (+7 blanking)
H	Top: (7 blanking ＋) dummy ＋ 1 frame scan

(7 blanking) is when DMYSEL=1

This register is invalid when the LCD displays pictures in synchronization with the external clock.

18. IS2200 Control

18.1. Reset Command to The IS2200

Software-reset can be executed to the IS2200 from the IS2100. By setting D0=GRES of the power supply system register 11(R34) as 1, this setting will be transferred to the IS2200 and a software reset will be executed in the IS2200. The hardware reset function by /GRESET pin is no longer available.

Please see “IS2200 specification” for more details.

18.2. Power Set-up of The IS2200

It controls each power supply used in the IS2100 and the IS2200.

Refer to “IS2200 specification” for further details.

19. Example of System Configuration

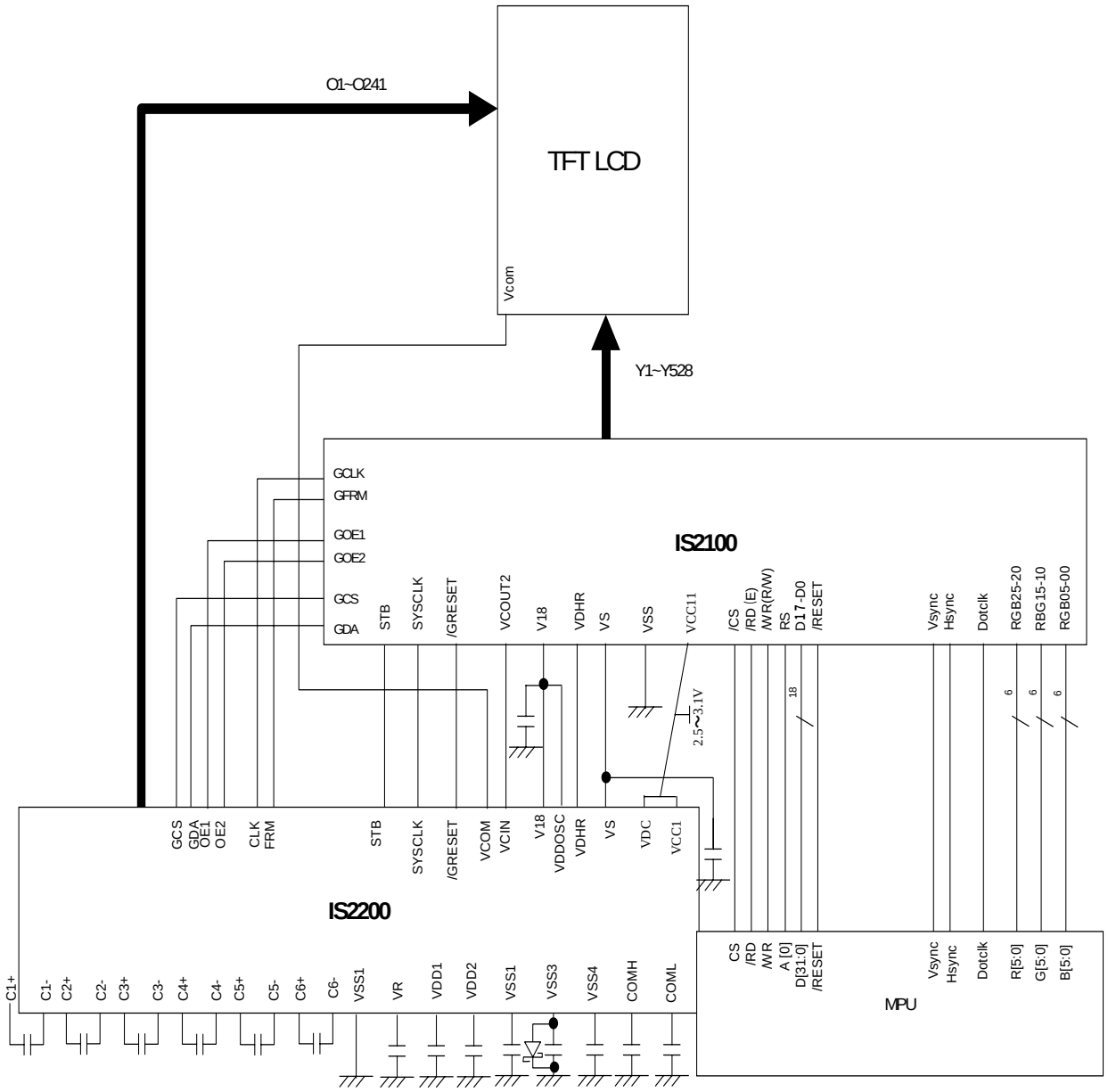


Fig. 19-1 Amorphous TFT LCD panel system connection

20. Device Code

Reading ID code register 1 (R49) enables you to obtain the manufacturer code and the version number of LSI. And reading the ID code register 2 (R50) enables to obtain the device code of LSI.

20.1. ID Code Register 1 (R49)

D7	D6	D5	D4	D3	D2	D1	D0
MCOD3	MCOD2	MCOD1	MCOD0	VCOD3	VCOD2	VCOD1	VCOD0

Manufacturer code (MCOD3 - 0) = 0001

Version code (VCOD3 - 0) = 0000

20.2. ID Code Register 2 (R50)

D7	D6	D5	D4	D3	D2	D1	D0
DCOD7	DCOD6	DCOD5	DCOD4	DCOD3	DCOD2	DCOD1	DCOD0

Device code (DCOD7 - 0) =00000000

21. Register Command Table

(W A0H)= (R/W register default value)

Register	Bit	Symbol	Function	Configuration
R0 Control register 1 **(W A0H)**	D7	DISP1	Source output data selection	Refer to “9.2. All 0/1 Display”
	D6	DISP0	Source output data selection	Refer to “9.2. All 0/1 Display”
	D5	ADC	Selection of the source address direction	In ADX=0 setting. 0: Y1, Y2 and Y3 output correspond to 00H of the display data RAM.. 1: Y528, Y527 and Y526 output correspond to 00H of the display data RAM.
	D4	DTY	Selection of the partial display	0: Normal display mode 1: Partial display mode
	D3	STBY	Selection of the stand-by	0: Normal operation 1: Stand-by mode
	D2	COLOR	Color mode selection	0: 262,144-color mode 1: 8-color mode
	D1			
	D0	GSM	Gate scan selection at the partial-off display area	0: Normal mode 1: Configure the scan cycle of the partial-off display area by the number set in the R52 register.
R1 Control register 2 **(W 00H)**	D7	ADX	X address setting	0: X0 → X175 1: X175 → X0 If RGBI/F, this setting is invalid and the only effective parameter is D7=D6=0.
	D6	ADR	Y address setting	0: Y0 → Y239 1: Y239 → Y0 If RGBI/F, this setting is invalid and the only effective parameter is D7=D6=0.
	D5			
	D4	GSEL	Specifies the potential of V0 and V63	0: Fix to V0=VDHR and V63=VSS 1: Depends on the configuration of GHP/GHN/GLP/GLN registers
	D3			
	D2			
	D1	LTS	Specifies the calibration period	0: 1 line cycle = tcal 1: 1 line cycle = tcal × 2 tcal = the number of clock by calibration x 1 cycle time of SYSCLK
	D0	OSCSTBY	IS2200 oscillation circuit control	0: Activates oscillation 1: Stops oscillation
R2 RGB interface register **(W 00H)**	D7			
	D6			
	D5			
	D4			
	D3	WNRGB	RGB interface circuit writing mode selection	0: Requires 1-frame data always. 1: Requires data only for the window area.
	D2	RGBS	RGB interface circuit mode selection	0: Capture mode 1: Prohibited
	D1	DISPCK	Selects display timing at the RGB interface circuit	0: Synchronized with SYSCLK and displays. 1: Synchronized with VSYNC and HSYNC, and displays.
	D0	NWRGB	RGB I/F pin control	0: Invalid to write to the display data RAM from the RGB interface circuit. 1: Writes to the display data RAM from the RGB interface circuit.
R3 Reset register **(W 00H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2			
	D1			
	D0	RES	Command reset of the IS2100	0: Normal operation 1: Reset operation This bit automatically becomes 0 when the first subsequent command or data is issued after the register initialization. All the registers for the IS2100 and the IS2200 will be initialized to the default settings.

Register	Bit	Symbol	Function	Configuration
R5 Data access control Register **(W 00H)**	D7			
	D6	BSTR	Selects writing mode to the display data RAM.	0: Normal write mode. 1: High-speed RAM-write mode.
	D5			
	D4	WAS	Specifies the window access mode.	0: Normal writing mode. 1: Window access mode. R2: D0=NWRGB=1 setting comes first to WAS setting, thus window access mode is active.
	D3			
	D2	INC	Specifies the increment direction of the address.	0: X address increment 1: Y address increment. ("1" is prohibited when the high speed RAM writing is in use. This setting is prohibited when RGB interface circuit is in use.)
	D1			
	D0			
R6 X address register **(W 00H)**	D7	XA7	R6: Specifies X-start address setting of the display data RAM.	Set within the range of 00H - AFH. *Note: R6 is invalid when R2:D0=NWRGB=1.
	D6	XA6		
	D5	XA5		
	D4	XA4		
	D3	XA3		
	D2	XA2		
	D1	XA1		
	D0	XA0		
R7 Y address register **(W 00H)**	D7	YA7	Specifies Y-start address of the display data RAM.	Set within the range of H - EFH. *Note: R7 is invalid when R2:D0=NWRGB=1.
	D6	YA6		
	D5	YA5		
	D4	YA4		
	D3	YA3		
	D2	YA2		
	D1	YA1		
	D0	YA0		
R8 MINX address register **(W 00H)**	D7	XMIN7	X-start address for the window access mode.	Set within the range of 00H - AFH. After X address increases up to a X address which is specified by the MAXX address register (R9), X address restarts back from the value of R8.
	D6	XMIN6		
	D5	XMIN5		
	D4	XMIN4		
	D3	XMIN3		
	D2	XMIN2		
	D1	XMIN1		
	D0	XMIN0		
R9 MAXX address register **(W 00H)**	D7	XMX7	X-end address for the window access mode.	
	D6	XMX6		
	D5	XMX5		
	D4	XMX4		
	D3	XMX3		
	D2	XMX2		
	D1	XMX1		
	D0	XMX0		
R10 MINY address register **(W 00H)**	D7	YMIN7	Y-start address for the window access mode.	Set within the range of 00H - EFH. After Y address increases up to a Y address, which is specified, by the MAXY address register (R11), Y address restarts back from the value of R11.
	D6	YMIN6		
	D5	YMIN5		
	D4	YMIN4		
	D3	YMIN3		
	D2	YMIN2		
	D1	YMIN1		
	D0	YMIN0		

Register	Bit	Symbol	Function	Configuration
R11 MAXY address register **(W 00H)**	D7	YMX7	Y-end address for the window access mode.	
	D6	YMX6		
	D5	YMX5		
	D4	YMX4		
	D3	YMX3		
	D2	YMX2		
	D1	YMX1		
	D0	YMX0		
R13 Display size setting register **(W 00H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2			
	D1			
	D0	NGO0	Selects the output number of the gate driver.	0: 240 raster-rows 1: 220 raster-rows
R15 Scroll area start register **(W 00H)**	D7	SSL7	Specifies the start line of the scroll area.	Set within the range of 00H - EFH. When the screen scroll display is in use, a displayed picture which is specified in the scroll area raster-row number register (R16) will be scrolled up by the amount which is specified in the scroll step number register (R17).
	D6	SSL6		
	D5	SSL5		
	D4	SSL4		
	D3	SSL3		
	D2	SSL2		
	D1	SSL1		
	D0	SSL0		
R16 Scroll area raster-row number register **(W 00H)**	D7	SAW7	Specifies the raster-row number of the scroll area.	
	D6	SAW6		
	D5	SAW5		
	D4	SAW4		
	D3	SAW3		
	D2	SAW2		
	D1	SAW1		
	D0	SAW0		
R17 Scroll step number register **(W 00H)**	D7	SST7	Specifies the amount of scroll.	
	D6	SST6		
	D5	SST5		
	D4	SST4		
	D3	SST3		
	D2	SST2		
	D1	SST1		
	D0	SST0		
R18 Partial-off area color register 1 **(W 00H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2			
	D1			
	D0	PSEL	Specifies the color of the partial-off area.	0: Display the color set in the R19 register. 1: Display the color that is determined by the upper bit of each pixel of the display data RAM.
R19 Partial-off area color register 2 **(W 00H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2	PGR	Specifies the display color for pixel 1.	0: Displays 0 1: Displays 1
	D1	PGG	Specifies the display color for pixel 2.	0: Displays 0 1: Displays 1
	D0	PGB	Specifies the display color for pixel 3.	0: Displays 0 1: Displays 1

Register	Bit	Symbol	Function	Configuration
R20 Partial 1 display area start register **(W 00H)**	D7	P1SL7	Specifies the starting raster-row number of the partial 1 area.	Set within the range of 00H – DBH (220 raster-rows) or 00H – EFH (240 raster-rows)
	D6	P1SL6		
	D5	P1SL5		
	D4	P1SL4		
	D3	P1SL3		
	D2	P1SL2		
	D1	P1SL1		
	D0	P1SL0		
R21 Partial 2 display area start register **(W 00H)**	D7	P2SL7	Specifies the starting raster-row number of the partial 2 area	Set within the range of 00H – DBH (220 raster-rows) or 00H – EFH (240 raster-rows)
	D6	P2SL6		
	D5	P2SL5		
	D4	P2SL4		
	D3	P2SL3		
	D2	P2SL2		
	D1	P2SL1		
	D0	P2SL0		
R22 Partial 1 display area raster-row number register **(W 00H)**	D7	P1AW7	Specifies the number of raster-rows in the partial 1 area.	Set "R20 + R22" within the range of 01H – DCH (220 raster-rows) or 01H – F0H (240 raster-rows) 1 raster-row will be displayed even when 00H is set.
	D6	P1AW6		
	D5	P1AW5		
	D4	P1AW4		
	D3	P1AW3		
	D2	P1AW2		
	D1	P1AW1		
	D0	P1AW0		
R23 Partial 2 display area raster-row number register **(W 00H)**	D7	P2AW7	Specifies the number of raster-rows in the partial 2 area.	Set "R21 + R23" within the range of 00H – DCH (220 raster-rows) or 00H – F0H (240 raster-rows)
	D6	P2AW6		
	D5	P2AW5		
	D4	P2AW4		
	D3	P2AW3		
	D2	P2AW2		
	D1	P2AW1		
	D0	P2AW0		
R24 Power supply system control register 1 **(W 00H)**	D7			
	D6	RGONR	Controls the VR regulator.	0: VR regulator = OFF. The output is Hi-Z 1: VR regulator = ON.
	D5			
	D4	VS3ON	Controls the step-up of VSS3 and VSS4.	0: VSS3 and VSS4 step-up OFF. The output is VSS1 1: VSS3 and VSS4 step-up ON
	D3	VS2ON	Controls the step-up of VSS2.	0: VSS2 step-up OFF. The output is VSS1 1: VSS2 step-up ON.
	D2	VD2ON	Controls the step-up of VDD2.	0: VDD2 step-up OFF. The output is VR. 1: VDD2 step-up ON.
	D1	VD1ON	Controls the step-up of VDD1.	0: VDD1 step-up OFF. The output is VDD2 1: VDD1 step-up ON.
	D0	DCON	Controls the DC/DC converter.	0: DC/DC converter OFF. VS, VDHR, VR, COMH, COML, VCOM, VGOFF become VSS1. 1: DC/DC converter ON.
R25 Power supply system control register 2 **(W 00H)**	D7			
	D6			
	D5			
	D4	VRSEL2	Selects the output voltage of the VR regulator.	(VRSEL2, VRSEL1, VRSEL0) = 000: 1.8V (VRSEL2, VRSEL1, VRSEL0) = 001: 1.9V (VRSEL2, VRSEL1, VRSEL0) = 010: 2.0V (VRSEL2, VRSEL1, VRSEL0) = 011: 2.2V (VRSEL2, VRSEL1, VRSEL0) = 100: 2.4V (VRSEL2, VRSEL1, VRSEL0) = 101: 2.6V (VRSEL2, VRSEL1, VRSEL0) = 110: 2.7V (VRSEL2, VRSEL1, VRSEL0) = 111: 2.8V
	D3	VRSEL1		
	D2	VRSEL0		
	D1			
	D0			

Register	Bit	Symbol	Function	Configuration
R26 Power supply system control register 3 **(W 05H)**	D7			
	D6	FUP	Specifies fdcdc frequency for the DC/DC converter.	0: fdcdc 1: fdcdc × 2
	D5	CLS1	Specifies frequency for the DC/DC Converter.	(CLS1, CLS0)=00：SYSCLK÷40 (CLS1, CLS0)=01：SYSCLK÷30 (CLS1, CLS0)=10：SYSCLK÷20 (CLS1, CLS0)=11：Prohibited
	D4	CLS0		
	D3	FS3	Selects step-up frequencies for VDD1, VSS2, VSS3 and VSS4.	(FS3, FS2) = 00: fdcdc/2 (FS3, FS2) = 01: fdcdc/4 (FS3, FS2) = 10: fdcdc/8 (FS3, FS2) = 11: fdcdc/16
	D2	FS2		
	D1	FS1	Selects the step-up frequency for VDD2.	(FS1, FS0) = 00: fdcdc/2 (FS1, FS0) = 01: fdcdc/4 (FS1, FS0) = 10: fdcdc/8 (FS1, FS0) = 11: fdcdc/16
	D0	FS0		
R27 Power supply system control register 4 **(W 0AH)**	D7			
	D6			
	D5			
	D4			
	D3	VSEL2	Selects the output voltage of the VS/VDHR regulator.	(VSEL2, VSEL1, VSEL0) = 000: 3.5V (Prohibited to use.) (VSEL2, VSEL1, VSEL0) = 001: 4.0V (VSEL2, VSEL1, VSEL0) = 010: 4.25V (VSEL2, VSEL1, VSEL0) = 011: 4.5V (VSEL2, VSEL1, VSEL0) = 100: 4.75V (VSEL2, VSEL1, VSEL0) = 101: 5.0V (VSEL2, VSEL1, VSEL0) = 110: 5.25V (VSEL2, VSEL1, VSEL0) = 111: 5.25V
	D2	VSEL1		
	D1	VSEL0		
	D0	RGON	Controls the VS/VDHR regulator.	0: VS regulator OFF; The VS output is Hi-Z, VDHR is VSS1 1: VS regulator ON
R29 Power supply system control register 6 **(W 07H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2	SCN2	Selects the gate scan mode.	(SCN2, SCN1, SCN0) = XX0: MODE5 (SCN2, SCN1, SCN0) = 001: MODE4 (SCN2, SCN1, SCN0) = 101: MODE3 (SCN2, SCN1, SCN0) = 011: MODE2 (SCN2, SCN1, SCN0) = 111: MODE1
	D1	SCN1		
	D0	SCN0		
R30 Power supply system control register 7 **(W 00H)**	D7			
	D6			
	D5			
	D4	COMHI	Controls the VCOM output.	0: Hi-Z 1: Output
	D3			
	D2			
	D1			
	D0			
R31 Power supply system control register 8 **(W 3FH)**	D7	DA7	Specifies the VCOM amplitude.	Set within the range of 33H – B4H. Other configurations are prohibited (VDC=2.8V.)
	D6	DA6		
	D5	DA5		
	D4	DA4		
	D3	DA3		
	D2	DA2		
	D1	DA1		
	D0	DA0		

Register	Bit	Symbol	Function	Configuration
R32 Power supply system control register 9 **(W 00H)**	D7	CDA7	Specifies the VCOM center value.	Set within the range of 00H - B6H. Other configurations are prohibited. (VDC=2.8V)
	D6	CDA6		
	D5	CDA5		
	D4	CDA4		
	D3	CDA3		
	D2	CDA2		
	D1	CDA1		
	D0	CDA0		
R33 Power supply system control register 10 **(W 00H)**	D7			
	D6			
	D5	PONM	Specifies the DC/DC boot mode.	0: External sequence 1: Internal sequence (Prohibited for use.)
	D4	PON	Controls the external sequence of the DC/DC booting.	0: Supply power-supply output 1: During sequence booting
	D3			
	D2			
	D1			
	D0			
R34 Power supply system control register 11 **(W 00H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2			
	D1			
	D0	RES	IS2200 command reset.	0: Normal operation This bit automatically becomes 1: Reset operation 0 after initializing the register.
R45 Calibration register **(W 01H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2			
	D1			
	D0	OC	Executes calibration.	0: Starts calibration 1: Stops calibration
R49 ID code register 1 **(W 10h)**	D7	MCOD3	A register to read manufacturer codes	1H for this product.
	D6	MCOD2		
	D5	MCOD1		
	D4	MCOD0		
	D3	VCOD3	A register to read the LSI version.	Depends on the version of the product.
	D2	VCOD2		
	D1	VCOD1		
	D0	VCOD0		
R50 ID code register 2 **(W 00H)**	D7	DCOD7	A register to read the LSI's device codes.	00H for this product.
	D6	DCOD6		
	D5	DCOD5		
	D4	DCOD4		
	D3	DCOD3		
	D2	DCOD2		
	D1	DCOD1		
	D0	DCOD0		
R51 n raster-row register **(W 01H)**	D7		Specifies the number of raster-rows for the n raster-row reverse	Set within the range of 01H - 78H.
	D6	NLINE6		
	D5	NLINE5		
	D4	NLINE4		
	D3	NLINE3		
	D2	NLINE2		
	D1	NLINE1		
	D0	NLINE0		

Register	Bit	Symbol	Function	Configuration
R52 Partial gate register 1 **(W 01H)**	D7	GSMLN7	Specifies the gate scanning of the Partial-off display area in the n raster-row reverse	0H: Doesn't scan the partial non-display area 1H: Scan the partial non-display area every other frames. 2H: Scan the partial non-display area every two frames : 255H: Scan the partial non-display area every 255 frames
	D6	GSMLN6		
	D5	GSMLN5		
	D4	GSMLN4		
	D3	GSMLN3		
	D2	GSMLN2		
	D1	GSMLN1		
	D0	GSMLN0		
R53 Partial gate register 2 **(W 00H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2			
	D1			
	D0	PNFRM	Specifies the gate reverse method in the partial-off display area	Only available in the raster-row reverse 0: Raster-row reverse. 1: Reversed frame.
R55 Gate-scan operation selection register **(W 00H)**	D7		Specifies the method of gate scanning	(GSCAN2, GSCAN1, GSCAN0) = (000): Frame reverse (GSCAN2, GSCAN1, GSCAN0) = (001): n raster-row reverse (GSCAN2, GSCAN1, GSCAN0) = (010): Skip reverse 1A (GSCAN2, GSCAN1, GSCAN0) = (011): Skip reverse 1B (GSCAN2, GSCAN1, GSCAN0) = (100): Skip reverse 1C (GSCAN2, GSCAN1, GSCAN0) = (101): Skip reverse 2A (GSCAN2, GSCAN1, GSCAN0) = (110): Skip reverse 2B
	D6			
	D5			
	D4			
	D3			
	D2	GSCAN2		
	D1	GSCAN1		
	D0	GSCAN0		
R58 IS2100 serial monitor register **(R 00H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2			
	D1			
	D0	SEND	IS2200 serial communication flag	0: Transfer completed 1: Under communication
R59 GOE1 output control register **(W 00H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2			
	D1			
	D0	GOE1ON	Controls the output of GOE1 pin	0: Fixes GOE1 to LOW (No turning on of the gate) 1: Normal operation
R62 RGB back porch register **(W 88H)**	D7	HBP3	Specifies the horizontal back porch period of the RGB interface.	Set equal or more than 1 H.
	D6	HBP2		
	D5	HBP1		
	D4	HBP0		
	D3	VBP3	Specifies the vertical back porch period of the RGB interface.	Set within the range of 01H - 0EH in the capture mode
	D2	VBP2		
	D1	VBP1		
	D0	VBP0		

Register	Bit	Symbol	Function	Configuration
R118 Dummy raster-row number selection register **(W 00H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2			
	D1			
	D0	DMYSEL	Configures the blanking period	0: 1 dummy raster-row only 1: 1 dummy raster-row ＋7 blanking period
R136 Source on register **(W 02H)**	D7	SON7	Specifies the start timing of the source output.	Specifies the time from horizontal period by the SYSCLK number
	D6	SON6		
	D5	SON5		
	D4	SON4		
	D3	SON3		
	D2	SON2		
	D1	SON1		
	D0	SON0		
R137 Gate-on register **(W 03H)**	D7	GON7	Specifies the start timing of the gate-output.	Specifies the time from horizontal period by the SYSCLK number.
	D6	GON6		
	D5	GON5		
	D4	GON4		
	D3	GON3		
	D2	GON2		
	D1	GON1		
	D0	GON0		
R 138 IS2200 expansion setting register **(W 00H)**	D7			
	D6	0		Must be fixed to 0
	D5			
	D4	0		Must be fixed to 0
	D3	QBST		Must be fixed to 0
	D2			
	D1	0		Must be fixed to 0
	D0	0		Must be fixed to 0
R139 Raster-row clock register **(W 25H)**	D7	HCK7	Specifies the period for the number of 1 raster-row.	R141: CLKM=0 => a calibrated clock number is written. R141: CLKM=1 => Set a raster-row clock number; the integer of HCK close to a target frame frequency calculated with SYSCLK number. *Note: HCK setting is invalid without setting CLKM=1, therefore the default setting of HCK=25H stays effective.
	D6	HCK6		
	D5	HCK5		
	D4	HCK4		
	D3	HCK3		
	D2	HCK2		
	D1	HCK1		
	D0	HCK0		
R140 Scan raster-row register **(R 00H)**	D7	SLR7	A register to read the raster-row number under scanning.	Capable of reading the raster-row number under scanning.
	D6	SLR6		
	D5	SLR5		
	D4	SLR4		
	D3	SLR3		
	D2	SLR2		
	D1	SLR1		
	D0	SLR0		
R141 Raster-row cycle control mode register **(W 40H)**	D7	GOF6	Specifies the period when the gate raster-rows is on.	Specify the period by the SYSCLK number.
	D6	GOF5		
	D5	GOF4		
	D4	GOF3		
	D3	GOF2		
	D2	GOF1		
	D1	GOF0		
	D0	CLKM	Specifies the raster-row frequency control mode.	0: Calibration mode 1: Register setting mode

Register	Bit	Symbol	Function	Configuration
R143 Gamma adjustment register 1 **(W 05H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”. Note: The setting of this register is invalid when D4=GSEL of the control register 2 (R1) is set as 0.
	D6			
	D5	GHP5		
	D4	GHP4		
	D3	GHP3		
	D2	GHP2		
	D1	GHP1		
	D0	GHP0		
R144 Gamma adjustment register 2 **(W 05H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”. Note: The setting of this register is invalid when D4=GSEL of the control register 2 (R1) is set as 0.
	D6			
	D5	GLP5		
	D4	GLP4		
	D3	GLP3		
	D2	GLP2		
	D1	GLP1		
	D0	GLP0		
R145 Gamma adjustment register 3 **(W 44H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”.
	D6	F1P2		
	D5	F1P1		
	D4	F1P0		
	D3			
	D2	F0P2		
	D1	F0P1		
	D0	F0P0		
R146 Gamma adjustment register 4 **(W 44H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”.
	D6	F3P2		
	D5	F3P1		
	D4	F3P0		
	D3			
	D2	F2P2		
	D1	F2P1		
	D0	F2P0		
R147 Gamma adjustment register 5 **(W 44H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”.
	D6	F5P2		
	D5	F5P1		
	D4	F5P0		
	D3			
	D2	F4P2		
	D1	F4P1		
	D0	F4P0		
R148 Gamma adjustment register 6 **(W 33H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”.
	D6	SLP2		
	D5	SLP1		
	D4	SLP0		
	D3			
	D2	SHP2		
	D1	SHP1		
	D0	SHP0		
R149 Gamma adjustment register 7 **(W 05H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”. Note: The setting of this register is invalid when D4=GSEL of the control register 2 (R1) is set as 0.
	D6			
	D5	GHN5		
	D4	GHN4		
	D3	GHN3		
	D2	GHN2		
	D1	GHN1		
	D0	GHN0		

Register	Bit	Symbol	Function	Configuration
R150 Gamma adjustment register 8 **(W 05H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”. Note: The setting of this register is invalid when D4=GSEL of the control register 2 (R1) is set as 0.
	D6			
	D5	GLN5		
	D4	GLN4		
	D3	GLN3		
	D2	GLN2		
	D1	GLN1		
	D0	GLN0		
R151 Gamma adjustment register 9 **(W 44H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”.
	D6	F1N2		
	D5	F1N1		
	D4	F1N0		
	D3			
	D2	F0N2		
	D1	F0N1		
	D0	F0N0		
R152 Gamma adjustment register 10 **(W 44H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”.
	D6	F3N2		
	D5	F3N1		
	D4	F3N0		
	D3			
	D2	F2N2		
	D1	F2N1		
	D0	F2N0		
R153 Gamma adjustment register 11 **(W 44H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”.
	D6	F5N2		
	D5	F5N1		
	D4	F5N0		
	D3			
	D2	F4N2		
	D1	F4N1		
	D0	F4N0		
R154 Gamma adjustment register 1 **(W 33H)**	D7		Gamma adjustment register	Refer to “11. Gamma Correction Function”.
	D6	SLN2		
	D5	SLN1		
	D4	SLN0		
	D3			
	D2	SHN2		
	D1	SHN1		
	D0	SHN0		
R157 MPU 5 mode MSB output switching register **(W 00H)**	D7			
	D6			
	D5			
	D4			
	D3			
	D2			
	D1			
	D0	MSBF	Selects the MPU5 mode	0: MPU5 mode A (Lower 6 bits are valid) 1: MPU5 mode B (Upper 6 bits are valid)

22. Absolute Maximum Ratings

Item	Symbol	Rated value	Unit	Note
Power supply (1)	V18-GND	-0.3 – +2.4	V	
Power supply (2)	VCC11-GND	-0.3 – +7.0	V	
Input voltage for digital system	Vin	-0.3 – VCC11+0.3	V	
Power supply (3)	VS-GND	-0.3 – +7.0	V	
Power supply (4)	VDHR-GND	-0.3 – +7.0	V	
Operating temperature	Topr	-40 – +85	°C	
Storage temperature	Tstr	-55 – +100	°C	

23. DC Characteristics

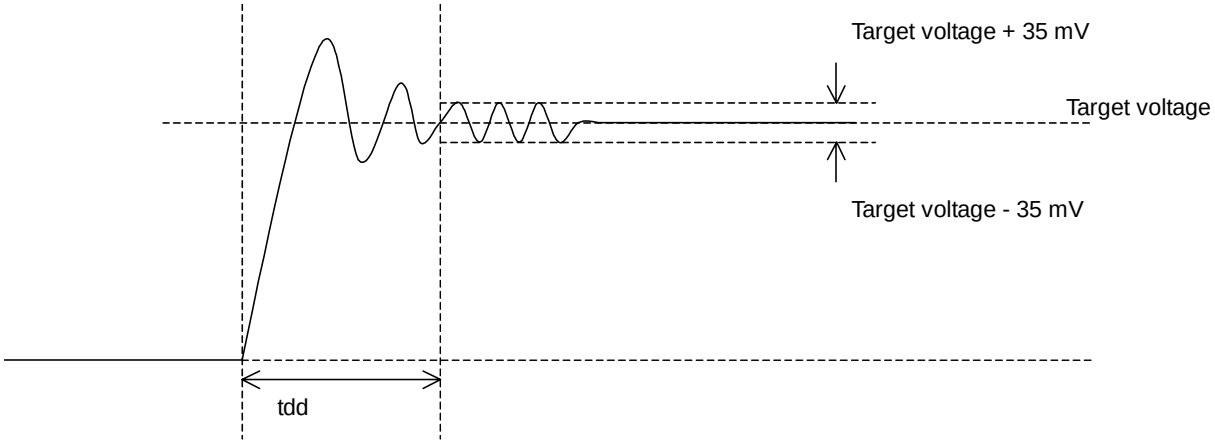
23.1. Electric Characteristics

TA = Room temperature

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Digital voltage		V18		1.8	2.0	2.2	V
I/O power supply		VCC11		1.7	1.8	1.95	V
				2.5	2.8	3.1	
Voltage for the source line drive		VS		4.0		5.25	V
Grayscale reference voltage		VDHR		4.0		5.25	V
Input voltage for digital system “H”		Vih		VCC11 x 0.8		VCC11	V
Input voltage for digital system “L”		Vil		VSS		VCC11 x 0.2	V
Output voltage for digital system “H”		Voh		VCC11 x 0.8		VCC11	V
Output voltage for digital system “L”		Vol		VSS		VCC11 x 0.2	V
Digital system	Operating current 1	I1	With no-load, 260,000-color still picture		150	350	uA
	Operating current 2	I2	With no-load, 8-color still picture		150	350	uA
	Operating current 3	I3	Stand-by current		2	10	uA
Analog system	Operating current 1	I4	When no-load, 260,000-color still picture		150	500	uA
	Operating current 2	I5	When no-load, 8-color still picture		150	500	uA
	Operating current 3	I6	Stand-by current		1	6	uA
Output resistance		Ron			3	5	kΩ
Output voltage deviation		ΔVo	VS = 5.0V Grayscale output = 1.65V		7	20	mV
			VS = 5.0V Grayscale output = 2.50V		7	20	mV
Output voltage range		Vo	GSEL=1 (The voltages of V0 and V63 at GSEL=0 are excluded.)	VSS + 0.2		VS - 0.2	V

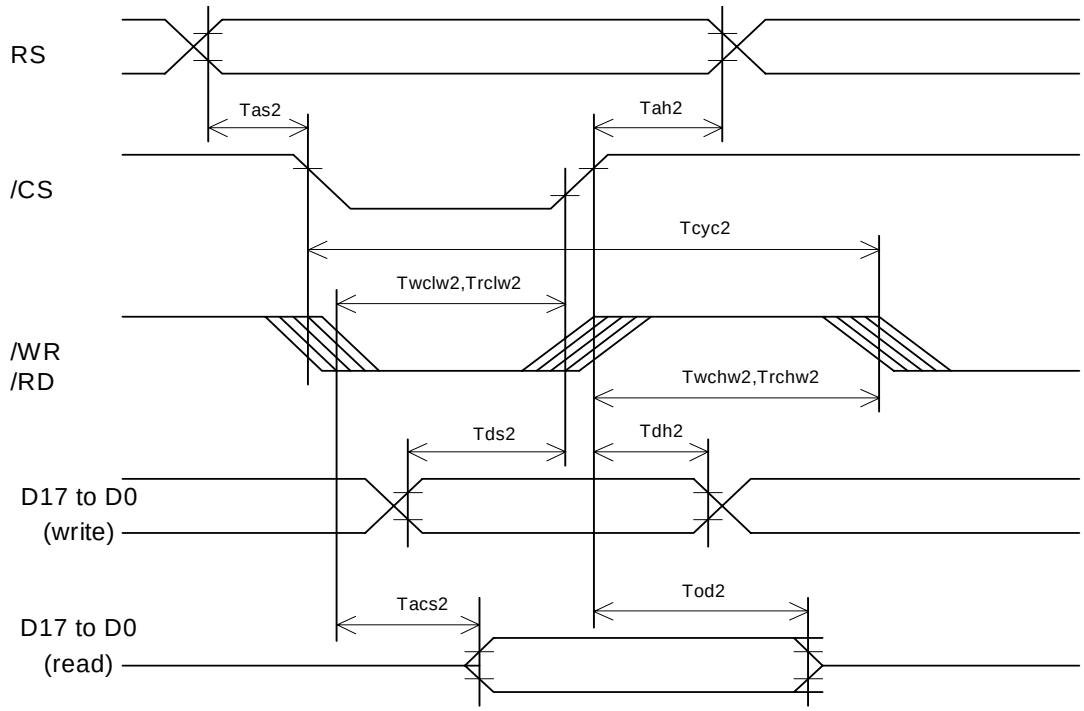
23.2. LCD Driver Output Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max
Driver output delay time	tdd	us	VDHR=5V VS=5V Ta=Room temperature 1 kΩ + 22pF		30	45



24. AC Characteristics

24.1. i80-series MPU Connection



[VCC11 = 2.5V - 3.1V, V18 = 1.8V - 2.2V, Ta = Room temperature] (In Normal writing mode)

Parameter	Symbol	Signal	Min.	Max.	Unit
Address set-up time	Tas2	RS /CS	0		ns
Address hold time	Tah2		0		ns
System cycle time	Tcyc2		390		ns
WR control H pulse length	Twchw2	/WR (R/W)	110		ns
WR control L pulse length	Twclw2		130		ns
RD control H pulse length	Trchw2	/RD (E)	100		ns
RD control L pulse length	Trclw2		140		ns
Data set-up time	Tds2	D17 to D0	80		ns
Data hold time	Tdh2		0		ns
Access time (CL=100pF)	Tacs2	D17 to D0		110	ns
Output invalid time	Tod2		10	100	ns

[VCC11 = 2.5V - 3.1V, V18 = 1.8V – 2.2V, Ta = Room temperature]

（In High-speed RAM write mode. / MPU1, MPU4）

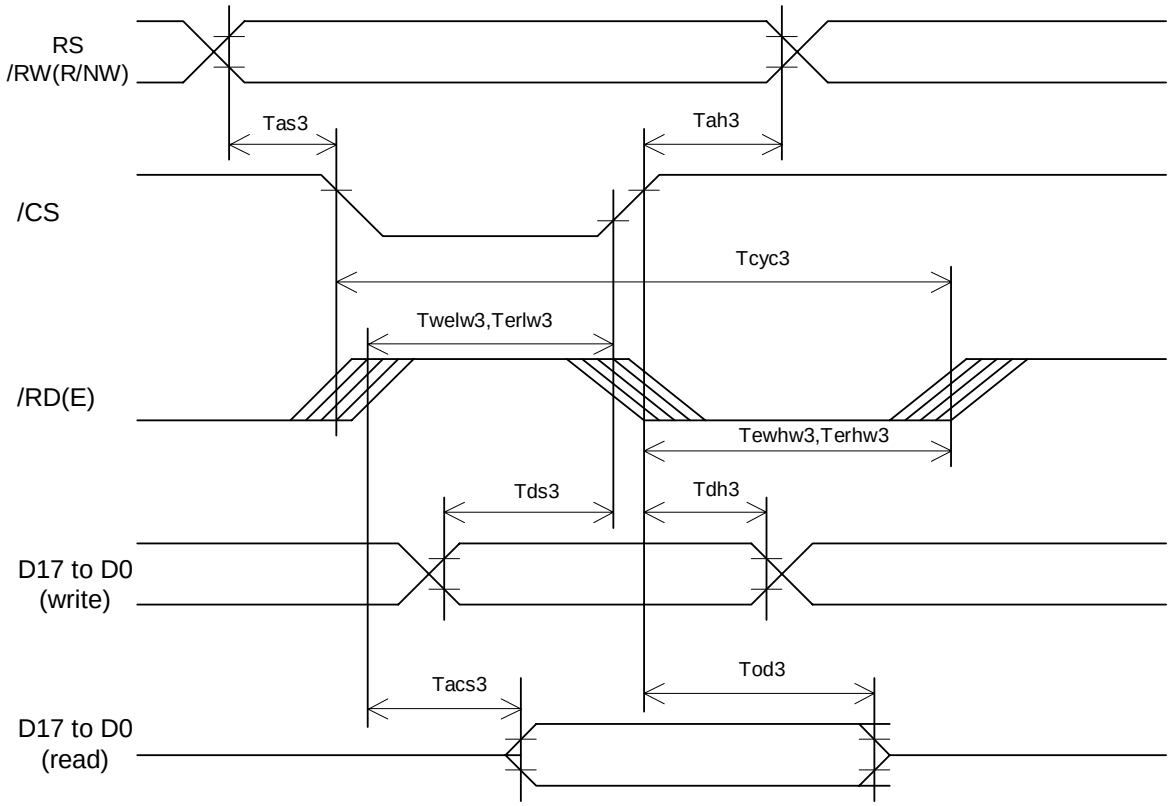
Parameter	Symbol	Signal	Min.	Max.	Unit
Address set-up time	Tas2	RS /CS	0		ns
Address hold time	Tah2		0		ns
System cycle time	Tcyc2		230		ns
WR control H pulse length	Twchw2	/WR (R/W)	110		ns
WR control L pulse length	Twclw2		120		ns
Data set-up time	Tds2	D17 to D0	40		ns
Data hold time	Tdh2		0		ns

[VCC11 = 2.5V - 3.1V, V18 = 1.8V – 2.2V, Ta = Room temperature]

（In High-speed RAM write mode./ MPU2, MPU3, MPU5 mode）

Parameter	Symbol	Signal	Min.	Max.	Unit
Address set-up time	Tas2	RS /CS	0		ns
Address hold time	Tah2		0		ns
System cycle time	Tcyc2		230		ns
WR control H pulse length	Twchw2	/WR (R/W)	110		ns
WR control L pulse length	Twclw2		120		ns
Data set-up time	Tds2	D17 to D0	40		ns
Data hold time	Tdh2		0		ns

24.2. M68-series MPU Connection



[VCC11 = 2.5V - 3.1V, V18 = 1.8V - 2.2V, Ta = Room temperature] (In normal writing mode)

Parameter	Symbol	Signal	Min.	Max.	Unit
Address set-up time	Tas3	RS /CS	0	---	ns
Address hold time	Tah3		0	---	ns
System cycle time	Tcyc3		390	---	ns
Enable H pulse length (write)	Tewhw3	NRD (E)	110	---	ns
Enable L pulse length (write)	Tewlw3		130	---	ns
Enable H pulse length (read)	Terhw3		100	---	ns
Enable L pulse length (read)	Terlw3		140	---	ns
Data set-up time	Tds3	D17 to D0	80	---	ns
Data hold time	Tdh3		0	---	ns
Access time (CL=100pF)	Tacs3	D17 to D0		110	ns
Output invalid time	Tod3			100	ns

[VCC11 = 2.5V - 3.1V, V18 = 1.8V - 2.2V, Ta = Room temperature]

(In High speed RAM writing mode/MPU1, MPU4 mode)

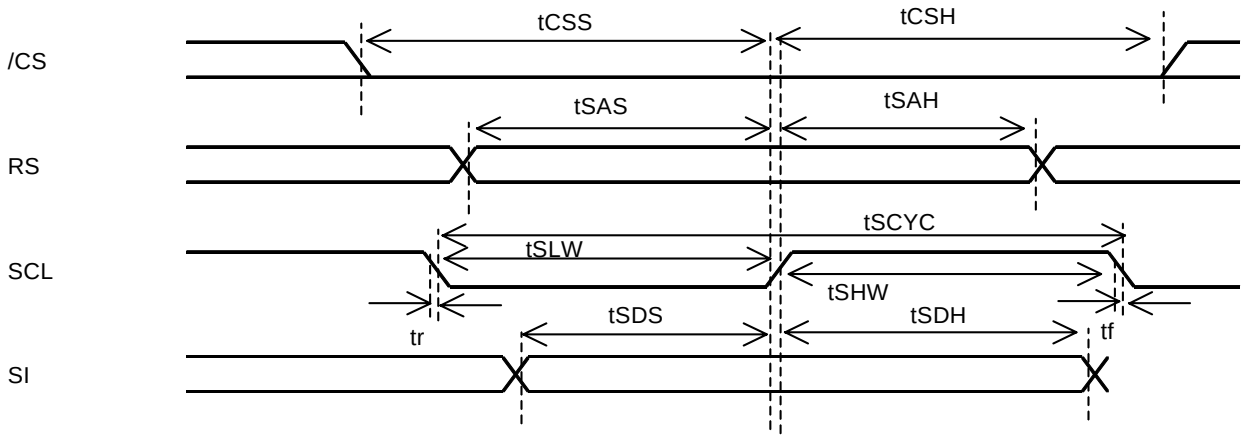
Parameter	Symbol	Signal	Min.	Max.	Unit
Address set-up time	Tas3	RS /CS	0	---	ns
Address hold time	Tah3		0	---	ns
System cycle time	Tcyc3		230	---	ns
Enable H pulse length (write)	Tewhw3	NRD (E)	110	---	ns
Enable L pulse length (write)	Tewlw3		120	---	ns
Data set-up time	Tds3	D17 to D0	40	---	ns
Data hold time	Tdh3		0	---	ns

[VCC11 = 2.5V - 3.1V, V18 = 1.8V - 2.2V, Ta = Room temperature]

(In High speed RAM writing mode/MPU2, MPU3, MPU5 mode)

Parameter	Symbol	Signal	Min.	Max.	Unit
Address set-up time	Tas3	RS /CS	0	---	ns
Address hold time	Tah3		0	---	ns
System cycle time	Tcyc3		230	---	ns
Enable H pulse length (write)	Tewhw3	NRD (E)	110	---	ns
Enable L pulse length (write)	Tewlw3		120	---	ns
Data set-up time	Tds3	D17 to D0	40	---	ns
Data hold time	Tdh3		0	---	ns

24.3 Serial Interface Circuit



[VCC11 = 2.5V - 3.1V, V18 = 1.8V - 2.2V, Ta = Room temperature]

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Serial clock cycle	tSCYC	SCL	200			ns
SCL H level pulse length	tSHW	SCL	60			ns
SCL L level pulse length	tSLW	SCL	85			ns
Address hold time	tSAH	RS	90			ns
Address set up time	tSAS	RS	90			ns
Data set-up time	tSDS	SI	60			ns
Data hold time	tSDH	SI	60			ns
CS - SCL time	tCSS	/CS	90			ns
	tCSH	/CS	90			ns

tr and tf are regulated at 15 ns or under.

24.4. RGB Interface Circuit

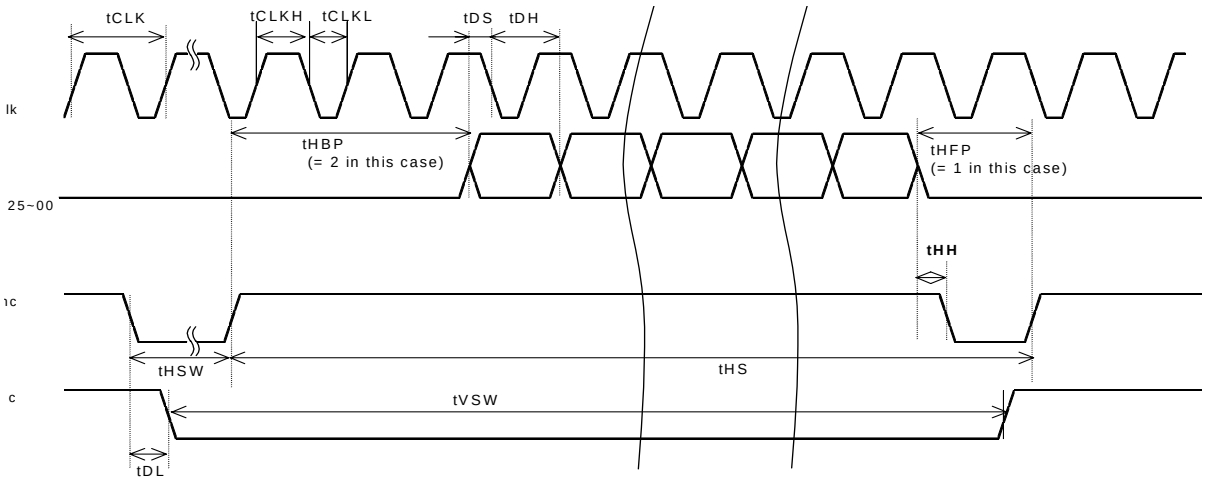


Fig. 24-1 Horizontal timing

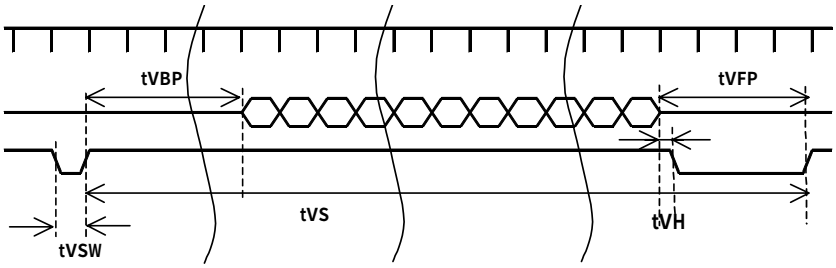


Fig. 24-2 Vertical timing

[VCC11 = 2.5V - 3.1V, V18 = 1.8V - 2.2V, Ta = Room temperature]

Item	Symbol	Conditions	Min.	Type.	Max.	Unit
Dot clock cycle	tCLK		500			ns
Dot clock H pulse width	tCLKH		125			ns
Dot clock L pulse width	tCLKL		125			ns
Data set up time	tDS		60			ns
Data hold time	tDH		60			ns
Hsync pulse width	tHSW		1			Dotclk
Hsync H pulse hold time	tHH		0			ns
Horizontal back porch time	tHBP		1			Dotclk
Horizontal front porch time	tHFP		1			Dotclk
Hsync cycle time	tHS		178		512	Dotclk
Vsync pulse width	tVSW		1			HS
Vsync H pulse hold time	tVH		0			ns
Vsync cycle time	tVS	R13: D0/NGO0=1	225			HS
		R13: D0/NGO0=0	245			HS
Vertical back porch time	tVBP		1			HS
Vertical front porch time	tVFP		1			HS
Vsync set-up time	tDL			0		Dotclk

27. Note

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28. Revision History

28.1. Complete revision from Version 0.72 to Version 1.0

28.2. Revision from Version 1.0 to Version 1.1

Page	Version 1.0	Version 1.1
All		Corrected any of the misspelled words and added missing words. No change to the content.
1,2		Added the Contents
21	6. Table 6-1	Changed back to the table in Version 0.72.
34	7.1.	Added Setting the start address when writing to the RAM
35	7.4. (Prohibited to use)	Deleted (Prohibited to use) Added; (ADC=1,ADX=1), (ADC=0, ADX=0)----Valid (ADC=1,ADX=0), (ADC=0, ADX=1)----Prohibited to use
42	9.1.3.	Added; R137, R141 setting restrictions (GON+GOF)=<(HCK-2)
50	11.5 Table 11-2	Changed to; SUMR: {ladder resistance sum(GH+GL+SH+SL+121)-GH}✕R GH: (GHP, GHN selected value) x R GL: (GLP, GLN selected value) x R SH: (SHP, SHN selected value) X 4R SL: (SLP, SLN selected value) X 4R
52	11.5 GHP/GHN GLP/GLN	Added; Note!! 1) If you set GHP/GHN and GLP/GLN other than as 0, please make sure to set as follows; V0≤VS-0.2V, V63≥VSS+0.2V. 2) If you set GHP/GHN as 0, V0 equals to VS. Please make sure to set as V1≤VS-0.2V. 3) If you set GLP/GLN as 0, V63 equals to VSS. Please make sure to set as V62≥VSS+0.2V.

<table>
<tr><td>71</td><td>17.4.</td><td>Added; <u>This register is invalid when the LCD displays pictures in synchronization with the external clock.</u></td></tr>
<tr><td>72</td><td>18.1 - 18.8</td><td>Deleted 18.1 - 18.8</td></tr>
<tr><td>78</td><td>R24</td><td>Changed VCC1 to VR, VDC to VDD2.</td></tr>
<tr><td>86</td><td>V18</td><td>Changed to;
<table>
<tr><th>Item</th><th>Symbol</th><th>Condition</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th></tr>
<tr><td>Digital voltage</td><td>V18</td><td></td><td>1.62</td><td>1.8</td><td>1.98</td><td>V</td></tr>
</table></td></tr>
<tr><td>88~93</td><td>24.1-24.4 V18 condition</td><td>Changed to 1.62V~1.98V</td></tr>
<tr><td>88</td><td>24.1. System cycle time:
Tcyc2 min</td><td>Changed to 500ns</td></tr>
<tr><td>89</td><td>24.1. System cycle time:
Tcyc2 min
(In High-speed RAM write mode MPU1, MPU4)</td><td>Changed to 180ns</td></tr>
<tr><td>89</td><td>24.1. System cycle time:
Tcyc2 min
（In High-speed RAM write mode and MPU2, MPU3, MPU5 mode）</td><td>Changed to 110ns</td></tr>
<tr><td>90</td><td>24.2. System cycle time:
Tcyc3 min</td><td>Changed to 500ns</td></tr>
<tr><td>91</td><td>24.2. System cycle time:
Tcyc3 min
(In High-speed RAM write mode MPU1, MPU4)</td><td>Changed to 180ns</td></tr>
<tr><td>91</td><td>24.2. System cycle time:
Tcyc3 min
（In High-speed RAM write mode and MPU2, MPU3, MPU5 mode）</td><td>Changed to 110ns</td></tr>
<tr><td>93</td><td>24.4. Dot clock cycle:
tclk min</td><td>Changed to 500ns</td></tr>
</table>

28.3. Revision from Version 1.1 to Version 1.52

Complete Revision

28.4. Revision from Version1.52.to Version1.6

Page	Version 1.52	Version 1.6
All		Corrected any of the misspelled words and added missing words. No change to the content.
4		Added (Note)
93		Absolute Maximum Ratings: Revised the values.

28.4. Revision from Version1.6 to Version1.61

Page / Chapter	Ver.1.6	Ver.1.61
All		Corrected any of the misspelled words and added missing words. No change to the content.
p.85 / c.21	R0: D5=ADC 0: Y1 output corresponds to 00H of the display data RAM. 1: Y1 output corresponds to AFH of the display data RAM.	<Revision> In ADX=0 setting. 0: Y1, Y2 and Y3 output correspond to 00H of the display data RAM. 1: Y528, Y527 and Y526 output correspond to 00H of the display data RAM.
p.85 / c.21	R1: D7=ADX D6=ADR	<Addition> R1: D7=ADX D6=ADR If RGBI/F, this setting is invalid and the only effective parameter is D7=C6=0.

p.85 / c.21	R3: D0=RES 1: Reset operation This bit automatically becomes 0 after initializing the resister.	<Revision and addition> R3: D0=RES 1: Reset operation This bit automatically becomes 0 when the first subsequent command or data is issued after the register initialization. All the registers for the IS2100 and the IS2200 will be initialized to the default settings.
p.86 / c.21	R5: D4=WAS 1: Window access mode.	<Addition> R5: D4=WAS 1: Window access mode. R2: D0=NWRGB=1 setting comes first to WAS setting, thus window access mode is active.
p.42 / c.7.3	By setting D4=WAS of the register as 1, this arbitrary address area access will be available.	<Addition> By setting D4=WAS of the register as 1, this arbitrary address area access will be available. The window access mode is active when R2: D0=NWRGB=1 despite of this D4=WAS setting.
p.86 / c.21	R6: Specifies X address of the display data RAM.	<Revision> R6: Specifies X-start address setting of the display data RAM. *Note: R6 is invalid when R2:D0=NWRGB=1.
p.86 / c.21	R7: Specifies Y address of the display data RAM.	<Revision> R7: Specifies Y-start address setting of the display data RAM. *Note: R7 is invalid when R2:D0=NWRGB=1.
p.90 / c.21	R33: D5=PONM 1: Internal sequence	<Addition> R33: D5=PONM 1: Internal sequence (Prohibited for use.)

p.92 / c.21	R139 Specify the horizontal period by the SYSCLK number. R141:CLKM=0 => a calibrated clock number is written. R141:CLKM=1 => a calculated raster-row clock number is written.	<Revision and addition> R139 R141: CLKM=0 => a calibrated clock number is written. R141: CLKM=1 => Set a raster-row clock number; the integer of HCK close to a target frame frequency calculated with SYSCLK number. *Note: HCK setting is invalid without setting CLKM=1, therefore the default setting of HCK=25H stays effective.
p.52 / c.8.2.2		<Addition> *Note: HCK setting is invalid without setting CLKM=1, therefore the default setting of HCK=25H stays effective.
p.39 / c.7.1	Fig. 7-1 The address increment direction INC=0 INC=1	<Addition> Fig. 7-1 The address increment direction INC=0 INC=1 ADX=ADR=0 ADX=ADR=0
p.39 / c.7.1	You can select the address increment direction, either X or Y, by using the D2=INC bit of the R5 register.	<Addition> You can select the address increment direction, either X or Y, by using the D2=INC bit of the R5 register. *Note: Provided that this setting is prohibited when RGB interface circuit is in use.
p.86 / c.21	R5: D2=INC=1 1: Y address increment. ("1" is prohibited when the high speed RAM writing is in use.)	<Addition> R5: D2=INC=1 1: Y address increment. ("1" is prohibited when the high speed RAM writing is in use. This setting is prohibited when RGB interface circuit is in use.)
p.14, 15 / c.5.4	Bump Type C for Bump No. 108, 109, 138-167, 183-218	<Revision> Bump type revised "C->B" for Bump No. 108, 109, 138-167, 183-218.
p.42 / c.7.3		<Addition> *Note: R6 and R7 are prohibited to use when RGB interface is in use.

p.103 / c.24.4		<Addition> Added tHH in "Fig. 25-1 Horizontal timing". Added tVH in "Fig.25-2 Vertical timing". Also added items (tHH and tVH) and revised items (tVS) in the charts at the bottom, and revised item's names.
p.71 / c.15	"... distance of more than 50µs..."	<Revision> "... distance of 50µs or more..."
p.102 / c.24.3	"... as under 15 ns."	<Revision> "... as 15ns or under."
p.32 / c.6.5	7.6.1 MPU1, MPU2, MPU3, MPU4 Type	6.5.1 MPU1, MPU2, MPU3, MPU4 Type
p.32 / c.6.5	7.6.2 MPU5, MPU6, MPU7 Type	6.5.2 MPU5, MPU6, MPU7 Type
p.33 / c.6.5	7.6.3 MPU8 Type	6.5.3 MPU8 Type
p.33 / c.6.5	7.6.4 MPU 9 Type	6.5.4 MPU 9 Type