HARRIS
S E M I C O N D U C T O R

CMOS Universal Asynchronous Receiver/Transmitter (UART)

March 1997

Features

- **Low Power CMOS Circuitry. . . . . 7.5mW (Typ) at 3.2MHz (Max Freq.) at V$_{DD}$ = 5V**
- **Baud Rate**
  - **DC to 200K Bits/s (Max) at. . . . . 5V, 85°C**
  - **DC to 400K Bits/s (Max) at. . . . . .10V, 85°C**
- **4V to 10.5 Operation**
- **Automatic Data Formatting and Status Generation**
- **Fully Programmable with Externally Selectable Word Length (5 - 8 Bits), Parity Inhibit, Even/Odd Parity, and 1, 1-1/2, or 2 Stop Bits**
- **Operating Temperature Range**
  - **CDP6402D, CD . . . . -55°C to +125°C**
  - **CDP6402E, CE . . . . -40°C to +85°C**
- **Replaces Industry Type IM6402 and Compatible with HD6402**

Ordering Information

PACK-AGE	TEMP. RANGE	5V/200K BAUD	10V/400K BAUD	PKG. NO.
PDIP	-40°C to +85°C	CDP6402CE	CDP6402E	E40.6
Burn-In		CDP6402CEX	-	
SBDIP	-40°C to +85°C	CDP6402CD	CDP6402D	D40.6
Burn-In		CDP6402CDX	CDP6402DX	

Description

The CDP6402 and CDP6402C are silicon gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits for interfacing computers or microprocessors to asynchronous serial data channels. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data channels. The receiver converts serial start, data, parity, and stop bits to parallel data verifying proper code transmission, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start parity and stop bits.

The data word can be 5, 6, 7 or 8 bits in length. Parity may be odd, even or inhibited. Stop bits can be 1, 1-1/2, or 2 (when transmitting 5-bit code).
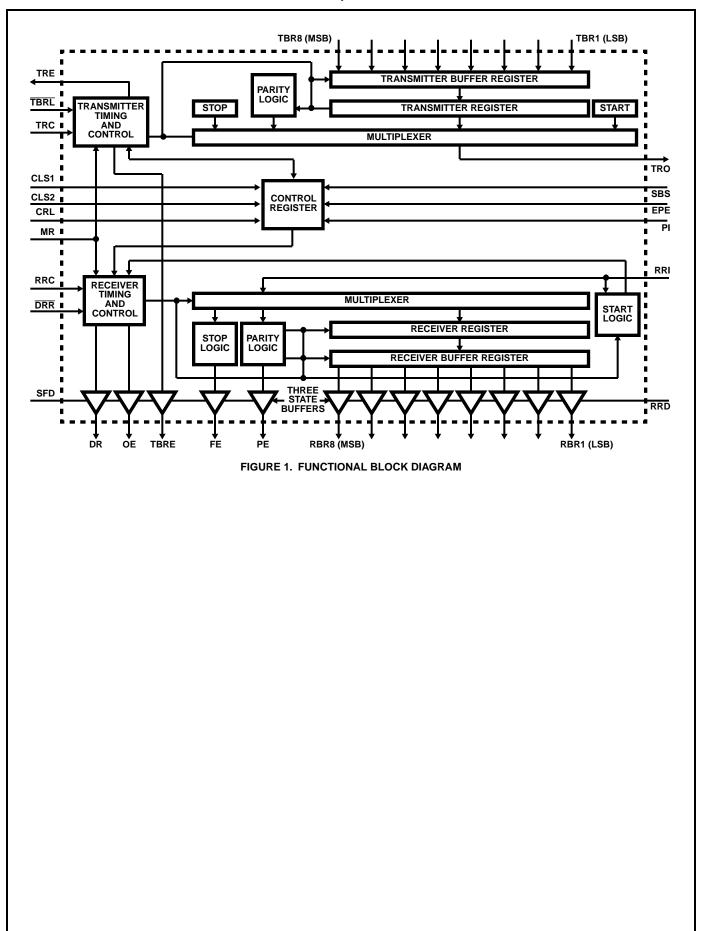
The CDP6402 and CDP6402C can be used in a wide range of applications including modems, printers, peripherals, video terminals, remote data acquisition systems, and serial data links for distributed processing systems.

The CDP6402 and CDP6402C are functionally identical. They differ in that the CDP6402 has a recommended operating voltage range of 4V to 10.5V, and the CDP6402C has a recommended operating voltage range of 4V to 6.5V.

Pinout

CDP6402, CDP6402C (PDIP, SBDIP)
TOP VIEW

Pin	Signal		Pin	Signal
1	V$_{DD}$		40	TRC
2	NC		39	EPE
3	GND		38	CLS1
4	RRD		37	CLS2
5	RBR8		36	SBS
6	RBR7		35	PI
7	RBR6		34	CRL
8	RBR5		33	TBR8
9	RBR4		32	TBR7
10	RBR3		31	TBR6
11	RBR2		30	TBR5
12	RBR1		29	TBR4
13	PE		28	TBR3
14	FE		27	TBR2
15	OE		26	TBR1
16	SFD		25	TRO
17	RRC		24	TRE
18	DRR		23	TBRL
19	DR		22	TBRE
20	RRI		21	MR

File Number **1328.2**

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings

DC Supply-Voltage Range, (V_{DD})
  CDP6402 . . . .-0.5 to +11V
  CDP6402C . . . .-0.5 to +7V
Input Voltage Range, All Inputs . . . . -0.5 to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . $\pm$100µA
Device Dissipation Per Output Transistor
  For T_A = Full Package-Temperature Range
  (All Package Types) 100mW
Operating-Temperature Range (T_A)
  Package Type D (SBDIP) . . . .-55°C to +125°C
  Package Type E (PDIP) . . . .-40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (^{o}C/W) θ_{JC} (^{o}C/W)
  PDIP Package   50   N/A
  SBDIP Package.   55   15
Maximum Junction Temperature
  Plastic Package . . . .+150°C
  Ceramic Package . . . .+175°C
Maximum Storage Temperature Range (T_{STG}) . . .-65°C to +150°C
Maximum Lead Temperature (Soldering 10s):
  At Distance 1/16 $\pm$1/32 inch (1.59 $\pm$0.79mm) . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Operating Conditions At T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

| | LIMITS | | | | |
| | CDP6402 | | CDP6402C | | |
PARAMETER	MIN	MAX	MIN	MAX	UNITS
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Static Electrical Specifications at T_A = -40°C to +85°C, V_{DD} $\pm$10%, Except as noted

| | | CONDITIONS | | | LIMITS | | | | | | |
| | | | | | CDP6402 | | | CDP6402C | | | |
PARAMETER		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	UNITS
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.01	50	-	0.02	200	µA
		-	0,10	10	-	1	200	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0,5	5	2	4	-	1.2	2.4	-	mA
		0.5	0,10	10	5	7	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-0.55	-1.1	-	-0.55	-1.1	-	mA
		9.5	0,10	10	-1.3	-2.6	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	0.8	-	-	0.8	V
		0.5, 9.5	-	10	-	-	0.2 V_{DD}	-	-	-	V

Static Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±10%, Except as noted **(Continued)**

PARAMETER		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP6402			CDP6402C			UNITS
		CONDITIONS			LIMITS						
					MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Input High Voltage	V_{IH}	0.5, 4.5	-	5	V_{DD}-2	-	-	V_{DD}-2	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0,5	5	-	±10^{-4}	±1	-	-	±1	μA
			0,10	10	-	±10^{-4}	±2	-	-	-	μA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	±10^{-4}	±1	-	±10^{-4}	±1	μA
		0, 10	0,10	10	-	±10^{-4}	±10	-	-	-	μA
Operating Current (Note 3)	I_{DD1}	-	0, 5	5	-	1.5	–	-	1.5	-	mA
		-	0,10	10	-	10	–	-	-	-	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = 25°C and nominal V_{DD}

2. I_{OL} = I_{OH} = 1μA.

3. Operating current is measured at 200kHz or V_{DD} = 5V and 400kHz for V_{DD} = 10V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2MHz).

Description of Operation

Initialization and Controls

A positive pulse on the MASTER RESET (MR) input resets the control, status, and receiver buffer registers, and sets the serial output (TRO) High. Timing is generated from the clock inputs RRC and TRC at a frequency equal to 16 times the serial data bit rate. The RRC and TRC inputs may be driven by a common clock, or may be driven independently by two different clocks. The CONTROL REGISTER LOAD (CRL) input is strobed to load control bits for PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECTS (SBS), and CHARACTER LENGTH SELECTS (CLS1 and CLS2). These inputs may be hand wired to V_{SS} or V_{DD} with CRL to V_{DD}. When the initialization is completed, the UART is ready for receiver and/or transmitter operations.

Transmitter Operation

The transmitter section accepts parallel data, formats it, and transmits it in serial form (Figure 2) on the TRO terminal.

FIGURE 2. SERIAL DATA FORMAT

Transmitter timing is shown in Figure 3. (A) Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{TBRL}$ input. Valid data must be present at least t_{DT} prior to, and t_{TD} following, the rising edge of $\overline{TBRL}$. If words less than 8-bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. (B) The rising edge of $\overline{TBRL}$ clears TBRE. 1/2 to 11/2 cycles later, depending on when the $\overline{TBRL}$ pulse occurs with respect to TRC, data is transferred to the transmitter register and TRE is cleared. TBRE is set to a logic High one cycle after that.

Output data is clocked by TRC. The clock rate is 16 times the data rate. (C) A second pulse on $\overline{TBRL}$ loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register and transmission of that character begins.
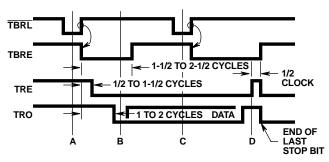

FIGURE 3. TRANSMITTER TIMING WAVEFORMS

Receiver Operation

Data is received in serial form at the RRI input. When no data is being received, RRI input must remain high. The data is clocked through the RRC. The clock rate is 16 times the data rate. Receiver timing is shown in Figure 4.
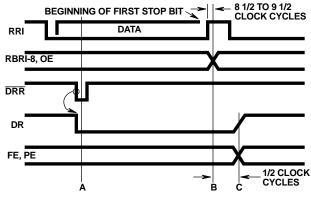

FIGURE 4. RECEIVER TIMING WAVEFORMS

(A) A low level on $\overline{DRR}$ clears the DR line. (B) During the first stop bit data is transferred from the receiver register to the RB Register. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OE indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR. (C) 1/2 clock cycle later DR is set to a logic high and FE is evaluated. A logic high on FE indicates an invalid stop bit was received. A logic high on PE indicates a parity error.

Start Bit Detection

The receiver uses a 16X clock for timing (Figure 5). The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7 1/2. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at 9 clocks into the first stop bit.
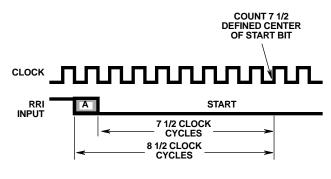

FIGURE 5. START BIT TIMING WAVEFORMS

TABLE 1. CONTROL WORD FUNCTION

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT (S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

NOTE: X = Don't Care

TABLE 2. FUNCTION PIN DEFINITION

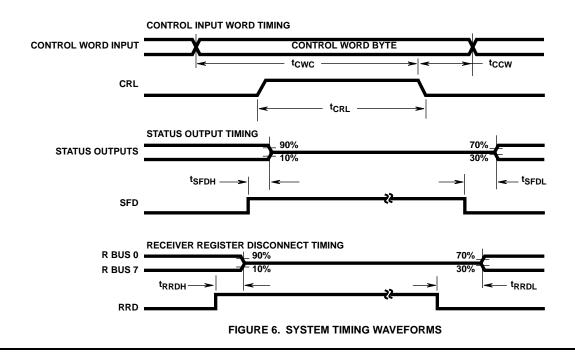| PIN	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	N/C	No Connection
3	GND	Ground (V_{SS})
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register ouputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 - RBR8
7	RBR6	
8	RBR5	
9	RBR4	
10	RBR3	
11	RBR2	
12	RBR1	
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if DRR has been performed (i.e., DRR; active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE and DR, and sets TRE, TBRE, and TRO. TRE is actually set on the first rising edge of TRC after MR goes high. MR should be strobed after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.

TABLE 2. FUNCTION PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits, the TBR8, 7, and 6 Inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 - TBR1
28	TBR3	
29	TBR4	
30	TBR5	
31	TBR6	
32	TBR7	
33	TBR8	
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI†	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS†	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2†	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits).
38	CLS1†	See Pin 37 - CLS2
39	EPE†	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

† See Table 1 (Control Word Function)

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

(NOTE 1) PARAMETER	V_{DD} (V)	CDP6402		CDP6402C		UNITS
		(NOTE 2) TYP	(NOTE 3) MAX	(NOTE 2) TYP	(NOTE 3) MAX	
SYSTEM TIMING (See Figure 6)						
Minimum Pulse Width t_{CRL} CRL	5	50	150	50	150	ns
	10	40	100	-	-	ns
Minimum Setup Time t_{CWC} Control Word to CRL	5	20	50	20	50	ns
	10	0	40	-	-	ns
Minimum Hold Time t_{CCW} Control Word after CRL	5	40	60	40	60	ns
	10	20	30	-	-	ns
Propagation Delay Time t_{SFDH} SFD High to SOD	5	130	200	130	200	ns
	10	100	150	-	-	ns
SFD Low to SOD t_{SFDL}	5	130	200	130	200	ns
	10	40	60	-	-	ns
RRD High to Receiver Register t_{RRDH} High Impedance	5	80	150	80	150	ns
	10	40	70	-	-	ns
RRD Low to Receiver Register t_{RRDL} Active	5	80	150	80	150	ns
	10	40	70	-	-	ns
Minimum Pulse Width MR	5	200	400	200	400	ns
	10	100	200	-	-	ns

NOTES:
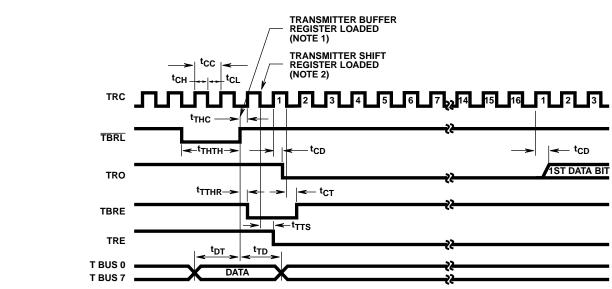
1. All measurements are made at the 50% point of the transition except three-state measurements.

2. Typical values for T_A = 25°C and nominal V_{DD}.

3. Maximum limits of minimum characteristics are the values above which all devices function.

FIGURE 6. SYSTEM TIMING WAVEFORMS

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

(NOTE 1) PARAMETER		V_{DD} (V)	CDP6402		CDP6402C		UNITS
			(NOTE 2) TYP	(NOTE 3) MAX	(NOTE 2) TYP	(NOTE 3) MAX	
TRANSMITTER TIMING (See Figure 7)							
Minimum Clock Period (TRC)	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width							
Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
$\overline{TBRL}$	t_{THTH}	5	80	200	80	200	ns
		10	40	100	-	-	ns
Minimum Setup Time							
$\overline{TBRL}$ to Clock	t_{THC}	5	175	275	175	275	ns
		10	90	150	-	-	ns
Data to $\overline{TBRL}$ ⟋	t_{DT}	5	20	50	20	50	ns
		10	0	40	-	-	ns
Minimum Hold-Time							
Data after $\overline{TBRL}$ ⟋	t_{TD}	5	40	60	40	60	ns
		10	20	30	-	-	ns
Propagation Delay Time							
Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	-	-	ns
Clock to TBRE	t_{CT}	5	330	400	330	400	ns
		10	100	150	-	-	ns
$\overline{TBRL}$ to TBRE	t_{TTHR}	5	200	300	200	300	ns
		10	100	150	-	-	ns
Clock to TRE	t_{TTS}	5	330	400	330	400	ns
		10	100	150	-	-	ns

NOTES:
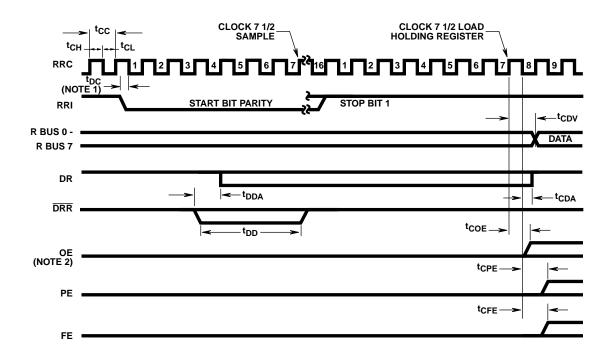
1. All measurements are made at the 50% point of the transition except three-state measurements.

2. Typical values for T_A = 25°C and nominal V_{DD}.

3. Maximum limits of minimum characteristics are the values above which all devices function.

NOTES:

1. The holding register is loaded on the trailing edge of $\overline{TBRL}$.

2. The transmitter shift register, if empty, is loaded on the first high-to-low transition of the clock which occurs at least 1/2 clock period + t_{THC} after the trailing edge of $\overline{TBRL}$ and transmission of a start bit occurs 1/2 clock period + t_{CD} later.

FIGURE 7. TRANSMITTER TIMING WAVEFORMS

NOTES:

1. If a start bit occurs at a time less than t_{DC} before a high-to-low transition of the clock, the start bit may not be recognized until the next high-to-low transition of the clock. The start bit may be completely asynchronous with the clock.

2. If a pending DA has not been cleared by a read of the receiver holding register by the time a new word is loaded into the receiver holding register, the OE signal will come true.

FIGURE 8. RECEIVER TIMING WAVEFORMS

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF

(NOTE 1) PARAMETERS		V_{DD} (V)	LIMITS CDP6402		LIMITS CDP6402C		UNITS
			(NOTE 2) TYP	(NOTE 3) MAX	(NOTE 2) TYP	(NOTE 3) MAX	
RECEIVER TIMING (See Figure 8)							
Minimum Clock Period (RRC)	t_{CC}	5	250	310	250	310	ns
		10	125	155	-	-	ns
Minimum Pulse Width							
Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	-	-	ns
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	-	-	ns
$\overline{\text{Data Received Reset}}$	t_{DD}	5	50	75	50	75	ns
		10	25	40	-	-	ns
Minimum Setup Time							
Data Start Bit to Clock	t_{DC}	5	100	150	100	150	ns
		10	50	75	-	-	ns
Propagation Delay Time							
$\overline{\text{Data Received Reset}}$ to Data Received	t_{DDA}	5	150	250	150	250	ns
		10	75	125	-	-	ns
Clock to Data Valid	t_{CDV}	5	275	400	275	400	ns
		10	110	175	-	-	ns
Clock to DR	t_{CDA}	5	275	400	275	400	ns
		10	110	175	-	-	ns
Clock to Overrun Error	t_{COE}	5	275	400	275	400	ns
		10	100	150	-	-	ns
Clock to Parity Error	t_{CPE}	5	240	375	240	375	ns
		10	120	175	-	-	ns
Clock to Framing Error	t_{CFE}	5	200	300	200	300	ns
		10	100	150	-	-	ns

NOTES:

1. All measurements are made at the 50% point of the transition except three-state measurements.

2. Typical values for T_A = 25°C and nominal V_{DD}.

3. Maximum limits of minimum characteristics are the values above which all devices function.