TECHNICAL NOTE

MIGRATING FROM FPM/EDO TO SDRAM

INTRODUCTION

With the advent of EDO/FPM DRAMs becoming obsolete, memory designers must convert their designs to the volume, industry standard DRAM. Today, this DRAM is the Synchronous DRAM (SDRAM). This technical note will provide a general overview of the differences between EDO/FPM and SDRAM memories. Indepth and detailed information on these technologies can be obtained from the Micron data sheets (located at www.micron.com/mti/msp/html/datasheet.html).

DRAM TECHNOLOGY

A FAST-PAGE-MODE (FPM) DRAM allows an entire page or row of the DRAM to be read or written to by opening a row and incrementing the column address quickly to access that entire row by subsequent column addresses supplied.

An EXTENDED DATA OUT (EDO) DRAM, also allows FPM capability, however this type of DRAM extends the period of time data is available from a READ command. The controller that uses this DRAM will have more time available to get data from the data bus. Synchronous DRAM utilizes an external clock to synchronize input commands, data and addresses with the rising edge of the clock. Such a use of the clock makes timing more precise with other system devices and components.

Other advantages of SDRAM include command driven functionality instead of signal driven; a user programmable Mode Register to select CAS# latency; and access modes for Burst length and Type.

FUNCTIONAL DIFFERENCES

The control of the outputs during a READ is a significant difference between FPM, EDO, and SDRAM devices. The basic functionality on all of these devices is very similar. Rows are opened by RAS# falling, and columns are opened by CAS# falling. On an SDRAM device, these commands must be available on a rising edge of CLK.

During a READ, a column is selected by CAS# falling and a column address being latched in from the address pins. READ data soon becomes available at the DQs or outputs. That data remains driven at the DQs for a period of time, and that amount of time is controlled in different methods dependent on the type of DRAM used. On an FPM device, valid data is available at the output pins until CAS# toggles HIGH. This causes the data to stop being driven and thus it will no longer be valid on the DQs. An EDO device, as its name suggests, allows the data to remain valid beyond when CAS# goes HIGH and until CAS# again falls and another column address is selected. Valid data on an EDO device is

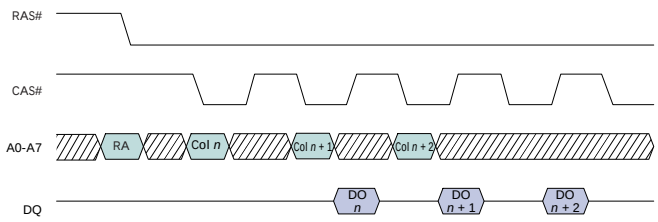

Figure 1
FPM READ

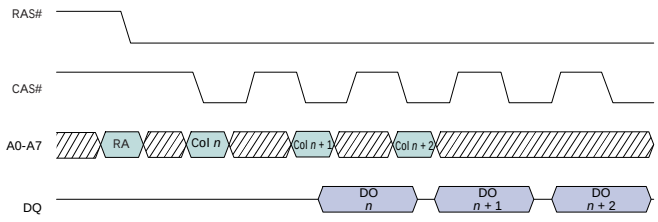

Figure 2
EDO READ

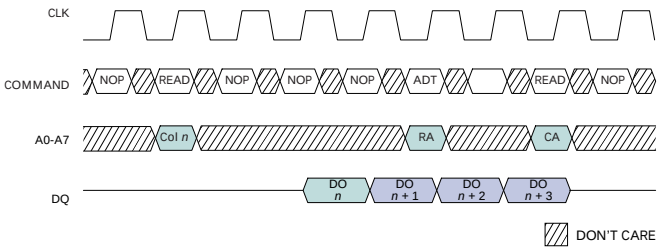

Figure 3
SDRAM READ

available for a longer period of time than an FPM device.

A Synchronous DRAM holds data on the outputs until the next rising edge of the CLK after a burst has completed, unless the BURST is interrupted.

There are other methods to control the output drivers on each type of DRAM. Other command signals are specifically used to control the data. OE# on FPM and EDO, and DQM on SDRAM devices.

PACKAGE

The package for EDO/FPM versus SDRAM devices is an important design consideration. For example, in 16Mb devices, the configuration determines the footprint. The 16 Meg x 4 EDO/FPM is in a 24/26-pin TSOP or 24/26-pin SOJ, while the 16 Meg x 4 SDRAM is in a 44-pin TSOP. Thus, a footprint change is required if the memory is soldered directly on the board. The 1 Meg x 16 TSOPs of EDO/FPM and SDRAM are in a 50-pin package However, the packages are not the same size and the pin assignments are different between the two types of devices, requiring board traces to be re-routed.

Micron 64Mb SDRAMs use the same package and footprint regardless of configuration, a 54-pin TSOP. This same package is being used for the 128Mb and 256Mb SDRAMs as well, providing an upgrade path for designs using the SDRAMs.

VOLTAGE

EDO/FPM Memories allow different voltage supply levels. There are 5V and 3.3V devices available. Many of the 3.3V devices allow 5V I/O tolerance. Synchronous DRAMs currently use 3.3V power supply (V_{DD}), and do not have 5V tolerant I/Os. If an application is migrating to SDRAM from a 5V EDO/FPM, the V_{DDS} should be supplied at 3.3V with either a separate supply or some other type of voltage regulation.

CONTROLLERS

There are controllers available that support both EDO/FPM and SDRAM. This is specific to the controller and should be thoroughly investigated for new designs.

ARCHITECTURE

Along with functionality, the internal architectural structure evolved from EDO/FPM to SDRAM to support multiple banks. The addition of multiple banks allows for multiple rows to be open simultaneously as long as the open rows reside in different banks. This allows seamless bursts of data when switching rows and omits many cycles that would otherwise be wasted. SDRAM have Bank Address (BA) pins to address the internal banks.

SIGNALS

The signals, CS#, RAS#, CAS#, and WE# are used in parallel to determine COMMAND to the SDRAM (Table 1). At every rising edge of the CLK, the command is latched and the SDRAM will perform that function. Command signals no longer need to be measured with respect to each other, but only execute with the rising CLOCK edge; this is true with ADDRESS and DATA as well.

DENSITY:CONFIGURATION	SDRAM	EDO/FPM
16Mb: x 4	44-pin TSOP	24/26-pin TSOP, 24/26-pin SOJ
16Mb: x 8	44-pin TSOP	24/26-pin TSOP, 24/26-pin SOJ
16Mb: x 16[1]	50-pin TSOP	50-pin TSOP, 42-pin SOJ
64Mb: x4/x8	54-pin TSOP	32-pin TSOP, 32-pin SOJ
64Mb: x16	54-pin TSOP	50-pin TSOP

NOTE: 1. The 50-pin TSOP used for the SDRAM and that used for the EDO/FPM have different dimensions, and thus different pad placement is needed. This footprint is not compatible.

CLOCKS AND COMMANDS

CLK is provided by the memory controller and is used to synchronize the SDRAM registering of input and output. The CLOCK rates allowable are bounded by the REFRESH rate of the DRAM at the low end, and the physical design on the high end—approximately 15.6 KHz to 250 MHz. The rising edge of the CLOCK signals the input buffer to decipher the command and initiates the functionality of that given command.

CLOCK ENABLE (CKE#) is used to control the SDRAM's use of the external clock (CLK). When CKE# is low, CLK is no longer used by the SDRAM. This signal is used to initiate POWER-DOWN, SELF-REFRESH, or to SUSPEND the CLOCK. It also turns off the Input Buffers to save power, and uses an internal clock to continue any ongoing commands.

The command pins on an SDRAM are similar to an EDO/FPM's RAS#, CAS#, and WE#. However, for an SDRAM while the OE# is absent, there is an additional command line (CHIP SELECT) to consider, plus Data Mask (DQM) signal which is used to control the DQs. The CHIP SELECT (CS#) pin, controls all access to the SDRAM. It can be used to a great advantage when using multiple SDRAMs in an application, whether that be in module form or for devices soldered down on a board. DQM signal is used to control the DQs. It has the ability to mask data coming out of the SDRAM (i.e., stop the DQs from driving) in the presence of possible data contigency.

MODE REGISTER

The MODE REGISTER is used to control some specific functionalities of the SDRAM, such as the burst length, burst type, and CAS latency. Burst length indicates how many column locations will be accessed sequentially for a READ or WRITE command. Burst lengths of 1, 2, 4, 8, or Full Page are allowed. Sequential or Interleaved Burst types are also available. Only sequential Burst is allowable for FULL PAGE Burst lengths. Burst type determines the order of column access within a BURST. CAS Latency (CL), is also programmable using the Mode Register. CAS Latency determines the number of clock cycles between issuing a READ command to when the subsequent data for that READ becomes available on the DQ's. Typical CAS latency values are 2 or 3.

Table 1
Commands and DQM Operation

NAME (COMMAND)	CS#	RAS#	CAS#	WE#	DQM	ADDRs	DQs
COMMAND INHIBIT	H	X	X	X	X	X	X
NO OPERATION (NOP)	L	H	H	H	X	X	X
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/Col	X
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/Col	Valid
BURST TERMINATE	L	H	H	L	X	X	Active
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X
AUTO REFRESH or SELF REFRESH (enter SELF REFRESH mode)	L	L	L	H	X	X	X
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X
Write Enable/Output Enable	–	–	–	–	L	–	Active
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z

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