Routine to initialize **=> until picture-data-transfer**

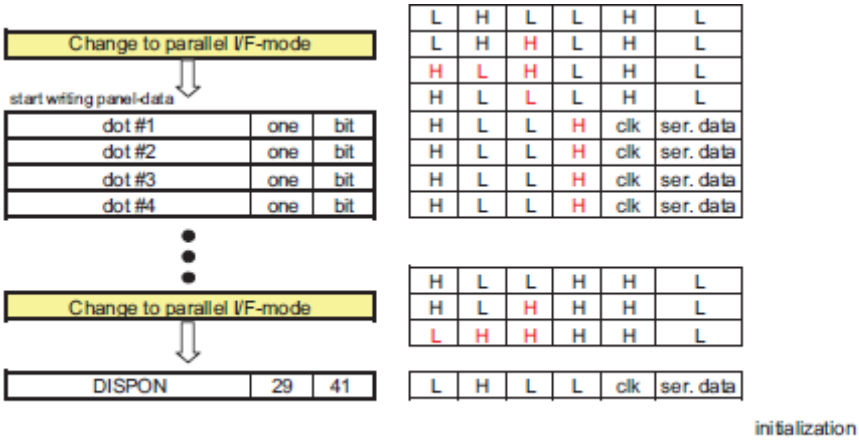
use of EEPROM

Status of I/F-pins:

P/S	C86	XCS	A0	XWR	D0	
HWRESET	L	H	L	L	clk	ser. data
Please wait over 5[ms]						
SLPOUT (Hex 11, Dec 17)	L	H	L	L	clk	ser. data
Please wait over 5 [ms] from SLPOUT						
send any additional command, e.g.						
CASET 2A 42	L	H	L	L	clk	ser. data
P1 00 00	L	H	L	H	clk	ser. data
P2 06 06	L	H	L	H	clk	ser. data e.g. 06 d
P3 00 00	L	H	L	H	clk	ser. data
P4 7D 125	L	H	L	H	clk	ser. data e.g. 125 d => 120 columns
PASET 2B 43	L	H	L	L	clk	ser. data
P1 00 00	L	H	L	H	clk	ser. data
P2 00 00	L	H	L	H	clk	ser. data e.g. 00 d
P3 00 00	L	H	L	H	clk	ser. data
P4 AF 175	L	H	L	H	clk	ser. data e.g. 175 d => 176 rows
COLMOD 3A 58	L	H	L	L	clk	ser. data
P1 02 2	L	H	L	H	clk	ser. data
RGBSET 2D 45	L	H	L	L	clk	ser. data
P1 00 00	L	H	L	H	clk	ser. data
P2 00 00	L	H	L	H	clk	ser. data
P3 00 00	L	H	L	H	clk	ser. data
P4 00 00	L	H	L	H	clk	ser. data
P5 00 00	L	H	L	H	clk	ser. data
P6 00 00	L	H	L	H	clk	ser. data
P7 00 00	L	H	L	H	clk	ser. data
P8 FF 255	L	H	L	H	clk	ser. data
P9 00 00	L	H	L	H	clk	ser. data
P10 00 00	L	H	L	H	clk	ser. data
P11 00 00	L	H	L	H	clk	ser. data
P12 00 00	L	H	L	H	clk	ser. data
P13 00 00	L	H	L	H	clk	ser. data
P14 00 00	L	H	L	H	clk	ser. data
P15 00 00	L	H	L	H	clk	ser. data
P16 00 00	L	H	L	H	clk	ser. data
P17 00 00	L	H	L	H	clk	ser. data
P18 00 00	L	H	L	H	clk	ser. data
P19 00 00	L	H	L	H	clk	ser. data
P20 00 00	L	H	L	H	clk	ser. data
P21 00 00	L	H	L	H	clk	ser. data
P22 00 00	L	H	L	H	clk	ser. data
P23 00 00	L	H	L	H	clk	ser. data
P24 FF 255	L	H	L	H	clk	ser. data
P25 00 00	L	H	L	H	clk	ser. data
P26 00 00	L	H	L	H	clk	ser. data
P27 00 00	L	H	L	H	clk	ser. data
P28 00 00	L	H	L	H	clk	ser. data
P29 00 00	L	H	L	H	clk	ser. data
P30 00 00	L	H	L	H	clk	ser. data
P31 00 00	L	H	L	H	clk	ser. data
P32 00 00	L	H	L	H	clk	ser. data
P33 00 00	L	H	L	H	clk	ser. data
P34 00 00	L	H	L	H	clk	ser. data
P35 00 00	L	H	L	H	clk	ser. data
P36 FF 255	L	H	L	H	clk	ser. data
P37 00 00	L	H	L	H	clk	ser. data
P38 00 00	L	H	L	H	clk	ser. data
P39 00 00	L	H	L	H	clk	ser. data
P40 00 00	L	H	L	H	clk	ser. data
P41 00 00	L	H	L	H	clk	ser. data
P42 00 00	L	H	L	H	clk	ser. data
P43 00 00	L	H	L	H	clk	ser. data
P44 00 00	L	H	L	H	clk	ser. data
P45 00 00	L	H	L	H	clk	ser. data
P46 00 00	L	H	L	H	clk	ser. data
P47 00 00	L	H	L	H	clk	ser. data
P48 00 00	L	H	L	H	clk	ser. data
RAMWR 2C 44	L	H	L	L	clk	ser. data

clk = clock

driver-IC reads init.-routine from EEPROM after receiving SLPOUT-command.


Change to parallel I/F-mode
start writing panel-data
dot #1 one bit
dot #2 one bit
dot #3 one bit
dot #4 one bit
Change to parallel I/F-mode
DISPON 29 41
L H L L H L
L H H L H L
H L H L H L
H L L L H L
H L L H clk ser. data
H L L H clk ser. data
H L L H clk ser. data
H L L H clk ser. data
H L L H H L
H L H H H L
L H H H H L
L H L L clk ser. data
initialization