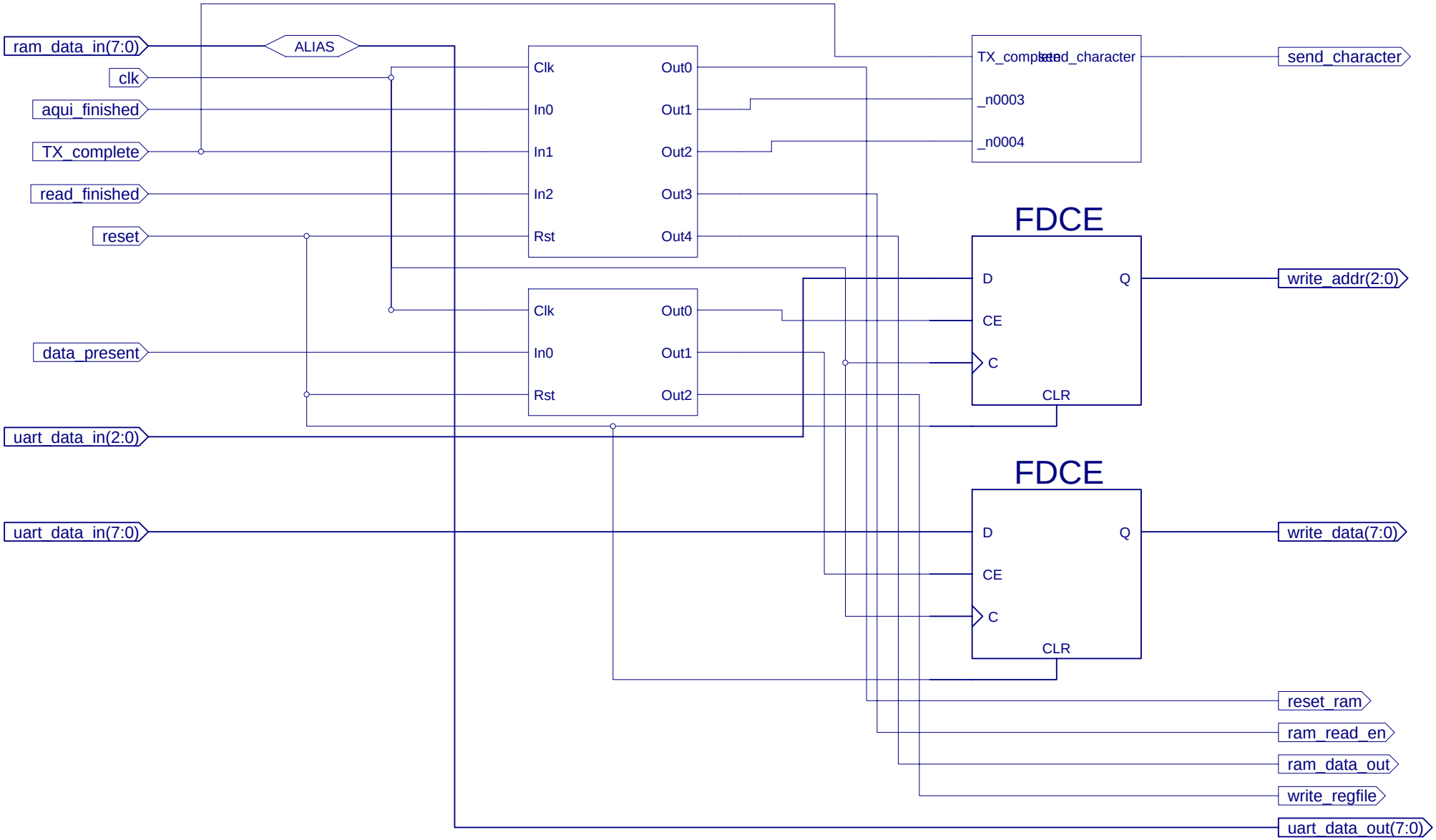
ram_data_in(7:0)
ALIAS
clk
aqui_finished
TX_complete
read_finished
reset
data_present
uart_data_in(2:0)
uart_data_in(7:0)
Clk
In0
In1
In2
Rst
Out0
Out1
Out2
Out3
Out4
Clk
In0
Rst
Out0
Out1
Out2
TX_complete
send_character
_n0003
_n0004
send_character
FDCE
D
CE
C
CLR
Q
write_addr(2:0)
FDCE
D
CE
C
CLR
Q
write_data(7:0)
reset_ram
ram_read_en
ram_data_out
write_regfile
uart_data_out(7:0)