AVR501: Replacing ATtiny15 with ATtiny25

8-bit AVR® Microcontrollers

Application Note

PRELIMINARY

Features

- General Porting Considerations
- Compatibility Mode
- Memories
- System Clock and Clock Options
- System Control and Reset
- Registers
- Interrupt Vectors
- Timer/Counters
- Analogue Comparator
- I/O Ports
- Memory Programming
- Electrical Characteristics

1 Introduction

This application note is a guide to assist users of ATtiny15 in converting existing designs to ATtiny25.

In addition to the differences described in this document, the electrical characteristics of the devices are different. Some of these differences are outlined in this document and some are not. Please check the latest data sheets for detailed information.

Improvements or added features in ATtiny25 that are not in conflict with those in ATtiny15 are not listed in this document.

Rev. 2590A-AVR-03/05

2 General Porting Considerations

Between the ATtiny25 and ATtiny15, some registers and register bits have changed name but note that they preserve the same functionality. They are all listed later in this document.

In relation to code porting, it is an advantage if register names and bit definitions has been used as substitution of these names and definitions can be performed rather painlessly. If absolute register addresses and bit values have been used in the code that is to be ported, the effort to port it is slightly higher – but never the less possible to overcome.

Examples using register and bit definitions are shown below.

```
PORTB |=  (1<<PORTB3);          // Set pin 3 on port B high
DDRB  &= ~(1<<PORTB3);          // Set pin 3 on port B as input

// Configure USI
USICR  =  (1<<USISIE)|(0<<USIOIE)|(1<<USIWM1)|(0<<USIWM0)|
          (1<<USICS1)|(0<<USICS0)|(0<<USICLK)|(0<<USITC);
```

Some of the reserved bits in ATtiny15 are in use on the ATtiny25. To avoid conflicts with added features and register functionality, please ensure that reserved bits and registers are not written. Reserved bits should always be written to zero if accessed. Using register and bit definitions will in general ensure that reserved bits are not accessed incorrectly and will thus ensure forward compatibility.

3 Compatibility Mode

The operation of ATtiny25 can be configured so that it closely resembles that of ATtiny15. This configuration is referred to as the (ATtiny15) Compatibility Mode and it is enabled by writing “0011” to the CKSEL fuses. In Compatibility Mode, the following modifications are in effect:

- Pin layout is compatible with ATtiny15
- Pin change interrupt is compatible with ATtiny15
- Timer/Counter1 is compatible with ATtiny15
- Timer/Counter prescaler is compatible with ATtiny15
- Clocking system is compatible with ATtiny15

The Compatibility Mode is also available in ATtiny45 and ATtiny85, but with the following differences:

- Pin layout is not compatible with ATtiny15 (PB3 and PB4 remain unchanged)
- Pin change interrupt is unchanged

4 Memories

ATtiny25 has more Flash and EEPROM than ATtiny15. Applications that rely on the size of memory may therefore misbehave when memory size is increased. For example, this may be the case with wrap-around indexing of EEPROM.

4.1 EEPROM

EEPROM write access times of ATtiny15 depend on the frequency of the internal RC oscillator. In ATtiny25 the access times are shorter and remain constant.

ATtiny25 is part of a pin and functionally compatible subfamily of tinyAVR™, where the size of EEPROM ranges from 128 to 512 bytes. This means more than eight data bits are required for memory addressing and, therefore, the EEPROM address register has been expanded from one 8-bit register (EEAR in ATtiny15) to two (EEARL and EEARH in ATtiny25, ATtiny45 and ATtiny85). Since the initial values of the registers are undefined it is important to always write both registers even when accessing only the bottom section of the EEPROM.

5 System Clock and Clock Options

ATtiny25 has a more advanced clock system than ATtiny15. In ATtiny15, there is no system clock prescaler and the clock source is constant (the 1.6 MHz internal RC oscillator). The ATtiny25 is more flexible and provides several oscillator sources, frequencies and prescaler options.

The clocking system of ATtiny25 can be operated in two modes: Default or ATtiny15 Compatibility Mode. In compatibility mode the frequency of the internal RC oscillator is adjusted and the multiplication factor of the PLL is set so that fast digital peripherals run at the same speed as in ATtiny15.

5.1 Default

By default, the device is shipped with internal RC oscillator enabled and running at 8 MHz, the system clock prescaler is set to 1/8 (divide by eight) and the PLL scaling factor is set to eight (input to PLL is the unscaled RC oscillator clock). Hence, the system clock will be 1 MHz and the fast peripheral clock 64 MHz.

Using the default fuse settings program execution is slower and the PLL clock is faster on ATtiny25.

5.2 Compatibility Mode

In compatibility mode the frequency of the internal RC oscillator is calibrated to 6.4 MHz, the PLL scaling factor is set to four and the system clock prescaler is set to four. In this mode of operation the CKDIV8 fuse has no effect on the system clock prescaler. Hence, the system clock will be 1.6 MHz and the fast peripheral clock 25.6 MHz.

Programs and fast peripherals will then run at the same speed on the ATtiny25 as they did in ATtiny15.

5.3 Calibration of Internal RC Oscillator

In both modes of operation the frequency of the internal RC oscillator of ATtiny25 can be calibrated using the OSCCAL register, similarly as in ATtiny15. The only difference is that in ATtiny25 the highest bit (CAL7) determines the range of operation, while in ATtiny15 all eight bits of the OSCCAL register are used to adjust the frequency within one, single range.

6 System Control and Reset

ATtiny25 has more fuse bits than ATtiny15. In addition, some fuse bits have a different functionality.

6.1 Start-up Times & Brown-out Detection

The table below illustrates how to modify the programming of fuses BODLEVEL, BODEN and CKSEL1…0.

Table 6-1. Configuring ATtiny25 for Similar Start-up Times (SUT) and Brown-out Detection (BOD) Levels as ATtiny15.

ATtiny15					ATtiny25			
CKSEL 1…0	**BODEN**	**BODLEVEL**	**BOD**	**SUT @ 5.0 V**	**BODLEVEL 2…0**	**CKSEL 0…3**	**SUT 1…0**	**Reset Delay**
00	X	X	Disabled	18 CK + 64 ms	111	0011	00	14 CK + 64 ms
01	X	X	Disabled	18 CK + 64 ms	111	0011	01	14 CK + 64 ms
10	X	X	Disabled	18 CK + 4 ms	111	0011	10	14 CK + 4 ms
11	0	0	4.0 V	18 CK + 32 us	100 (1)	0011	11	14 CK
11	0	1	2.7 V	18 CK + 32 us	101	0011	11	14 CK
11	1	X	Disabled	18 CK + 8 us	111	0011	11	14 CK

Notes: 1. On ATtiny15 the BOD level for this setting is 4.0 V, on ATtiny25 the closest match is 4.3 V.

Due to electrical differences between ATtiny15 and ATtiny25 there may be minor dissimilarities in start-up times. The above table mainly illustrates how to find the closest match between fuse settings of the two devices.

Please see device data sheets for more detailed information.

6.2 Power-On Reset

The threshold levels of power-on reset are not identical for ATtiny15 and ATtiny25. In ATtiny15 the threshold level depends on if the Brown-out Detection is enabled or disabled. In ATtiny25 there is no such dependency.

Please see device data sheets for more detailed information.

6.3 External Reset

Reset characteristics of ATtiny15 and ATtiny25 differ slightly. The minimum pulse width required on the reset pin to trigger a device reset is typically longer on the ATtiny25. This means a very narrow pulse (spike) on the reset input pin may trigger a device reset on ATtiny15 but not on the ATtiny25.

Please see device data sheets for more detailed information.

6.4 Watchdog Timer

The ATtiny25 has the Enhanced Watchdog Timer (WDT) and is improved compared to the one in ATtiny15.

If the operating voltage is 5V and the WDTON fuse is left unprogrammed, the WDT will behave similar on ATtiny15 and ATtiny25.

The frequency of the Watchdog Oscillator in ATtiny25 is approximately128kHz for all supply voltages. The typical frequency of the Watchdog Oscillator in ATtiny15 is close to 1.0 MHz at 5V, but the Time-out period increases with decreasing V_{CC}. This means that the selection of Time-out period for the Watchdog Timer (in terms of number of WDT Oscillator cycles) must be reconsidered when porting the design to ATtiny25.

If the WDT is not used, it is still recommended to disable it initially in the application code to clear unintentional WDT enabled events.

6.5 Internal Voltage Reference

The start-up time of the internal voltage reference is longer on ATtiny25. Please see device data sheets for more information.

7 Registers

Some of the register names have changed and some registers have moved.

7.1 Renamed Registers

The below tables list the registers which have been renamed but still exist at the same physical address and have maintained their functionality. It is only required to update the register name in the application.

Table 7-1. Changes to Register Names.

Address [hex]	Name in ATtiny15	Name in ATtiny25
$33	TCCR0	TCCR0B
$2C	SFIOR	GTCCR
$1E	EEAR	EEARL
$06	ADCSR	ADCSRA

7.2 Moved Registers

The below table summarizes the registers which have been moved.

Table 7-2. Changes to Register Location.

Register Name	Address in ATtiny15 [hex]	Address in ATtiny25 [hex]
OCR1B	$2D	$2B

7.3 Renamed Bits

The below table lists the bits that have been renamed, but still exist in the same register and in the same register location.

Table 7-3. Changes to Bit Names.

ATtiny15			ATtiny25
Bit Name	**Register**	**Address**	**Bit Name**
PWM1	TCCR1	$30	PWM1A
WDTOE	WDTCR	$21	WDCE
EEMWE	EECR	$1C	EEMPE
EEWE	EECR	$1C	EEPE
ADFR	ADCSR	$06	ADATE

8 Interrupt Vectors

ATtiny25 has more interrupt vectors than ATtiny15, but all ATtiny15 vectors exist in identical locations on the ATtiny25. Programs can still use the end of ATtiny15 interrupt vector table as a starting address on ATtiny25, provided that ATtiny25 specific interrupts are not enabled.

9 Timer/Counters

Timer/Counter1 of ATtiny25 is by default not identical to timer/counter1 of ATtiny15; however, it can be operated in ATtiny15 Compatibility Mode by writing 0011 to CKSEL fuses.

9.1 Compatibility Mode

See section 7 for renamed registers and bits. The output compare register OCR1B in ATtiny15 is replaced with OCR1C, which have the same functionality. See ATtiny25/45/85 data sheet for full details on timer1 operation in compatibility mode.

10 Analogue Comparator

The bandgap reference voltage in ATtiny25 is not the same as in Attiny15; In ATtiny15 the nominal bandgap voltage is 1.22 V and in ATtiny25 it is 1.1 V (or 2.56V). This means that ATtiny15 applications where the positive input of the comparator is routed to the internal reference voltage may behave differently on ATtiny25. The default setting is not to route the internal reference voltage to the input of the analogue comparator.

11 I/O Ports

Port pin PB5 of ATtiny15 can be configured as an input or an open-drain output, while in ATtiny25 it performs as a general I/O like PB0:4, with pull-up capability.

11.1 Drive Strength

Port drivers of ATtiny15 have a higher current sink rating but a lower current source rating than those of ATtiny25. This means that ATtiny15 applications where high current is sunk via I/O pins may exceed ATtiny25 device limits. Applications where I/O pins are used for sourcing current are not affected. Port driver characteristics are outlined in the Table 11-1.

Table 11-1. Port Driver Characteristics, Vcc = 5V.

Condition	Port Pin	Pin Rating [mA]		Sum Rating [mA]	
		ATtiny15	ATtiny25	ATtiny15	ATtiny25
Current Sink	PB0:4	20	10	100	60
	PB5	12			
Current Source	PB0:5	3	10		

12 Memory Programming

Both the In System and High Voltage programming interface and algorithms have changed. Refer to the datasheets for details. The most recent version of AVR Studio automatically supports any updates in memory programming algorithms in all programming tools provided by Atmel.

12.1 Fuse Bits

The number of fuse bits has been increased and fuse bits are scattered over three bytes in ATtiny25. Read and write algorithms must be updated for proper fuse programming. If using Atmel programming tools, these are automatically updated when installing a new version of AVR Studio.

The functionality of the following fuse bits has changed:

- The BODLEVEL fuse bit of ATtiny15 has been expanded to three fuse bits (BODLEVEL2…0) on ATtiny25.
- The functionality of ATtiny15 fuse bit BODEN has been integrated into fuse bits BODLEVEL2…0 of ATtiny25.
- Functionality of ATtiny15 fuse bits CKSEL1…0 has been integrated into fuse bits BODLEVEL2…0, CKSEL0 and SUT1…0, as mentioned previously in this document.

12.2 Signature Bytes

Signature bytes reside in a separate address space and can only be read external to the device. Therefore, this notion only applies to programmers, et al, and not to the actual program being migrated.

Signature bytes have been updated as illustrated in the table below.

Table 12-1. Summary of Signature Bytes.

Byte	ATtiny15	ATtiny25	ATtiny45	ATtiny85
$000	$1E	$1E	$1E	$1E
$001	$90	$91	$92	$93
$002	$06	$08	$06	$0B

13 Electrical Characteristics

ATtiny25 is manufactured using a different process then ATtiny15 and electrical characteristics will therefore differ between these devices. Please consult the data sheets for details on electrical characteristics.

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature