DIP 28

The S 178 A is an MOS circuit using p-channel metal-gate-technology with enhancement and depletion transistors, featuring the following technical characteristics:

The **video pulse generator** produces the sync, control, and erase signals required for the control of cameras, mixers, and other equipment.

The following signals are generated:

- Gating signal A
- Sync signal S
- Horizontal pulse H
- Vertical pulse V
- Terminal pulse K_t
- Horizontal gating pulse A (H)
- Double line frequency $H/_2$ } → $H/_2 + V_R$ signal with external signal mixing
  half vertical frequency V_R }
- Vidicon gating signal V_A

Features

All pulses are derived digitally from an input frequency corresponding to a pulse scheme, with a duty cycle of 1 : 1.

Pulse width according to latest CCIR and EIA standards.

The following 6 pulse schemes have been programmed permanently (by 3-bit coding and line number coding):

525 lines (60 Hz)	required input frequency	1.008 MHz
625 lines (50 Hz)	required input frequency	1.000 MHz
735 lines (60 Hz)	required input frequency	1.4112 MHz
875 lines (50 Hz)	required input frequency	1.400 MHz
1023 lines (60 Hz)	required input frequency	1.96416 MHz
1249 lines (50 Hz)	required input frequency	1.9984 MHz

Deviating from the above, any line number between 512 and 1535 lines may be programmed.

It should be noted, however, that a frame frequency of 50 Hz (partial picture duration 20 ms) or 60 Hz (16.66) is achieved.

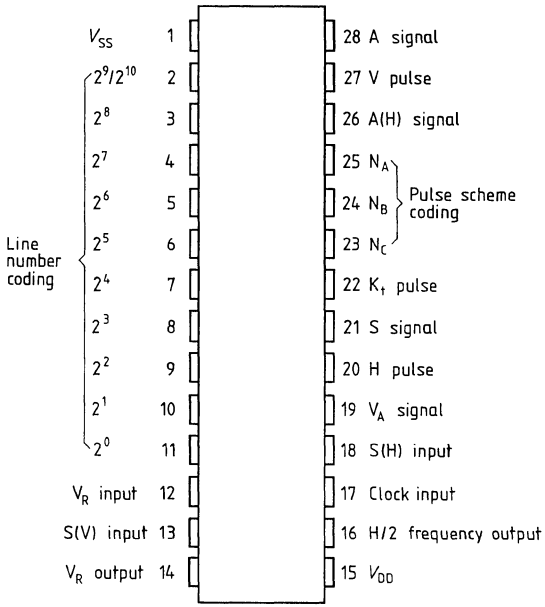
Within the operating frequency it is, however, possible to mix any standard position with any line number.

The following relation applies:

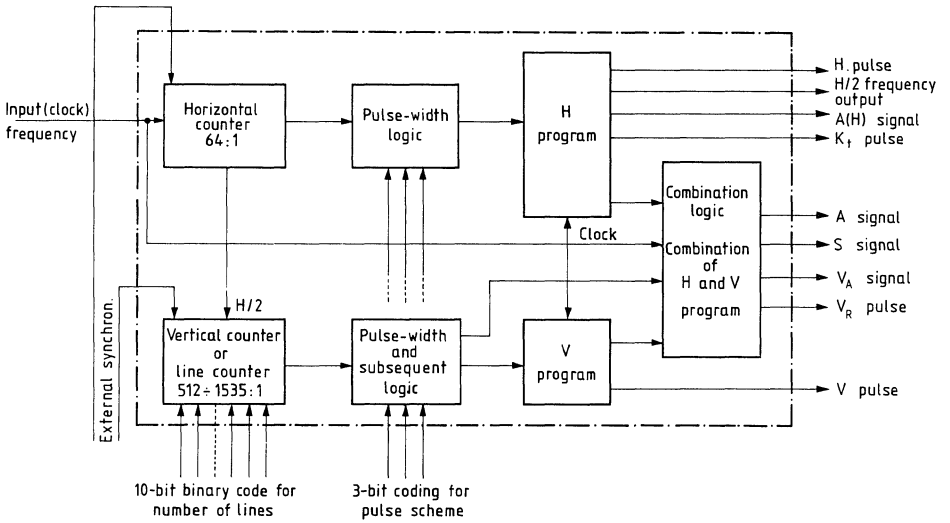
Input frequency f_I = 64: line period H
= 32: line number Z x frame frequency f_{fr}

Not for new design

Pin configuration
top view



Block diagram



Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage, referred to $V_{SS} = 0$ V	V_{DD}	−12	0.3	V
Voltage at all inputs, referred to $V_{SS} = 0$ V	V_I	−20	0.3	V
Input current ($V_I = 0.3$ V; $V_{SS} = 0$ V)	I_I		100	µA
Output current	I_{QH}		−100	µA
	I_{QL}		2	mA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Ambient temperature during operation	T_{amb}	−25	75	°C

Characteristics

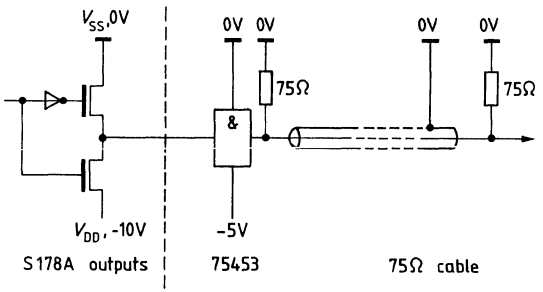
$T_{amb} = 25$ °C

		Test conditions	Lower limit B	typ	Upper limit A	
Supply voltage	$-V_{DD}$		9.5	10	10.5	V
Supply current	I_{DD}			60	70	mA
Inputs		direct control with TTL output level				
H input voltage	V_{IH}		$V_{SS}-1.5$		V_{SS}	V
L input voltage	V_{IL}		$-V_{DD}$		$-V_{DD}+5.5$	V
Outputs		when loaded with one TTL input:				
H output voltage	V_{QH}	$I_{QH} = -40$ µA	$V_{SS}-2.6$			V
L output voltage	V_{QL}	$I_{QL} = 1.6$ mA	TTL GND−0.7		TTL GND+0.4	V
		when loaded with 2 LPS inputs:				
H output voltage	V_{QH}	$I_{QH} = -40$ µA	$V_{SS}-2.6$			V
L output voltage	V_{QL}	$I_{QL} = 0.8$ mA	LPS GND−0.7		LPS GND+0.4	V
		for capacitive load only:				
H output voltage	V_{QH}		$V_{SS}-2.6$			V
L output voltage	V_{QL}		V_{DD}		$V_{DD}+1$	V
Signal transition time of outputs	t_T	when loaded with 2 LPS inputs			100	ns
Input frequency	f_{CLK}		1		2	MHz
Propagation delay time	t_P	clock slope – signal output	0.2		0.4	µs

Interface to 75 Ω cable

A driver stage is required as the pulse generator outputs can be loaded with one TTL input, each. The circuit is to be designed according to the diagram below.

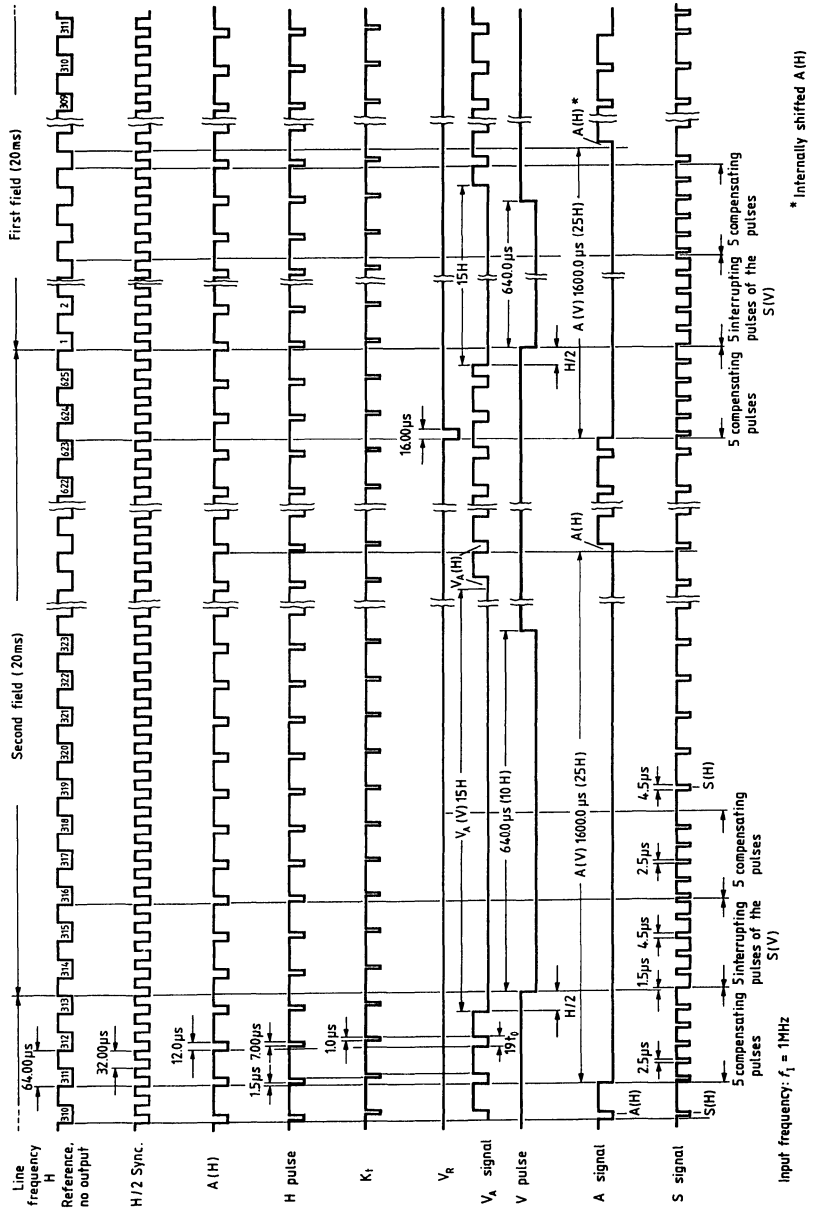
As a driver stage for the 75 Ω coaxial cable, the TTL circuit 75453 (maximum output current 300 mA; pulse delay 11 ns) is recommended.



Programming list for line number coding

Pin number	2	3	4	5	6	7	8	9	10	11	25	24	23
Line number	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	N_A	N_B	N_C
525	H	L	L	L	L	L	H	H	L	H	L	L	L
524	H	L	L	L	L	L	H	L	H	L			
625	H	L	L	H	H	H	L	L	L	H	L	L	H
624	H	L	L	H	H	L	H	H	H	L			
735	H	L	H	H	L	H	H	H	H	H	L	H	L
734	H	L	H	H	L	H	H	H	L	L			
875	H	H	L	H	H	L	H	L	H	H	L	H	H
874	H	H	L	H	H	L	H	L	L	L			
1023	H	H	H	H	H	H	H	H	H	H	H	L	L
1022	H	H	H	H	H	H	H	H	L	L			
1249	L	L	H	H	H	L	L	L	L	H	H	L	H
1248	L	L	H	H	L	H	H	H	H	L			

Pulse scheme for 625 lines



Pulse width table for the programmed line numbers

Pin No.		525 $f = 1.008$ MHz $t_0 = 0.49603\ \mu s$		625 $f = 1.000$ MHz $t_0 = 0.5\ \mu s$		735 $f = 1.4112$ MHz $t_0 = 0.3543\ \mu s$		875 $f = 1.400$ MHz $t_0 = 0.3514\ \mu s$		1023 $f = 1.96416$ MHz $t_0 = 0.25456\ \mu s$		1249 $f = 1.9984$ MHz $t_0 = 0.2502\ \mu s$	
		μs	t_0	μs	t_0	μs	t_0	μs	t_0	μs	t_0	μs	t_0
–	Line period H	63.492	128	64.00	128	45.3514	128	45.7142	128	32.583	128	32.0256	128
16	H/2 synchronization	31.75	64	32.00	64	22.68	64	22.86	64	16.29	64	16.01	64
20	H pulse	6.45	13	7.0	14	4.96	14	4.99	14	2.54	10	2.5	10
26	Horizontal gating A (H)	10.91	22	12.0	24	7.08	20	8.57	24	7.13	28	6.0	24
21	Horizontal synchronization S (H)	4.46	9	4.5	9	2.83	7	2.85	7	2.54	10	2.5	10
20	Front porch	1.48	3	1.5	3	1.06	3	1.07	3	0.76	3	0.75	3
21	Equalizing pulses	2.48	5	2.5	5	1.414	4	1.42	4	1.02	4	1.00	4
21	Interruption of the V-synchronization pulse	4.46	9	4.5	9	2.48	7	2.5	7	1.78	7	1.75	7
22	Terminal pulse K_t	1.49	3	1	2	0.7	2	0.71	2	1.53	6	1.5	6
19	Vidicon gating V_A (H)	9.42	19	9.5	19	6.73	19	6.78	19	4.83	19	4.75	19
19	Vidicon gating V_A (V)	15 H + $19t_0$		15 H + $19t_0$		20 H + $19t_0$		20 H + $19t_0$		30 H + $19t_0$		30 H + $19t_0$	
28	Vertical gating A (V)	20 H + $22t_0$		25 H + $24t_0$		30 H + $20t_0$		30 H + $24t_0$		40 H + $28t_0$		40 H + $24t_0$	
14	V_R signal	15.87	32	16.0	32	11.34	32	11.43	32	8.15	32	8.01	32
27	V pulse	9.5 H		10 H		14.5 H		15 H		20 H		20 H	
21	Number of pre- and post equalizing pulses	6		5		6		5		6		6	

Duty cycle $f_1 = 50\% \frac{1}{f_1} = 2\ t_0$

Line programming

Any line number between 512 and 1535 lines is binary-programmable. A binary "1" is applied to the pins 2^0 to 2^9 with condition $V_{SS} \geq V_I \geq V_{SS} - 1.5$ V and a binary "0" with $V_{DD} \leq V_I \leq V_{SS} - 4.5$ V. The correct programming of the MSB 2^{10} is carried out automatically via pin 2^9 within the line number range of 512 to 1535.

Uneven line numbers (interlaced scanning method)

The binary form of the desired line number is switched to the corresponding pins.

Even line numbers

The desired line number is reduced by 1 and the binary form is switched to pins 2^0 to 2^9, the LSB (2^0) is switched invertedly.

Functional description

The principal units of the pulse generator are the horizontal and the vertical counter (see block diagram). The horizontal counter, divider ratio 64 :1, divides the input frequency down to twice the line frequency $H/_2$.

An additional logic ensures, that a defined condition of the switching stages is submitted to the counter after a maximum of one picture change. The vertical counter is externally programmable to a defined line number.

Due to the external 3-bit enconding, the desired pulse scheme is programmed internally; i.e. the appropriate switching units for realizing the H and V program, are enabled. The pulses are now fed either directly to the outside, or are logically mixed and masked in the combination logic. The pulse start or the pulse widths, respectively occur at $H/_2$ sync defined according to time. In the case of even line numbers, only the first field appears for all pulse schemes, preceded by a V_R pulse.

In the case of uneven line numbers with first and second fields (interlaced scanning), the V_R pulse precedes only the first field.

According to the CCIR standard, the first field starts, when the leading edge of the V pulse is synchronous with the leading edge of A (H).

External synchronization with $H/_2 + V_R$ or S signal

For video mixing and cross-fading, the BAS signals of the individual cameras or video recorders must be sycnrhonized, i.e. correspond in line and picture. In the case of external synchronization, these two components must be contained in the external signal: either the horizontal and vertical frequency in the case of the S signal: S (H) and S (V), or S (H), and half of the vertical frequency ($H/_2 + V_R$).

At the beginning of the leading edge, short pulses must be derived from these two H and V components, and thereby the defined setting of the horizontal and the vertical counter is accomplished.

(Standard value: H component 300 ns < clock period
V component 1 µs < $H/_2$)

Because of the time deviation of the front edges of the line frequency H and S (H), which is 1.5 periods of the input frequency, the horizontal counter would be set incorrectiy. For this reason, an input S (H) has been selected for the horizontal component, which sets the counter to the correct position when activated.

The same is valid for the vertical components of $H/_2 + V_R$ and the S signal. The first frame frequency pulse follows 2.5 or 3 line periods behind the V_R pulse, depending on the scheme. The two inputs provided for the pulses from V_R or S (V), respectively, and the correspondingly encoded line scheme enable a proper setting of the vertical counter. Through the possibility of a defined setting of the counters it is ensured that a proper standard pulse scheme is obtained at the outputs even in the case of external synchronization involving different phase conditions of the synchronization signals.

Note:

At the time of setting the horizontal counter to a defined position, the phase relation of the input frequency is undefined and consequently the tolerance of the synchronization would be one clock period (i.e. ≤ 1 µs for 625 lines). By means of an external phase synchronization circuit with frequency multiplication, the input clock can be derived from the vertical component and, thereby, a defined phase relation of the reset pulse achieved relative to the input clock. Hence a common line deviation (jitter) of < 20 ns absolute value can be achieved.

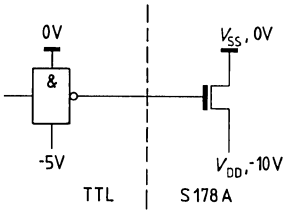
Control

The pulse generator derives the required pulses from the output frequency. As additionally half a clock period is used for the generation of the pulse widths, and as both the leading and trailing edges are used, an input duty cycle of 1:1 is required.

It is, therefore, recommended to operate the quartz oscillator at twice the input frequency and to divide it 2:1 by an external stage, thereby obtaining an accurate duty cycle of 1:1.

Inputs which are not used must be connected to V_{SS} (H level).

Control with TTL



A TV clock generator, externally synchronizable, using the integrated video pulse generator S 178 A.