iPlay™ Media Player Controller

MP600

Datasheet

Revision 0.8

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Magic Pixel Inc.

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1 General Description

The MP600 is a high integration SOC (System On Chip) for digital picture frame application. It implements all necessary peripherals in one chip, including a high performance JPEG Codec engine (Decoding Speed: 32MPixel/sec), Audio DAC with Speaker Amplifier and Headphone driver, USB 2.0 HS Device, USB 1.1 Host, Digital TCON for glue-less LCD interface and etc.

The central part of the chip is a high performance 32-bit RISC CPU which allows flexible system control. It contains 4KB of Instruction Cache, 2KB of Data Cache and 24-Kbyte scratch pad memory to save the memory fetch overhead and hence boost the software performance further.

High qualities Audio DAC & Power Amplifier are integrated to MP600. It can playback MP3, WMA as the background music when playing Slide-Show. It also supports Motion JPEG captured by digital camera up to VGA@30FPS.

The Image Display Unit *(IDU)* is implemented to provide digital TV signals up to 1920x1080i which allows HD-quality PHOTO to be displayed on LCD /Plasma TVs through external HDMI Tx chip. A scaling unit is included for scan conversion. It also supports On-Screen Display with high-resolution for friendly user interface.

MP600 provides a versatile hardwired interface to support most of popular memory card standards, including Compact Flash, SD/ mini SD/ Micro SD (It can support SD2.0 for SDHC specification), MMC/RS-MMC, xD and Memory Stick/Pro. It offers the maximum flexibility and reliability to the customers.

For data transfer to/from PC/Pict-Bridge enabled printer, it provides both USB and popular UART interfaces. It includes a USB 2.0 device controller that is compliant with the USB 2.0 standard. 4 endpoints have been implemented to achieve variety of requirements for image/audio data upload or download. It also includes an IR (Infra-Red) controller supporting NEC Button and Remote Point Mouse protocols.

For flexible peripheral control and user interface, it provides several GPIOs, including PWM output. The mass storage interface is designed to support most types of NAND Flash (Support SLC/MLC and multiple-die package NAND Flash).

With the abundant features and superior performance and quality, MP600 provides a best cost-effective solution for digital photo frame application.

2 Features

- **Power**
  - Dual Power. 1.8V for core, and 3.3V/1.8V for I/O
- **Image Processing Unit**
  - Fine-step hardware scaling engine to scale up and down images for resolution conversion or image zooming.
- **JPEG Codec**
  - Support JPEG resolution up to 16MPixel
  - High speed JPEG compression and decompression (32MPixel/sec)
  - Support image sub-sampling after JPEG decompression
  - Support image rotation (by S/W) / Zoom In / Panning.
- **Audio/Video decoding accelerator**
  - Full bit-rate support of MP3, WMA
  - Hardware Motion-JPEG up to VGA@30fps
- **Memory Interface**
  - SDRAM support
  - Support 4Mx16 SDRAM for Pure Digital Picture Frame application.
  - Support 8Mx16 / 16Mx 16 DDR for TV Box application.
  - Variety of NAND Flash memory support (for MP600B only), including SLC/MLC, multiple-die NAND Flash with multi-chip-select (e.g. 8Gb/16Gb/32Gb), Small block, Big block and etc. for maximum flexibility
  - Support NOR-type Flash memory, up to 4MB with x8 or x16-bit data width for both BIOS access and data storage. MP600A can only support 8-bit data width of NOR Flash.
  - Support program boot up from NAND flash memory
- **Memory Card and Hard drive Interface**
  - MP600A
    - Support MMC(Multi-Media Card), Security Disk (SD1.1 & SDHC with SD 2.0), Memory Stick / Pro.
  - MP600B
    - Support Compact Flash, Multi-Media Card, Security Disk (SD1.1 & SDHC with SD 2.0), Memory Stick Pro, xD Picture Card
  - Support multi-block DMA
- **Embedded Audio DAC & Power Amplifier**
  - Audio DAC
  - High performance Audio DAC (16bit, 93dB)
  - Stereo Headphone Driver
  - Stereo Speaker Amplifier up to 1 Watt (0.5W +0.5W)

- **USB Interface**
  - MP600A embedded USB Host / MP600B embedded USB Device & Host
  - High-speed USB 2.0 High-Speed device function with embedded USB PHY
  - Embed USB1.1 Host Controller to connect to USB thumb-drive /Digital Camera
  - Support Direct Print function (Pict-Bridge)
  - Power saving control to comply with USB spec.
  - Support uploading and downloading capability
  - Support USB Mass Storage Class for both High Speed Device and Full Speed Host functions
- **Display Interface**
  - MP600A
    - Digital CCIR 656
  - MP600B
    - Embedded Digital TCON for Digital Panel
    - Support digital YUV data output conforming to ITU-R BT.601/656/709 up to D3 resolution (1920x1080i)
    - Support digital RGB888/666/565 data output up to WXGA @50Hz (1366x768) / XGA @60Hz (1024x768).
    - Maximum Pixel Rate: 75MPixel/sec
- **Colorful Graphic OSD**
  - Support On-Screen-Display with high resolution for content-rich display user-interface
  - 2nd OSD engine supports 2-, 4- or 8-bit palette-indexed Bit-mapped On Screen Display (OSD).
- **CPU & Misc.**
  - Embedded high performance 32-bit RISC processor with 4KB instruction cache and 2KB data cache, 24KB scratch-pad memory and 512MB memory addressing capability
  - BIOS storage in Flash memory with in-system-programming (ISP) capability
  - Embedded phase-locked loop(PLL) with independently programmable multiple clock outputs
  - Support up to 120MHz system clock
  - Flexible GPIO control for variety of peripheral control.
  - Most pins can be re-configured as GPIO pins when their primary-defined functions are not in use
- **Package**
  - MP600A 128-pin QFP (14mm x 20mm x 2.75mm)
  - MP600B 216-pin LQFP (24mm x 24mm x 1.4mm)
- **System Development Kit & Software Support**

- Support real time-OS
- u-iTron
- Schematics and application note
- UI (User Interface) Builder

3 Block diagram

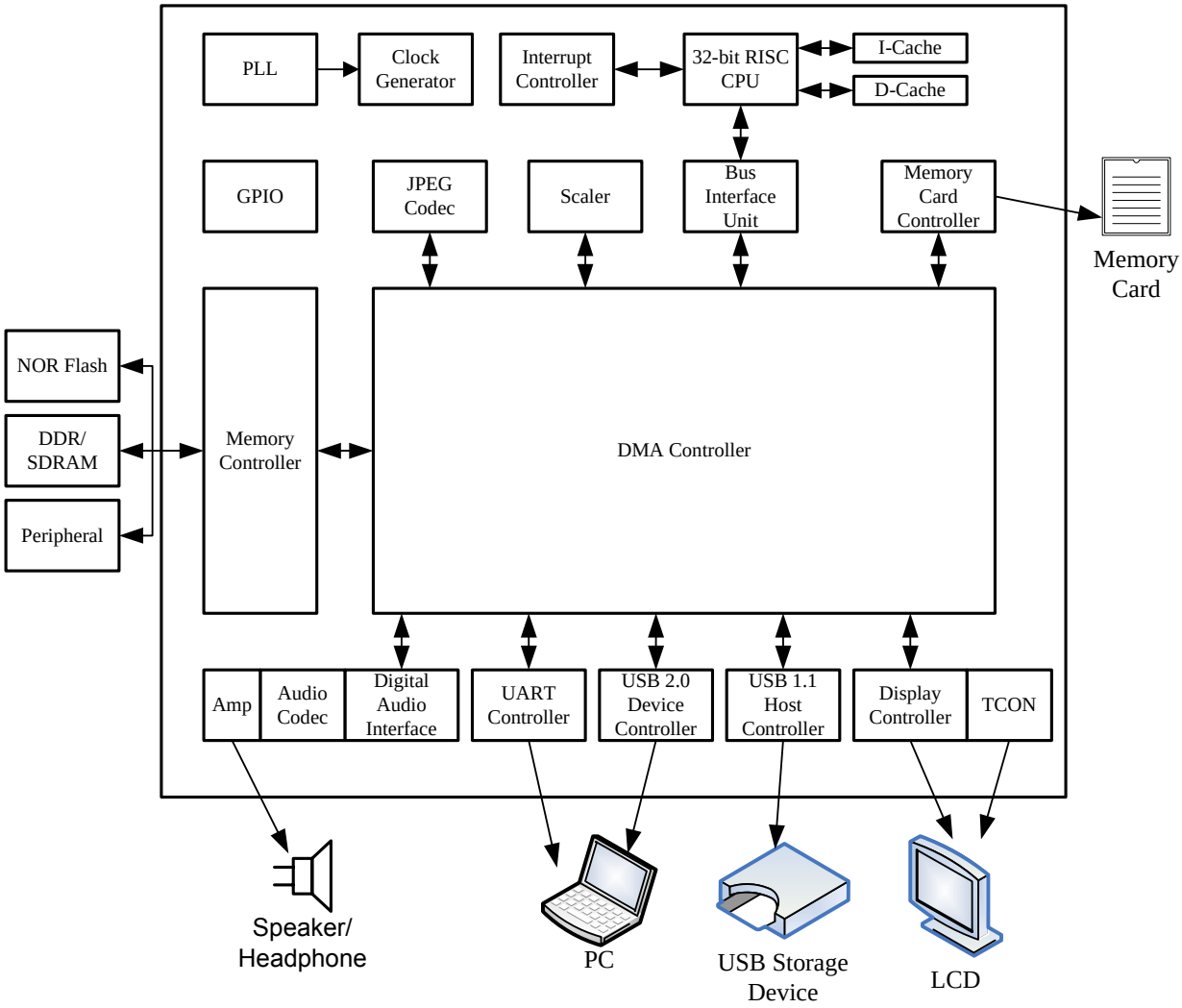


Figure 3-1 MP600 Block Diagram

4 Functional Description

The MP600 is a high-integration SOC (System On Chip) for DPF (Digital Picture Frame) application. It implements all necessary peripherals in one chip.

4.1 Image Processing Unit (IPU)

To be capable of full screen display and image zoom-in function for variable size of pictures, the MP600 embeds a flexible scaling engine. The core of image resizing is a bi-linear scaler and two image sub-sampling blocks. Image shrinking and enlargement are both supported. By applying multi-pass image scaling, the allowable processing resolution is virtually unlimited.

4.2 Image Display Unit (IDU)

The Image Display Unit supports variety of digital LCD interface. Besides, it also supports digital video outputs as ITU. BT.601 , BT.656, and BT.709 up to D4 resolution(1920x1080i). A programmable color space conversion unit is also implemented to support both RGB and YCbCr/YPbPr outputs.

MP600 provides great flexibility in display timing settings. Typical display output timing is illustrated in Fig. 4-2-1 and Fig. 4-2-2. All the parameters shown in the figures are programmable.

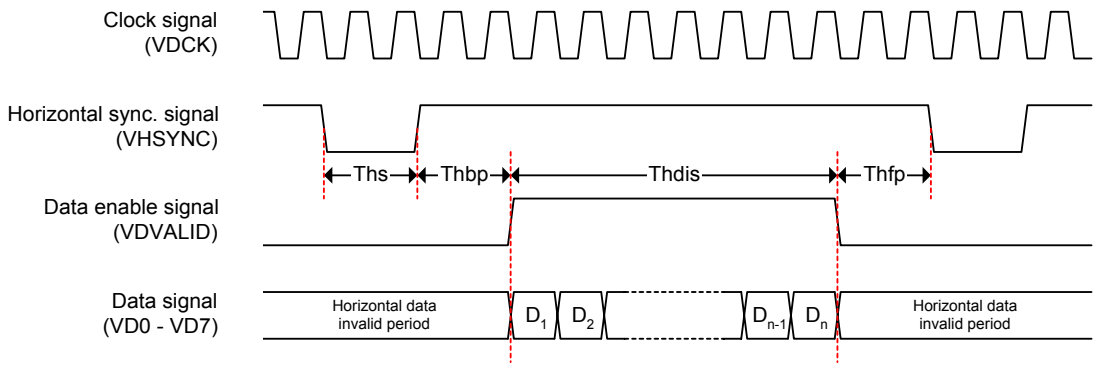


Fig. 4-2-1. Display output horizontal timing diagram

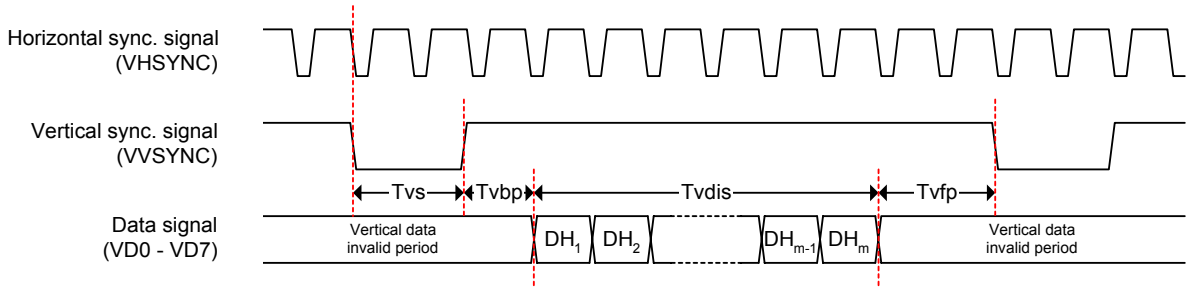


Fig. 4-2-2. Display output vertical timing diagram

A bitmap OSD is also included. 8 , 4 or 2 bits index per pixel can be chosen. With 8-bit index, 128 OSD colors and 8 programmable blending colors can be selected. Or with 2-bit index, only 3 programmable blending colors can be used. But the latter case will save the required memory size of the OSD bitmap. Through the Palette registers that specify the OSD color and blending ratio, it allows quite flexible and content-rich user interface.

A digital TCON is also included to support glue-less connection with variety of panels. With most parameters programmable, it can support variety of panels with maximum flexibility.

4.3 JPEG CODEC

A standard JPEG Compression/Decompression engine is embedded. It is compliant to the Baseline JPEG Standard. It accepts image data in YCbCr 4:2:2 or 4:4:4 format. YCbCr 4:2:0 compression format is also supported, but the source image in DRAM buffer should be in 4:2:2 format still. CDU will perform the sub-sampling on Cb and Cr.

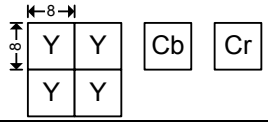
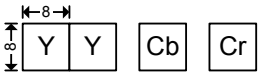
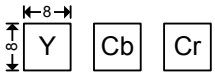
	4:2:0	4:2:2	4:4:4
MCU Types			
MCU size	16 × 16	16 × 8	8 × 8

Table 4-3-1. MCU types supported by CDU

It is capable of processing image with resolution up to 4Kx4K. The image source and compressed stream are both acquired from and delivered to SDRAM through DMA. It needs no CPU intervention for data transfer. Single cycle throughput can be achieved to allow real-time capturing. It can always catch up and deliver high performance for continuous image or video capturing.

It supports two sets of Quantization and Huffman tables respectively. They are both programmable for better compression quality adjustment. The latter is usually fixed in factory, while the Quantization table can be adjusted with pre-determined values for image quality and compression ratio tradeoff controlled by the end users.

It also supports Restart Marker insertion and detection when enabled. Other markers or headers should be handled by the firmware instead.

The JPEG module consists of System Bus Interface, configuration registers, dedicated SRAM modules, system memory interface, Scaling Unit and Control Unit.

CPU can configure and start/stop encoding/decoding process via the 32-bit System Bus Interface.

In encoding mode, it reads in images pixel data, from external system SDRAM and outputs the encoded stream data back to SDRAM.

While decoding, stream data is read from SDRAM, with header information (Huffman tables, quantization tables, etc.) already peeled by CPU. Pixel data is output MCU by MCU.
An interrupt is triggered when encoding/decoding process is finished.

4.4 CPU

The MP600 embeds a 32-bit RISC CPU, with a 32-bit MAC unit and instruction extension for audio performance enhancement. It also includes 4KB and 2KB of Instruction and Data Cache respectively, plus 24KB of Data memory to enhance the performance further. It offers good performance for audio processing and other application extensions that require intensive signal processing.
The operating frequency of CPU can be dynamically adjusted. Lower frequency setting can be used to save the power consumption. SLEEP instruction can also be used to put the CPU into sleep mode, which will reduce the power consumption of CPU to the minimum level. Any enabled interrupt can then be used to wake up the CPU to normal operation.
It supports complete tool chain, including firmware, driver and debug utilities to facilitate software development.

4.5 Memory Mapping

The CPU supports 4GB of virtual addressing. It is divided into 4 segments as the following table. The 4GB of virtual address space are mapped to 512MB of physical space by ignoring the 3 MSBs.

Virtual Address Space	Description	Mapped Physical Address
0xE000_0000 ~ 0xFFFF_FFFF	KSEG2. 1GB. Addressable in Kernel mode. Cached	0x0000_0000 ~ 0x1FFF_FFFF
0xC000_0000 ~ 0xDFFF_FFFF		0x0000_0000 ~ 0x1FFF_FFFF
0xA000_0000 ~ 0xBFFF_FFFF	KSEG1. 512MB. Addressable in Kernel mode. Uncached	0x0000_0000 ~ 0x1FFF_FFFF
0x8000_0000 ~ 0x9FFF_FFFF	KSEG0. 512MB. Addressable in Kernel mode. Cached	0x0000_0000 ~ 0x1FFF_FFFF
0x6000_0000 ~ 0x7FFF_FFFF	KUSEG. 2GB. Addressable in Kernel or User mode. Cached	0x0000_0000 ~ 0x1FFF_FFFF
0x4000_0000 ~ 0x5FFF_FFFF		0x0000_0000 ~ 0x1FFF_FFFF
0x2000_0000 ~ 0x3FFF_FFFF		0x0000_0000 ~ 0x1FFF_FFFF
0x0000_0000 ~ 0x1FFF_FFFF		0x0000_0000 ~ 0x1FFF_FFFF

The 512MB of physical space is further mapped as follows:

Physical Space	Range	Description
0x1C00_0000 ~ 0x1FFF_FFFF	448 ~ 512MB	Code Flash/ROM
0x1800_6000 ~ 0x1BFF_FFFF	408 ~ 448MB	Reserved
0x1800_0000 ~ 0x1800_5FFF	384 ~ 408MB	Scratch Pad Data Memory
0x1400_0000 ~ 0x17FF_FFFF	320 ~ 384MB	Reserved
0x1000_0000 ~ 0x13FF_FFFF	256 ~ 320MB	Peripheral
0x0800_0000 ~ 0x0FFF_FFFF	128 ~ 256MB	Register File
0x0000_0000 ~ 0x07FF_FFFF	0 ~ 128MB	DRAM

The following table also summarizes the register file mapping.

Physical Space	Contents
0x0FC0_8000 ~ 0x0FC0_83FF	Reserved
0x0FC0_0000 ~ 0x0FC0_3FFF	Reserved
0x0803_8000 ~ 0x0FBF_FFFF	Reserved
0x0803_4000 ~ 0x0803_7FFF	Reserved
0x0803_0000 ~ 0x0803_3FFF	Reserved
0x0802_6000 ~ 0x0802_FFFF	Reserved
0x0802_4000 ~ 0x0802_5FFF	Reserved
0x0802_2000 ~ 0x0802_3FFF	CDU Registers
0x0802_0000 ~ 0x0802_1FFF	Memory Card Control Registers
0x0801_E000 ~ 0x0801_FFFF	IDU/OSD Registers
0x0801_C000 ~ 0x0801_DFFF	GPIO Registers
0x0801_A000 ~ 0x0801_BFFF	RTC Registers
0x0801_9000 ~ 0x0801_9FFF	USB 1.1 Host Registers
0x0801_8000 ~ 0x0801_8FFF	USB 2.0 Device Registers
0x0801_6000 ~ 0x0801_7FFF	Reserved
0x0801_4000 ~ 0x0801_5FFF	AIU Registers
0x0801_2000 ~ 0x0801_3FFF	UARTH Registers
0x0801_0000 ~ 0x0801_1FFF	SIO Registers
0x0800_E000 ~ 0x0800_FFFF	Timer Registers
0x0800_C000 ~ 0x0800_DFFF	DMA Control Registers
0x0800_B000 ~ 0x0800_BFFF	Interrupt Handler Control Registers
0x0800_A000 ~ 0x0800_AFFF	Clock Generator Registers
0x0800_8000 ~ 0x0800_9FFF	BIU/System Control Registers
0x0800_4000 ~ 0x0800_4FFF	IPU SRAM Registers
0x0800_0000 ~ 0x0800_1FFF	IPU Registers

4.6 DMA Controller

The DMA Controller manages all the SDRAM access requests from internal module or external peripheral. It arbitrates among the requests with the pre-defined priority. Through each channel, data is transferred from DRAM to device, or vice versa. The DMA channels that require real-time and high data bandwidth are assigned with high priorities. Memory to memory DMA can also be supported in certain configuration. It can also be enabled to take advantage of the bank-interleave feature of SDRAM to increase the memory bandwidth. To save the SDRAM power consumption, several levels of power down mode can also be employed. A quite flexible addressing scheme is supported to maximize SDRAM space usage. It supports a wide range of SDRAM types, from 16Mb to 256Mb, x16-bit bus. It also supports DDR SDRAM, from 16Mb to 256Mb, x16-bit bus. It allows the customer to make the best choice for their application. The SDRAM timing is also programmable to be fit to variety of SDRAM performance.

Besides SDRAM, it also takes care of the ROM/Code Flash and external peripheral accesses. The DMA Controller arbitrates among the 3 types of requests automatically. A Memory Bus Interface Unit is included to handle the interfaces with these 3 kinds of devices. It supports multiple configurations and programmable timing for maximum compatibility. Up to 8MB of Code Flash/ROM can be supported. Not only for firmware code, the NOR Flash interface can also be used for image storage if desired.

4.7 Memory Card Controller

The Memory Card Controller is responsible of controlling the data accesses with external image storage media. It supports Compact Flash, Smart Media, Secure Digital Memory Card (SD), Multi Media Card (MMC), xD , Memory Stick, Memory Stick Pro and Micro Drive. Coexist with the memory cards, on-board NAND Flash can also be supported.

For Compact Flash interface, only Memory mode can be supported. Hardware ECC and CRC are implemented for Smart Media and MMC/SD support respectively.

Data transfer with Compact Flash or Smart Media can be accomplished through DMA or CPU. For MMC or SD, however, it allows only through DMA. The bus interface timing is programmable for maximum compatibility.

4.8 USB Device Controller

The built-in USB Device Controller support several endpoints for communication with USB Host.

- Control Read/Write transfer
- Interrupt Transfer
- Downstream Bulk Transfer from Host
- Upstream Bulk Transfer to Host
- Upstream Video Isochronous /Bulk Transfer to Host
- Upstream Audio Isochronous /Bulk Transfer to Host

The upstream bulk or isochronous transfer is accomplished with DMA operation.

4.9 Digital Audio Interface Unit (AIU)

The Digital Audio Interface Unit (AIU) handles data communication between MP600 and internal/external audio CODEC. Both audio playback and recording are supported. It implements a quite flexible interface for standard AC97 or other I2S or generic audio codec. It supports both Master and Slave clocking. It also supports variety of audio data format, 8 or 16-bit, mono or stereo, and sampling rate for both recording and playback.

4.10 Analog Audio Interface

MP522 supports 3 voice inputs and 3 audio outputs, including 1 differential input for microphone, 2 auxiliary sound inputs, stereo head phone output, speaker and auxiliary audio outputs.

4.10.1 *External Circuit for Speaker Amplifier*

AEQ1, AEQ2 and AEQ3 can be used to fine-tune the speaker tone and gain. The reference circuit is shown as below.

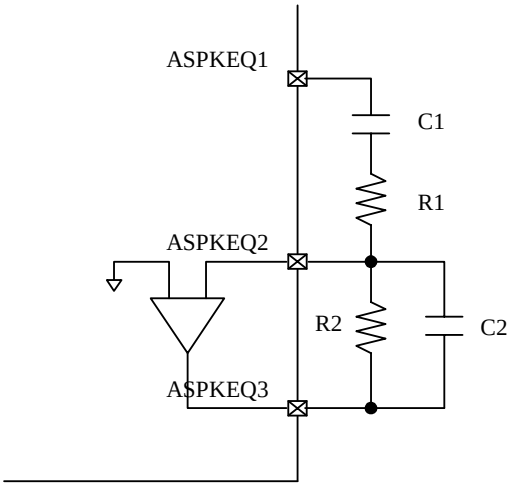


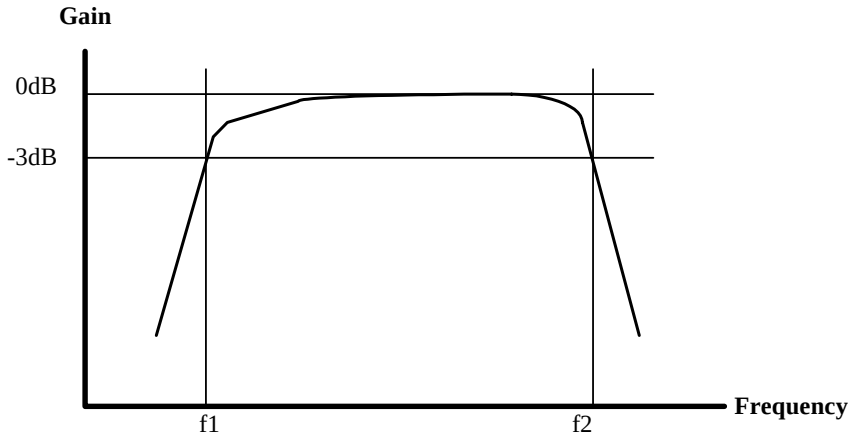
Figure 4-1 RC filter circuit for Speaker Amplifier

C1, R1 and C2, R2 are used to set the low and high cut-off frequency of the Speaker Amplifier respectively.

$$\text{Gain} = \frac{R_2}{R_1}$$

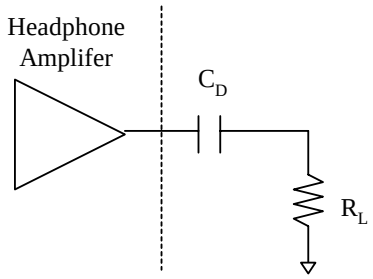
$$f_1 = \frac{1}{2\pi \times R_1 \times C_1}$$

$$f_2 = \frac{1}{2\pi \times R_2 \times C_2}$$



4.10.2 *External Circuit for Headphone Amplifier*

The reference circuit for Headphone is shown as below:



C_D : capacitance of the DC blocking capacitor

R_L : DC loading resistance of the Headset

Figure 4-2 Reference circuit for Headphone

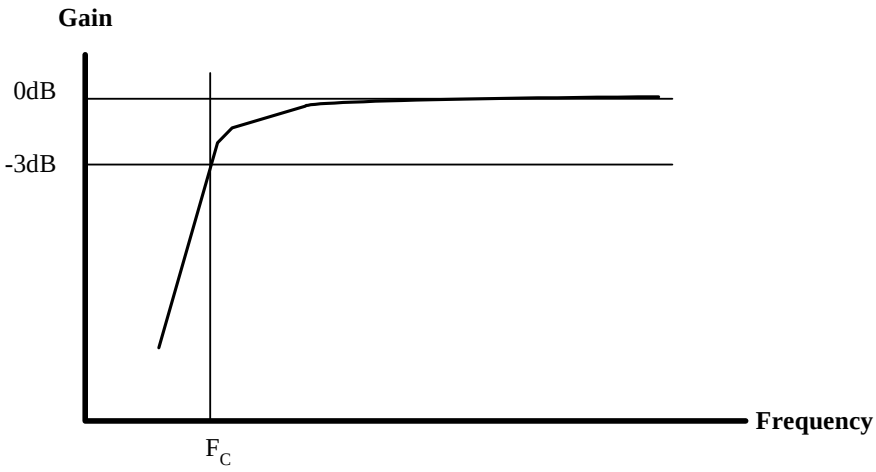
C_D and R_L determines the cut-off frequency of the hi-pass filter as the following equation:

$$F_c = \frac{1}{2\pi \times C_D \times R_L}$$

e.g.

1. C_D = 10 μF → F_c = 1/(2x3.14x10 μ x 32ohm) = 497Hz
2. C_D = 22 μF → F_c = 1/(2x3.14x22 μ x 32ohm) = 226Hz
3. C_D = 47 μF → F_c = 1/(2x3.14x47 μ x 32ohm) = 105Hz

For MP3 application, it is suggested to use the 3rd value for better bass performance.



4.11 GPIO

The MP600 provides 8 dedicated GPIO pins. There are also additional 68 pins can be configured as GPIO if the associated function is not used. Most of the pins can be programmed for alternative functions by setting corresponding configuration register. Those dedicated GPIO pins can be enabled to generate interrupt with level or edge trigger. The polarity of level or edge interrupt is programmable to fit variety of application requirement.

The GPIO input pins with interrupt capability, when enabled, can also be used to wake up the chip from deep power down mode.

5 Operation Modes

To fulfill the functions that a digital photo frame requires, the MP600 can be used in, but not limited to, the following operation modes:

- **Playback/OS command mode**

- The stored images/audio files can be played back to LCD panel, and speaker output port in this mode
- Executable software can be run at this mode for any application
- Manage the available modules of DPF

- **USB upload mode**

- The stored images/audio can be uploaded to PC for further application

- **USB download mode**

- DPF firmware can be updated by downloading the new firmware code and activated automatically
- Executable codes for 32-bit RISC can be downloaded from PC and run at embedded OS environment
- Image or MP3 files can be playback by using the existing hardware inside the DPF

6 Pin Configuration

Pin Definition *(Gray part is only available in MP600B; Pin Number demonstrates as MP600A/MP600B)*

1. Memory Interface (39/45)

Pin Name	*Default*			*Alt. Func. 1*	*Alt. Func. 2*	*Type*
	Function	*SDRAM*	*PROM/ NOR Flash*			
MD[7:0]	MD[7:0]	MD[7:0]	MD[7:0]			IO
MD[11:8]	MD[11:8]	MD[11:8]	MA[20:17]			IO
MD[15:12]	MD[15:12]	MD[15:12]	MD[15:12]			IO
MA[7:0]	MA[7:0]	MA[7:0]	MA[7:0]			O
MA[11:8]	MA[11:8]	MA[11:8]	MA[11:8]			O
MA[12]	MA[12]	MA[12]	MA[21]			O
MBA[0]	BA[0]	BA[0]	MA[12]			O
MBA[1]	BA[1]	BA[1]	MA[13]			O
MRASx	RAS#	RAS#	MA[14]			O
MCASx	CAS#/MOE#	CAS#	MOE#			O
MWEx	MWE#	MWE#	MWE#			O
MDQM[0]	DQM[0]	DQM[0]	MA[15]			O
MDQM[1]	DQM[1]	DQM[1]	MA[16]			O
MSDCK	SDCLK	SDCLK				IO
MSDCKE	SDCKE	SDCKE				O
MSDCSx	SDRAMCS#	SDRAMCS#				O
MROMCSx	MROMCS#		MROMCS#			O
MSDCKx	SDCLKx	SDCLKx				IO
MSDVREF	MSDVREF	MSDVREF				A
MSDLDQS	LDQS	LDQS				IO
MSDUDQS	UDQS	UDQS				IO
MROMDW	MROMDW		MROMDW			I

Pin Name		Pin Number	I/O	Definition
MD[7:0]	MD[7:0]	15, 14, 13, 12, 9, 8, 7, 6 / 19, 18, 17, 16, 11, 10, 9, 8	I/O	DRAM Data Bus bit 7~0
				PROM/NOR Flash Data bit 7~0
MD[11:8]	MD[11:8]	20, 19, 18, 17 / 25, 24, 23, 22	I/O	DRAM Data Bus bit 11~8
	MA[20:17]		O	PROM/NOR Flash Address bit 20~17
MD[15:12]	MD[15:12]	26, 25, 24, 23 / 32, 31, 30, 29	I/O	DRAM Data Bus bit 15
				PROM/NOR Flash Data bit 15~12
MA[7:0]	MA[7:0]	121, 120, 119, 118, 117, 116, 115, 114 / 207, 206, 205, 204, 202, 201, 200, 199	O	DRAM Address Bus bit 7~0
				PROM/NOR Flash Address Bus bit 7~0
MA[11:8]	MA[11:8]	125, 124, 123, 122 / 211, 210, 209, 208	O	DRAM Address Bus bit 11~8
				PROM/NOR Flash Address Bus bit 11~8
MA[12]	MA[12]	-- / 3	O	DRAM Address Bus bit 12
	MA[21]			PROM/NOR Flash Address Bus bit 21
MBA[0]	BA[0]	110 / 195	O	DRAM Bank Selection 0
	MA[12]			PROM/NOR Flash Address Bus bit 12
MBA[1]	BA[1]	111 / 196	O	DRAM Bank Selection 1
	MA[13]			PROM/NOR Flash Address Bus bit 13

MRASx	RAS#	126 / 212	O	DRAM Row Address Strobe (Active low)
	MA[14]			PROM/NOR Flash Address Bus bit 14
MCASx	CAS#	128 / 214	O	DRAM Column Address Strobe (Active low)
	MOE#			PROM/NOR Flash Output Enable (Active low)
MWEx	MWE#	127 / 213	O	DRAM Write Enable (Active low)
				PROM/NOR Flash Write Enable (Active low)
MDQM[0]	DQM[0]	5 / 7	O	DRAM Data Input/Output Mask 0
	MA[15]			PROM/NOR Flash Address Bus bit 15
MDQM[1]	DQM[1]	16 / 21	O	DRAM Data Input/Output Mask 1
	MA[16]			PROM/NOR Flash Address Bus bit 16
MSDCK	SDCLK	3 / 4	I/O	(1) SDCLK: Output Clock to SDRAM
MSDCKx	SDCLK#	-- / 6	I/O	(2) SDCLK&SDCLK#: Output Clock to DDR SDRAM SDCLK and SDCLK# are differential clock Outputs.
MSDCKE	SDCKE	2 / 2	O	Clock Enable Signal for DRAM Clock
MSDCSx	SDRAMCS#	1 / 1	O	DRAM Chip Select
MROMCSx	MROMCS#	107 / 190	O	PROM/NOR Flash Chip Select
MSDVREF	MSDVREF	-- / 20	Analog	DRAM Reference Voltage
MSDLDQS	LDQS	-- / 14	I/O	Data Strobe : Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
MSDUDQS	UDQS	-- / 27	I/O	
MROMDW	MROMDW	-- / 12	I	Select 16-bit Data Bus Width for PROM/NOR Flash

2. Memory Card Interface (CF/SM/SD/MMC/MS Pro/xD) (14/33)

Pin Name	*Default*	*Alt. Func. 1*								*Alt. Func. 2*	*Type*
		CF (Memory)	*SM (NAND Flash)*	*MMC/SD*	*SDIO (MP600A)*	*SDIO (MP600B)*	*MS Pro (MP600A)*	*MS Pro (MP600B)*	*xD*		
FD[3:0]	FGPIO[3:0]	FD[3:0]	SD[3:0]	DAT[3:0]			MSD[3:0]		XD[3:0]		IO
FD[7:4]	FGPIO[7:4]	FD[7:4]	SD[7:4]	DAT[7:4]	DAT[3:0]	DAT[3:0]			XD[7:4]	ROMHD [11:8]	IO
FCLE	FGPIO[8]	FA[0]	SCLE	CMD	CMD		BS	BS	XCLE		IO
FALE	FGPIO[9]	FA[1]	ALE	CLK	CLK	CLK	SCLK	SCLK	XALE		IO
FCEx	FGPIO[10]		SCE1#						XCE#		IO
FRB	FGPIO[11]	FRDY/ BUSY#	SRB						XRB		IO
FOEx	FGPIO[12]	FOE#	SRE#						XRE#		IO
FWEx	FGPIO[13]	FEW#	WE#						XWE#		IO
FSCE0x	FGPIO[14]		SCE0#								IO
FWP	FGPIO[15]		WP#	WP#					XWP#		IO
FPWREN	FGPIO[16]	FPWREN	FPWREN	FPWREN	FPWREN	FPWREN	FPWREN	FPWREN	FPWREN		IO
FSMXDCDx	FGPIO[17]		CDx						XCDx		IO
FSDCDx	FGPIO[18]			CD#							IO
FMSINS	FGPIO[19]						MS_INS	MS_INS			IO
FA2	FGPIO[20]	FA[2]				CMD					IO
FA3	FGPIO[21]	FA[3]									IO
FCE1x	FGPIO[22]	FCE1#									IO
FCE2x	FGPIO[23]	FCE2#									IO
FCD1x	FGPIO[24]	FCD1#									IO
FCD2x	FGPIO[25]	FCD2#									IO
FRESET	FGPIO[26]	FRESET									IO
FWAITx	FGPIO[27]	FWAIT#									IO
FREGx	FGPIO[28]	FREG#									IO
FMSD[3:0]	FGPIO[32:29]							MSD[3:0]			IO

Note: FGPIO[15], FGPIO[19:17] has interrupt capability

Pin Name		Pin Number	I/O	Definition
FD[3:0]	FD[3:0]	67, 66, 65, 64 / 117, 116, 115, 114	I/O	(MP600B) COMPACT FLASH(MEMORY) Data Bus 3~0
	SD[3:0]		I/O	(MP600B) SMART MEDIA(NAND FLASH) Data Bus 3~0
	DAT[3:0]		I/O	MMC/SD Data Bus 3~0
	MSD[3:0]		I/O	(MP600A) MEMORY STICK PRO Data Bus 3~0
	XD[3:0]		I/O	(MP600B) xD Data Bus 3~0
	FGPIO[3:0]		I/O	General purpose I/O 3~0 shared with memory card
FD[7:4]	FD[7:4]	71, 70, 69, 68 / 121, 120, 119, 118	I/O	(MP600B) COMPACT FLASH(MEMORY) Data Bus 7~4
	SD[7:4]		I/O	(MP600B) SMART MEDIA(NAND FLASH) Data Bus 7~4
	DAT[7:4]		I/O	MMC/SD Data Bus 7~4
	DAT[3:0]		I/O	SDIO Data Bus 3~0
	XD[7:4]		I/O	(MP600B) xD Data bus 7~4
	FGPIO[7:4]		I/O	General purpose I/O 7~4 shared with memory card
	ROMHD[11:8]		I/O	PROM/NOR Flash Data bit 11~8
FCLE	FA[0]	75 / 125	O	(MP600B) COMPACT FLASH(MEMORY) Address 0 FA[3:0] along with the FREG# signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
	SCLE		O	(MP600B) SMART MEDIA(NAND FLASH) Command Latch Enable
	CMD		I/O	MMC/SD Command
	CMD		I/O	(MP600A) SDIO Command
	BS		O	MEMORY STICK PRO Bus State
	XCLE		O	(MP600B) xD Clock Enable
	FGPIO[8]		I/O	General purpose I/O 8 shared with memory card
FALE	FA[1]	76 / 126	O	(MP600B) COMPACT FLASH(MEMORY) Address 1
	ALE		O	(MP600B) SMART MEDIA(NAND FLASH) Address Latch Enable
	CLK		O	MMC/SD Clock
	CLK		O	SDIO Clock
	SCLK		O	MEMORY STICK PRO Clock
	XALE		O	(MP600B) xD Address Latch Enable
	FGPIO[9]		I/O	General purpose I/O 9 shared with memory card
FCEx	SCE1#	-- / 127	I/O	(MP600B) SMART MEDIA(NAND FLASH) Chip Enable Strobe (Active low)
	XCE#		I/O	(MP600B) xD Chip Enable Strobe (Active low)
	FGPIO[10]		I/O	General purpose I/O 10 shared with memory card
FRB	FRDY/BUSY#	-- / 128	I/O	(MP600B) COMPACT FLASH(MEMORY) Ready & Busy
	SRB		I/O	(MP600B) SMART MEDIA(NAND FLASH) Ready & Busy

	XRB		I/O	(MP600B) xD Ready & Busy
	FGPIO[11]		I/O	General purpose I/O 11 shared with memory card
FOEx	FOE#	-- / 129	I/O	(MP600B) COMPACT FLASH(MEMORY) Output Enable (Active low)
	SRE#		I/O	(MP600B) SMART MEDIA(NAND FLASH) Read Enable Strobe (Active Low)
	XRE#		I/O	(MP600B) xD Read Enable Strobe (Active low)
	FGPIO[12]		I/O	General purpose I/O 12 shared with memory card
FWEx	FWE#	-- / 130	I/O	(MP600B) COMPACT FLASH(MEMORY) Write Enable Strobe (Active low)
	WE#		I/O	(MP600B) SMART MEDIA(NAND FLASH) Write Enable Strobe (Active low)
	XWE#		I/O	(MP600B) xD write Enable Strobe (Active low)
	FGPIO[13]		I/O	General purpose I/O 13 shared with memory card
FSCE0x	SCE0#	-- / 131	I/O	(MP600B) SMART MEDIA(NAND FLASH) Chip Enable Strobe (Active Low)
	FGPIO[14]		I/O	General purpose I/O 14 shared with memory card
FWP	WP#	77 / 132	I/O	(MP600B) SMART MEDIA(NAND FLASH) Write Protect(Active low)
	WP#		I/O	MMC/SD Write Protect(Active low)
	XWP#		I/O	(MP600B) xD Write Protect (Active low)
	FGPIO[15]		I/O	General purpose I/O 15 shared with memory card
FPWREN	FPWREN	78 / 133	I/O	CF/SMART MEDIA(NAND FLASH)/MMC/SD/SDIO/ MEMORY STICK PRO/xD Power Enable
	FGPIO[16]		I/O	General purpose I/O 16 shared with memory card
FSMXDCDx	CDx	79 / 134	I/O	(MP600B) SMART MEDIA(NAND FLASH) Card Detect (Active low)
	XCDx		I/O	(MP600B) xD Card Detect(Active low)
	FGPIO[17]		I/O	General purpose I/O 17 shared with memory card
FSDCDx	CD#	80 / 135	I/O	MMC/SD Card Detect(Active low)
	FGPIO[18]		I/O	General purpose I/O 18 shared with memory card
FMSINS	MS_INS	81 / 136	I/O	MEMORY STICK PRO Insert
	FGPIO[19]		I/O	General purpose I/O 19 shared with memory card
FA2	FA[2]	-- / 137	I/O	(MP600B) COMPACT FLASH(MEMORY) Address 2
	CMD		I/O	(MP600B) SDIO Command
	FGPIO[20]		I/O	General purpose I/O 20 shared with memory card
FA3	FA[3]	-- / 138	I/O	(MP600B) COMPACT FLASH(MEMORY) Address 3
	FGPIO[21]		I/O	General purpose I/O 21 shared with memory card
FCE1x	FCE1#	-- / 139	I/O	(MP600B) COMPACT FLASH(MEMORY) Card Enable FCE1# accesses the even byte or the Odd byte of the word depending on FA0 and FCE2#
	FGPIO[22]		I/O	General purpose I/O 22 shared with memory card
FCE2x	FCE2#	-- / 140	I/O	(MP600B) COMPACT FLASH(MEMORY) Card Enable FCE2# always accesses the odd byte of the word.

	FGPIO[23]		I/O	General purpose I/O 23 shared with memory card
FCD1x	FCD1#	-- / 184	I/O	(MP600B) COMPACT FLASH(MEMORY) Card Detect 1
	FGPIO[24]		I/O	General purpose I/O 24 shared with memory card
FCD2x	FCD2#	-- / 185	I/O	(MP600B) COMPACT FLASH(MEMORY) Card Detect 2
	FGPIO[25]		I/O	General purpose I/O 25 shared with memory card
FRESET	FRESET	-- / 141	I/O	(MP600B) COMPACT FLASH(MEMORY) Reset
	FGPIO[26]		I/O	General purpose I/O 26 shared with memory card
FWAITx	FWAIT#	-- / 143	I/O	(MP600B) COMPACT FLASH(MEMORY) Wait Enable (Active Low)
	FGPIO[27]		I/O	General purpose I/O 27 shared with memory card
FREGx	FREG#	-- / 146	I/O	(MP600B) COMPACT FLASH(MEMORY) Register (Active low)
	FGPIO[28]		I/O	General purpose I/O 28 shared with memory card
FMSD[3:0]	MSD[3:0]	-- / 150, 149,	I/O	(MP600B) MEMORY STICK PRO Data Bus 3~0
	FGPIO[32:29]	148, 147	I/O	General purpose I/O 32~29 shared with memory card

3. UART Interface (2/2)

Pin Name	*Default*	*Alt. Fnuc. 1*	*Type*
HURX	UGPIO[0]	HURX	IO
HUTX	UGPIO[1]	HUTX	IO

Pin Name		Pin Number	I/O	Definition
HURX	HURX	93 / 159	I/O	High-Speed UART Receive signal
	UGPIO[0]		I/O	General purpose I/O 0 shared with UART
HUTX	HUTX	94 / 160	I/O	High-Speed UART Transmit signal
	UGPIO[1]		I/O	General purpose I/O 1 shared with UART

4. USB Interface (2/10)

Pin Name	*Default*	*Type*		
USBFDM	USBDM	Analog	FS	
USBFDP	USBDP	Analog	FS	
USBHDM	USBHDM	Analog	HS	
USBHDP	USBHDP	Analog	HS	
UREFEXT	UREFEXT	Analog	HS	
URDATAP	URDATAP	Analog	HS	
URDATAN	URDATAN	Analog	HS	
UHVBUS	UHVBUS	I	HS	
UHSXTALI	UHSXTALI	I	HS	
UHSXTALO	UHSXTALO	O	HS	12MHZ

Pin Name		Pin Number	I/O	Definition
USBFDM	USBDM	102 / 181	ANALOG	USB Host full speed D- signal
USBFDP	USBDP	103 / 182	ANALOG	USB Host full speed D+ signal
USBHDM	USBHDM	-- / 168	ANALOG	USB Device full speed D- signal
USBHDP	USBHDP	-- / 167	ANALOG	USB Device full speed D+ signal
UREFEXT	UREFEXT	-- / 170	ANALOG	
URDATAP	URDATAP	-- / 164	ANALOG	
URDATAN	URDATAN	-- / 165	ANALOG	
UHVBUS	UHVBUS	-- / 186	I	
UHSXTALI	UHSXTALI	-- / 179	I	
UHSXTALO	UHSXTALO	-- / 178	O	

5. Digital LCD Interface (12/28)

Pin Name	*Default*	*Alt. Func. 1*				*Alt. Func. 2 (TCON + RGB-666)*	*Alt. Func. 3*	*Type*
		CCIR-656	*CCIR-601*	*YCbCr 24bit*	*RGB 24bit*			
VD0	VGPIO[0]	YC[0]	YC[0]	VY[0]	VR0	R0		IO
VD1	VGPIO[1]	YC[1]	YC[1]	VY[1]	VR1	R1		IO
VD2	VGPIO[2]	YC[2]	YC[2]	VY[2]	VR2	R2		IO
VD3	VGPIO[3]	YC[3]	YC[3]	VY[3]	VR3	R3		IO
VD4	VGPIO[4]	YC[4]	YC[4]	VY[4]	VR4	R4		IO
VD5	VGPIO[5]	YC[5]	YC[5]	VY[5]	VR5	R5		IO
VD6	VGPIO[6]	YC[6]	YC[6]	VY[6]	VR6	G0		IO
VD7	VGPIO[7]	YC[7]	YC[7]	VY[7]	VR7	G1		IO
VD8	VGPIO[8]		VCCIR_C[0]	VCb[0]	VG0	G2		IO
VD9	VGPIO[9]		VCCIR_C[1]	VCb[1]	VG1	G3		IO
VD10	VGPIO[10]		VCCIR_C[2]	VCb[2]	VG2	G4		IO
VD11	VGPIO[11]		VCCIR_C[3]	VCb[3]	VG3	G5		IO
VD12	VGPIO[12]		VCCIR_C[4]	VCb[4]	VG4	B0		IO
VD13	VGPIO[13]		VCCIR_C[5]	VCb[5]	VG5	B1		IO
VD14	VGPIO[14]		VCCIR_C[6]	VCb[6]	VG6	B2		IO
VD15	VGPIO[15]		VCCIR_C[7]	VCb[7]	VG7	B3		IO
VD16	VGPIO[16]			VCr[0]	VB0	B4		IO
VD17	VGPIO[17]			VCr[1]	VB1	B5		IO
VD18	VGPIO[18]			VCr[2]	VB2	GPOL		IO
VDCK	VGPIO[19]	VDCK (27 MHz …)	VDCK	VDCK	VPXCK	SCKH		IO
VHSYNC	VGPIO[20]	VHSYNC	VHSYNC	VHSYNC	DVHSYNC	SSTH		IO
VDVALID	VGPIO[21]	VDVALID	VDVALID	VDVALID	DVDVALID	GSTV		IO
VVSYNC	VGPIO[22]	VVSYNC	VVSYNC	VVSYNC	DVVSYNC	GCKV		IO
VSPOL	VGPIO[23]			VCr[3]	VB3	SPOL		IO
VSREV	VGPIO[24]			VCr[4]	VB4	SREV		IO
VSLD	VGPIO[25]			VCr[5]	VB5	SLD		IO
VGOEV	VGPIO[26]			VCr[6]	VB6	GOEV		IO
VDRVPDN	VGPIO[27]			VCr[7]	VB7	PWRDN		IO

Pin Name		Pin Number	I/O	Definition
VD0	YC[0]	30 / 52	O	CCIR656/CCIR601 Data Bus Bit 0
	VY[0]		O	YCbCr Data Bus Y Bit 0
	VR0		O	RGB 24bit Data Bus Bit 0
	R0		O	TCON Data Bus R Bit 0
	VGPIO[0]		I/O	General purpose I/O 0 Shared with Video Output pin
VD1	YC[1]	31 / 53	O	CCIR656/CCIR601 Data Bus Bit 1
	VY[1]		O	YCbCr Data Bus Y Bit 1
	VR1		O	RGB 24bit Data Bus Bit 1
	R1		O	TCON Data Bus R Bit 1
	VGPIO[1]		I/O	General purpose I/O 1 Shared with Video Output pin
VD2	YC[2]	32 / 54	O	CCIR656/CCIR601 Data Bus Bit 2
	VY[2]		O	YCbCr Data Bus Y Bit 2
	VR2		O	RGB 24bit Data Bus Bit 2
	R2		O	TCON Data Bus R Bit 2
	VGPIO[2]		I/O	General purpose I/O 2 Shared with Video Output pin
VD3	YC[3]	33 / 65	O	CCIR656/CCIR601 Data Bus Bit 3
	VY[3]		O	YCbCr Data Bus Y Bit 3
	VR3		O	RGB 24bit Data Bus Bit 3
	R3		O	TCON Data Bus R Bit 3
	VGPIO[3]		I/O	General purpose I/O 3 Shared with Video Output pin
VD4	YC[4]	34 / 66	O	CCIR656/CCIR601 Data Bus Bit 4
	VY[4]		O	YCbCr Data Bus Y Bit 4
	VR4		O	RGB 24bit Data Bus Bit 4
	R4		O	TCON Data Bus R Bit 4
	VGPIO[4]		I/O	General purpose I/O 4 Shared with Video Output pin
VD5	YC[5]	35 / 67	O	CCIR656/CCIR601 Data Bus Bit 5
	VY[5]		O	YCbCr Data Bus Y Bit 5
	VR5		O	RGB 24bit Data Bus Bit 5
	R5		O	TCON Data Bus R Bit 5
	VGPIO[5]		I/O	General purpose I/O 5 Shared with Video Output pin
VD6	YC[6]	36 / 68	O	CCIR656/CCIR601 Data Bus Bit 6
	VY[6]		O	YCbCr Data Bus Y Bit 6
	VR6		O	RGB 24bit Data Bus R Bit 6
	G0		O	TCON Data Bus G Bit 0
	VGPIO[6]		I/O	General purpose I/O 6 Shared with Video Output pin
VD7	YC[7]	39 / 71	O	CCIR656/CCIR601 Data Bus Bit 7
	VY[7]		O	YCbCr Data Bus Y Bit 7
	VR7		O	RGB 24bit Data Bus R Bit 7
	G1		O	TCON Data Bus G Bit 1
	VGPIO[7]		I/O	General purpose I/O 7 Shared with Video Output pin
VD8	VCCIR_C[0]	-- / 33	O	CCIR601 Data Bus Bit 8
	VCb[0]		O	YCbCr data bus Cb bit 0
	VG0		O	RGB 24bit data bus G bit 0
	G2		O	TCON Data Bus G Bit 2

	VGPIO[8]		I/O	General purpose I/O 8 Shared with Video Output pin
VD9	VCCIR_C[1]	-- / 34	O	CCIR601 Data Bus Bit 9
	VCb[1]		O	YCbCr data bus Cb bit 1
	VG1		O	RGB 24bit data bus G bit 1
	G3		O	TCON Data Bus G Bit 3
	VGPIO[9]		I/O	General purpose I/O 9 Shared with Video Output pin
VD10	VCCIR_C[2]	-- / 35	O	CCIR601 Data Bus Bit 10
	VCb[2]		O	YCbCr data bus Cb bit 2
	VG2		O	RGB 24bit data bus G bit 2
	G4		O	TCON Data Bus G Bit 4
	VGPIO[10]		I/O	General purpose I/O 10 Shared with Video Output pin
VD11	VCCIR_C[3]	-- / 36	O	CCIR601 Data Bus Bit 11
	VCb[3]		O	YCbCr data bus Cb bit 3
	VG3		O	RGB 24bit data bus G bit 3
	G5		O	TCON Data Bus G Bit 5
	VGPIO[11]		I/O	General purpose I/O 11 Shared with Video Output pin
VD12	VCCIR_C[4]	-- / 37	O	CCIR601 Data Bus Bit 12
	VCb[4]		O	YCbCr data bus Cb bit 4
	VG4		O	RGB 24bit data bus G bit 4
	B0		O	TCON Data Bus B Bit 0
	VGPIO[12]		I/O	General purpose I/O 12 Shared with Video Output pin
VD13	VCCIR_C[5]	-- / 38	O	CCIR601 Data Bus Bit 13
	VCb[5]		O	YCbCr data bus Cb bit 5
	VG5		O	RGB 24bit data bus G bit 5
	B1		O	TCON Data Bus B Bit 1
	VGPIO[13]		I/O	General purpose I/O 13 Shared with Video Output pin
VD14	VCCIR_C[6]	-- / 39	O	CCIR601 Data Bus Bit 14
	VCb[6]		O	YCbCr data bus Cb bit 6
	VG6		O	RGB 24bit data bus G bit 6
	B2		O	TCON Data Bus B Bit 2
	VGPIO[14]		I/O	General purpose I/O 14 Shared with Video Output pin
VD15	VCCIR_C[7]	-- / 40	O	CCIR601 Data Bus Bit 15
	VCb[7]		O	YCbCr data bus Cb bit 7
	VG7		O	RGB 24bit data bus G bit 7
	B3		O	TCON Data Bus B Bit 3
	VGPIO[15]		I/O	General purpose I/O 15 Shared with Video Output pin
VD16	VCr[0]	-- / 41	O	YCbCr data bus Cr bit 0
	VB0		O	RGB 24bit data bus B bit 0
	B4		O	TCON Data Bus B Bit 4
	VGPIO[16]		I/O	General purpose I/O 16 Shared with Video Output pin
VD17	VCr[1]	-- / 42	O	YCbCr data bus Cr bit 1
	VB1		O	RGB 24bit data bus B bit 1
	B5		O	TCON Data Bus B Bit 5
	VGPIO[17]		I/O	General purpose I/O 17 Shared with Video Output pin
VD18	VCr[2]	-- / 43	O	YCbCr data bus Cr bit 2
	VB2		O	RGB 24bit data bus B bit 2

	GPOL		O	TCON Gate Driver Polarity Select
	VGPIO[18]		I/O	General purpose I/O 18 Shared with Video Output pin
VDCK	VDCK	28 / 45	O	CCIR656/CCIR601 CLOCK
	VDCK		O	YCbCr CLOCK
	VPXCK		O	RGB 24bit CLOCK
	SCKH		O	TCON CLOCK
	VGPIO[19]		I/O	General purpose I/O 19 Shared with Video Output pin
VHSYNC	VHSYNC	40 / 72	O	CCIR656/CCIR601 VHSYNC
	VHSYNC		O	YCbCr VHSYNC
	DVHSYNC		O	RGB 24bit VHSYNC
	SSTH		O	TCON CLOCK
	VGPIO[20]		I/O	General purpose I/O 20 Shared with Video Output pin
VDVALID	VDVALID	41 / 73	O	CCIR656/CCIR601 VDVALID
	VDVALID		O	YCbCr VDVALID
	DVDVALID		O	RGB 24bit VDVALID
	GSTV		O	TCON Gate driver Start Pulse
	VGPIO[21]		I/O	General purpose I/O 21 Shared with Video Output pin
VVSYNC	VVSYNC	42 / 74	O	CCIR656/CCIR601 VVSYNC
	VVSYNC		O	YCbCr VVSYNC
	DVVSYNC		O	RGB 24bit VVSYNC
	GCKV		O	TCON Gate Driver Shift Clock
	VGPIO[22]		I/O	General purpose I/O 22 Shared with Video Output pin
VSPOL	VCr[3]	-- / 47	O	YCbCr data bus Cr bit 3
	VB3		O	RGB 24bit data bus B bit 3
	SPOL		O	TCON Source Driver Polarity Select
	VGPIO[23]		I/O	General purpose I/O 23 Shared with Video Output pin
VSREV	VCr[4]	-- / 48	O	YCbCr data bus Cr bit 4
	VB4		O	RGB 24bit data bus B bit 4
	SREV		O	TCON Source Driver Data Reverse Control
	VGPIO[24]		I/O	General purpose I/O 24 Shared with Video Output pin
VSLD	VCr[5]	-- / 49	O	YCbCr data bus Cr bit 5
	VB5		O	RGB 24bit data bus B bit 5
	SLD		O	TCON Source Driver Latch Pulse and Output Enable
	VGPIO[25]		I/O	General purpose I/O 25 Shared with Video Output pin
VGOEV	VCr[6]	-- / 50	O	YCbCr data bus Cr bit 6
	VB6		O	RGB 24bit data bus B bit 6
	GOEV		O	TCON Gate Driver Output Disable
	VGPIO[26]		I/O	General purpose I/O 26 Shared with Video Output pin
VDRVPDN	VCr[7]	-- / 51	O	YCbCr data bus Cr bit 7
	VB7		O	RGB 24bit data bus B bit 7
	PWRDN		O	TCON Power Down Timing
	VGPIO[27]		I/O	General purpose I/O 27 Shared with Video Output pin

6. Audio Interface (0/5)

Pin Name	*Default*	*Alt. Func. 1*	*Type*
ACLK	AGPIO[0]	ACLK	IO
AMCLK	AGPIO[1]	AMCLK/ ARSYNC	IO
AFSYNC	AGPIO[2]	AFSYNC/ ATSYNC	IO
ADIN	AGPIO[3]	ADIN	IO
ADOUT	AGPIO[4]	ADOUT	IO

Pin Name		Pin Number	I/O	Definition
ACLK	ACLK	-- / 109	I/O	Acknowledge signal
AMCLK	AMCLK/ ARSYNC	-- / 110	I/O	
AFSYNC	AFSYNC/ ATSYNC	-- / 111	I/O	
ADIN	ADIN	-- / 112	I/O	
ADOUT	ADOUT	-- / 113	I/O	

7. Audio DAC Analog Interface (13/15)

Pin Name	***Default***	***Type***
ASPKLP	ASPKLP	A
ASPKLN	ASPKLN	A
ASPKRP	ASPKRP	A
ASPKRN	ASPKRN	A
ASPKEQ1	ASPKEQ1	A
ASPKEQ2	ASPKEQ2	A
ASPKEQ3	ASPKEQ3	A
ASPKEQ4	ASPKEQ4	A
ASPKEQ5	ASPKEQ5	A
ASPKEQ6	ASPKEQ6	A
AHPL	AHPL	A
AHPR	AHPR	A
ALOUTL	ALOUTL	A
ALOUTR	ALOUTR	A
AVCOM	AVCOM	A

Pin Name		Pin Number	I/O	Definition
ASPKLP	ASPKLP	61 / 95	I/O	Non-inverting L speaker-driver output. The maximum signal swing = 3.2 volt. peak-to-peak for 8 Ohm load between ASPKLP and ASPKLN.
ASPKLN	ASPKLN	62 / 96	I/O	Inverting L speaker-driver output. The maximum signal swing = 3.2 volt. peak-to-peak for 8 Ohm load between

				ASPKLP and ASPKLN.
ASPKRP	ASPKRP	57 / 91	I/O	Non-inverting R speaker-driver output. The maximum signal swing = 3.2 volt. peak-to-peak for 8 Ohm load between ASPKRP and ASPKRN.
ASPKRN	ASPKRN	58 / 92	I/O	Inverting R speaker-driver output. The maximum signal swing = 3.2 volt. peak-to-peak for 8 Ohm load between ASPKRP and ASPKRN.
ASPKEQ1	ASPKEQ1	53 / 87	I/O	Equalizer pin 1.
ASPKEQ2	ASPKEQ2	54 / 88	I/O	Equalizer pin 2.
ASPKEQ3	ASPKEQ3	55 / 89	I/O	Equalizer pin 3.
ASPKEQ4	ASPKEQ4	52 / 86	I/O	Equalizer pin 4.
ASPKEQ5	ASPKEQ5	51 / 85	I/O	Equalizer pin 5.
ASPKEQ6	ASPKEQ6	50 / 84	I/O	Equalizer pin 6.
AHPL	AHPL	48 / 80	I/O	Headphone L channel output, the maximum signal swing is 1.6 volt. peak-to-peak for 32 Ohm load.
AHPR	AHPR	47 / 79	I/O	Headphone R channel output, the maximum signal swing is 1.6 volt. peak-to-peak for 32 Ohm load.
ALOUTL	ALOUTL	-- / 83	I/O	Line Buffer L channel output.
ALOUTR	ALOUTR	-- / 82	I/O	Line Buffer R channel output.
AVCOM	AVCOM	45 / 77	I/O	Analog reference voltage. The voltage is about half of the voltage of AVDD.

8. GPIO Interface (8/8)

Pin Name	*Default*	*Alt. Func. 1*	*Alt. Func. 2*	*Alt.Func. 3*	*Type*	
GPIO0	GPIO0	SMCKO				SMCKO and SMDQ are for I2C master
GPIO1	GPIO1	SMDQ				
GPIO2	GPIO2/IRDIN					IRDIN is the IR data input
GPIO3	GPIO3	PWMQ3				
GPIO4	GPIO4					
GPIO5	GPIO5					
GPIO6	GPIO6/SSCKI					SSCKI and SSDQ are for I2C slave
GPIO7	GPIO7	SSDQ				

Pin Name	Default	Pin Number	I/O	Definition
GPIO0	GPIO0	85 / 151	I/O	Dedicated General purpose I/O 0
	SMCKO		O	I2C interface clock pin (Master mode)
GPIO1	GPIO1	86 / 152	I/O	Dedicated General purpose I/O 1
	SMDQ		O	I2C interface data pin (Master mode)
GPIO2	GPIO2	87 / 153	I/O	Dedicated General purpose I/O 2
	IRDIN		I	Infra Red signal data input
GPIO3	GPIO3	88 / 154	I/O	Dedicated General purpose I/O 3
	PWMQ3		O	Pulse width Modulated Output 3
GPIO4	GPIO4	89 / 155	I/O	Dedicated General purpose I/O 4
GPIO5	GPIO5	90 / 156	I/O	Dedicated General purpose I/O 5
GPIO6	GPIO6	91 / 157	I/O	Dedicated General purpose I/O 6
	SSCKI		I/O	I2C interface clock pin (Slave mode)
GPIO7	GPIO7	92 / 158	I/O	Dedicated General purpose I/O 7
	SSDQ		I/O	I2C interface data pin (Slave mode)

9. RTC Interface (0/3)

Pin Name	*Default*	*Type*
RXIN	RXIN	I
RXOUT	RXOUT	O
RALARM	RALARM	O

Pin Name		Pin Number	I/O	Definition
RXIN	RXIN	-- / 174	I	
RXOUT	RXOUT	-- / 175	O	
RALARM	RALARM	-- / 176	O	

10. Miscellaneous (4/5)

Pin Name	*Default*	*Type*	
RESETx	RESETx	I	
CLKIN	CLKIN	I	
CLKOUT	CLKOUT	O	
NAFBOOT	NAFBOOT	I	Boot up from NAND Flash
TESTMD	TESTMD	I	

Pin Name		Pin Number	I/O	Definition
RESETx	RESETx	95 / 161	I	
CLKIN	CLKIN	106 / 189	I	
CLKOUT	CLKOUT	105 / 188	O	
NAFBOOT	NAFBOOT	-- / 187	I	
TESTMD	TESTMD	96 / 162	I	

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Units
VPP	I/O supply Voltage (VPP1~4, VPPM1~3, UHVPP)	-1.0 to 4.6	V
VPPA	Audio I/O supply Voltage (VPPA_A1, VPPA_HP, VPPA_SPKR, VPPA_SPKL)	-0.5 to 4.5	V
VDD	Core supply Voltage (VDD1~6, VDDA_P12, VDDA_P3)	-1.0 to 4.6	V
Vin5	DC Input Voltage for 5V-tolerant I/O [2]	-1.0 to 5.5	V
Vin	DC Input Voltage for non-5V-tolerant I/O	-1.0 to 4.6	V
TSTG	Storage Temperature	-40 to 125	°C
ESD	ESD Rating (Rzap = 1.5K Ω, Czap = 100pf)	TBD	V

Note: 1. Permanent device damage may occurs if the specification for the Absolute Maximum Ratings are exceeded.

2. 5V tolerant I/O including HURX, HUTX, GPIO[7:0].

3. All voltages are defined with respect to ground.

7.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VPP	I/O supply Voltage (VPP1~4, VPPM1~3, UHVPP)	3.1	3.3	3.6	V
VPPA	Audio I/O supply Voltage (VPPA_A1, VPPA_HP, VPPA_SPKR, VPPA_SPKL)	2.7	3.6	4.2	V
VDD	Core supply Voltage (VDD1~6, VDDA_P12, VDDA_P3)	1.68	1.8	1.98	V
TA	Ambient Operating Temperature	0	-	70	°C

7.3 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	TTL			0.8	V
V_{IH}	Input High Voltage	TTL	2.2			V
V_{IL} –SCH [1]	Schmitt-triggered Input Low Voltage	Schmitt Trig. TTL			0.9	V
V_{IH} –SCH [1]	Schmitt trig. Input High Voltage	Schmitt Trig. TTL	1.9			V
V_{OL}	Output Low Voltage	4mA load			0.4	V
V_{OH}	Output High Voltage	4mA load	0.8*VPP			V

R_d [2]	Pull Down Resistance	-	91	120	215	KΩ
I_i	Input Leakage Current	Vo = 3.3V or 0V	-	10nA	1μA	
Ioz	Tri-state Output Leakage Current	Vo = 3.3V or 0V		10nA	1μA	

Note: 1. The I/O with Schmitt-trigger: TESTMD, RESETx and GP[1:0].

2. The I/O with pull-down: TESTMD.

7.4 Capacitance

Symbol	Parameter	Min.	Typ.	Max.	Units
C_{XIN}	Clock Input, CLKIN, capacitance		7		pF
C_{IN}	Input pin capacitance		5		pF
C_{BI}	Bidirectional pin capacitance		5		pF
C_{BI5}	Bidirectional pin capacitance for 5V-tolerant I/O		7		pF
C_{OUT}	Output pin capacitance		5		pF

7.5 AC Characteristics

7.5.1 *Reset Timing*

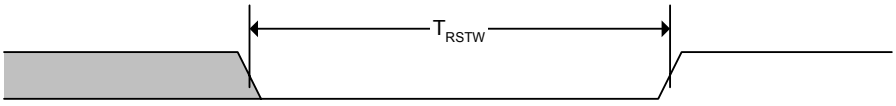
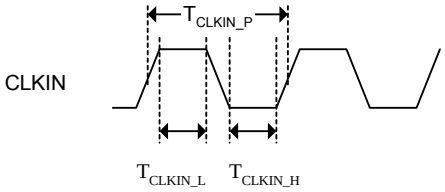


Fig. 7-1 Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{RSTW}	Reset Pulse Width	1			ms

7.5.2 *Input Clock*

Fig. 7-2 CLKIN AC Characteristic



Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{CLKIN}	CLKIN Master Clock Input Frequency		13.5		MHZ
T_{CLKIN_P}	CLKIN Master Clock Input Period		74		ns
T_{CLKIN_L}	CLKIN Master Clock Input Low Width	33.3		40.7	ns
T_{CLKIN_H}	CLKIN Master Clock Input High Width	33.3		40.7	ns
DT_{CLKIN}	CLKIN Duty Cycle	45		55	%

7.5.3 *SDRAM Interface Timing*

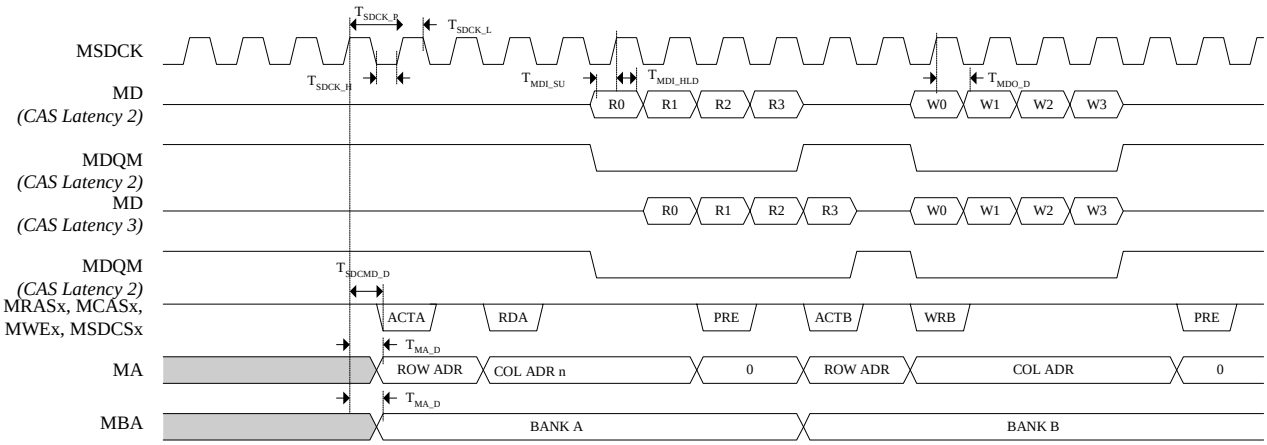


Fig. 7-3 Basic SDRAM Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{SDCK_P}	SDRAM Clock Output Period	13.9			ns
T_{SDCK_H}	SDRAM Clock Output High Pulse Width	4.6			ns
T_{SDCK_L}	SDRAM Clock Output Low Pulse Width	4.6			ns
T_{MDI_SU}	SDRAM Data Input Setup Time	TBD			ns
T_{MDI_HLD}	SDRAM Data Input Hold Time	TBD			ns
T_{MA_D}	SDRAM Address Valid Delay			TBD	ns
T_{MDO_D}	SDRAM Data Output Valid Delay			TBD	ns
T_{SDCMD_D}	SDRAM Command Valid Delay			TBD	ns

7.5.4 *Display Output*

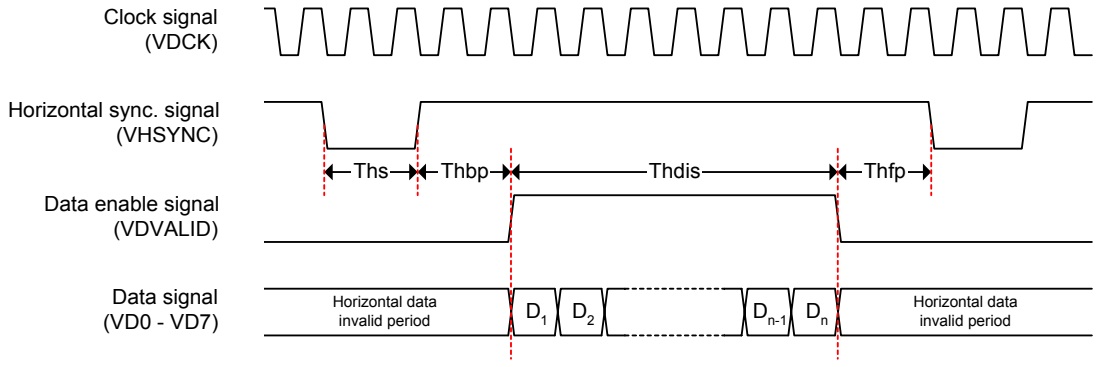


Fig. 7-4 Display/CCIR-601 Output Horizontal Timing

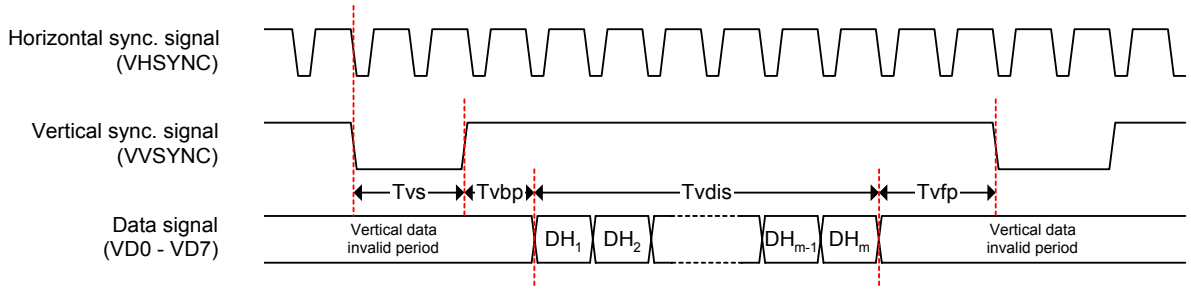


Fig. 7-5 Progressive Display Output Vertical Timing

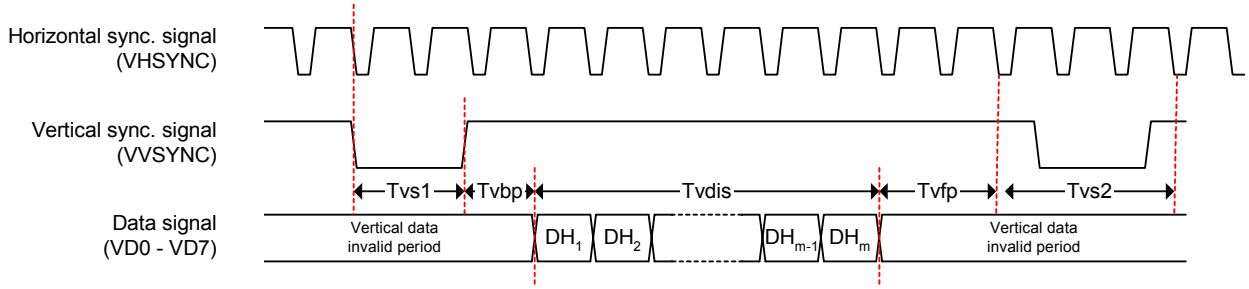


Fig. 7-6 Progressive Display Output Vertical Timing

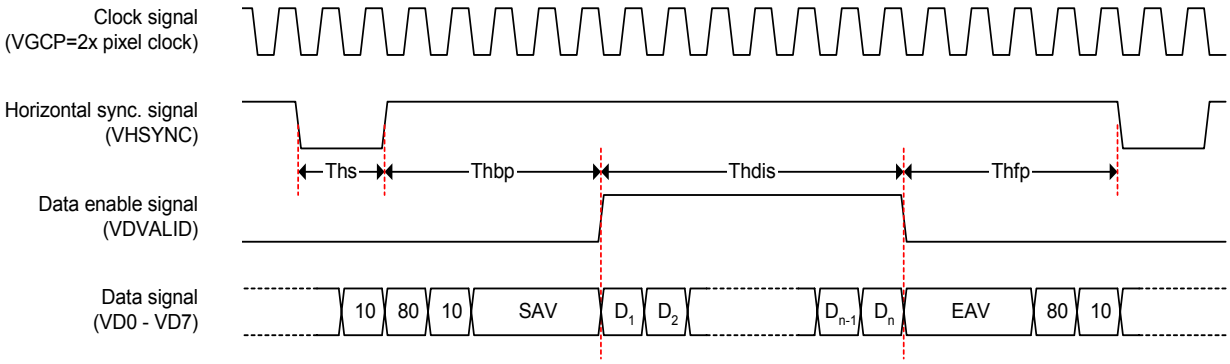


Fig. 7-7 CCIR-656 Output Horizontal Timing

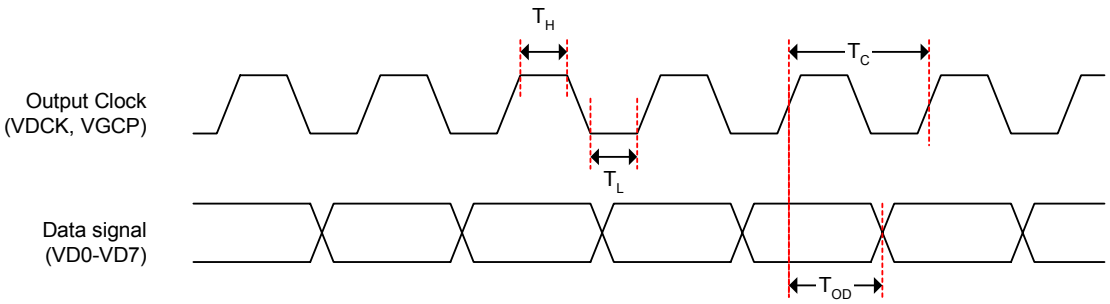
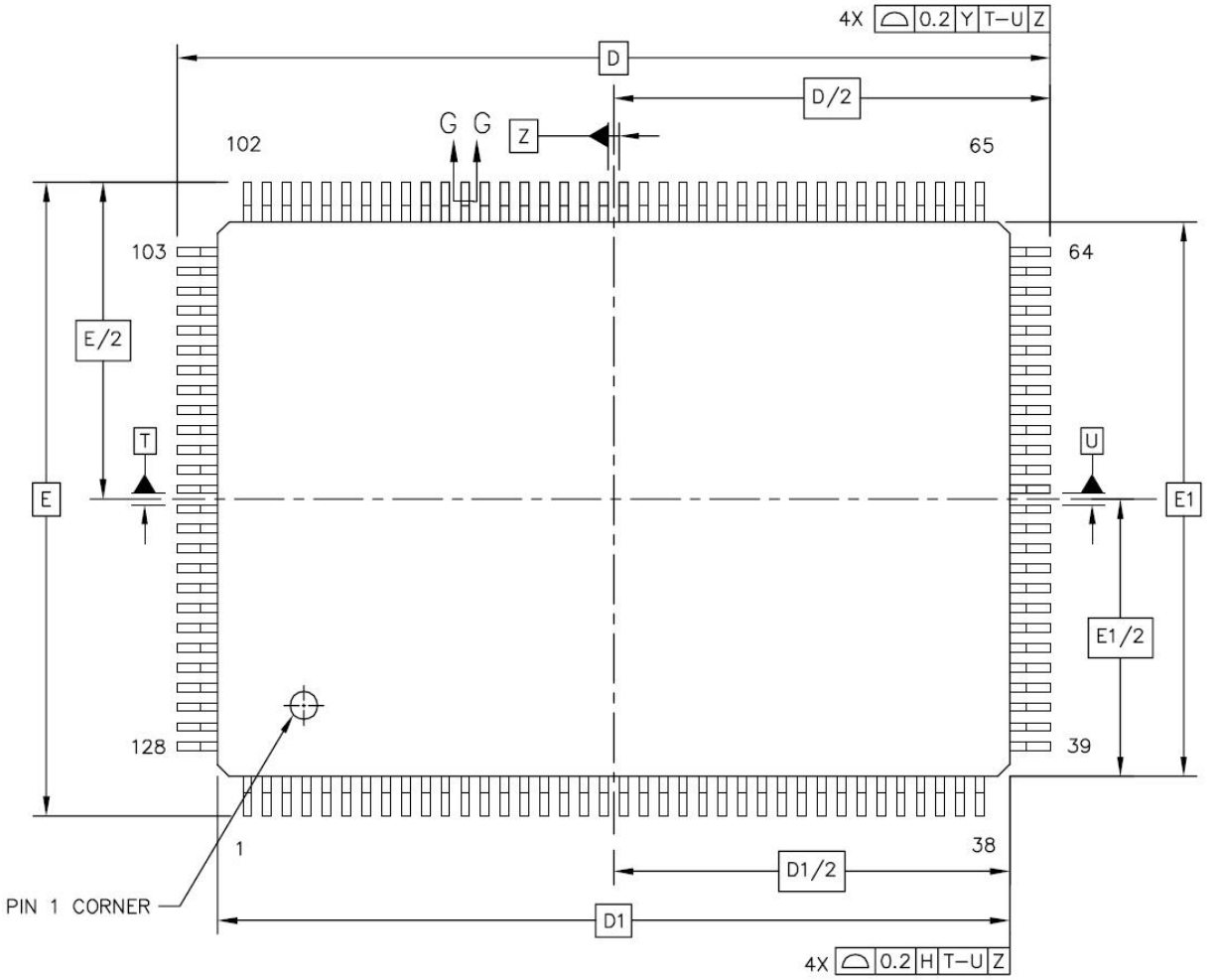


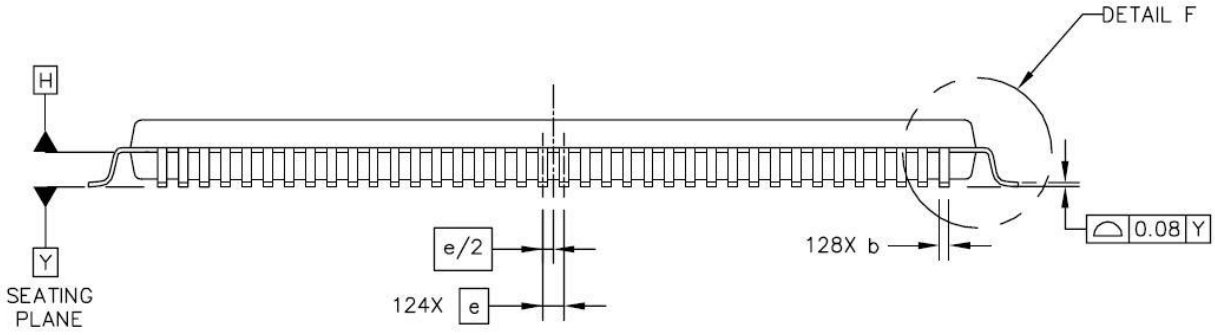
Fig. 7-8 Display Output Clock, and Data Sample Timing

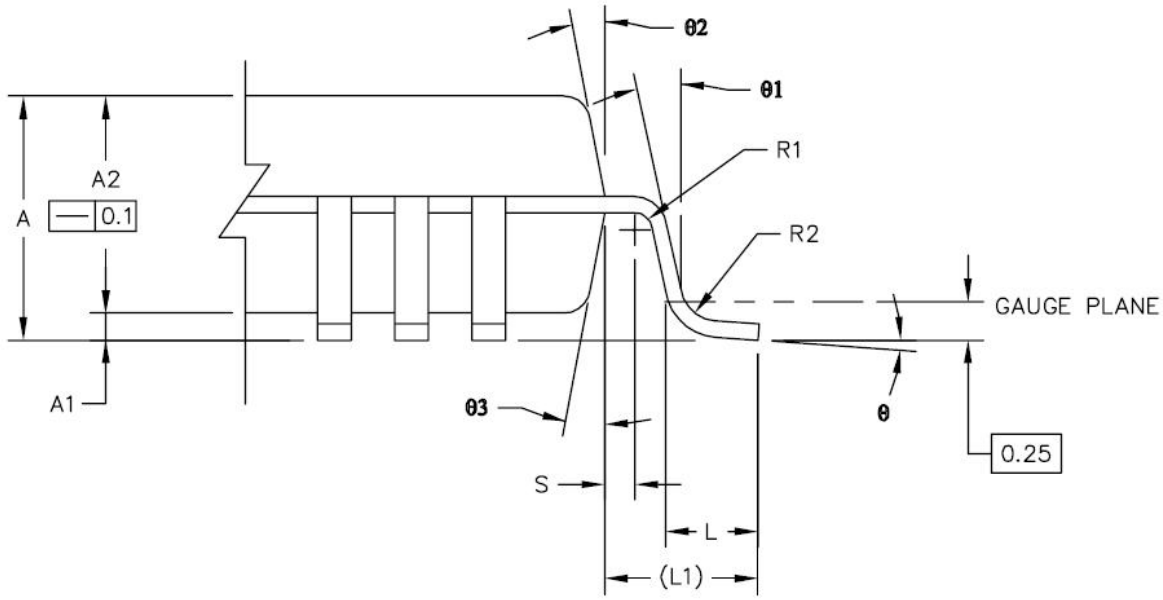
Symbol		Parameter	Min.	Typ.	Max.	Unit
T_{hs}		Horizontal Sync. Pulse Width	1		256	VDCK
T_{hbp}		Display Horizontal Back Porch Width	1		256	VDCK
T_{hdis}		Horizontal Display Enable Width	1		2048	VDCK
T_{hfp}		Display Horizontal Front Porch Width	1		256	VDCK
T_{vs}		Vertical Sync. Pulse Width	1		256	line
T_{vbp}		Display Vertical Back Porch Width	1		256	line
T_{vdis}		Vertical Display Enable Width	1		2048	line
T_{vfp}		Display Vertical Back Porch Width	1		256	line
T_C	VDCK	VDCK Clock Cycle Time	65			ns
	VGCP	VGCP (2x of VDCK) Clock Cycle Time	33			ns
T_H	VDCK	VDCK Clock High Pulse Width	20			ns
	VGCP	VGCP (2x of VDCK) Clock High Pulse Width	11			ns
T_L	VDCK	VDCK Clock Low Pulse Width	20			ns
	VGCP	VGCP (2x of VDCK) Clock Low Pulse Width	11			ns
T_{OD}	VDCK	Display Data Output delay time relative to the rising edge of VDCK			TBD	ns
	VGCP	Display Data Output delay time relative to the rising edge of VGCP			TBD	ns

7.6 Package Dimensions

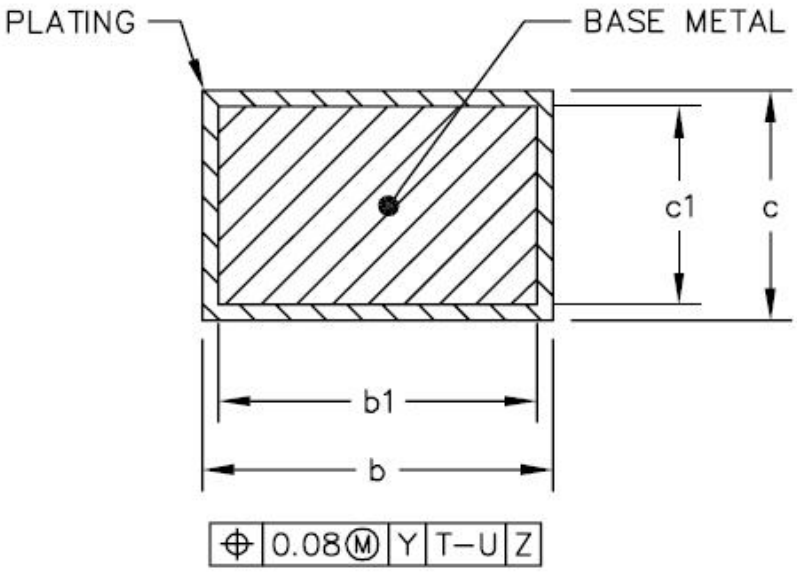
MP600A Package Outline for QFP 128 Pin (14mm x 20mm x 2.75mm, Pin Pitch = 0.5mm)







DETAIL F



3 SECTION G–G

NOTES:

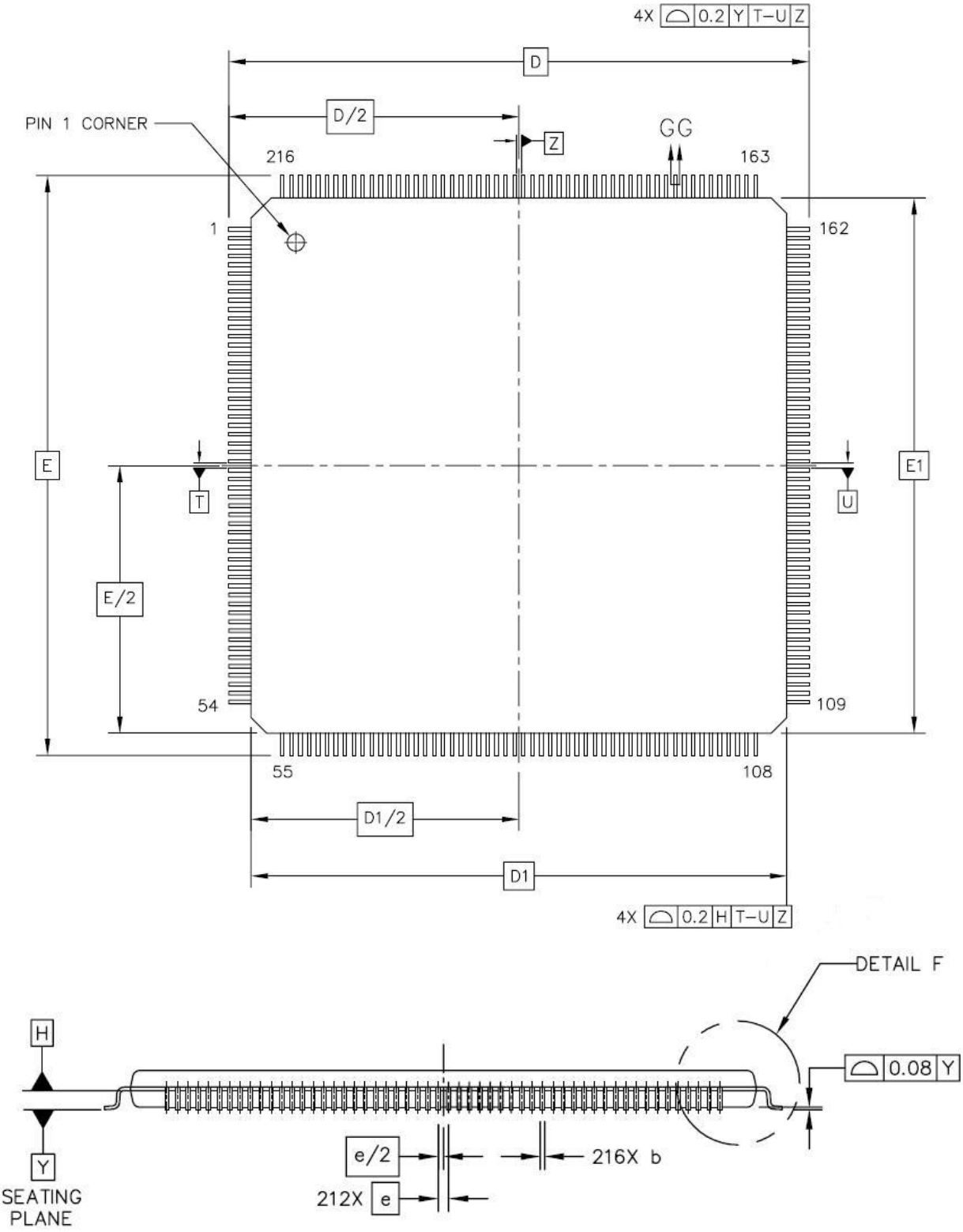
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

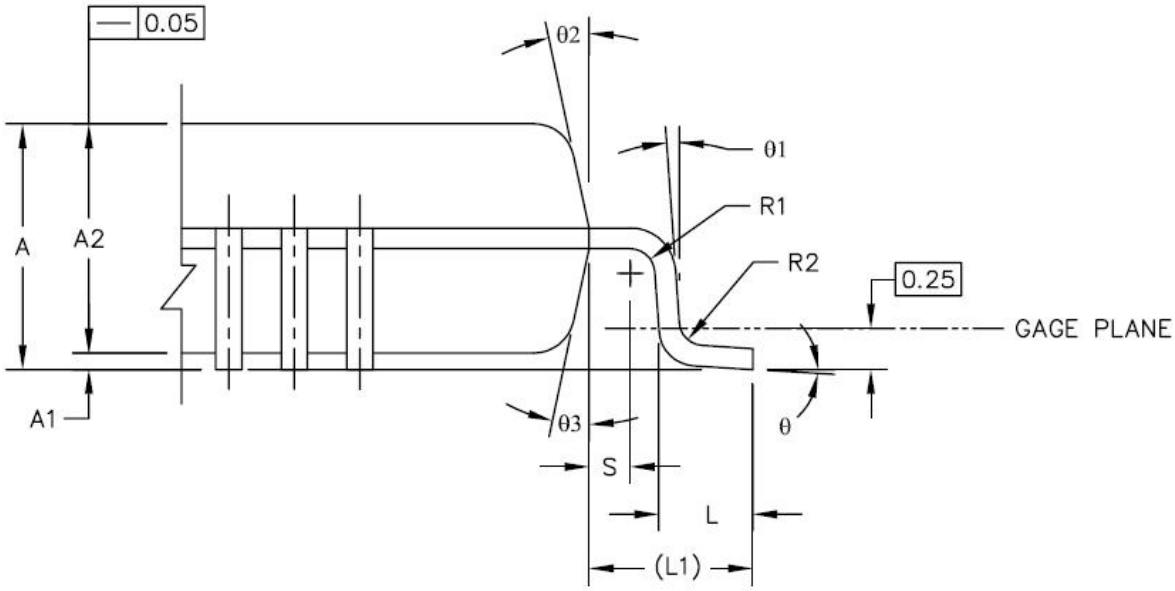
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGES.

3 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1mm AND 0.25mm FROM THE LEAD TIP.

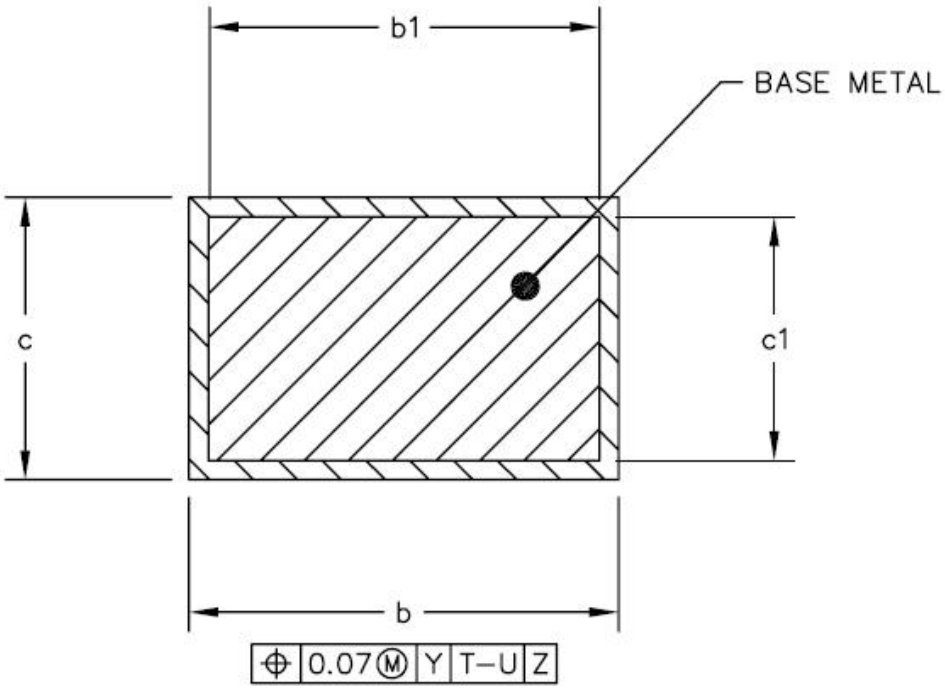
DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	---		3.4	L1		1.6 REF	
A1	0.25		---	R1	0.13		---
A2	2.5	2.72	2.9	R2	0.13		0.3
b	0.17	0.2	0.27	S	0.2		---
b1	0.17	0.2	0.23	θ	0°	3.5°	7°
c	0.11	0.15	0.23	θ1	0°		---
c1	0.09		0.16	θ2		15° REF	
D		23.2 BSC		θ3		15° REF	
D1		20 BSC					
e		0.5 BSC					
E		17.2 BSC					
E1		14 BSC					
L	0.73	0.88	1.03				

MP600B Package Outline for LQFP 216 Pin (24mm x 24mm x 1.4mm, Pin Pitch = 0.4mm)





DETAIL F



SECTION G–G

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX
A	---		1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09		0.2
c1	0.09		0.16
D		26 BSC	
D1		24 BSC	
e		0.4 BSC	
E		26 BSC	
E1		24 BSC	
L	0.45	0.6	0.75

DIM	MIN	NOM	MAX
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S	0.2		---
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°

8 Revision History

Date	Revision	Description
Mar. 02. 2007	0.1	Initial Version
Mar. 05. 2007	0.2	Spike Update
Mar. 05. 2007	0.3	First version for Release
Mar. 08. 2007	0.8	Initial Release