# PC Camera Controller

# SN9C128 Specification

## Released Version 1.0

## Jan 5, 2005

| Revision Number | Date | Description |
|---|---|---|
| 1.0 | Jan 5, 2005 | Released |

# Table of Content

# 1 General Description

SN9C128 provides a low power-consumption, cost effective and superior image quality solution for PC camera controller with VGA image sensor. It integrates sensor interface, image signal processing, image compression and USB transfer function into one single chip. SN9C128 supports various image sensors with RGB Bayer pattern and comes with image signal processing blocks such as gamma and color correction, edge enhancement, auto exposure and auto white balance controls. The built-in JPEG compression engine makes the VGA frame rate up to 30fps on USB1.1 to come true. With the auxiliary hardware windowing and scaling, we can provide a variety of image format. The driver of SN9C128 has passed Microsoft's WHQL certification and it is 48-pin LQFP package without external memory needed.

# 2 Features

§ Provide several effects like 'cavas', 'neon light', 'ellipse', 'glass tile', 'wind' that applied to the video stream dynamically..

§ Several default frames can be applied to the video stream to create the postcard and greeting card.

§ Customer can load the self-created frames.

§ Up to 30fps@VGA video streaming

§ Support Image sensor with 9-bit RGB Bayer pattern raw data input

§ Support CIF/VGA CMOS sensors, such as Hynix 7131D/E/R, Micron 0343/0360, OmniVision 7648/7649/7660, …etc

§ Provide pixel offset compensation and individual R/G/B digital color gain controls

§ Provide defect pixel cancellation by EEPROM

§ Provide hardware windowing, 1/2, 1/4 scaling function with smooth filter

§ Provide programmable gamma and color correction

§ Provide noise clearing and edge enhancement

§ Embedded hardware color DSP and JPEG baseline capability of compression encoder

§ Auto exposure control

§ Auto white balance control

§ Provide snapshot function

§ Support operation mode in image quality/frame rate selection

§ Support video data transfer either in USB isochronous or bulk modes

§ Up to 9 alternated setting for USB isochronous transfer of video data

§ Built-in external EEPROM controller for customer V_ID, P_ID

§ Provide internal up to 26 various P_ID in default setting

§ USB 1.1 compliance and support suspend mode

§ USB 4 endpoints: control, isochronous read, bulk read, interrupt read

§ 12MHz crystal, 3.3V I/O, 1.8V core

§ 48 pins LQFP package

§ No external memory needed

# 3 System Application
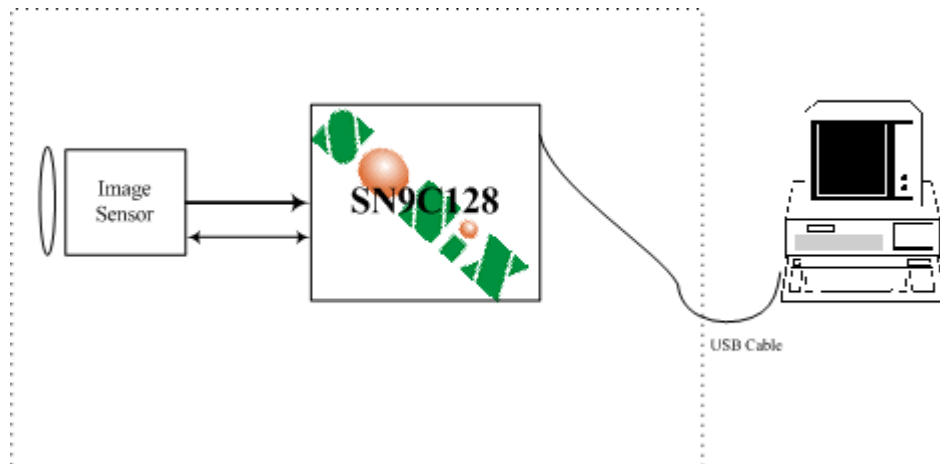


# 4 Functional Block Diagram
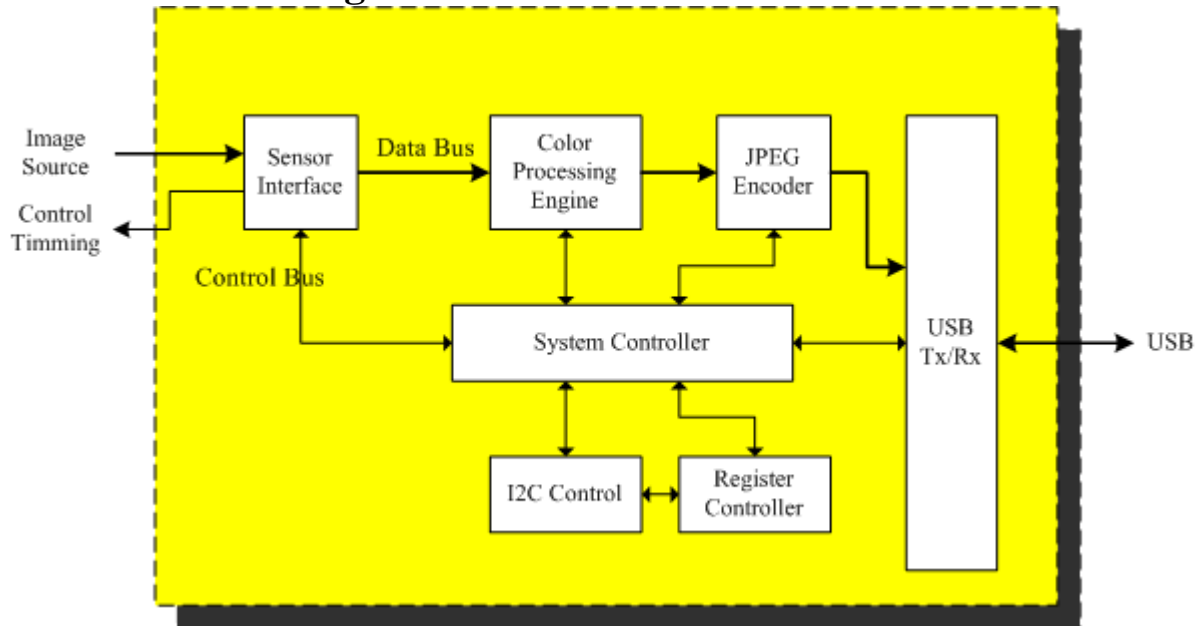
## 5 Pin Assignment

| LQFP 48 | PIN NAME | DIR | Description | Note |
|---|---|---|---|---|
| 1 | GPIO2 | B | General purpose I/O | |
| 2 | GPIO0 | B | General purpose I/O | |
| 4 | PID_SEL2 | I | Product ID selection (H,L,Z)[2] | |
| 5 | PID_SEL1 | I | Product ID selection (H,L,Z)[2] | |
| 6 | PID_SEL0 | I | Product ID selection (H,L,Z)[2] | |
| 8 | KEY | I | KEY input (wake-up) | |
| 9 | RST | I | Chip reset | |
| 14 | GND18 | P | CORE Ground | |
| | TAVSS | P | GND for USB driver and regulator | |
| 15 | DN | B | D- for USB | |
| 16 | DP | B | D+ for USB | |
| x | LDO_EN_ | I | Regulator enable | |
| 17 | TAVDD | P | VDD for USB driver and regulator (3.3V) | |
| 18 | VDDAL | P | Regulator output (1.8V) | |
| | VDD18 | P | CORE Power (1.8V) | |
| 19 | GPIO1 | B | General purpose I/O | |
| 20 | TEST | I | Test mode | |
| 21 | S_PWR_DN | O | Power down for sensor | |
| 22 | LED | O | LED output | |
| 23 | VDD3 | P | IO Power (3.3V) | |
| 24 | GND3 | P | IO Ground (also connect to substrate) | *1 |
| 25 | SDA | B | SDA for I2C interface (data) | |
| 26 | SCL | O | SCL for I2C interface (clock) | |
| 27 | S_PCK | B | Sensor pixel clock | |
| 28 | VDD3 | P | IO Power (3.3V) | |
| 29 | GND3 | P | IO Ground | |
| | GND18 | P | CORE Ground | |
| 30 | SEN_CLK | O | Sensor clock | |
| 31 | S_VSYNC | B | Sensor vsync | |
| 32 | S_HSYNC | B | Sensor hsync | |
| 33 | S_IMG0 | B | Sensor image data | |
| 34 | S_IMG1 | B | Sensor image data | |
| 35 | S_IMG2 | B | Sensor image data | |
| 36 | S_IMG3 | B | Sensor image data | |
| 37 | GND3 | P | IO Ground | |
| 38 | VDD3 | P | IO Power (3.3V) | |
| 39 | S_IMG4 | B | Sensor image data | |
| 40 | S_IMG5 | B | Sensor image data | |
| 41 | S_IMG6 | B | Sensor image data | |

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| 42 | S_IMG7 | B | Sensor image data | |
| 43 | S_IMG8 | B | Sensor image data | |
| 44 | VDD3 | P | IO Power (3.3V) | |
| 45 | XIN | I | OSC input (Rf=1M) (12MHz) | |
| 46 | XOUT | B | OSC output (Rf=1M) | |
| 47 | GND3 | P | IO Ground | |
| | GND18 | P | CORE Ground | |
| 48 | VDD18 | P | CORE Power (1.8V) | |
| | | | | |

# 6 Electrical Characteristics

## 6.1 DC Operating Condition

### 6.1.1 *Absolute maximum ratings:*

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| Vcc | Power Supply | -0.3 to 3.6 | V |
| Vin | Input Voltage | -0.3 to Vcc+0.3 | V |
| Vout | Output Voltage | -0.3 to Vcc+0.3 | V |
| Tstg | Storage Temperature | -55 to 150 | °C |

### 6.1.2 *Recommended operating conditions:*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Vcc | Power Supply | 3.0 | 3.3 | 3.6 | V |
| Vin | Input voltage | 0 | | Vcc | V |
| Topr | Operating Temperature | 0 | | 70 | °C |

### 6.1.3 *DC electrical characteristics:*

(Under Recommended Operating Conditions and Vcc=3.0 ~ 3.6V , Tj=0 to +115 °C )

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Vil | Input low voltage | CMOS | -0.3 | | 0.3Vcc | V |
| Vih | Input high voltage | CMOS | 0.7Vcc | | Vcc+0.3 | V |
| Vil | Input low voltage | TTL | -0.3 | | 0.8 | V |
| Vih | Input high voltage | TTL | 2.0 | | 5.3 | V |
| Iil | Input low current | no pull-up or pull-down | -1 | | 1 | uA |
| Iih | Input high current | no pull-up or pull-down | -1 | | 1 | uA |
| Ioz | Tri-state leakage current | | -1 | | 1 | uA |
| Vil | Schmitt input low voltage | CMOS | | 1.20 | | V |
| Vih | Schmitt input high voltage | CMOS | | 2.10 | | V |
| Vol | Output Low voltage | Iol=4mA | | | 0.4 | V |
| Voh | Output high voltage | Ioh=4mA | 2.4 | | | V |
| Cin | Input capacitance | | | 2.8 | | pF |
| Cout | Output capacitance | | 2.7 | | 4.9 | pF |
| Cbid | Bi-directional buffer Capacitance | | 2.7 | | 4.9 | pF |

## 6.2 AC Operating Condition

| Symbol | Description | Max operation Frequency | Notes |
|---|---|---|---|
| SEN_CLK | Sensor clock | 48MHz | |
| XIN | Crystal input clock | 12 MHz | |
| SCK | I2C clock frequency | 400KHz | |

# 7 Serial Control Interface

The SN9C128 supports I²C™-bus transfer protocol and is acting as a master device. It supports receiving and transmitting speed of 100 kHz and 400 kHz (Note: Downloading from EEPROM when power on requires speed of 400 kHz.)
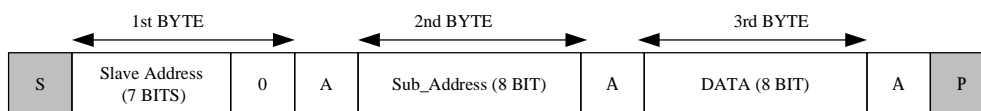
## 7.1 Serial Bus Overview

§ Only two wires SDA (serial data) and SCL (serial clock) are needed to carry information between the devices connected to the serial bus. Normally both SDA and SCL lines are open-collector structures and pulled high by external pull-up resistors.

§ Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).

§ Start and stop condition: A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition.

§ Valid data: The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read/write control bit is the LSB of the first byte.

§ Both the master and slave can transmit and receive data through the serial bus.

§ Acknowledge: The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transfer by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

## 7.2 Data Transfer Format

### 7.2.1 *Master device transmits data to slave device (write cycle)*

§ S : Start

§ A: Acknowledgement from slave device.

§ P : Stop

§ R/W: The LSB of 1st byte decides the current cycle is read or write. R/W=1 read; R/W=0 write.

§ Slave Address: serial slave device address.

§ Sub Address: The slave device control register address.

| | 1st BYTE | | | 2nd BYTE | | 3rd BYTE | | |
|---|---|---|---|---|---|---|---|---|
| S | Slave Address (7 BITS) | 0 | A | Sub_Address (8 BIT) | A | DATA (8 BIT) | A | P |

*Master transmits and Slave receives(write)*

During write cycle, the master device (SONIX'S PC CAMERA CONTROLLER) generates start condition and then places the 1st byte data which contains slave address (7 bits) and the Read/Write control bit onto SDA line. After slave device issues an acknowledgment, the master places the 2nd byte (sub-address data) data onto SDA line. And then followed the slave acknowledgment, the

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master places the 8 bits data on SDA line and transmits to slave device control register (address was assigned by 2$^{nd}$ byte). After slave issues an acknowledgment, the SUI110 can generate a stop condition to end this write cycle. This chip only supports 8 bytes multiple write function. *That is, master can write only 8 continuous address data into slave device.*

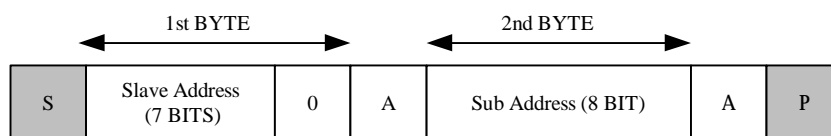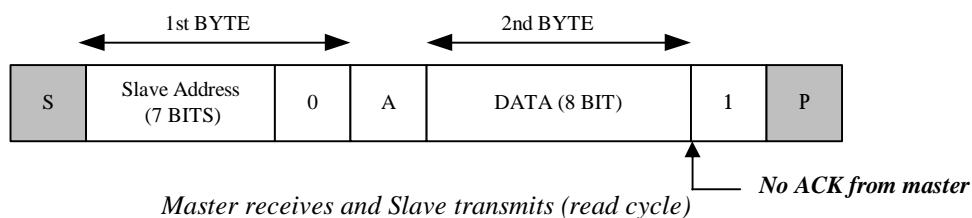7.2.2    *Slave device transmits data to master device (read cycle)*

The read cycle of the SUI110 has 2 phases, dummy write phase and read phase. *Note, this SUI110 supports single read only.* That is, one dummy write phase plus one read phase can get only one byte data from slave device internal register.

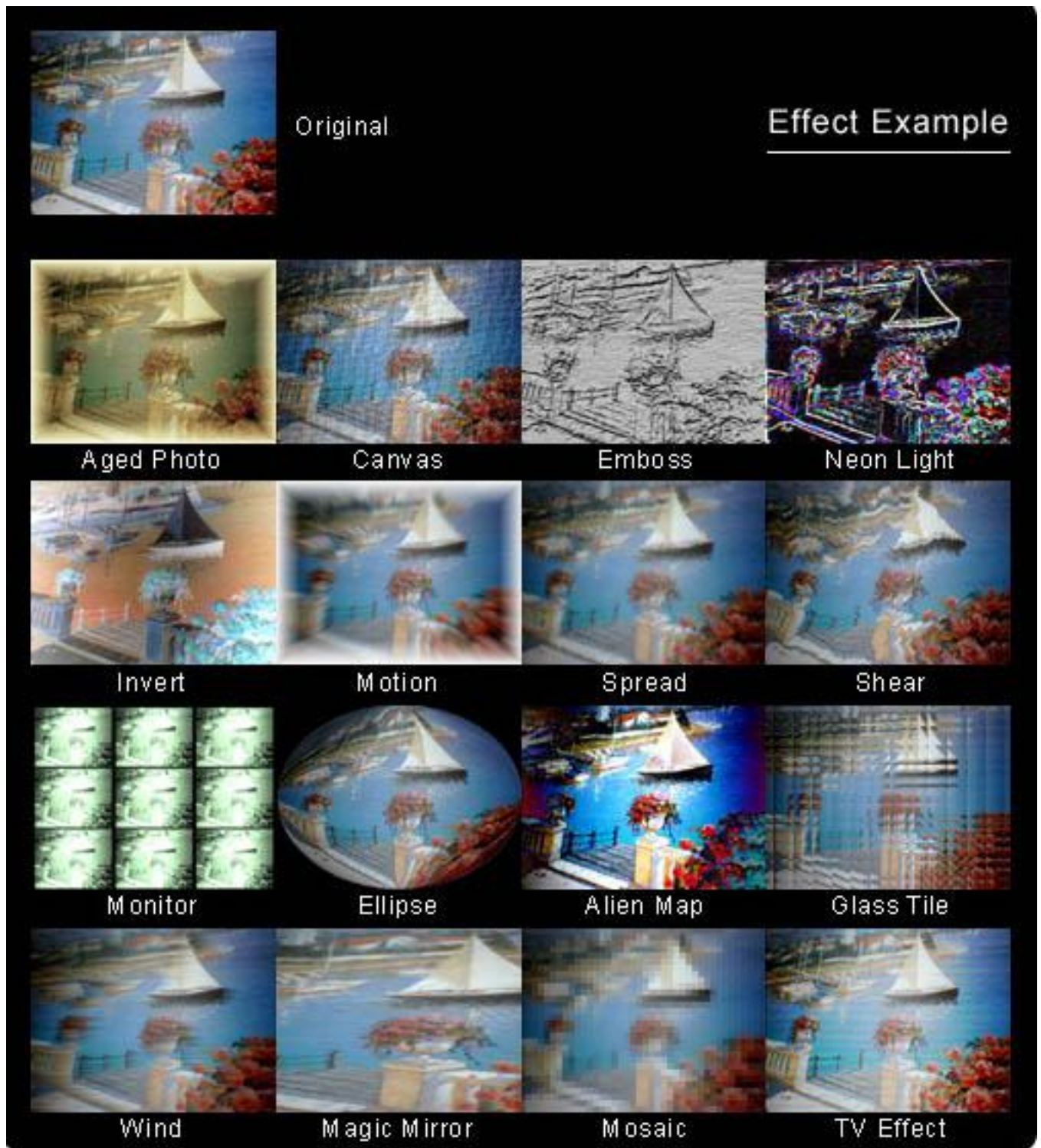§    The 1$^{st}$ phase (dummy write phase)
The dummy write phase is the same as the general serial write. The only difference is the write data is the address of the register. The Sub-Address is the register address inside the slave device
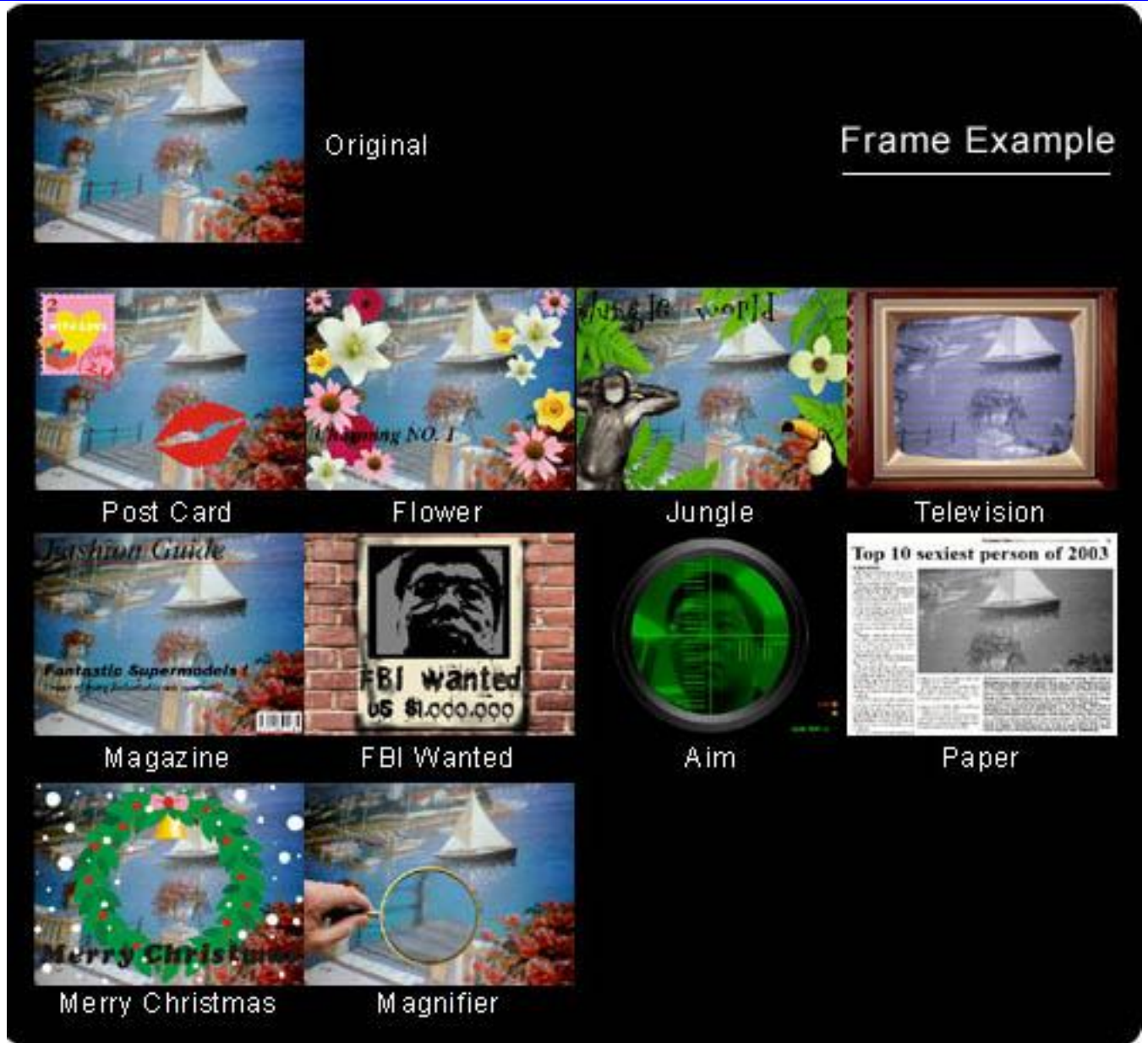
§    The 2$^{nd}$ phase (read phase)
he *SUI110* generates start condition and then place the 1$^{st}$ byte data, which contains slave address (7 bits) and a Read/Write control bit onto SDA line. After salve device issues an acknowledgment, the 8 bits data coming from slave device internal register will be placed onto the SDA line serially. The address of the 8 bit data was assigned by previous dummy write cycle. *Note, there is no acknowledgement issued by master device.*
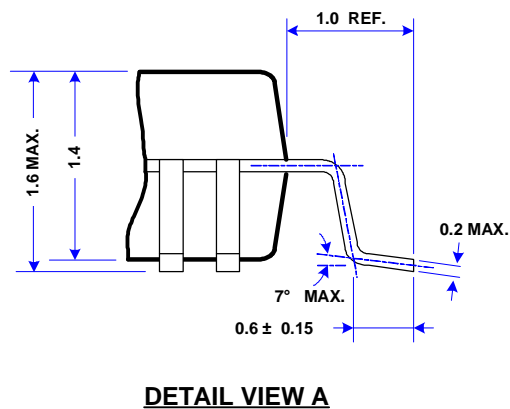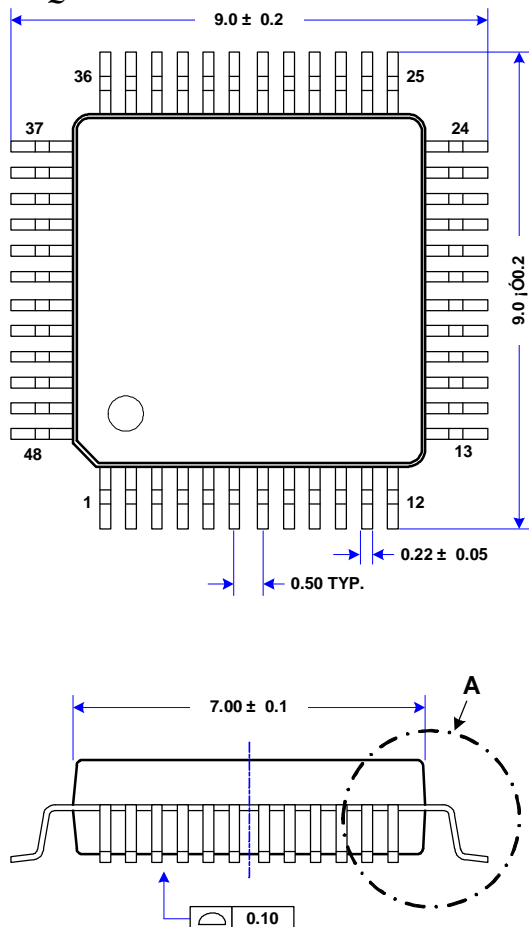
| | 1st BYTE | | | 2nd BYTE | | |
|---|---|---|---|---|---|---|
| S | Slave Address (7 BITS) | 0 | A | DATA (8 BIT) | 1 | P |

*No ACK from master*

*Master receives and Slave transmits (read cycle)*

| | 1st BYTE | | | 2nd BYTE | | |
|---|---|---|---|---|---|---|
| S | Slave Address (7 BITS) | 0 | A | Sub Address (8 BIT) | A | P |

*Master transmits and Slave receives (Dummy write cycle)*

# 8 Effect & Frame Example

# 9 Package Information

§   *48pin LQFP*

**9.0 ± 0.2**

36    25

37    24

**9.0 ¡Ó0.2**

48    13

1    12

**0.22 ± 0.05**

**0.50 TYP.**

**1.0  REF.**

**1.6 MAX.**    **1.4**

**0.2 MAX.**

**7°  MAX.**

**0.6 ± 0.15**

**DETAIL VIEW A**

**7.00 ± 0.1**    **A**

**0.10**

(All dimensions are in Millimeters)

# 10 Application Circuit



sensor interface