# SD Memory Card Specifications

***Simplified Version of :***

# Part 1
# PHYSICAL LAYER SPECIFICATION
# Version 1.01

**April 15 2001**


**SD Group**

**Matsushita Electric Industrial Co., Ltd. (MEI)**

**SanDisk Corporation**

**Toshiba Corporation**



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## Revision History

| Date | Version | Changes compared to previous issue |
|---|---|---|
| March 22th, 2000 | 1.0 | Base version |
| April 15th, 2001 | 1.01 | Detailed description of the revision history is given in the full version of Spec Ver 1.01. |
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# 1 General description

SD Memory Card (Secure Digital Memory Card) is a memory card that is specifically designed to meet the security, capacity, performance and environment requirements inherent in newly emerging audio and video consumer electronic devices. The SD Memory Card will include a copyright protection mechanism that complies with the security of the SDMI standard and will be faster and capable for higher Memory capacity. The SD Memory Card security system uses mutual authentication and a "new cipher algorithm" to protect from illegal usage of the card content. A none secured access to the user's own content is also available. The physical form factor, pin assignment and data transfer protocol are forward compatible with the MultiMediaCard with some additions.

The SD Memory Card communication is based on an advanced 9-pin interface (Clock, Command, 4xData and 3xPower lines) designed to operate in at maximum operating frequency of 25MHz of and low voltage range. The communication protocol is defined as a part of this specification. The SD Memory Card host interface supports regular MultiMediaCard operation as well. In other words, MultiMediaCard forward compatibility was kept. Actually the main difference between SD Memory Card and MultiMediaCard is the initialization process.

The SD Memory Card Specifications were divided to several documents. The SD Memory Card documentation structure is given in Figure 1.

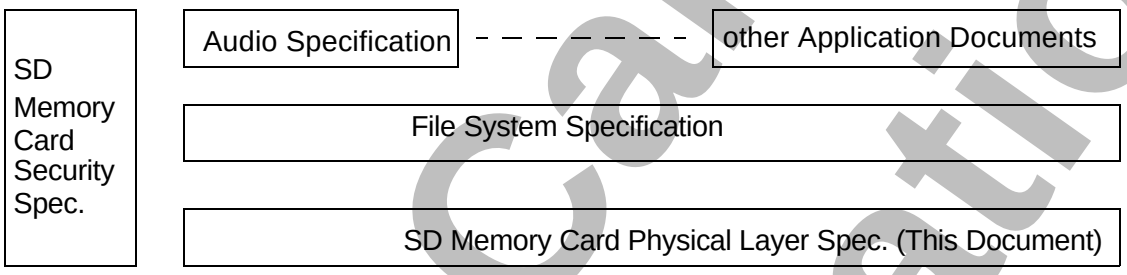


**Figure 1: SD Memory Card Documentation Structure**

- **SD Memory Card Audio Specification:**

This specification along with other application specifications describe the specification of certain application (in this case - Audio Application) and the requirements to implement it.

- **SD Memory Card File System Specification:**

Describes the specification of the file format structure of the data saved in the SD Memory Card (in protected and un-protected areas).

- **SD Memory Card Security Specification:**

Describes the copyright protection mechanism and the application specific commands that support it.

- **SD Memory Card Physical Layer Specification (this document):**

Describes the physical interface and the command protocol used by the SD Memory Card.

The purpose of the SD Memory Card Physical Layer specification is the definition of the SD Memory Card, its environment and handling.

The document is split up into several portions. Chapter 3 gives a general overview of the system

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concepts. The common SD Memory Card characteristics are described in Chapter 4. As this description defines an overall set of card properties, we recommend to use the product documentation in parallel. The card registers are described in Chapter 5.

Chapter 6 defines the electrical parameters of the SD Memory Card's hardware interface.

Chapter 8 describes the physical and mechanical properties of the SD Memory Cards and the minimal recommendations to the card slots or cartridges.

As used in this document, "shall" or "will" denotes a mandatory provision of the standard. "Should" denotes a provision that is recommended but not mandatory. "May" denotes a feature whose presence does not preclude compliance, that may or may not be present at the option of the implementor.

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# 2 System features

- **Targeted for portable and stationary applications**
- **Voltage range:**

  **SD Memory Card -**
  **Basic communication (CMD0, CMD15, CMD55, ACMD41): 2.0 - 3.6V**
  **Other commands and memory access: 2.7 - 3.6V**

  **SDLV Memory Card (low voltage) - Operating voltage range: 1.6 - 3.6V**
- **Designed for read-only and read/write cards.**
- **Variable clock rate 0 - 25 MHZ**
- **Up to 10MByte/sec Read/Write rate (using 4 parallel data lines).**
- **Maximum data rate with up to 10 cards**
- **Correction of memory field errors**
- **Card removal during read operation will never harm the content**
- **Forward compatibility to MultiMediaCard**
- **Copyrights Protection Mechanism - Complies with highest security of SDMI standard.**
- **Password Protection of cards (option)**
- **Write Protect feature using mechanical switch**
- **Built-in write protection features (permanent and temporary)**
- **Card Detection (Insertion/Removal)**
- **Application specific commands**
- **Comfortable erase mechanism**
- **Protocol attributes of the communication channel:**

| SD Memory Card Communication Channel |
|---|
| Six-wire communication channel (clock, command, 4 data lines) |
| Error-protected data transfer |
| Single or Multiple block oriented data transfer |

- **SD Memory Card thickness is defined as either 2.1mm (normal) and 1.4mm (Thin SD Memory Card) .**

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# 3 SD Memory Card System Concept

The SD Memory Card provides application designers with a low cost mass storage device, implemented as a removable card, that supports high security level for copyright protection and a compact, easy-to-implement interface.

SD Memory Cards can be grouped into several card classes which differ in the functions they provide (given by the subset of SD Memory Card system commands):

- Read/Write (RW) cards (Flash, One Time Programmable - OTP, Multiple Time Programmable - MTP). These cards are typically sold as blank (empty) media and are used for mass data storage, end user recording of video, audio or digital images.
- Read Only Memory (ROM) cards. These cards are manufactured with a fixed data content. They are typically used as a distribution media for software, audio, video etc.

In terms of operating supply voltage, two types of SD Memory Cards are defined:

- SD Memory Cards which supports initialization/identification process with a range of 2.0-3.6v and operating voltage within this range as defined in the CSD register.
- SDLV Memory Cards - Low Voltage SD Memory Cards, that can be operate in voltage range of 1.6-3.6V. The SDLV Memory Cards will be labeled differently then SD Memory Cards.

SD Memory Card system includes the SD Memory Card (or several cards) the bus and their Host / Application. The Host and Application specification is beyond the scope of this document. The following sections provides an overview of the card, bus topology and communication protocols of the SD Memory Card system. The copyright protection (security) system description is given in “SD Memory Card Security Specification” document.

## 3.1 Bus Topology

The SD Memory Card system defines two alternative communication protocols: SD and SPI. Applications can choose either one of modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. Therefore, applications which uses only one communication mode do not have to be aware of the other.

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### 3.1.1 SD bus

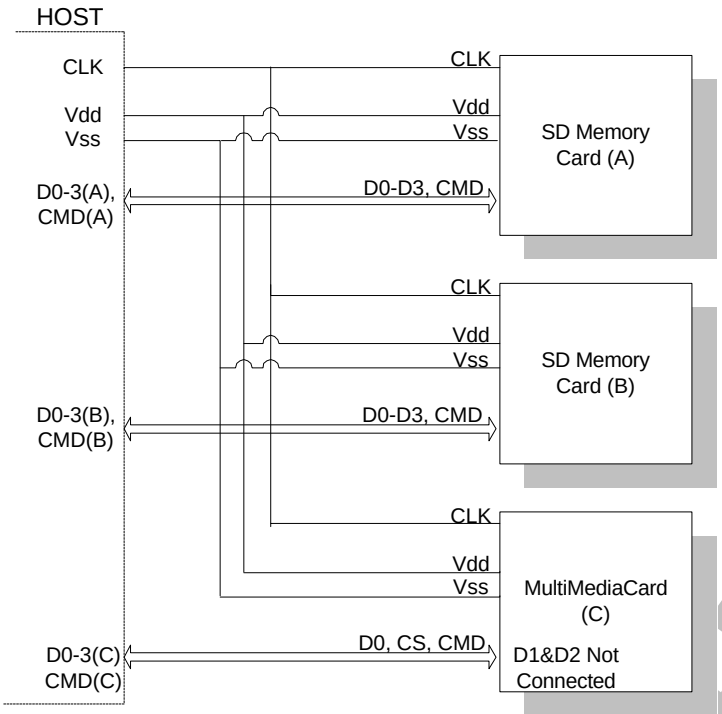


**Figure 2: SD Memory Card system bus Topology**

The SD bus includes the following signals:

| | |
|---|---|
| **CLK:** | Host to card clock signal |
| **CMD:** | Bidirectional Command/Response signal |
| **DAT0 - DAT3:** | 4 Bidirectional data signals. |
| **VDD, VSS1, VSS2:** | Power and ground signals. |

The SD Memory Card bus has a single master (application), multiple slaves (cards), synchronous star topology (refer to Figure 2). Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0 - DAT3) signals are dedicated to each card providing continues point to point connection to all the cards.

During initialization process commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent (received) to (from) each card individually. However, in order to simply the handling of the card stack, after the initialization process, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.

SD bus allows dynamic configuration of the number of data lines. After power up, by default, the SD Memory Card will use only DAT0 for data transfer. After initialization the host can change the bus width (number of active data lines). This feature allows easy trade off between HW cost and system performance. **Note that while DAT1-DAT3 are not in use, the related Host's DAT lines should be in tri-state (input mode).**

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### 3.1.2 SPI bus

The SPI compatible communication mode of the SD Memory Card is designed to communicate with a SPI channel, commonly found in various microcontrollers in the market. The interface is selected during the first reset command after power up and cannot be changed as long as the part is powered on.

The SPI standard defines the physical link only, and not the complete data transfer protocol. The SD Memory Card SPI implementation uses the same command set of the SD mode. From the application point of view, the advantage of the SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance, relatively to the SD mode which enables the wide bus option.

The SD Memory Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device the SD Memory Card SPI channel consists of the following four signals:

**CS:** Host to card Chip Select signal.

**CLK:** Host to card clock signal

**DataIn:** Host to card data signal.

**DataOut:** Card to host data signal.

Another SPI common characteristic are byte transfers, which is implemented in the card as well. All data tokens are multiples of bytes (8 bit) and always byte aligned to the CS signal.

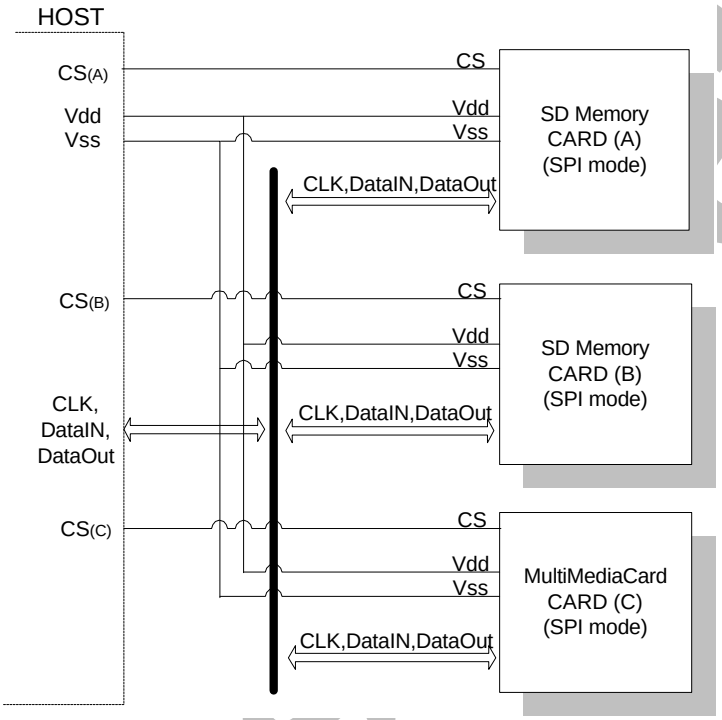


**Figure 3: SD Memory Card system (SPI mode) bus topology**

The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting

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(active low) the CS signal (see Figure 3).

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.

The SPI interface uses the 7 out of the SD 9 signals (DAT1 and DAT 2 are not used, DAT3 is the CS signal) of the SD bus.

## 3.2 Bus Protocol

### 3.2.1 SD bus

Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- **Command**: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- **Response**: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- **Data**: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

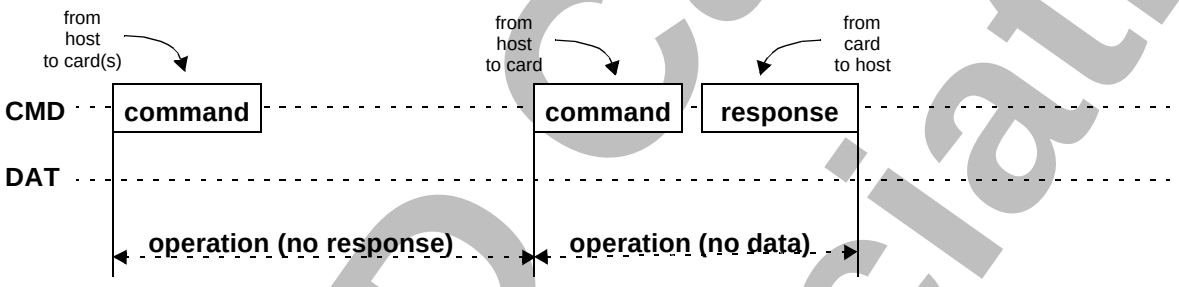


**Figure 4: "no response" and "no data" operations**

Card addressing is implemented using a session address, assigned to the card during the initialization phase. The structure of commands, responses and data blocks is described in Chapter 4. The basic transaction on the SD bus is the command/response transaction (refer to Figure 4). This type of bus transactions transfer their information directly within the command or response structure. In addition, some operations have a data token.

Data transfers to/from the SD Memory Card are done in blocks. Data blocks always succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer can be configured by the host to use single or multiple data lines.

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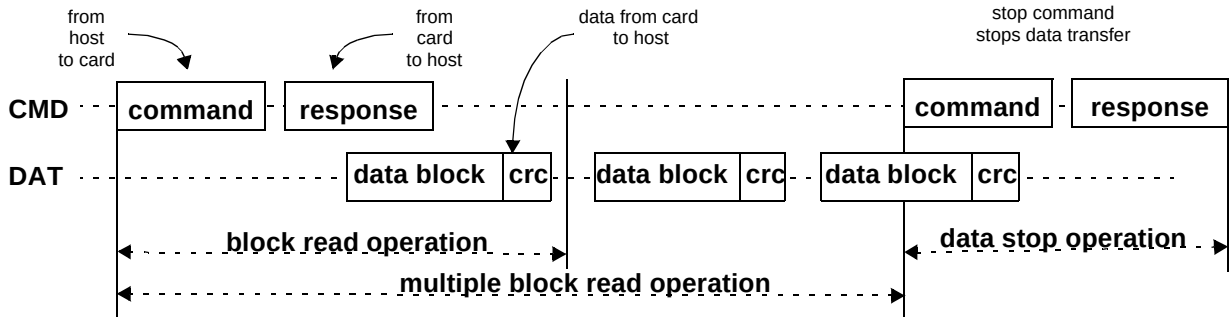


**Figure 5: (Multiple) Block read operation**

The block write operation uses a simple busy signaling of the write operation duration on the DAT0 data line (see Figure 6) regardless of the number of data lines used for transferring the data.

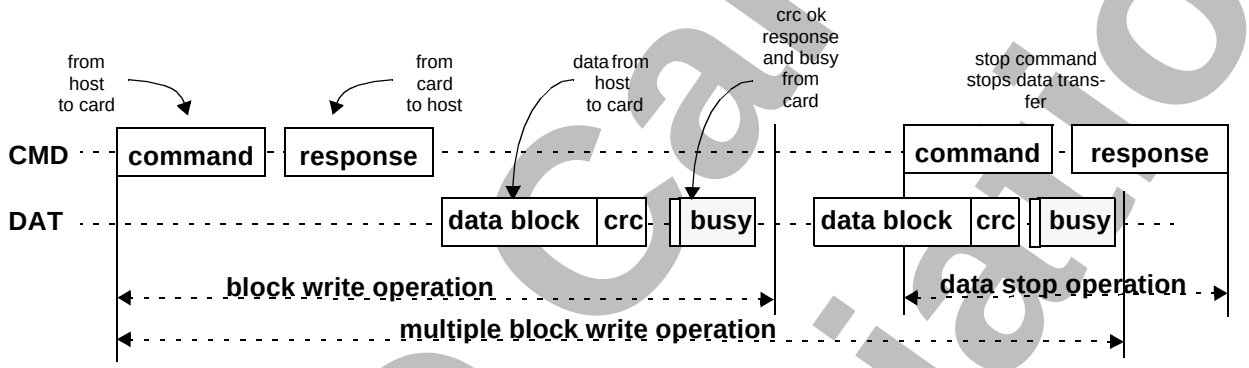


**Figure 6: (Multiple) Block write operation**

Command tokens have the following coding scheme:

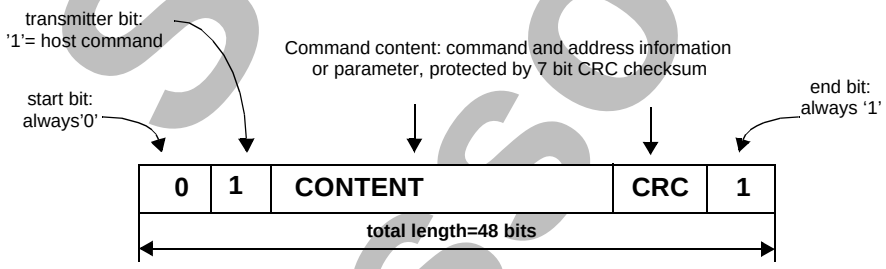


**Figure 7: Command token format**

Each command token is preceded by a start bit ('0') and succeeded by an end bit ('1'). The total length is 48 bits. Each token is protected by CRC bits so that transmission errors can be detected and the operation may be repeated.

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Response tokens have four coding schemes depending on their content. The token length is either 48 or 136 bits. The detailed commands and response definition is given in Chapter 4.7. The CRC protection algorithm for block data is a 16 bit CCITT polynomial. All used CRC types are described in Chapter 4.5.

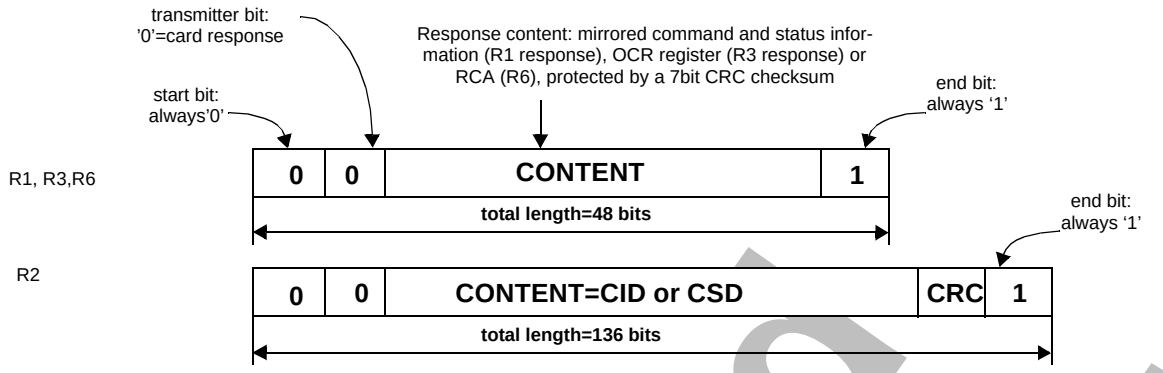


**Figure 8: Response token format**

In the CMD line the MSB bit is transmitted first the LSB bit is the last.

when the wide bus option is used, the data is transferred 4 bits at a time (refer to Figure 9). Start and end bits, as well as the CRC bits, are transmitted for every one of the DAT lines. CRC bits are calculated and checked for every DAT line individually. The CRC status response and Busy indication will be sent by the card to the host on DAT0 only (DAT1-DAT3 during that period are don't care).

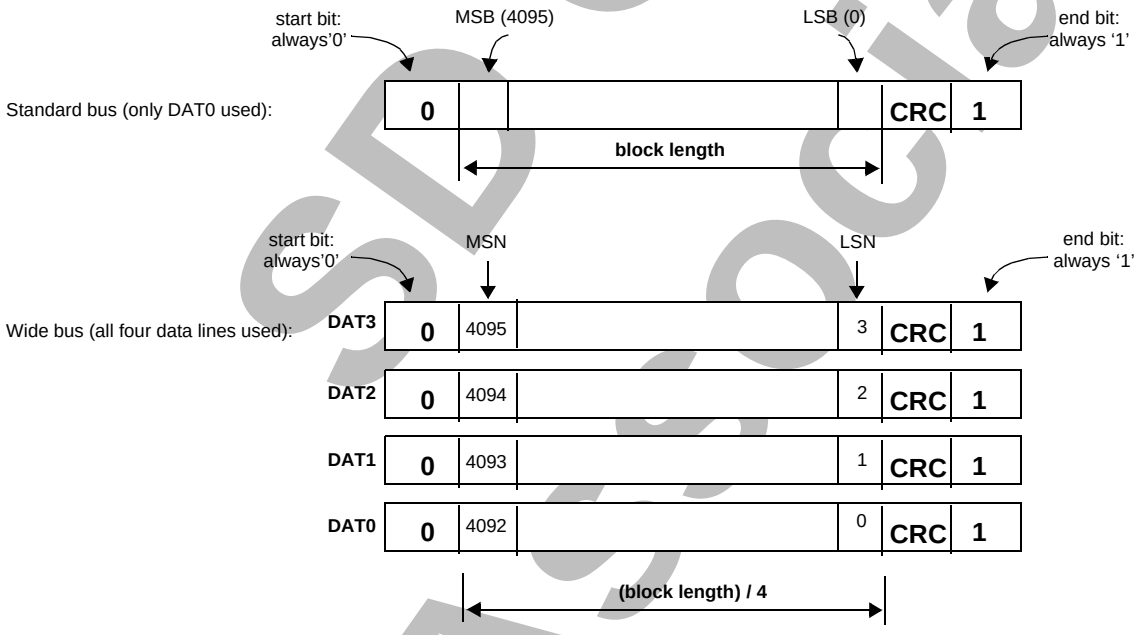


**Figure 9: Data packet format**

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### 3.2.2 SPI Bus

While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal (i.e. the length is a multiple of 8 clock cycles).

Similar to the SD protocol, the SPI messages consist of command, response and data-block tokens All communication between host and cards is controlled by the host (master). The host starts every bus transaction by asserting the CS signal low.

The response behavior in the SPI mode differs from the SD mode in the following three aspects:

- The selected card always responds to the command.
- Two new (8 & 16 bit) response structure is used
- When the card encounters a data retrieval problem, it will respond with an error response (which replaces the expected data block) rather than by a time-out as in the SD mode.

In addition to the command response, every data block sent to the card during write operations will be responded with a special data response token.

- **Data Read**

Single and multiple block read commands are supported in SPI mode. However, in order to comply with the SPI industry standard, only two (unidirectional) signal are used (refer to Chapter 10). Upon reception of a valid read command the card will respond with a response token followed by a data token of the length defined in a previous SET_BLOCKLEN (CMD16) command. A multiple block read operation is terminated, similar to the SD protocol, with the STOP_TRANSMISSION command.

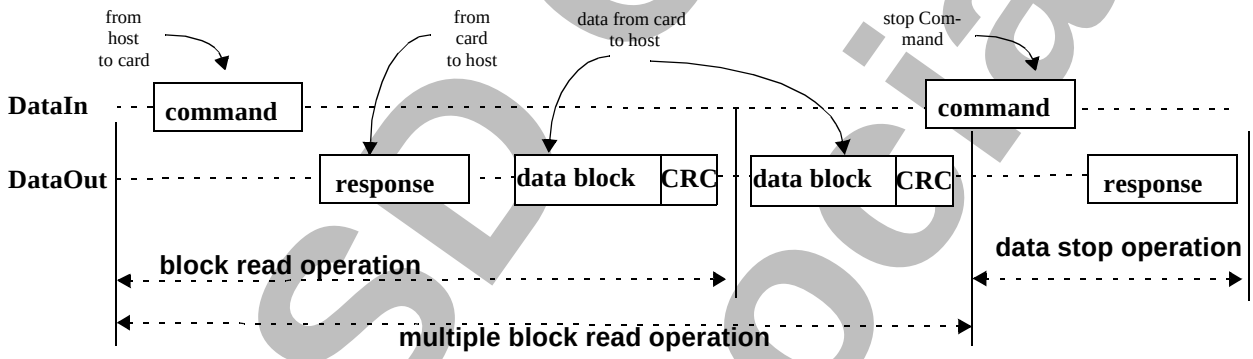


**Figure 10: Read operation**

A valid data block is suffixed with a 16 bit CRC generated by the standard CCITT polynomial $x^{16}+x^{12}+x^5+1$.

In case of a data retrieval error, the card will not transmit any data. Instead, a special data error token will be sent to the host. Figure 11 shows a data read operation which terminated with an error

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token rather than a data block.

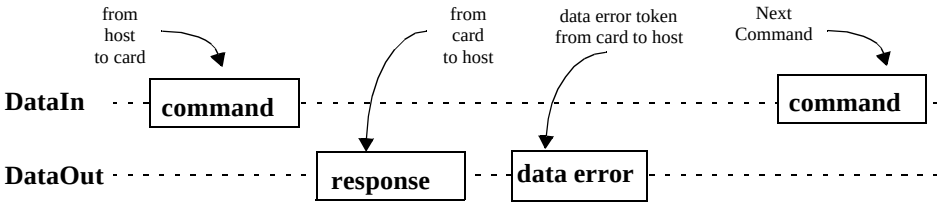


**Figure 11: Read operation - data error**

- **Data Write**

Single and multiple block write operations are supported in SPI mode. Upon reception of a valid write command, the card will respond with a response token and will wait for a data block to be sent from the host. CRC suffix, block length and start address restrictions are identical to the read operation (see Figure 12).

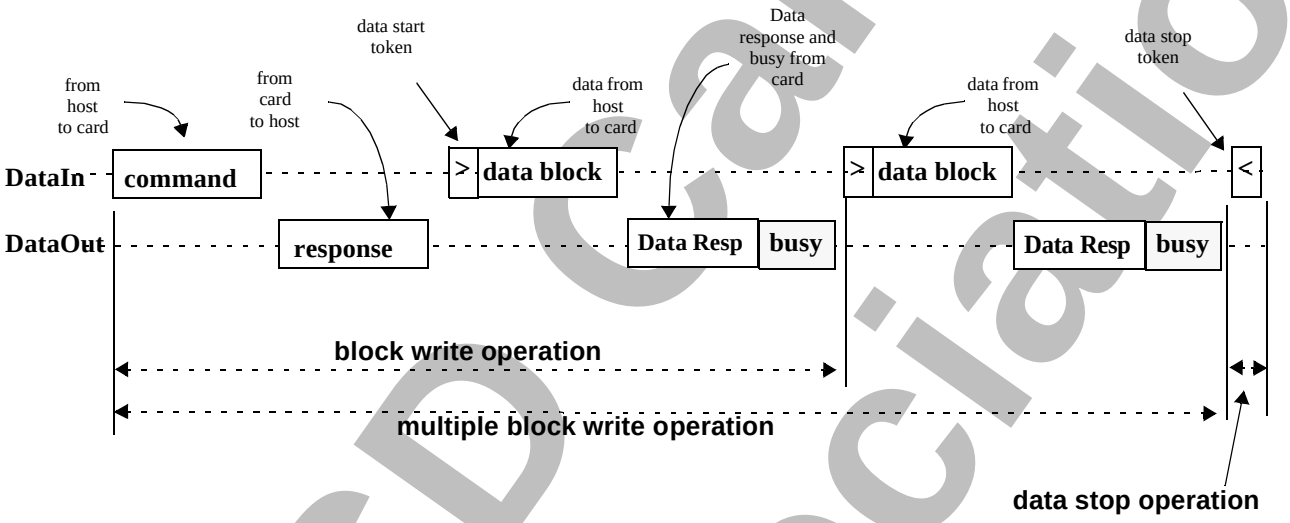


**Figure 12: Write operation**

After a data block has been received, the card will respond with a data-response token. If the data block has been received without errors, it will be programmed. As long as the card is busy programming, a continuous stream of busy tokens will be sent to the host (effectively holding the DataOut line low).

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## 3.3 SD Memory Card - Pins and Registers

The SD Memory Card has the form factor 24mm x 32mm x 2.1mm.

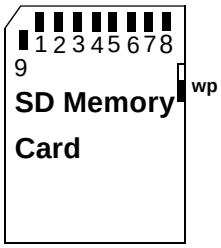


**Figure 13: SD Memory Card shape and interface (top view)**

Figure 13 describes the general idea of the shape and interface contacts of SD Memory Card. The detailed physical dimensions and mechanical description is given in chapter 9.

The following table defines the card contacts:

| Pin # | SD Mode | | | SPI Mode | | |
|---|---|---|---|---|---|---|
| | Name | Type[1] | Description | Name | Type | Description |
| 1 | CD/DAT3[2] | I/O/PP[3] | Card Detect / Data Line [Bit 3] | CS | I | Chip Select (neg true) |
| 2 | CMD | PP | Command/Response | DI | I | Data In |
| 3 | $V_{SS1}$ | S | Supply voltage ground | VSS | S | Supply voltage ground |
| 4 | $V_{DD}$ | S | Supply voltage | VDD | S | Supply voltage |
| 5 | CLK | I | Clock | SCLK | I | Clock |
| 6 | $V_{SS2}$ | S | Supply voltage ground | VSS2 | S | Supply voltage ground |
| 7 | DAT0 | I/O/PP | Data Line [Bit 0] | DO | O/PP | Data Out |
| 8 | DAT1 | I/O/PP | Data Line [Bit 1] | RSV | | |
| 9 | DAT2 | I/O/PP | Data Line [Bit 2] | RSV | | |

**Table 1: SD memory Card Pad Assignment**

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMediaCards.
3) After power up this line is input with 50KOhm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command

Each card has a set of information registers (see also Chapter 5 in the SD Memory Card Physical

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Layer Specification):

| Name | Width | Description |
|---|---|---|
| CID | 128 | Card identification number; card individual number for identification. **Mandatory**. |
| RCA[1] | 16 | Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**. |
| DSR | 16 | Driver Stage Register; to configure the card's output drivers. **Optional.** |
| CSD | 128 | Card Specific Data; information about the card operation conditions. **Mandatory** |
| SCR | 64 | SD Configuration Register; information about the SD Memory Card's Special Features capabilities. **Mandatory** |
| OCR | 32 | Operation condition register. **Mandatory.** |

**Table 2: SD Memory Card registers**

1) RCA register is not used (available) in SPI mode.

The host may reset the cards by switching the power supply off and on again. Each card shall have its own power-on detection circuitry which puts the card into a defined state after the power-on. No explicit reset signal is necessary. The cards can also be reset by sending the GO_IDLE (CMD0) command.

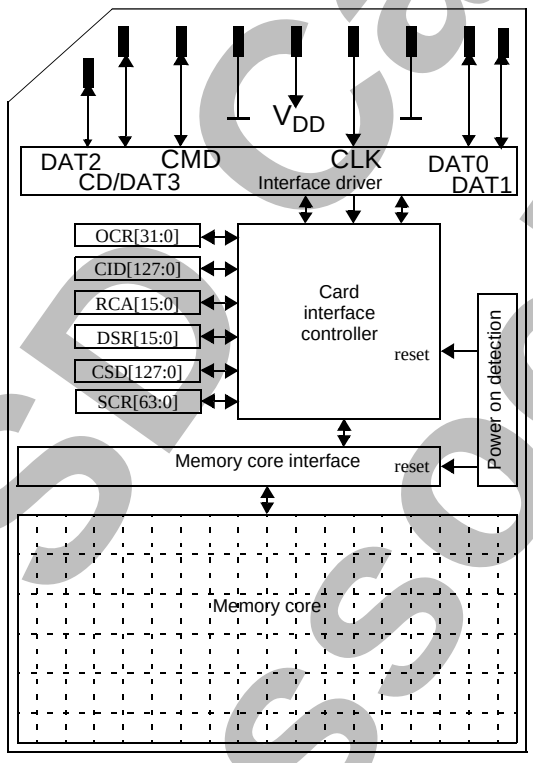


**Figure 14: SD Memory Card architecture**

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## 3.4 Compatibility to MultiMediaCard

The SD Memory Card protocol is designed to be a super-set of the MultiMediaCard protocol[1]. The main additions are the wide bus option and the content protection support (refer to Table 3 for details). It is very easy to design host systems, capable of supporting both types of cards. The intent is to enable application designers to make use of the exiting install base of MultiMediaCard, unless the application cannot do without either the fast data transfer rate (wide bus), or content security.

| | SD Memory Card | MultiMediaCard | Comments |
|---|---|---|---|
| Bus width | 1bit or 4 bits | 1 bit only | |
| System bus organization (multiple cards connection) | Star Topology | Bus Topology | |
| Initialization commands | CMD0<br>ACMD41<br>CMD2<br>CMD3 | CMD0<br>CMD1<br>CMD2<br>CMD3 | In MultiMediaCard CMD1 and CMD2 are sent concurrently from all cards using the OD drivers. In SD memory card each card is reset and identified indepen-dently and the RCA (CMD3) is assigned by the card. |
| Operation Commands | SEND_NUM_WR_BLOCK<br>SET_WR_BLK_COUNT | | two new command for improved write performance (ACMD23, ACMD22) are supported in SD. |
| Maximum Clock rate | 25MHz | 20MHz | |
| Copyright protection | supported (optional in Read Only type of cards) | not supported | |
| Write protect switch | supported | not supported | When MultiMediaCard is inserted into an SD Memory Card slot, it always perceived as non-write-protected card (window closed) |
| Feature of Pin #1 | Has a card internal pull-up resistor | Defined as "not connected" | In SD Memory Card pin #1 may be used for card detection. |
| CSD Structure | Different from MMC (mainly Sector Size/ Groups is different) | | |
| CID Structure | Different from MMC | | In SD the Manufacturing date field is bigger. Product ID field is smaller. |
| SPI R/W Multiple Block | Supported | Not supported | |
| Stream R/W mode | not supported | supported (optional) | SD Memory Card supports only single and multiple block read/ write operations. |

1. As defined in the MultiMediaCard system specification V2.11. Published by the MMCA technical commitee.

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| | SD Memory Card | MultiMediaCard | Comments |
|---|---|---|---|
| I/O Mode | not supported | supported (optional) | I/O (Interrupt) mode is not supported in SD Memory Card. |

**Table 3: Differences between SD Memory Card and MultiMediaCard Feature set**

The only difference (as opposed to addition) between the SD Memory Card and the MultiMediaCard is the bus topology and initialization protocol. While the MultiMediaCard stack is connected on the same bus and being identified using synchronous transmission of Open-drain outputs, each SD Memory Card has an independent point-to-point connection to the host, and the cards are identified serially, one at a time (refer to Table 4 for a command set comparison between SD Memory Card and MultiMediaCard. Detailed description of the SD Memory card protocol commands can be found in Chapter 4).

The initializing procedure in the SD protocol is defined to successfully identify either a MultiMediaCard or a SD Memory Card, which ever is currently connected on the bus. After card detection, the host executes the initializing procedure and ends up with an identified card of a known type.

Once the card is initialized the application can determine the card capabilities by querying the various configuration registers, and decide whether or not to use it.

The physical dimension of the SD Memory Card is thicker than MultiMediaCard (2.1mm vs. 1.4mm; refer to Chapter 9) but it is defined in such a way that a MultiMediaCard can be inserted into SD Memory Card socket. Note that because of the small differences between the mechanical definition of the pads layout of MultiMediaCard it is required that the SD Host will set its own DAT1-DAT3 lines to be in Input Mode (Tri-State) while they are not in use.

Three different card detect mechanisms are defined for the SD Memory Card (e.g. mechanical insertion which can be sensed using the WP switch, Electrical insertion which can be sensed using the pull-up resistor on DAT3 and periodical attempts to initialize the card). Since some of these methods may be not relevant (or behave differently) for the MultiMediaCard, it is recommended not to depend on the preemptive card detects methods only. The host should implement a polling mechanism or allow the operator to request card identification.

| Class | CMD | SD Memory Card | MultiMedia Card | Comment |
|---|---|---|---|---|
| Class 0 | CMD0 | CMD0 (Mandatory) | CMD0 | Same command. |
| | CMD1 | Reserved | CMD1 | In SD Memory Card ACMD41 is used instead of CMD1 |
| | CMD2 | CMD2 (Mandatory) | CMD2 | Similar command except buffer type used to transmit to response of the card. (SD Memory Card: push-pull, MultiMediaCard: open-drain) |
| | CMD3 | CMD3 (Mandatory) | CMD3 | In both protocols this command is used to assign a logical address to the card. While In MultiMediaCard the host assigned the address, in SD memory Card it is the responsibility of the card. |
| | CMD 4-10 | CMD4-10 (Mandatory) | CMD4-10 | Same commands. |

**Table 4: Commands comparison table.**

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| Class | CMD | SD Memory Card | MultiMedia Card | Comment |
|---|---|---|---|---|
| Class 1 | CMD11 | Reserved | CMD11 | SD Memory Card doesn't support stream access. |
| Class 0 | CMD12 -15 | CMD12-15 (Mandatory) | CMD12-15 | Same commands. |
| Class 2 | CMD16 -19 | CMD16-19 (Mandatory) | CMD16-19 | Same commands. |
| Class 3 | CMD20 | Reserved | CMD20 | SD Memory Card dose not support stream access. |
| | CMD21 -23 | Reserved | Reserved | All reserved. |
| Class 4 | CMD24 -27 | CMD24-27 (Mandatory for Writable card) | CMD24-27 | Same commands. |
| Class 6 | CMD28 -31 | CMD28-31 (Optional) | CMD28-31 | Same commands. |
| Class 5 | CMD32 -33 | CMD32-33 (Mandatory for Writable card) | CMD32-33 | Same commands. |
| | CMD34 -37 | Reserved | CMD34-37 | SD Memory Card dose not support TAG and Erase Group commands |
| | CMD38 | CMD38 (Mandatory for Writable card) | CMD38 | Same Command. |
| Class 9 | CMD39 -41 | Reserved | CMD39-41 | SD Memory Card dose not support I/O mode. |
| Class 7 | CMD42 -54 | CMD42-54 (Optional) | CMD42-54 | Same commands. |
| Class 8 | CMD55 -56 | CMD55-56 (Mandatory) | CMD55-56 | Same commands. |
| | CMD60 -63 | CMD60-63 (reserved for manufac-turer) | CMD60-63 (reserved for manu-facturer) | |

**Table 4: Commands comparison table.**

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# 4 SD Memory Card Functional Description

This chapter is omitted from the simplified version of the physical layer specification

# 5 Card Registers

This chapter is omitted from the simplified version of the physical layer specification

# 6 SD Memory Card Hardware Interface

This chapter is omitted from the simplified version of the physical layer specification

# 7 SPI Mode

This chapter is omitted from the simplified version of the physical layer specification

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# 8 SD Memory Card mechanical specification

This chapter describes the mechanical and electromechanical features of the SD Memory Card, and furthermore the minimal recommendations to the SD Memory Card connector. All technical drafts follow DIN ISO standard.

**The functions of the card package are:**

- protecting the chip
- easy handling for the end user
- reliable electrical interconnection
- reliable write protect/card detection capability
- bearing textual information and image
- appealing appearance

**The functions of the connector are:**

- attaching and fixing the card
- electrical interconnecting the card to the system board
- write protect/card detect indication
- optional: switch on/off power supply
- protection against card inverse insertion

## 8.1 Card package

Every card package shall have the characteristics described in the following sections.

### 8.1.1 External signal contacts (ESC)

| Number of ESC | 9 |
|---|---|
| distance from front edge | 1.2 mm |
| ESC grid | 2.5mm |
| contact dimensions | 1.7mm x 4.0mm |
| electrical resistance | 30 mΩ (worst case: 100 mΩ) |
| micro interrupts | < 0.1 µs |

**Table 5: SD Memory Card Package - External Signal Contacts**

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### 8.1.2 Design and format

| | |
|---|---|
| Dimensions SD Memory Card package | 24mm x 32mm; (min. 23.9mm x 31.9mm; max.24.1mm x 32.1mm)<br>other dimensions Figure 15<br>testing according to MIL STD 883, Meth 2016 |
| thickness | 'Inter Connect Area': 2.1mm +/- 0.15mm or 1.4mm+/-0.15mm for Thin SD Card.<br>'Substrate Area': Max 2.25mm or Max 1.55 for Thin SD Card - see Figure 17. |
| label or printable area | In 'Substrate Area' only - see Figure 17. |
| surface | plain (except contact area) |
| edges | smooth edges, see Figure 16, Figure 17 |
| inverse insertion | protection on left corner (top view) see Figure 19 |
| position of ESC contacts | along middle of shorter edge |

**Table 6: SD Memory Card Package - Dimensions**

### 8.1.3 Reliability and durability

| | |
|---|---|
| temperature | operation: -25°C / 85°C (Target spec)<br>storage: -40°C (168h) / 85°C (500h)<br>junction temperature: max. 95°C |
| moisture and corrosion | operation: 25°C / 95% rel. humidity<br>storage: 40°C / 93% rel. hum./500h<br>salt water spray:<br>3% NaCl/35C; 24h acc. MIL STD Method 1009 |
| durability | 10.000 mating cycles; Test procedure: tbd. |
| bending (note 1) | 10N |
| torque (note 1) | 0.15N.m or +/-2.5 deg . |
| drop test | 1.5m free fall |
| UV light exposure | UV: 254nm, 15Ws/cm² according to ISO 7816-1 |
| visual inspection<br>shape and form (note 1) | no warpage; no mold skin; complete form; no cavities<br>surface smoothness <= -0.1 mm/cm² within contour; no cracks; no pollution (fat, oil dust, etc.) |
| Minimum moving force of WP switch | 40gf (Ensures that the WP switch will not slide while it is inserted to the connector). |
| WP Switch cycles | minimum 1000 Cycles (@ Slide force 0.4N to 5N) |

Note (1): The SDA's recommended test methods for Torque, bending and Warpage are defined in seperate Application Notes document.

**Table 7: Reliability and Durability**

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### 8.1.4 Electrical Static Discharge (ESD) Requirements

ESD testing should be conducted according to IEC61000-4-2

Required ESD parameters are:

(1) Human body model +- 4 KV 100 pf / 1.5 Kohm

(2) Machine model +- 0.25 KV 200 pf / 0 ohm

**Contact Pads:**

+/- 4kV, Human body model according to IEC61000-4-2

**Non Contact Pads area:**

+/-8kV (coupling plane discharge)
+/-15kV (air discharge)
Human body model according to IEC61000-4-2

The SDA's recommended test methods for the non-contact/air discharge tests are given in a separate Application Note document.

### 8.1.5 Quality assurance

The product traceability shall be ensured by an individual card identification number.

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## 8.2 Mechanical form factor

The following 3 technical drawings define the card package of SD Memory Card with 2.1+/-0.15mm card thickness (the Thin SD Memory Card drawings are given in Chapter 8.4 ).

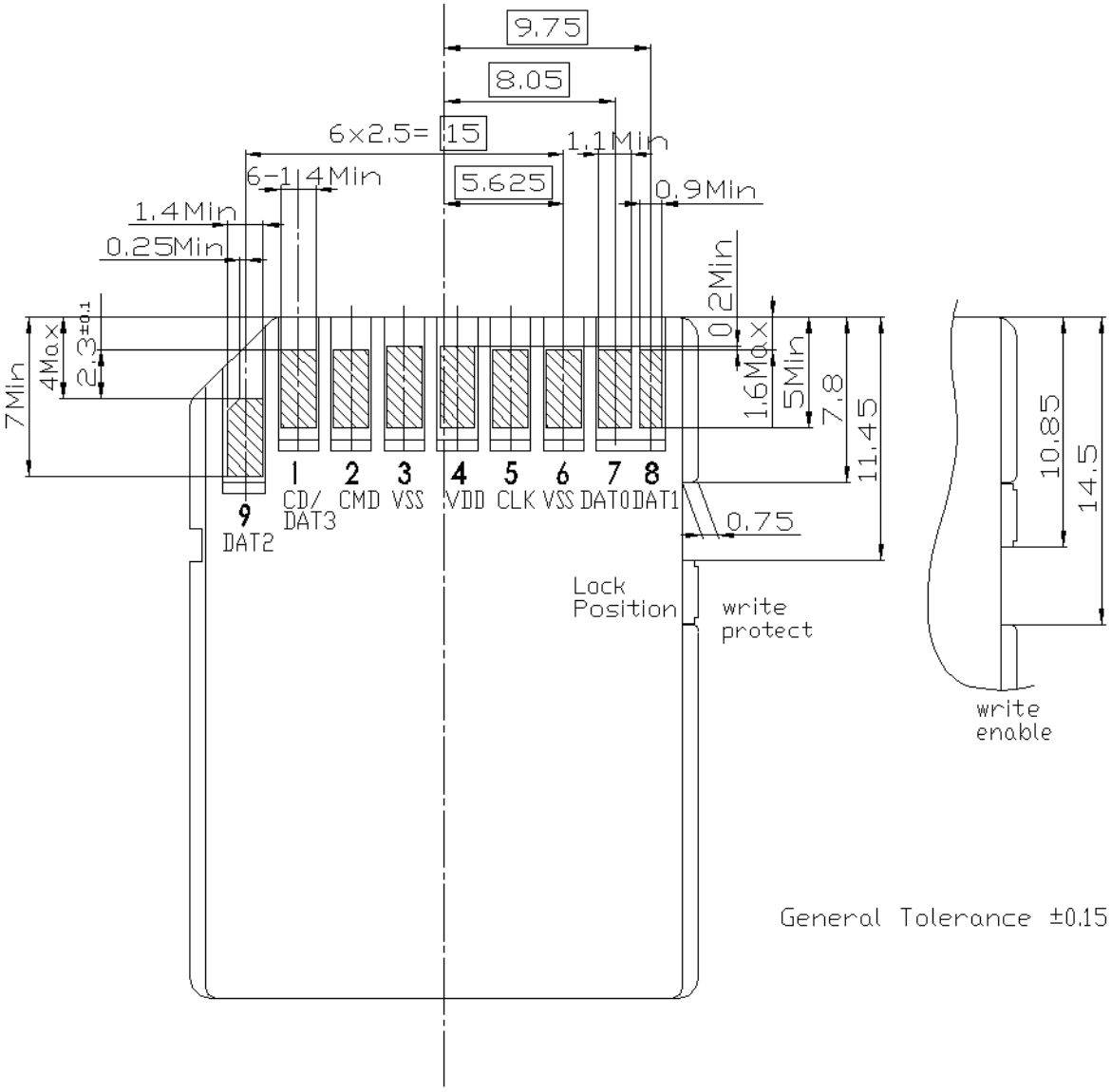


**Figure 15: SD Memory Card - Mechanical Description (1 out of 3)**

Notes for all the mechanical descriptions of the SD Memory Card (including Thin SD Memory Card):

1) The numbers enclosed by a square means that it is the distance between base lines. Those values are for information only (the given general tolerances are not related to them).

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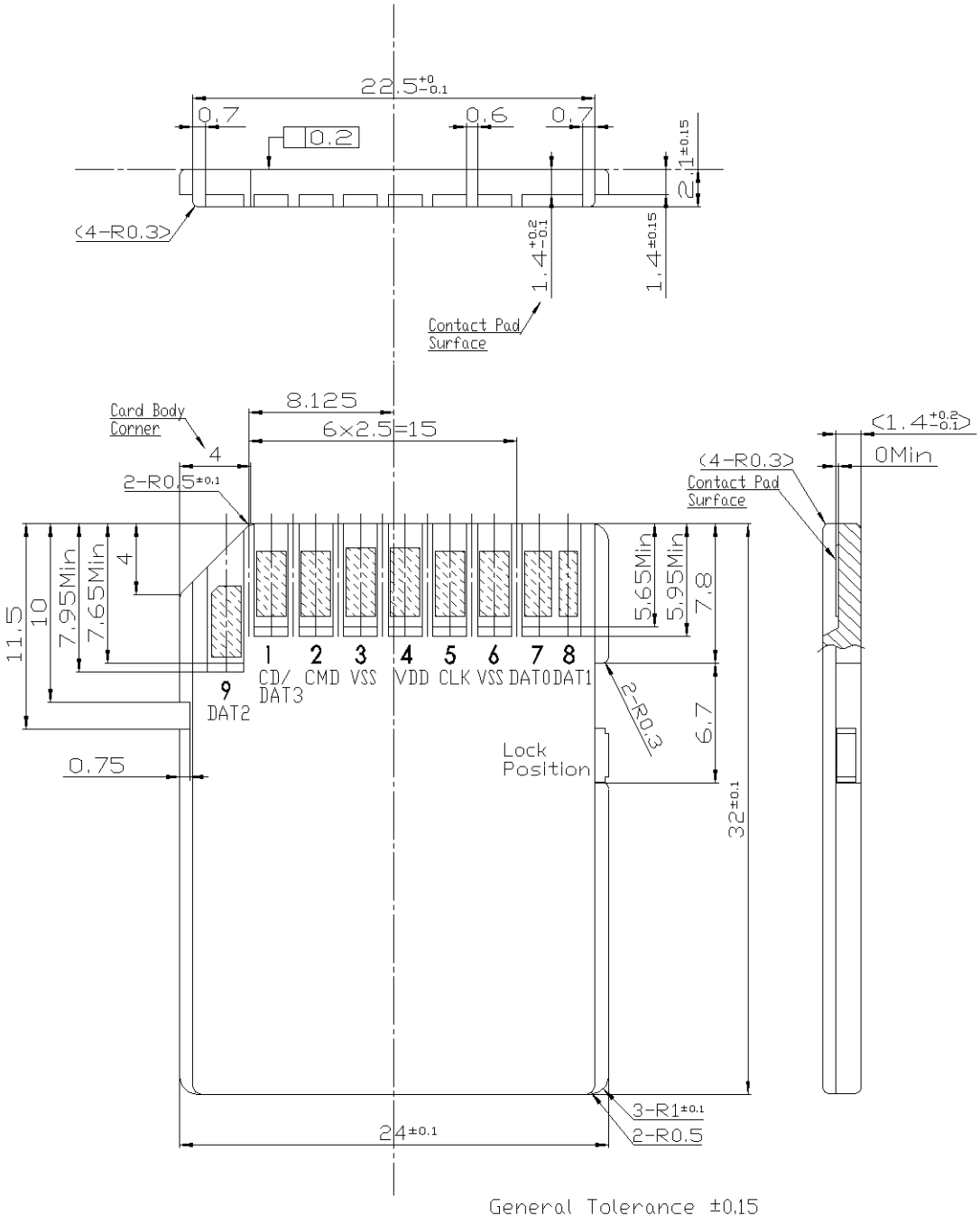


**Figure 16: SD Memory Card - Mechanical Description (2 out of 3)**

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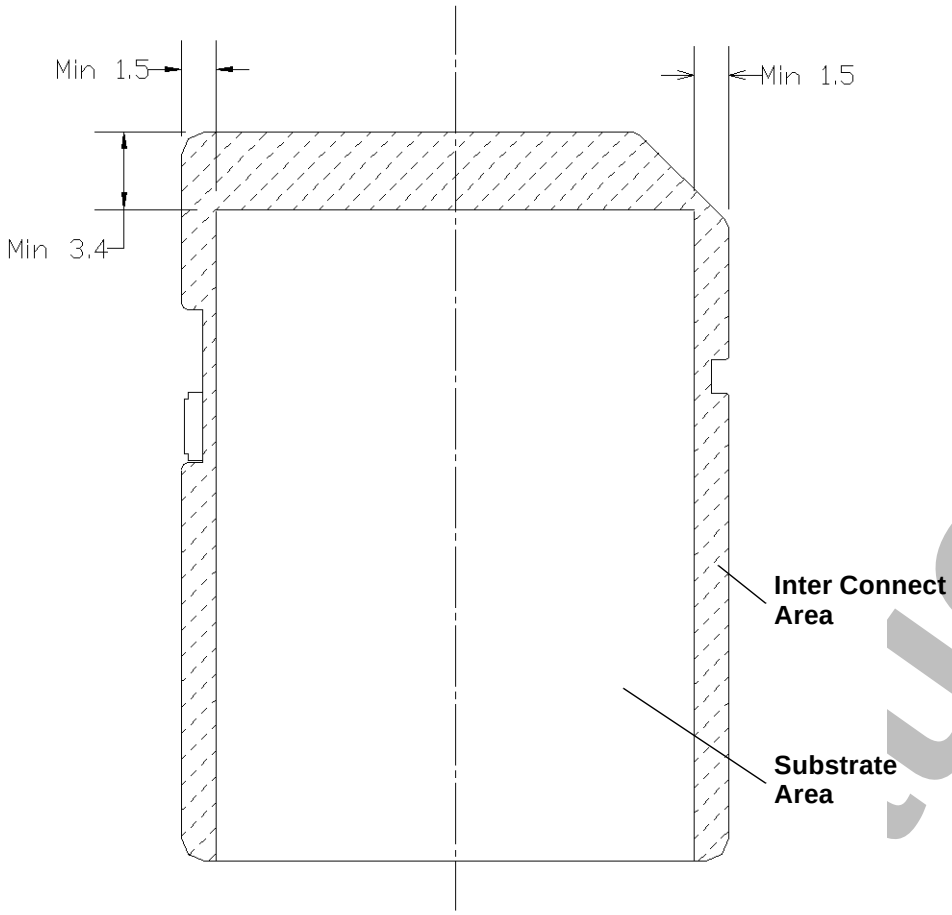


Note: Refer to Table 6 for the definition of 'substrate' and 'Inter Connect' areas.

**Figure 17: SD Memory Card - Mechanical Description (3 out of 3)**

Figure 18 describes the Write Protect switch position at all various cases and card types.

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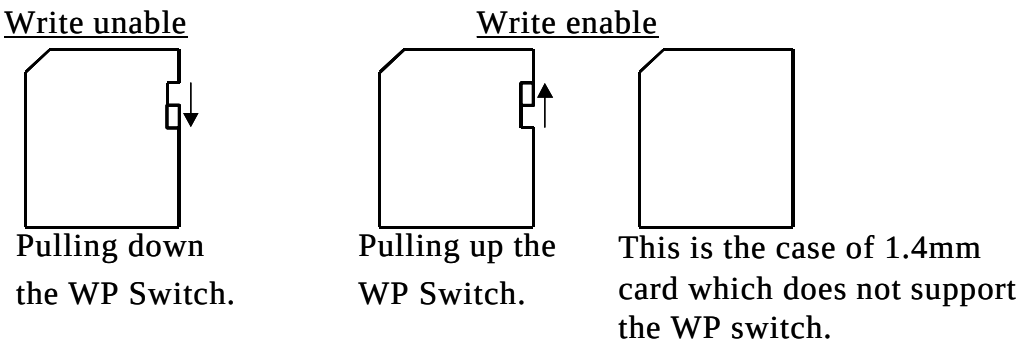
- R/W card(WP switch is movable)




- ROM card(WP area is fixed)

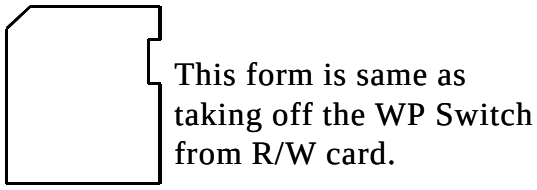



**Figure 18: WP Switch definition for all cases and card types**

## 8.3 System: card and connector

The description of the connector is out of the scope of this document. However, minimal recommendations to the connector comprise the ability to guarantee Write Protect and Card Detection, hot insertion and removal of the card, and to prevent inverse insertion.

### 8.3.1 Card hot insertion

To guarantee a reliable initialization during hot insertion, some measures shall be taken on the host side. For instance, a special hot-insertion capable card connector may be used to guarantee the proper sequence of card pin connection.

The card contacts are contacted in three steps:

1) Ground Vss (pin 3) and supply voltage Vdd (pin 4).
2) CLK, CMD, DAT0, DAT1, DAT2 and Vss (pin 6).
3) CD / DAT3 (pin 1).

Pins 3 and 4 should make first contact when inserting, and release last when extracting.

As another method, a switch could ensure that the power is switched on only after all card pads are contacted. Of course, any other similar mechanism is allowed.

### 8.3.2 Inverse insertion

Inverse insertion is prevented by the reclining corners of SD Memory Card and connector.

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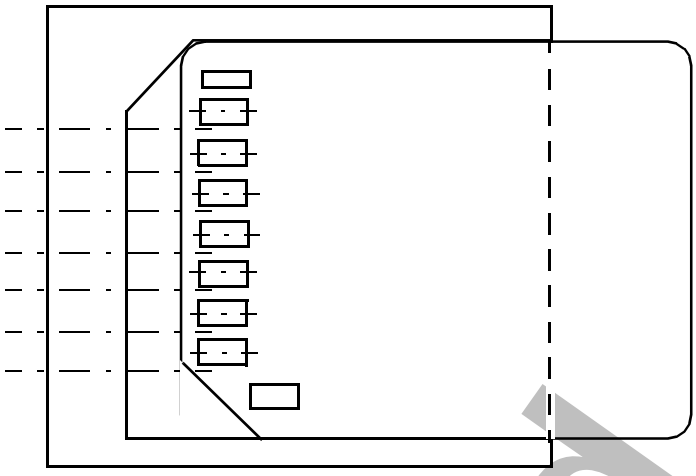

**Figure 19: Inverse insertion**

### 8.3.3 Card Orientation

For the benefit of unified terminology when discussing the three dimensional orientation of a card (e.g. for connector definition), the non contact-pads side (the side with the card label) is defined as the TOP side of the card and the contact-pads side of the card is defined as the BOTTOM side of the card.

## 8.4 Thin (1.4mm) SD Memory Card

SD Memory cards with mechanical dimensions that will be suitable for extra small applications will be available.

The "Thin SD Memory card" has very similar form factor as the SD Memory Card that is given in Chapter 8.2 above except it thickness. The thickness of the "Thin SD Memory Card" is 1.4mm+/-0.15mm.

Figure 20, 21 and 17 are the mechanical drawings of Thin SD Memory Card.

Note that even though the WP switch appears in the given diagram it was defined as an optional for Thin SD Memory Card.

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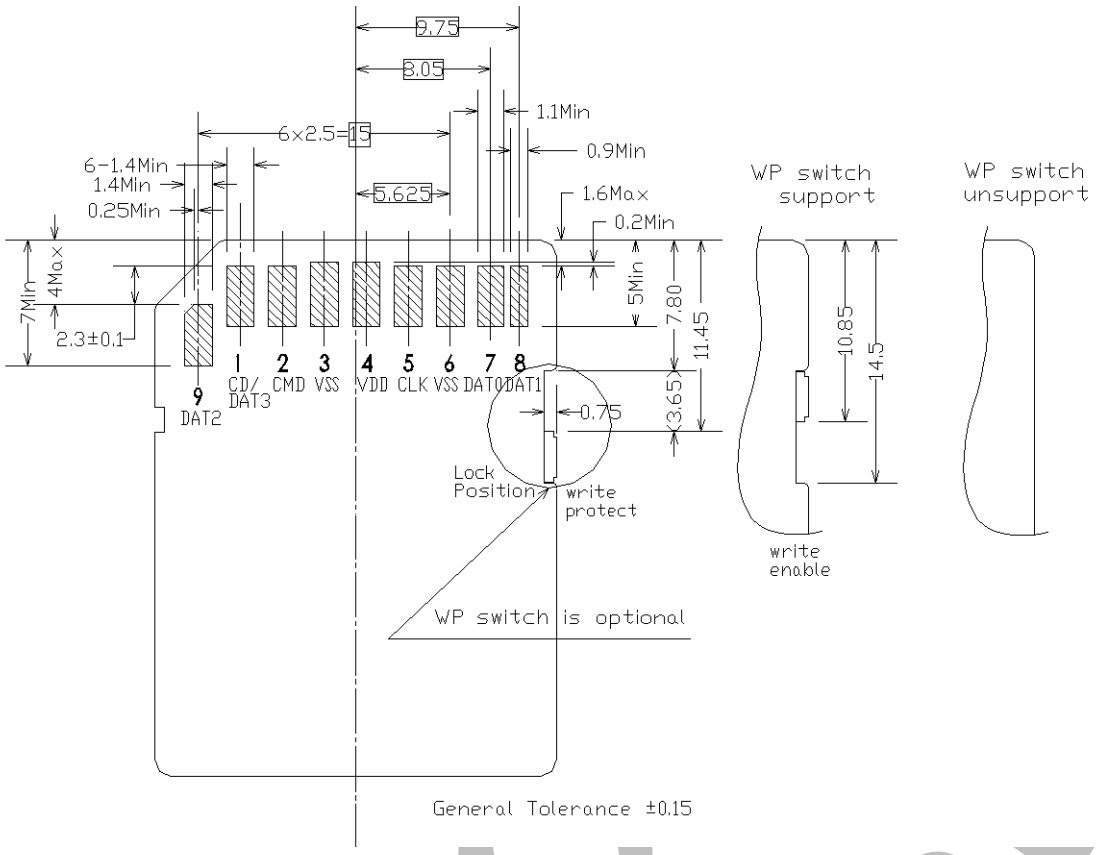


**Figure 20: Mechanical Drawing of Thin SD Memory Card**

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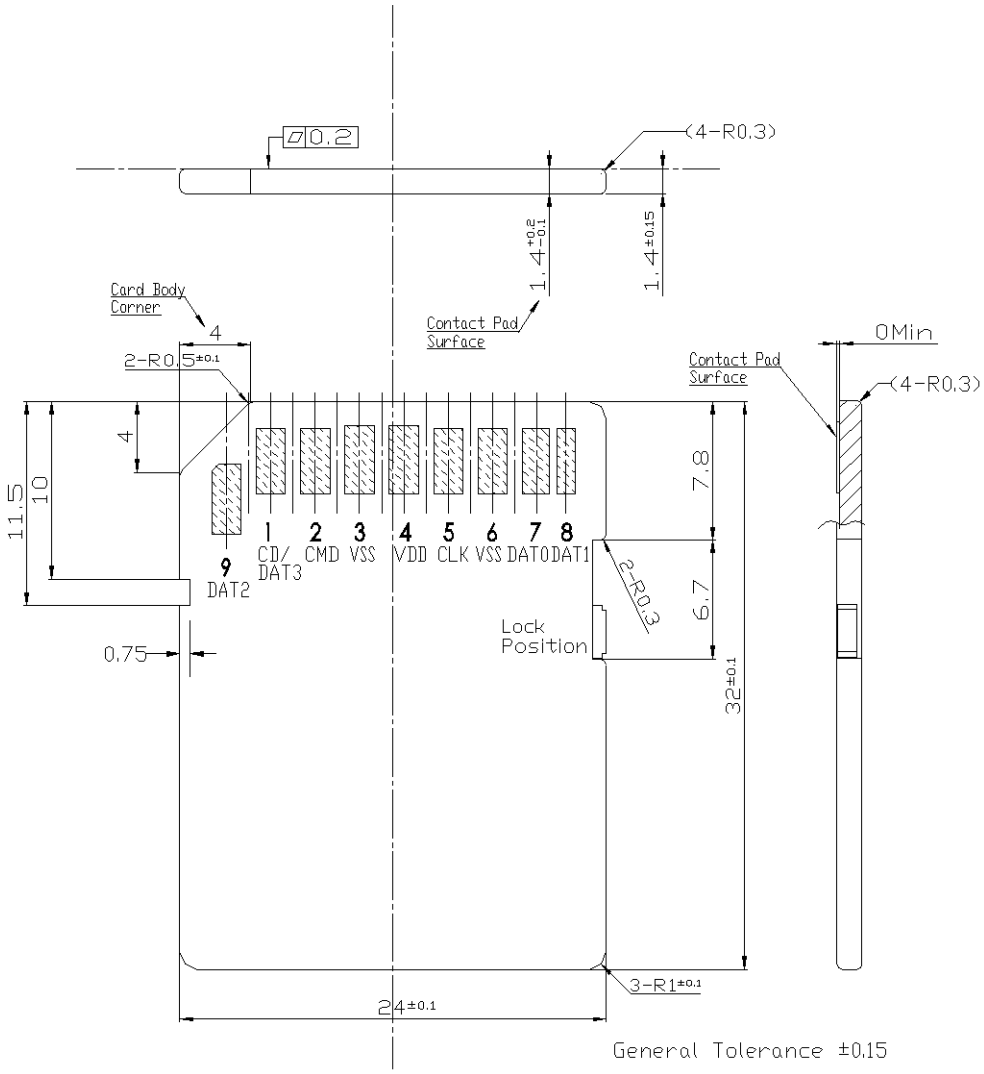


**Figure 21: Mechanical Drawing of Thin SD Memory Card**

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# 9 Appendix

This chapter is omitted from the simplified version of the physical layer specification

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# 10 Abbreviations and terms

| | |
|---|---|
| block | a number of bytes, basic data transfer unit |
| broadcast | a command sent to all cards on the SD bus |
| CID | Card IDentification number register |
| CLK | clock signal |
| CMD | command line or SD bus command (if extended CMDXX) |
| CRC | Cyclic Redundancy Check |
| CSD | Card Specific Data register |
| DAT | data line |
| DSR | Driver Stage Register |
| ECC | Error Correction Code |
| Flash | a type of multiple time programmable non volatile memory |
| group | a number of sectors, composite erase and write protect unit |
| LOW, HIGH | binary interface states with defined assignment to a voltage level |
| NSAC | defines the worst case for the clock rate dependent factor of the data access time |
| MSB, LSB | the Most Significant Bit or Least Significant Bit |
| MTP | Multiple Time Programmable memory |
| OCR | Operation Conditions Register |
| OTP | One Time Programmable memory |
| payload | net data |
| push-pull | a logical interface operation mode, a complementary pair of transistors is used to push the interface level to HIGH or LOW |
| RCA | Relative Card Address register |
| ROM | Read Only Memory |
| sector | a number of blocks, basic erase unit |
| stuff bit | filling bits to ensure fixed length frames for commands and responses |
| SPI | Serial Peripheral Interface |
| TAAC | defines the time dependent factor of the data access time |
| tag | marker used to select groups or sector to erase |
| TBD | To Be Determined (in the future) |
| three-state driver | a driver stage which has three output driver states: HIGH, LOW and high impedance (which means that the interface does not have any influence on the interface level) |
| token | code word representing a command |
| $V_{DD}$ | + power supply |
| $V_{SS}$ | power supply ground |

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