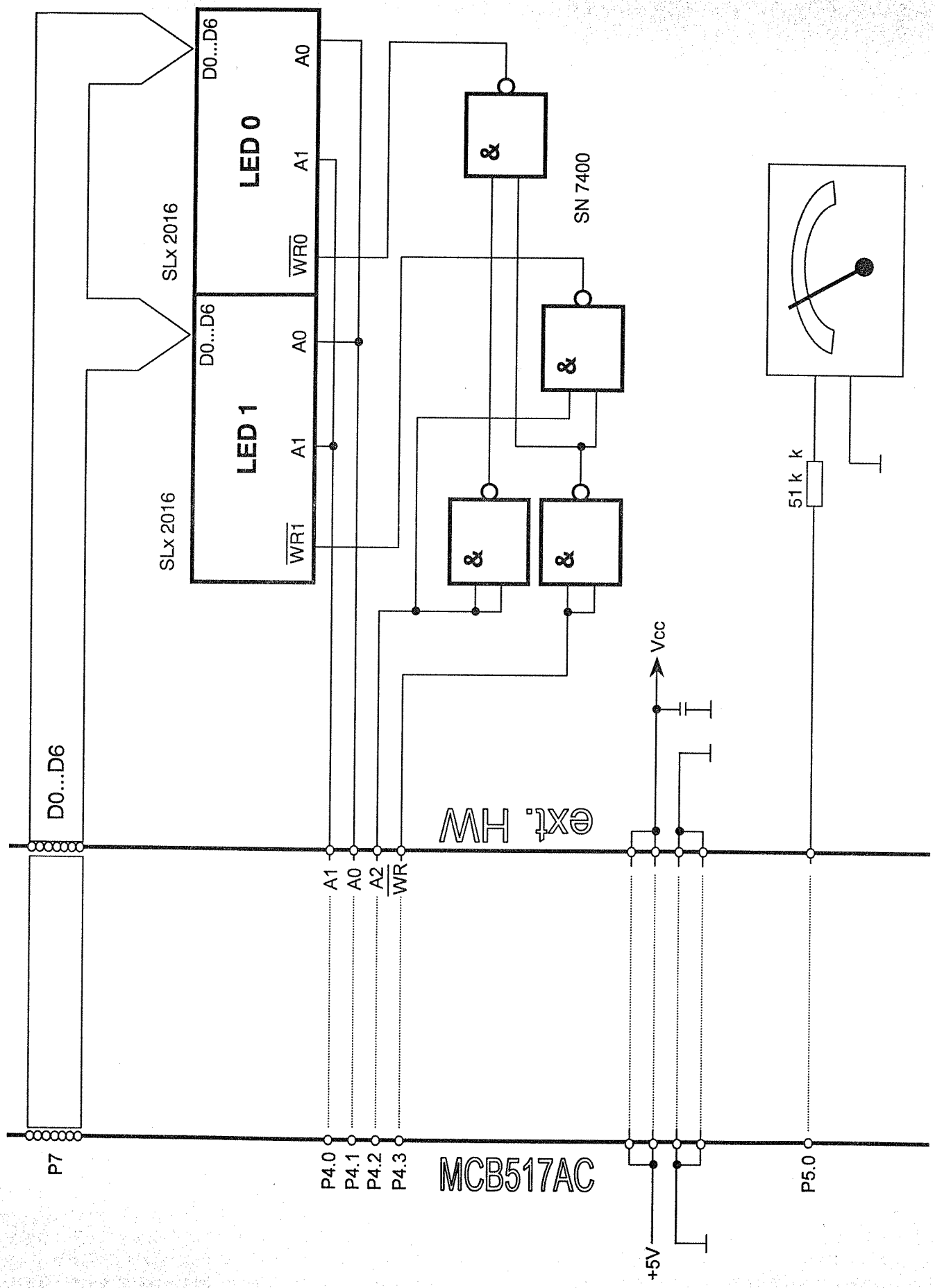
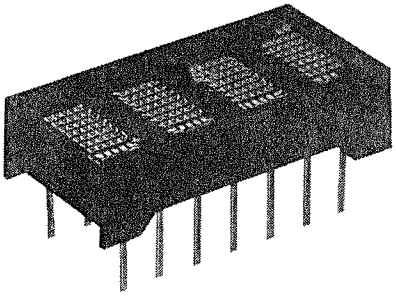

LED 0
LED 1
D0...D6
A0
A1
WR0
WR1
SLx 2016
SLx 2016
SN 7400
&
51 k
Vcc
+5V
ext. HW
D0...D6
A1
A0
A2
WR
P7
P4.0
P4.1
P4.2
P4.3
P5.0
MCB517AC

Infineon technologies

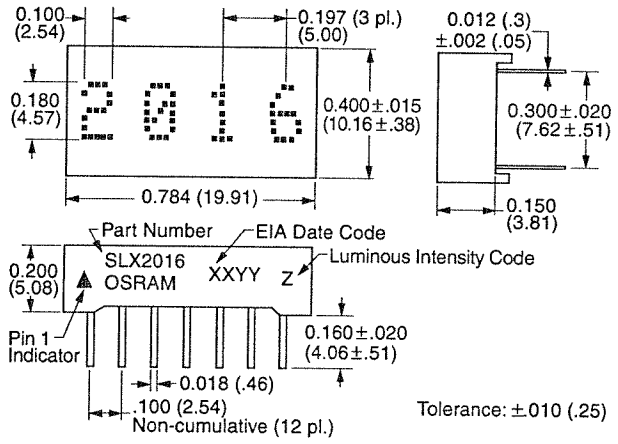
OSRAM

RED SLR2016
HIGH EFFICIENCY RED SLO2016
GREEN SLG2016
YELLOW SLY2016

X/Y Stackable 0.180" 4-Digit 5 x 7 Dot Matrix Alphanumeric Intelligent Display® Devices with Memory/Decoder/Driver



Dimensions in inches (mm)



FEATURES

- **Very Close Multi-line Spacing, 0.4" Centers**
- **0.180" 5 x 7 Dot Matrix Characters**
- **128 Special ASCII Characters for English, German, Italian, Swedish, Danish, and Norwegian Languages**
- **Wide Viewing Angle: X axis 50° Maximum, Y Axis ±75° Maximum**
- **Fast Access Time, 110 ns at 25°C**
- **Full Size Display for Stationary Equipment**
- **Built-in Memory**
- **Built-in Character Generator**
- **Built-in Multiplex and LED Drive Circuitry**
- **Direct Access to Each Digit Independently and Asynchronously**
- **Clear Function that Clears Character Memory**
- **True Blanking for Intensity Dimming Applications**
- **End-stackable, 4-Character Package**
- **Intensity Coded for Display Uniformity**
- **Extended Operating Temperature Range: –40°C to +85°C**
- **Superior ESD Immunity**
- **100% Burned-in and Tested**
- **Wave Solderable**
- **TTL Compatible over Operating Temperature Range**

See Appnotes 18, 19, 22, and 23 at www.infineon.com/opto for additional information.

DESCRIPTION

The SLR/SLO/SLG/SLY2016 is a four digit 5 x 7 dot matrix display module with a built-in CMOS integrated circuit. This display is X/Y stackable.

The integrated circuit contains memory, a 128 ASCII ROM decoder, multiplexing circuitry and drivers. Data entry is asynchronous. A display system can be built using any number of SLR/SLO/SLG/SLY2016 since each digit can be addressed independently and will continue to display the character last stored until replaced by another.

System interconnection is very straightforward. Two address bits (A0, A1) are normally connected to the like-named inputs of all displays in the system.

Data lines are connected to all SLR/SLO/SLG/SLY2016s directly and in parallel as is the write line ($\overline{WR}$). The display will then behave as a write-only memory.

The SLR/SLO/SLG/SLY2016 has several features superior to competitive devices. 100% burn-in processing insures that the SLR/SLO/SLG/SLY2016 will function in more stressful assembly and use environments. True "blanking" allows the designer to dim the display for more flexibility of display presentation. Finally the $\overline{CLR}$ clear function will clear the ASCII character RAM.

DESCRIPTION (continued)

The character set consists of 128 special ASCII characters for English, German, Italian, Swedish, Danish, and Norwegian.

All products are 100% burned-in and tested, then subjected to out-going AQL's of .25% for brightness matching, visual alignment and dimensions, .065% for electrical and functional.

Maximum Ratings

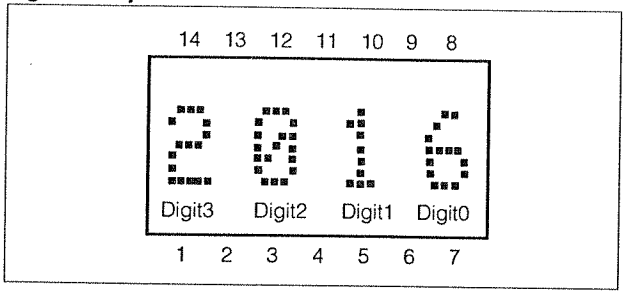
DC Supply Voltage ..... –0.5 V to +7.0 Vdc
Input Voltage, Respect to GND
(all inputs) ..... –0.5 V to V_{CC} +0.5 Vdc
Operating Temperature ..... –40 °C to +85°C
Storage Temperature ..... –40 °C to +100°C
Relative Humidity at 85°C 85%
Maximum Solder Temperature, 0.063" (1.59 mm)
below Seating Plane, t<5.0 s ..... 260 °C

Optical Characteristics

Spectral Peak Wavelength
Red ..... 660 nm typ.
HER ..... 635 nm typ.
Green ..... 565 nm typ.
Yellow ..... 585 nm typ.
Digit Height ..... 0.180" (4.57 mm)
Time Averaged Luminous Intensity [1]
at V_{CC}=5.0 V
Red ..... 50 µcd/LED min.
HER/Yellow ..... 60 µcd/LED min.
Green ..... 75 µcd/LED min.
LED to LED Intensity Matching, V_{CC}=5.0 V ..... 1.8:1.0 max.
Viewing Angle (off normal axis)
Horizontal ..... ±50° max.
Vertical ..... ±75° max.

Note:
1) Peak luminous intensity values can be calculated by multiplying these values by 7.

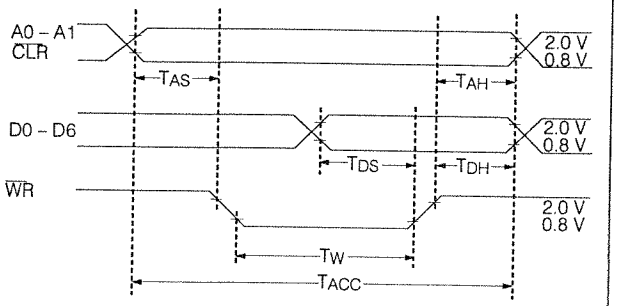
Figure 1. Top View



Pin Function

Pin	Function	Pin	Function
1	$\overline{WR}$ Write	8	D3 Data
2	A1 Digit Select	9	D4 Data
3	A0 Digit Select	10	D5 Data
4	V_{CC}	11	D6 Data
5	D0 Data	12	$\overline{BL}$ Display Blank
6	D1 Data	13	$\overline{CLR}$ Clear
7	D2 Data	14	GND

Figure 2. Timing Characteristics—Write Cycle Waveforms



DC Characteristics at 25°C

Parameters	Min.	Typ.	Max.	Units	Conditions
V_{CC}	4.5	5.0	5.5	V	—
I_{CC} Blank	—	2.3	3.0	mA	V_{CC}=5.0 V
I_{CC} (80 dots on)	—	80	105	mA	V_{CC}=5.0 V
V_{IL} (all inputs)	—	—	0.8	V	4.5 V <V_{CC} <5.5 V
V_{IH} (all inputs)	2.0	—	—	V	4.5 V <V_{CC} <5.5 V
I_{IL} (all inputs)	25	—	100	µA	4.5 V <V_{CC} <5.5 V, V_{IN}=0.8 V

AC Characteristics (guaranteed minimum timing parameters at V_{CC}=5.0 V ±0.5 V)

Parameter	Symbol	–40°C	+25°C	+85°C	Unit
Address Set Up Time	T_{AS}	10	10	10	ns
Write Time	T_W	60	70	90	ns
Data Set Up Time	T_{DS}	20	30	50	ns
Address Hold Time	T_{AH}	20	30	40	ns
Data Hold Time	T_{DH}	20	30	40	ns
Access Time	T_{ACC} (1)	90	110	140	ns
Clear Disable Time	T_{CLRD}	1.0	1.0	1.0	µs
Clear Time	T_{CLR}	1.0	1.0	1.0	ms

Note:

1) T_{ACC}=Set Up Time + Write Time + Hold Time

Loading Data

The desired data code (D0–D6) and digit address (A0, A1) must be held stable during the write cycle for storing new data.

Data entry may be asynchronous. Digit 0 is defined as right hand digit with A1=A2=0.

Clearing the entire internal four-digit memory can be accomplished by holding the clear ($\overline{CLR}$) low for 1.0 msec minimum. The clear function will clear the ASCII RAM. Loading an illegal data code will display a blank.

Typical Loading State Table

WR	A1	A0	D6	D5	D4	D3	D2	D1	D0	Digit			
										3	2	1	0
H			previously loaded display							G	R	E	Y
L	L	L	H	L	L	L	H	L	H	G	R	E	E
L	L	H	H	L	H	L	H	L	H	G	R	U	E
L	H	L	H	L	L	H	H	L	L	G	L	U	E
L	H	H	H	L	L	L	L	H	L	B	L	U	E
L	L	H	H	L	L	L	H	L	H	B	L	E	E
L	L	L	H	L	H	L	H	H	H	B	L	E	W
L	X	X	see character code							see char. set			

Display Blanking

Blank the display by loading a blank or space into each digit of the display or by using the ($\overline{BL}$) display blank input. Setting the ($\overline{BL}$) input low does not affect the contents of data memory.

A flashing circuit can easily be constructed using a 555 as table multivibrator. Figure 3 illustrates a circuit in which varying R1 (100K~10K) will have a flash rate of 1.0 Hz~10 Hz.

The display can be dimmed by pulse width modulating the ($\overline{BL}$) at a frequency sufficiently fast to not interfere with the internal clock. The dimming signal frequency should be 2.5 kHz or higher. Dimming the display also reduces power consumption.

An example of a simple dimming circuit using a 556 is illustrated in Figure 4. Adjusting potentiometer R3 will dim the display by changing the blanking pulse duty cycle.

Figure 3. Flashing Circuit Using a 555 and Flashing (Blanking) Timing

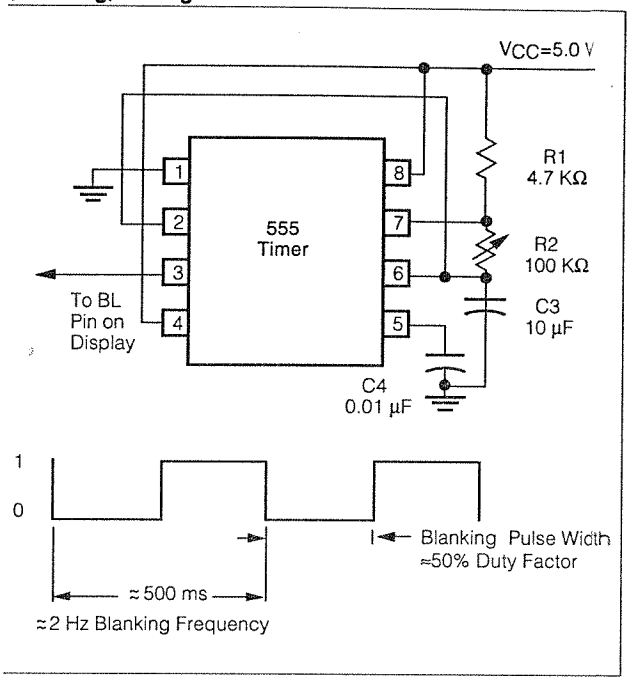


Figure 4. Dimming Circuit Using a 556 and Dimming (Blanking) Timing

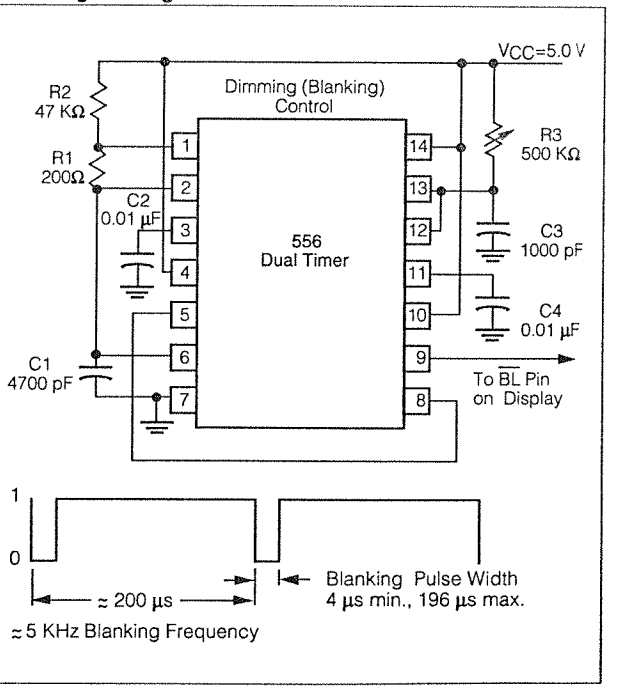
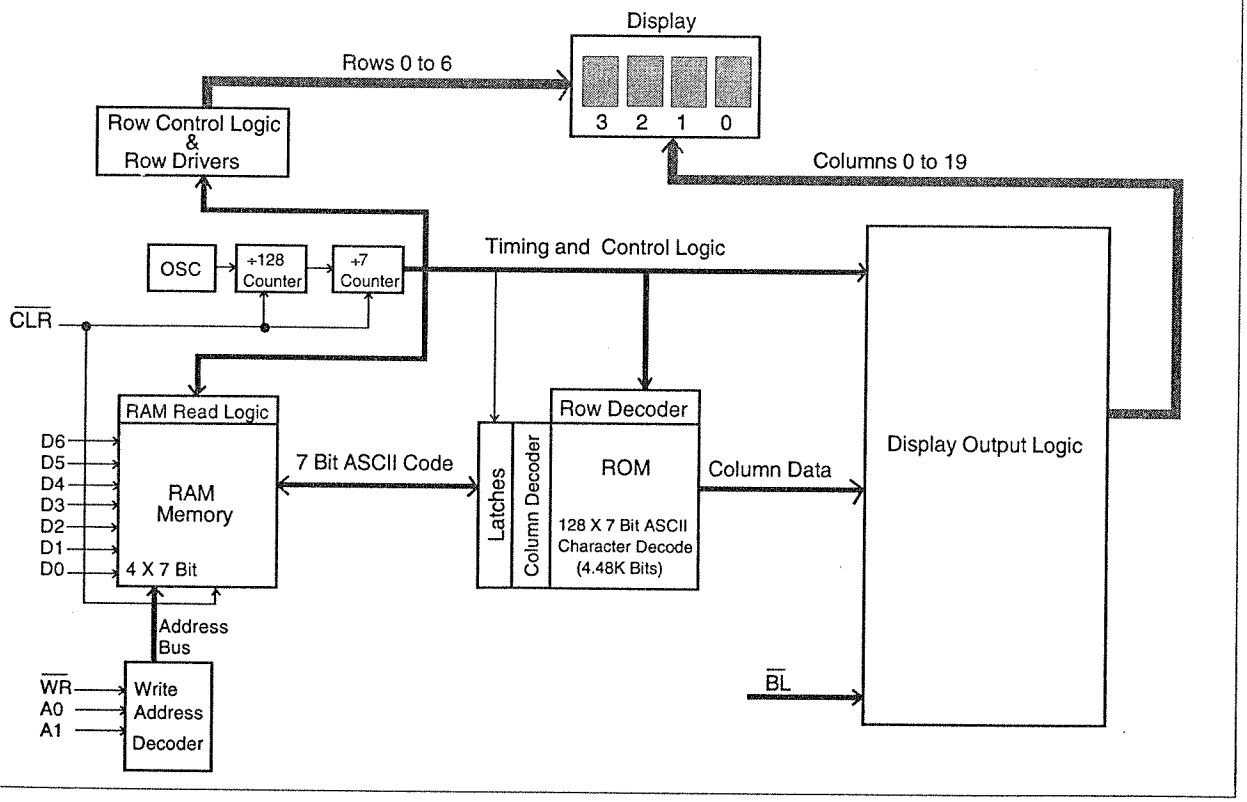


Figure 5. Character Set

ASCII CODE				D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
D6	D5	D4	HEX		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0																	
0	0	1	1																	
0	1	0	2																	
0	1	1	3																	
1	0	0	4																	
1	0	1	5																	
1	1	0	6																	
1	1	1	7																	

Notes:
1. High=1 level
2. Low=0 level
3. Upon power up, the device will initialize in a random state.

Figure 6. Block Diagram



2.2 Hardware

Die Entwicklung der Hardware war für diese Aufgabe nicht mit einem sehr grossen Aufwand verbunden.
Nach langem Warten bekamen wir von Herrn Bazali die versprochene Schaltung, die das LED-Display umfasst und konnten dann endlich mit der Entwicklung einer Software für die Ansteuerung des Displays beginnen.
Die Leiterplatte, die die Displays und die Logik für die Umschaltung trägt, ist mit einem 20-poligen Flachbandkabel mit der Mikrocontroller-Platte verbunden. Das analoge Drehspuhlmesswerk ist mit einem 2-poligen Flachbandkabel mit dem Controller verbunden. Das Netzgerät, welches uns die Spannungswerte für Strom, Spannung, Offset und GND liefert haben wir mit einem 4-poligen Flachbandkabel mit dem Controller verbunden.

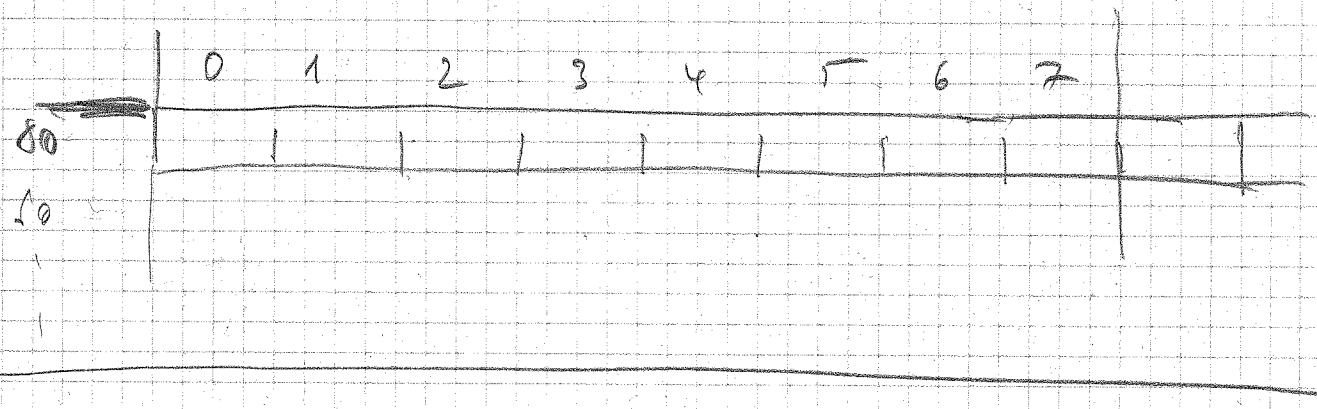
Verdrahtungsplan:

Pin	Bez	Farbe	Port
1	D0	braun	P1.0
2	D2	orange	P1.2
3	D4	grün	P1.4
4	D6	violet	P1.6
5	A0	weiss	P4.0
6	A2	braun	P4.2
7	/	orange	
8	/	grün	
9	V+	violet	+5V
10	V+	weiss	+5V
11	D1	rot	P1.1
12	D3	gelb	P1.3
13	D5	blau	P1.5
14	D7	grau	P1.7
15	A1	schwarz	P4.1
16	WR	rot	P4.3
17	/	gelb	
18	/	blau	
19	GND	grau	
20	GND	schwarz	
	PWM	grau	P5.0
	uu	grau	P7.0
	ui	grau	P7.1
	uo	grau	P7.2

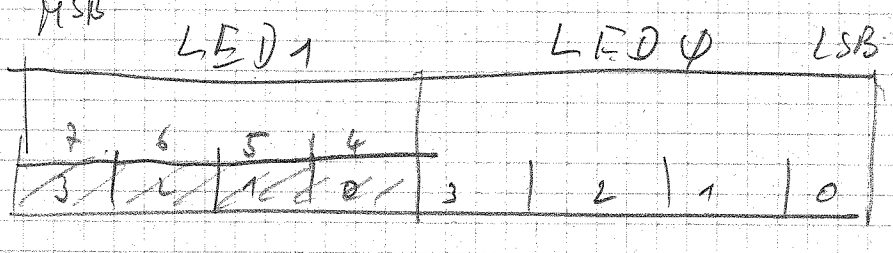
Auf der folgenden Seite ist das komplette Hardware-Schema abgebildet.

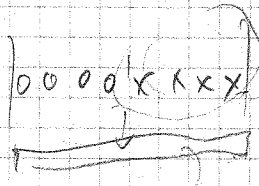
ind. RAM 80 → FFH

AVR: 80 – 87 (8 Byte)
für ASCII-Zeichencode

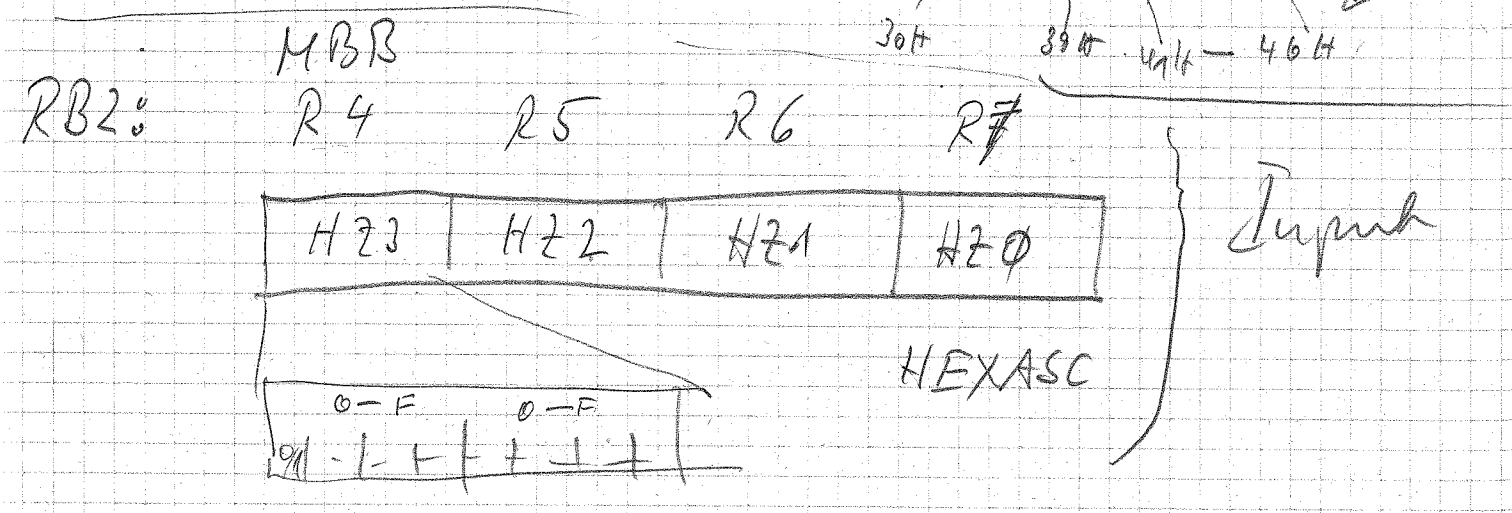


aus ind. RAM → an LED-Anzeige schreib





ASCII-Zeilencode: Zeilen 0 – 9, A – F



RB2 : {R4 — R7}

↓

~~AB~~ Hex-Zahl ~~Adr~~

↓

wandeln in ASCII-Code

↓

auf Startbefehl am Anfang des Programms

(bei Aufruf mit LCALL <name>